TEXAS INSTRUMENTS

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INNOVATOR IN ELECTRONICS

Creation Date May 31, 2018
Report No. TT-637

Proposal for power design by using Murata Low ESL Cap.

For Jacinto 7

Application Engineering Sec.
Capacitor Division 2
Components Business Unit

Meeting purpose

Murata propose best solution for Jacinto 7 project!!

Key words

Cost down

MLCC Reduction

Low impedance

Downsizing

Agenda

1. Latest Murata's solution
2. Simulation result (Jacinto 6+)
3. Other topics

Cap Value Trend for Automotive Grade Cap

Higher Capacitance can be achieved Murata cutting-edge technology!!

Product RM for LowESL MLCC (NFM_HC Series)

LowESL (3-Term) MLCC : NFM_HC Series (Automotive TS Grade)

Capacitor Dimension

Series	Inch (mm)	Dimension
NFM15	0402(1005)	1.0 x 0.5 mm
NFM18	0603 (1608)	1.6 x 0.8 mm
NFM21	0805(2012)	2.0 x 1.25 mm
NFM31	1206 (3216)	3.2 x 1.6 mm

Temperature Characteristics

TC	Temp. Range	Cap. Change
X7R	-55 to 125°C	+/- 15 %
X7S	-55 to 125°C	+/- 22 %

Type	Temp. Char.	Rated Voltage	Capacitance Value												Capacitance Range
			100pF		1,000pF		0.01uF		0.1uF		1uF		10uF		
NFM15	X7*	6.3 V													1uF
NFM18	X7S	16 V													1,000pF~1uF
	X7*	6.3 V													4.7uF~10uF
NFM21	X7R	50 V													220pF~22nF
	X7R	16 V													1uF
	X7R	10 V													0.1uF~0.47uF
NFM31	X7S	100 V													10nF
		50 V													10nF~0.1uF

NEW

MP : In MP
Sample : Available

MP : 18CQ3
Sample : Available

MP : 19CQ2
ES Sample : Available

Note) This is Murata development schedule, which may change without any notice.

Under Developing!

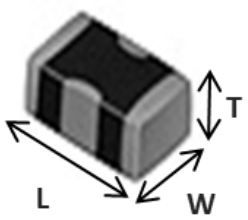
Murata LowESL MLCC Proposal P/N

Part Number	Size(inch/mm)	TC	Cap.Value	Cap.Tol.	Volt.
NFM18HC105C1C*	0603/1608	X7S	1uF	+/-20%	16V

Engineering Sample:
Available

MP Schedule:
18CQ3

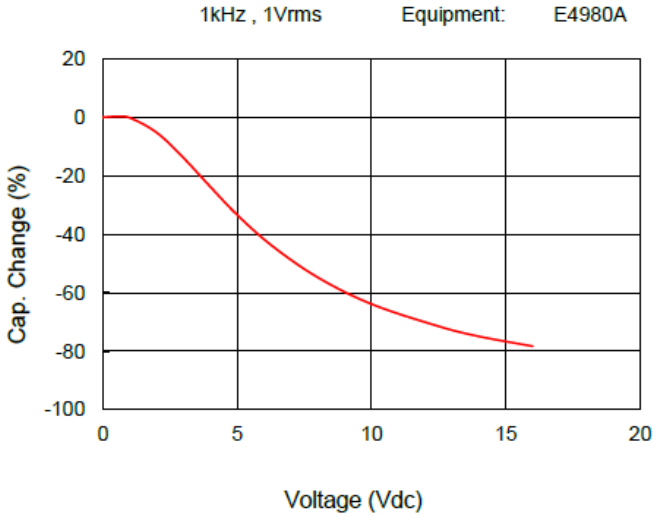
Dimension



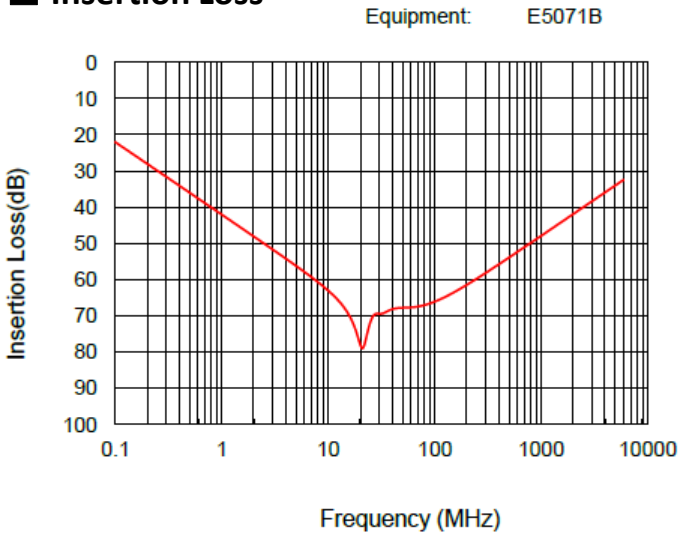
Size (inch/mm)	L(mm)	W(mm)	T(mm)
0603/1608	1.60+/-0.10	0.80+/-0.10	0.60+/-0.10

Electrical Characteristics Data

DC-Bias



Insertion Loss



Under Developing!

Murata LowESL MLCC Proposal P/N

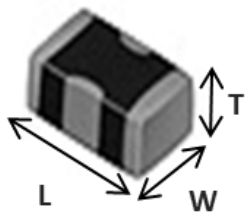
Part Number	Size(inch/mm)	TC	Cap.Value	Cap.Tol.	Volt.
NFM18HC106*0J*	0603/1608	X7T	10uF	+/-20%	6.3V

Engineering Sample:
Available

Reel Sample:
18CQ3

MP Schedule:
19CQ1

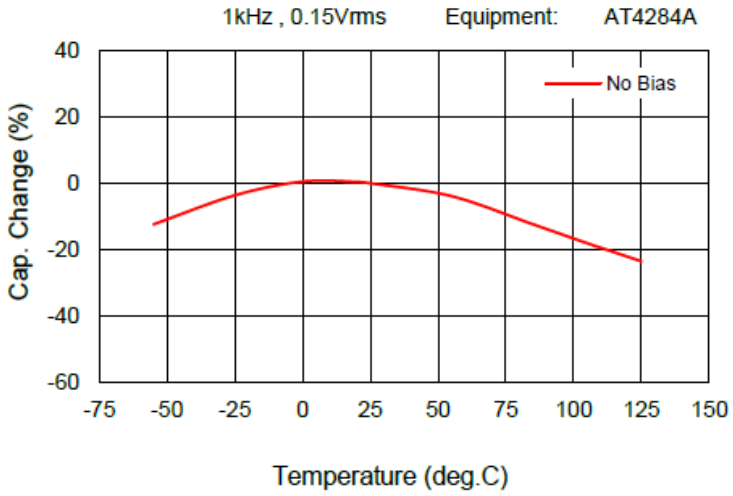
Dimension



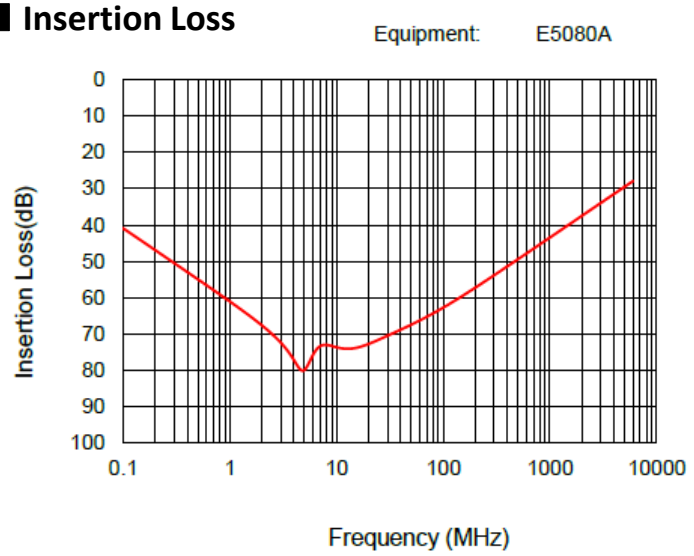
Size (inch/mm)	L(mm)	W(mm)	T(mm)
0603/1608	1.60+/-TBD	0.80+/-TBD	TBD

Electrical Characteristics Data

■ DC-Bias



■ Insertion Loss



Agenda

1. Latest Murata's solution
2. Simulation result (Jacinto 6+)
3. Other topics

Murata made analysis and simulation of Jacinto 6 +.

This is mainly for explaining and providing Murata's best solution with Jacinto 7 project.

0. Overview

■Summary

We compared TI reference board replaced by the low ESL capacitors with Initial one.
By using the low ESL capacitors, we are able to achieve parts reduction.

■Target

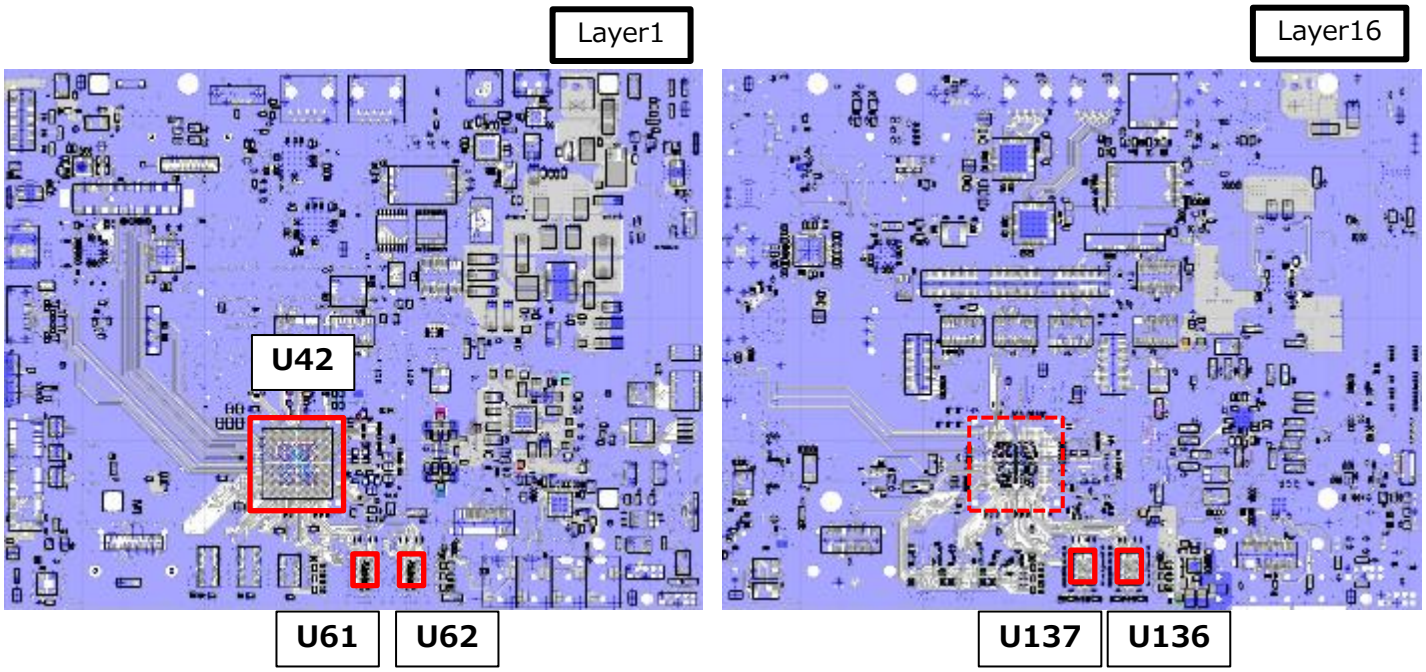
- Target Set :TI Jacinto6+ board
- Target IC :Jacinto6+_U42 DDR_U61,U62,U136,U137
- Power Line :refer below

<U42>

VDDR_SOC_1V35
VDDSHV_3V3
VDDS_1V8
VDD_CORE_AVS
VDD_DSPEVE_AVS
VDD_GPU_AVS
VDD_MPU_AVS

<DDR>

VDDR_MEM_1V35



0. Overview

■ Summary

Effect of Low ESL Capacitors

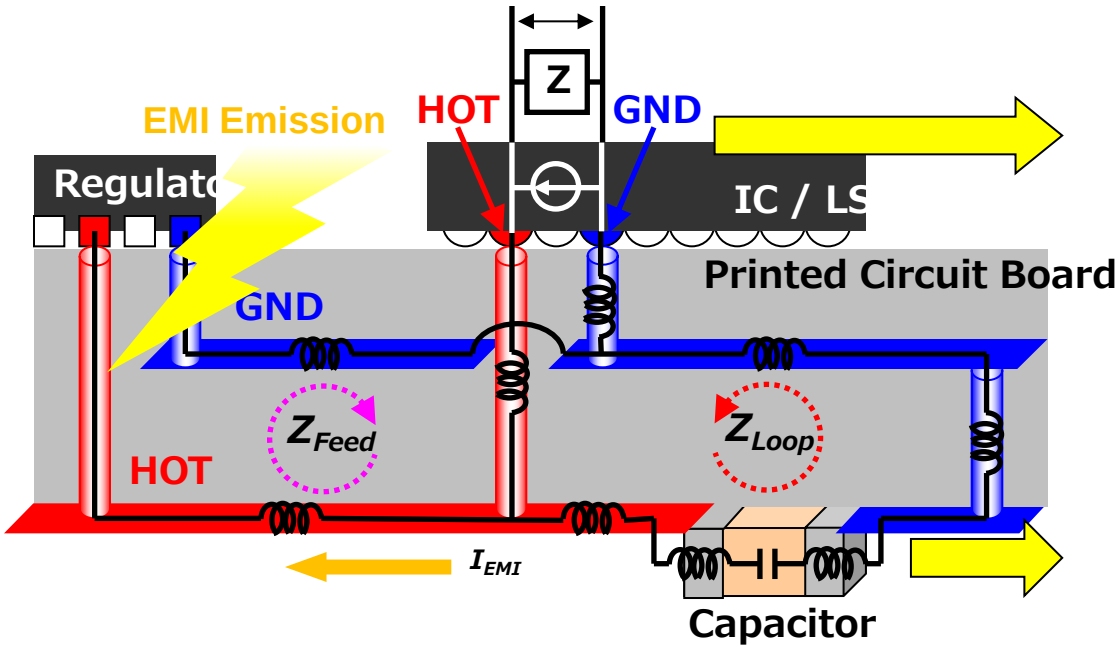
- ➢ Parts reduction : -38pcs
- ➢ Impedance : +1.05%

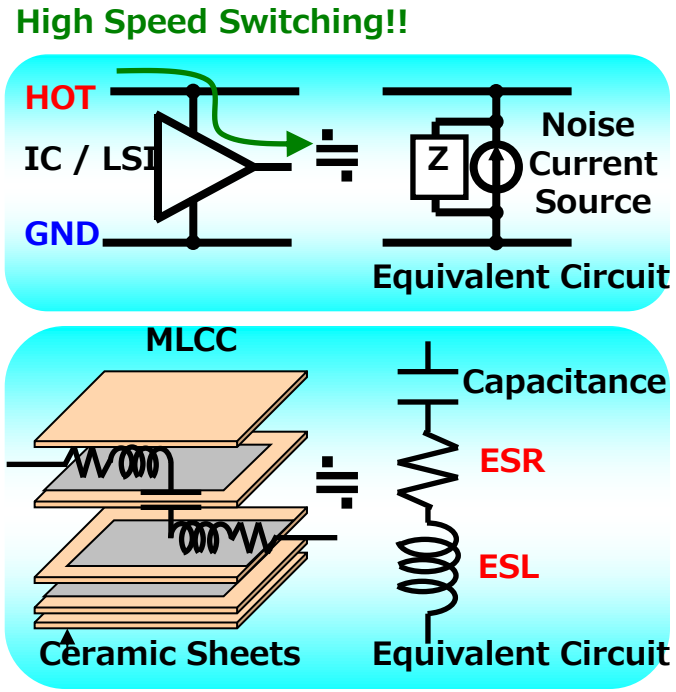
	IC	Net	QTY[pcs]								Z[mΩ] @100MHz
			0402 CM 1005/0.1uF	0402 CM 1005/0.47uF	0402 RT 1005/0.22uF	0805 CM 2012/10uF	0508 L 1220/1uF	0402 M 1005/1uF	0603 FM 1608/10uF	Total Mount	
Initial	U42	VDDR_SOC_1V35		16		2	2			20	79.11
		VDDSHV_3V3	10	2		1				13	63.29
		VDDS_1V8	7	3		1	1			12	113.6
		VDD_CORE_AVS		5		1	4			10	83.42
		VDD_DSPEVE_AVS	2	4		2	5			13	73.94
		VDD_GPU_AVS	2	4		1	3			10	86.37
		VDD_MPU_AVS	2	4		2	5			13	62.90
	DDR	VDDR_MEM_1V35	18	20	48					86	44.73
		Total/Ave	41	58	48	10	20	0	0	177	75.92
Optimal	U42	VDDR_SOC_1V35		13		2	2	1		18	77.84
		VDDSHV_3V3	6	2		1		1		10	64.67
		VDDS_1V8	2	2				2	1	7	114.1
		VDD_CORE_AVS		5		1		1	1	8	85.43
		VDD_DSPEVE_AVS	2	2		2		2	1	9	74.09
		VDD_GPU_AVS	1	3		1		2	1	8	86.63
		VDD_MPU_AVS	2	2		2		2	1	9	65.20
	DDR	VDDR_MEM_1V35	18	20	26			6		70	45.76
		Total/Ave	31	49	26	9	2	17	5	139	76.72
Effect			-10	-9	-22	-1	-18	17	5	-38	1.05%

1. Introduction

- Necessity of Low ESL Cap

Low impedance design is desired with low voltage and large current.





To reduce the Z_{Loop},

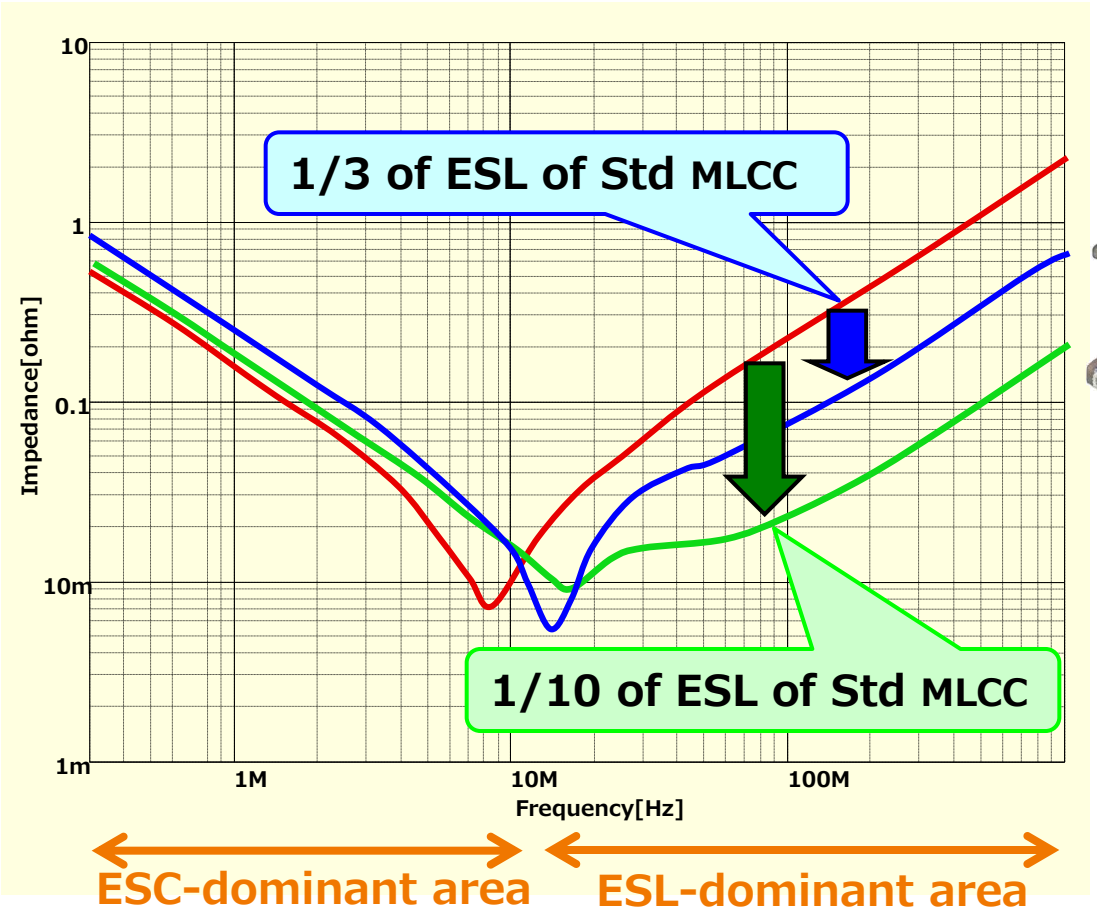
✓Need to optimize power supply loop(IC_HOTpin~Caps~IC_GNDpin)!

✓Optimization of Caps and Substrate are effective!

1. Introduction

- Optimization by using Low ESL Cap

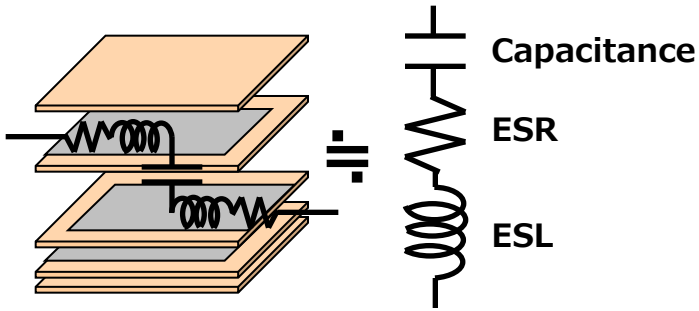
Low Impedance/Quantity, Area and Cost reduction are achieved!




Standard MLCC


Reverse geometry cap


3 terminal cap

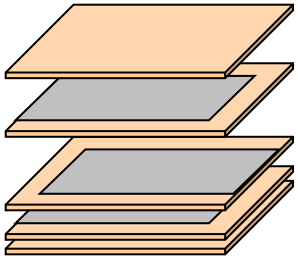


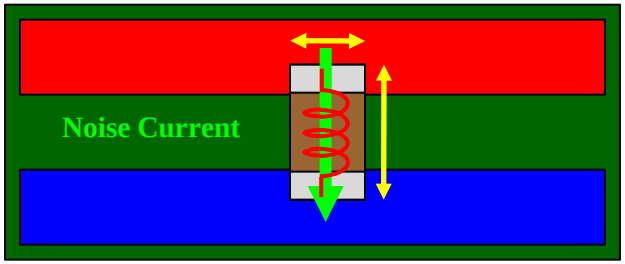
1. Introduction

- Inner structure of Low ESL Cap

Low ESL is achieved by a device of the inner structure!

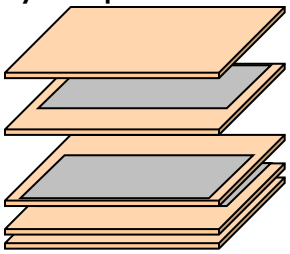
<Standard MLCC>

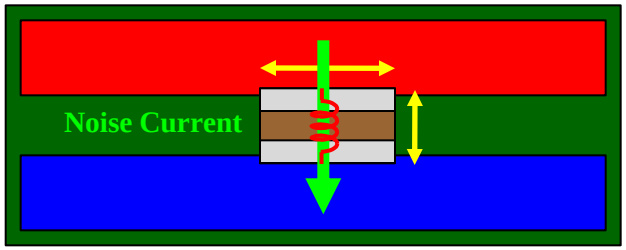




Bad : Long current path
Bad : Small sectional area for current path

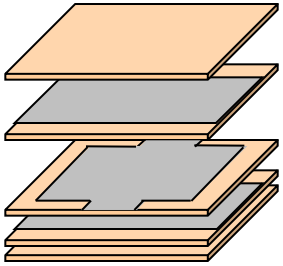
<Reverse geometry cap>

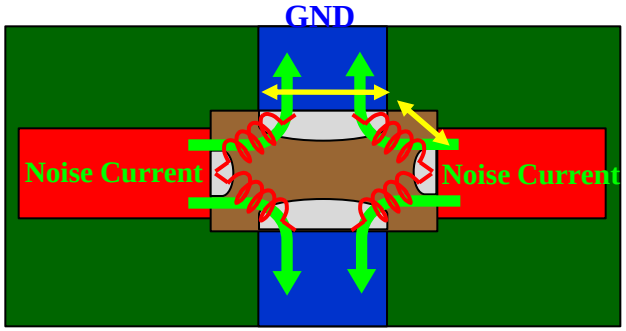




Good : Short current path
Good : Large sectional area for current path

<3 terminal cap>



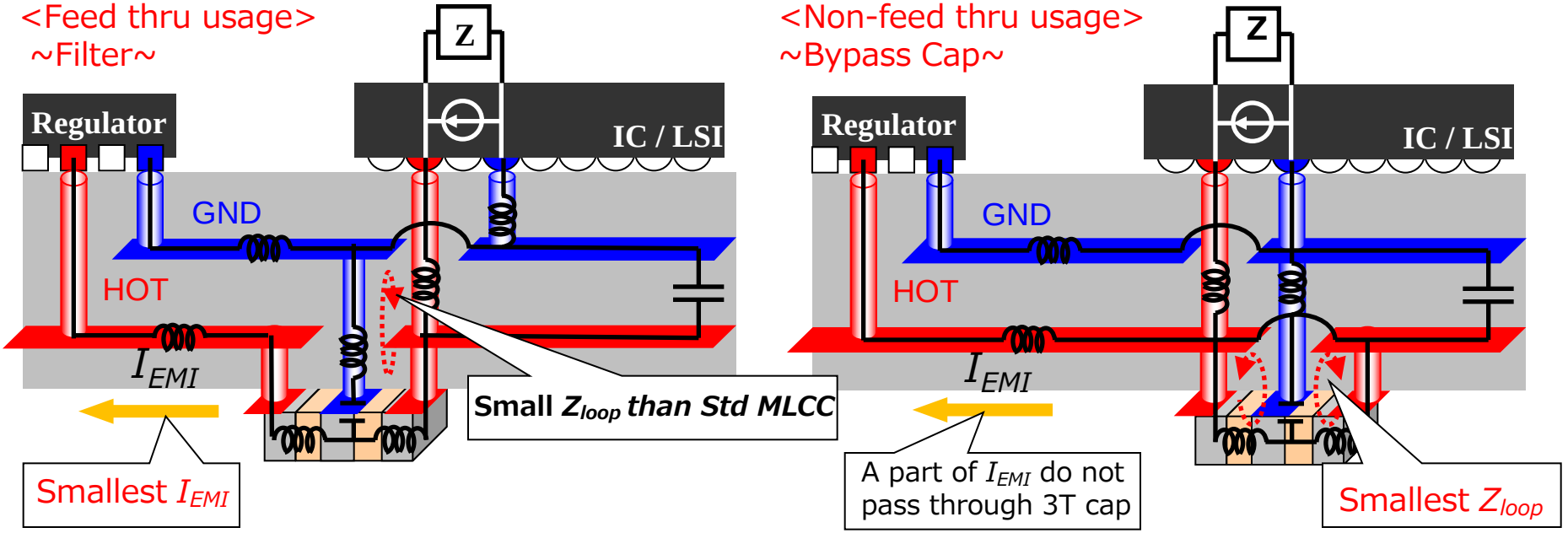


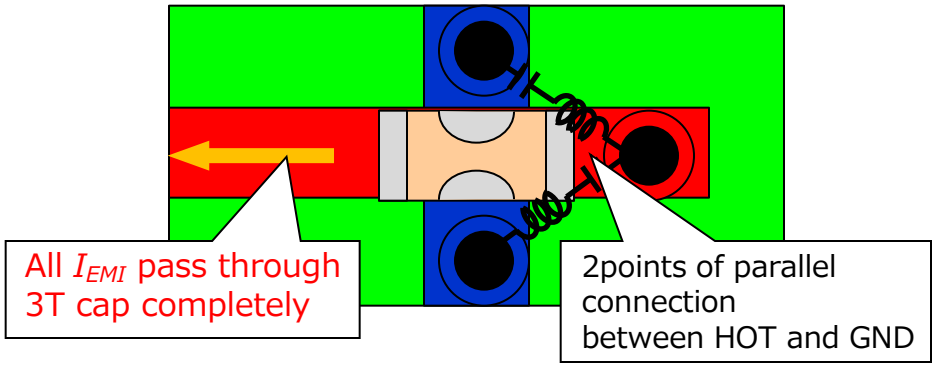
Good : Short current path
Good : Large sectional area for current path
Good : Multiple current path

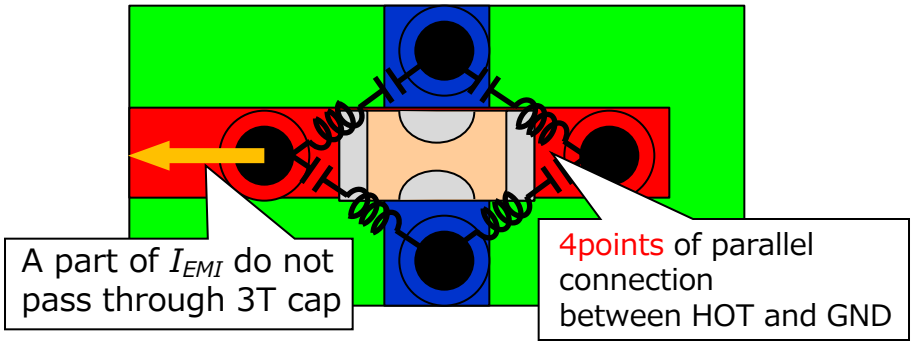
1. Introduction

- Usage example of 3 terminal Cap

Excellent performance is shown in Filter use and Bypass Cap use!



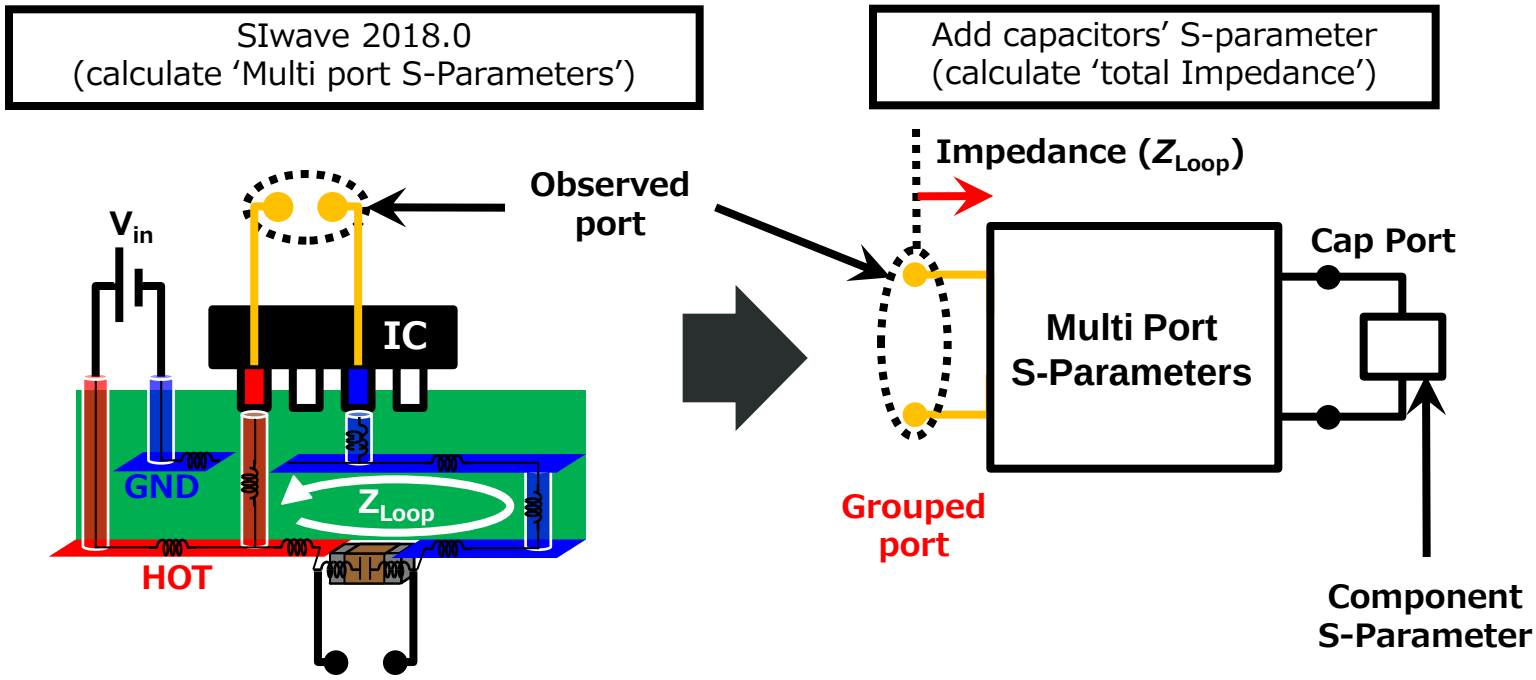




2. Consideration of optimization

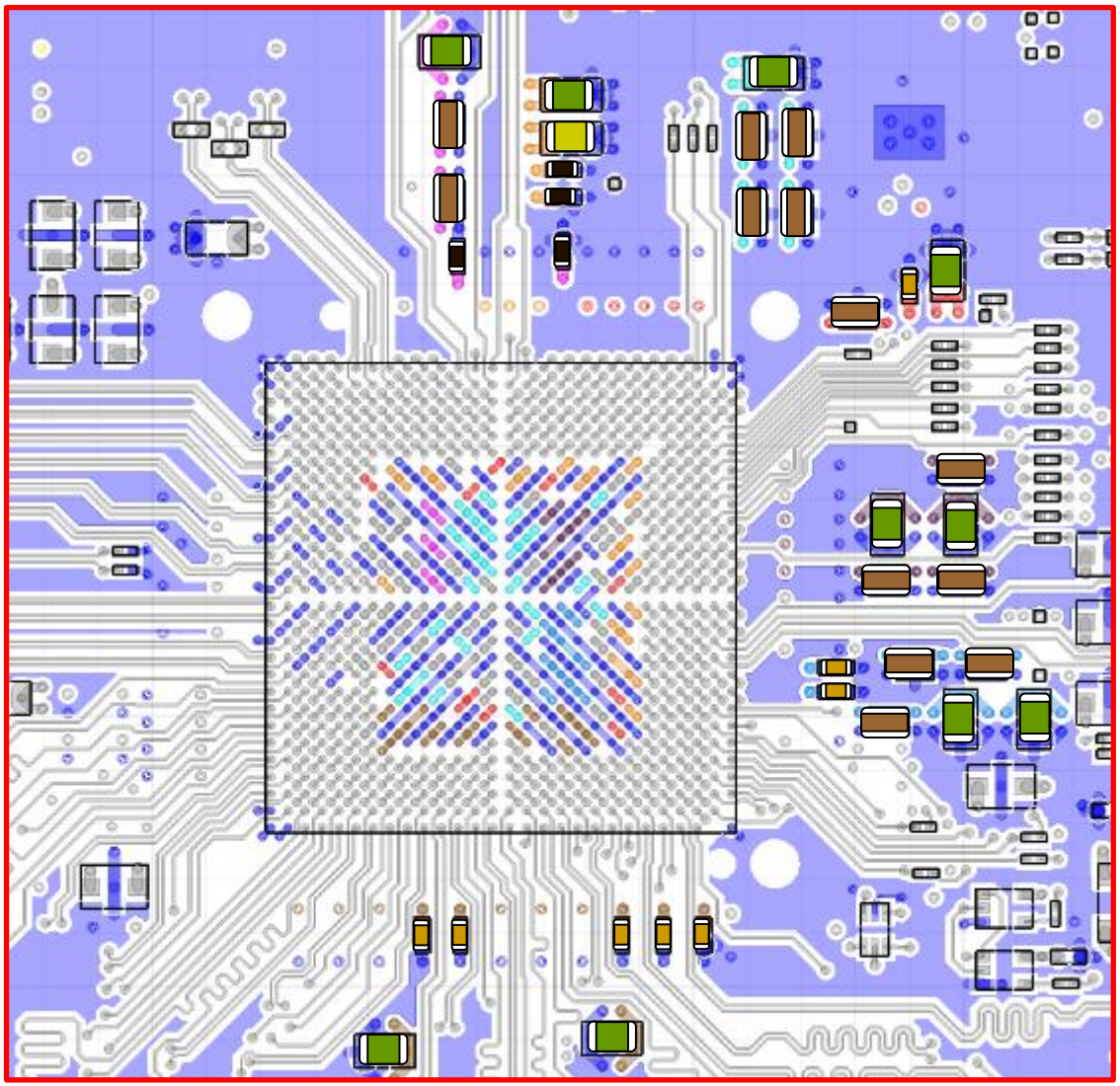
- Simulation method and condition

CAD file :SPRR313_DRA76xP_DRA77xP_TDA2Px_ACD CPU Board PCB Rev C.brd
Simulator : Electromagnetic field simulator “SIwave 2018.0”
Observed ports : Grouping port
Frequency : 100kHz to 1GHz , Logarithm sweep , 100pts./Decade



2. Consideration of optimization

■ Cap. Layout : Initial(Top) – U42



	0402/0.1uF GCM155R71C104	× 4 pcs
	0402/0.47uF GCM155C71A474	× 8 pcs
	0805/4.7uF GCM21BR71C475	× 1 pcs
	0805/10uF GCM21BR71A106	× 10 pcs
	0508/1uF LLL215C70G105	× 13 pcs
	0402/1uF NFM15HC105	× 0 pcs
	0603/10uF NFM18HC106	× 0 pcs

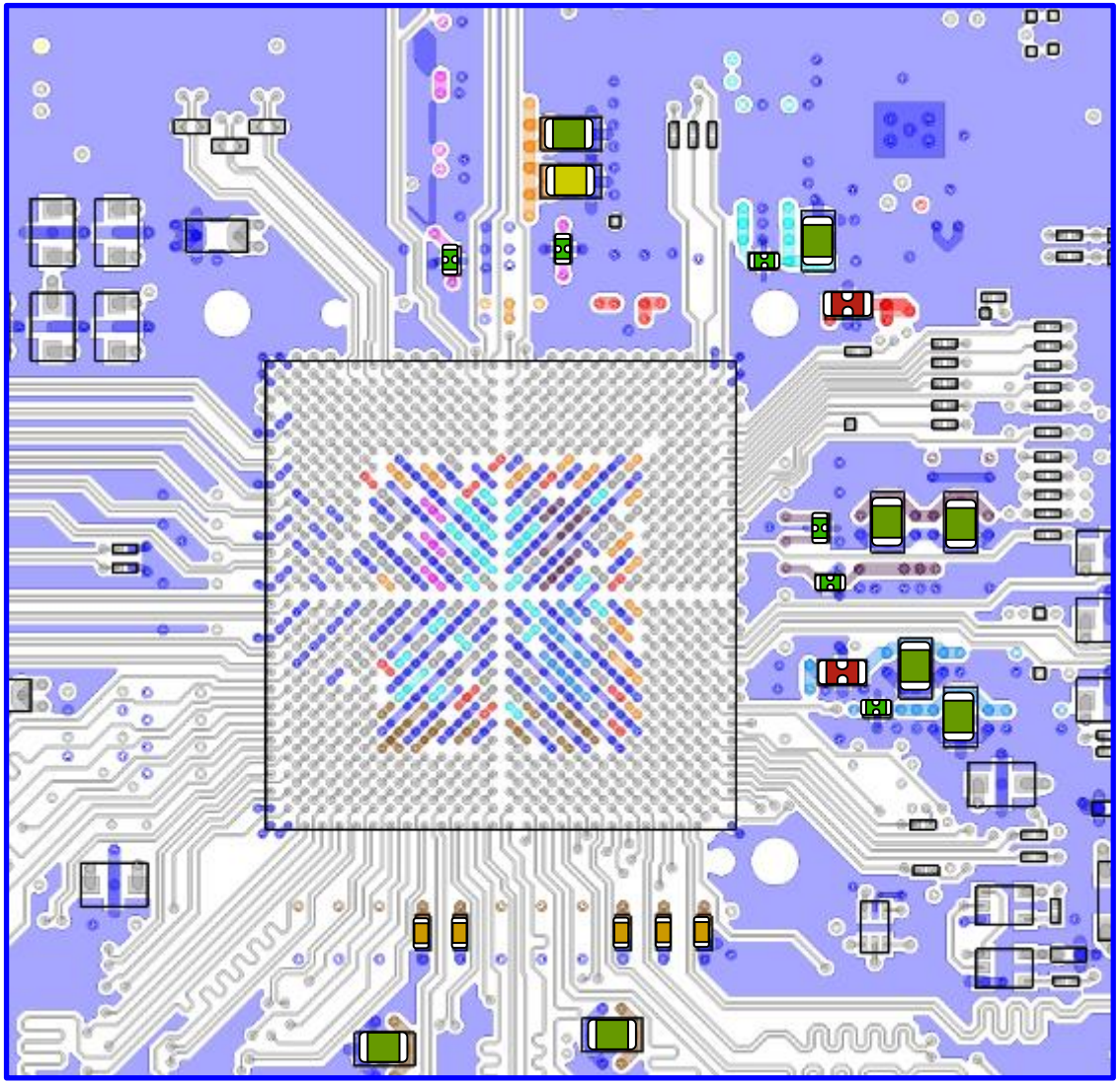
VDDR_SOC_1V35
VDDSHV_3V3
VDDS_1V8
VDD_CORE_AVS
VDD_DSPEVE_AVS
VDD_GPU_AVS
VDD_MPU_AVS

※ We simulated with including all capacitors on the target power lines.

2. Consideration of optimization

14pcs Reduction

■ Cap. Layout : Replacement(Top) – U42



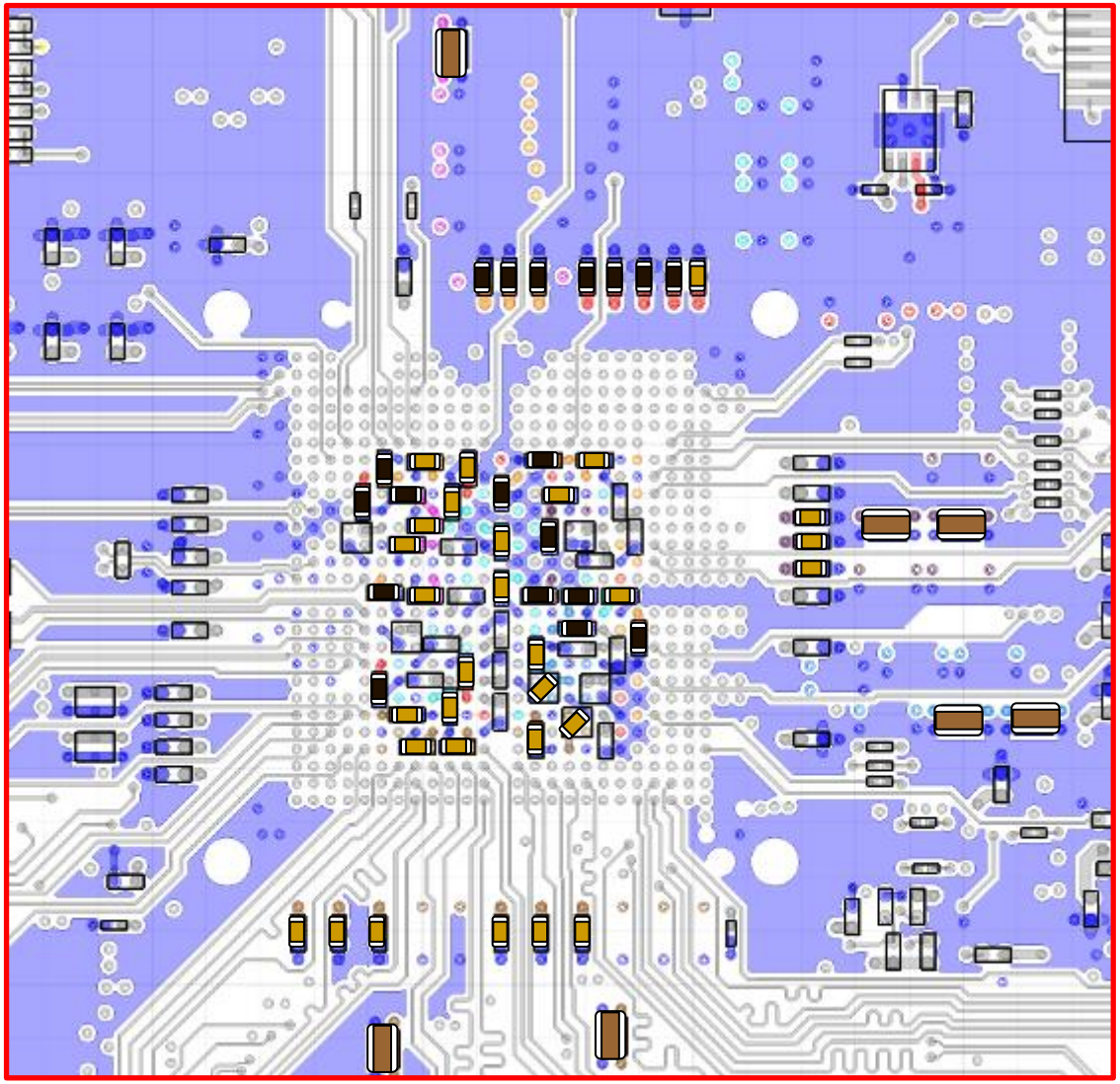
	0402/0.1uF GCM155R71C104	× 0pcs
	0402/0.47uF GCM155C71A474	× 5pcs
	0805/4.7uF GCM21BR71C475	× 1 pcs
	0805/10uF GCM21BR71A106	× 8 pcs
	0508/1uF LLL215C70G105	× 0 pcs
	0402/1uF NFM15HC105	× 6 pcs
	0603/10uF NFM18HC106	× 2 pcs

VDDR_SOC_1V35
VDDSHV_3V3
VDDS_1V8
VDD_CORE_AVS
VDD_DSPEVE_AVS
VDD_GPU_AVS
VDD_MPU_AVS

※ We simulated with including all capacitors on the target power lines.

2. Consideration of optimization

■ Cap. Layout : Initial(Bottom) – U42



	0402/0.1uF GCM155R71C104	× 19 pcs
	0402/0.47uF GCM155C71A474	× 30 pcs
	0805/4.7uF GCM21BR71C475	× 0 pcs
	0805/10uF GCM21BR71A106	× 0 pcs
	0508/1uF LLL215C70G105	× 7 pcs
	0402/1uF NFM15HC105	× 0 pcs
	0603/10uF NFM18HC106	× 0 pcs

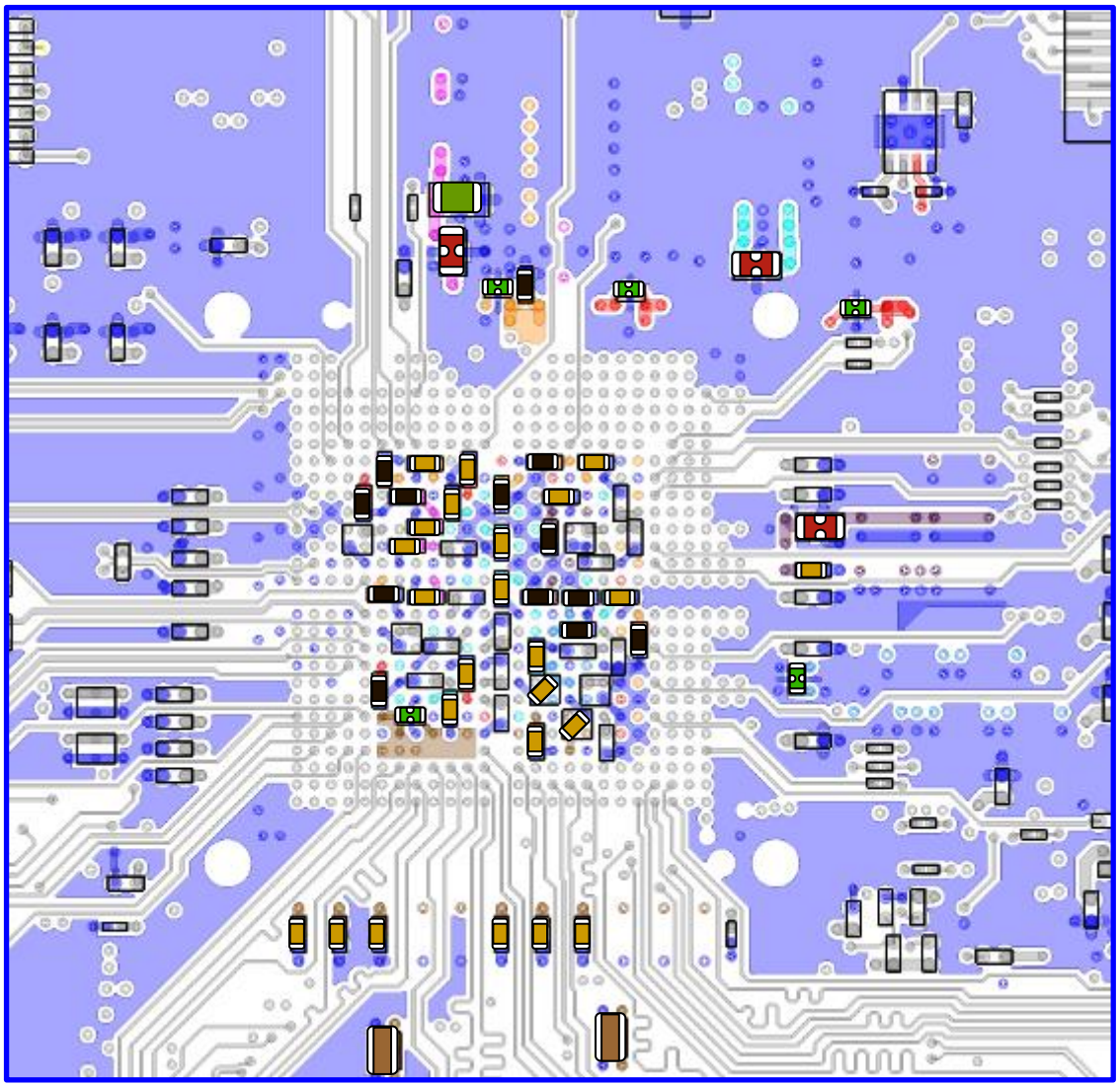
VDDR_SOC_1V35
VDDSHV_3V3
VDDS_1V8
VDD_CORE_AVS
VDD_DSPEVE_AVS
VDD_GPU_AVS
VDD_MPU_AVS

※ We simulated with including
all capacitors on the target power lines.

2. Consideration of optimization

8pcs Reduction

■ Cap. Layout : Replacement(Bottom) – U42



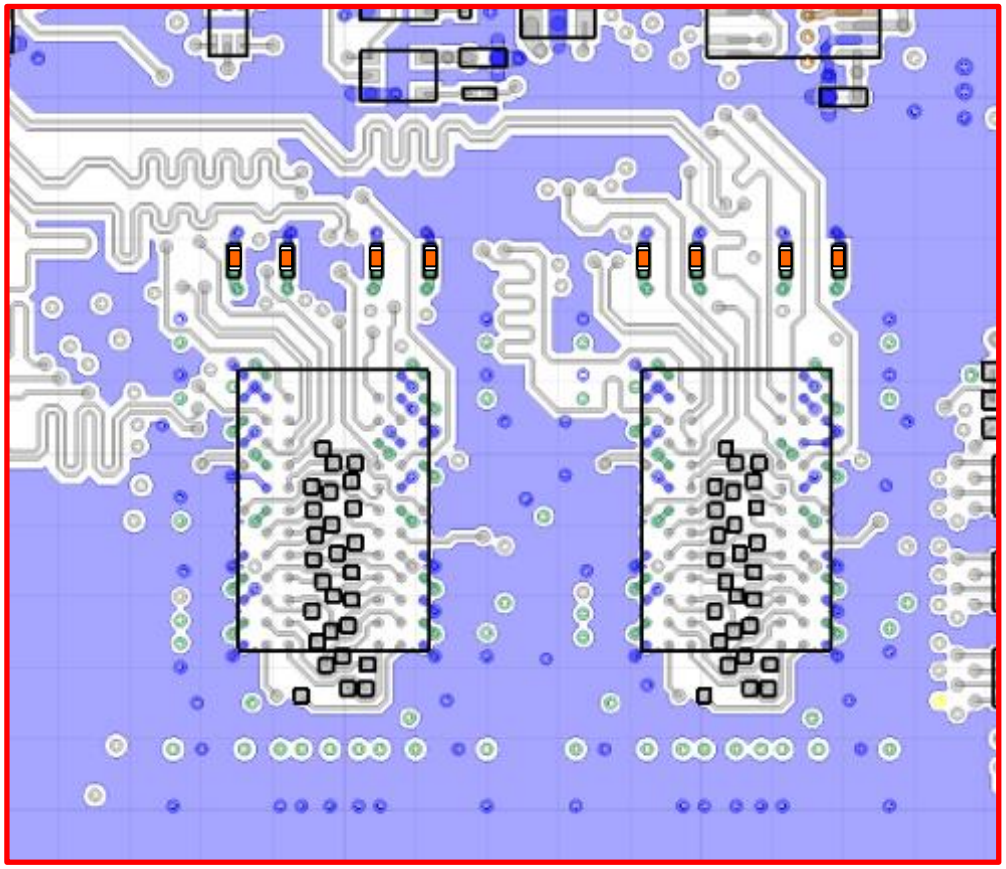
	0402/0.1uF GCM155R71C104	× 13pcs
	0402/0.47uF GCM155C71A474	× 24pcs
	0805/4.7uF GCM21BR71C475	× 0 pcs
	0805/10uF GCM21BR71A106	× 1 pcs
	0508/1uF LLL215C70G105	× 2 pcs
	0402/1uF NFM15HC105	× 5 pcs
	0603/10uF NFM18HC106	× 3 pcs

VDDR_SOC_1V35
VDDSHV_3V3
VDDS_1V8
VDD_CORE_AVS
VDD_DSPEVE_AVS
VDD_GPU_AVS
VDD_MPU_AVS

※ We simulated with including all capacitors on the target power lines.

2. Consideration of optimization

■ Cap. Layout : Initial(Top) – DDR



	0201/0.22uF GRT033C80J224	× 8 pcs
	0603/10uF GCM188D70J106	× 0 pcs
	0402/1uF NFM15HC105	× 0 pcs

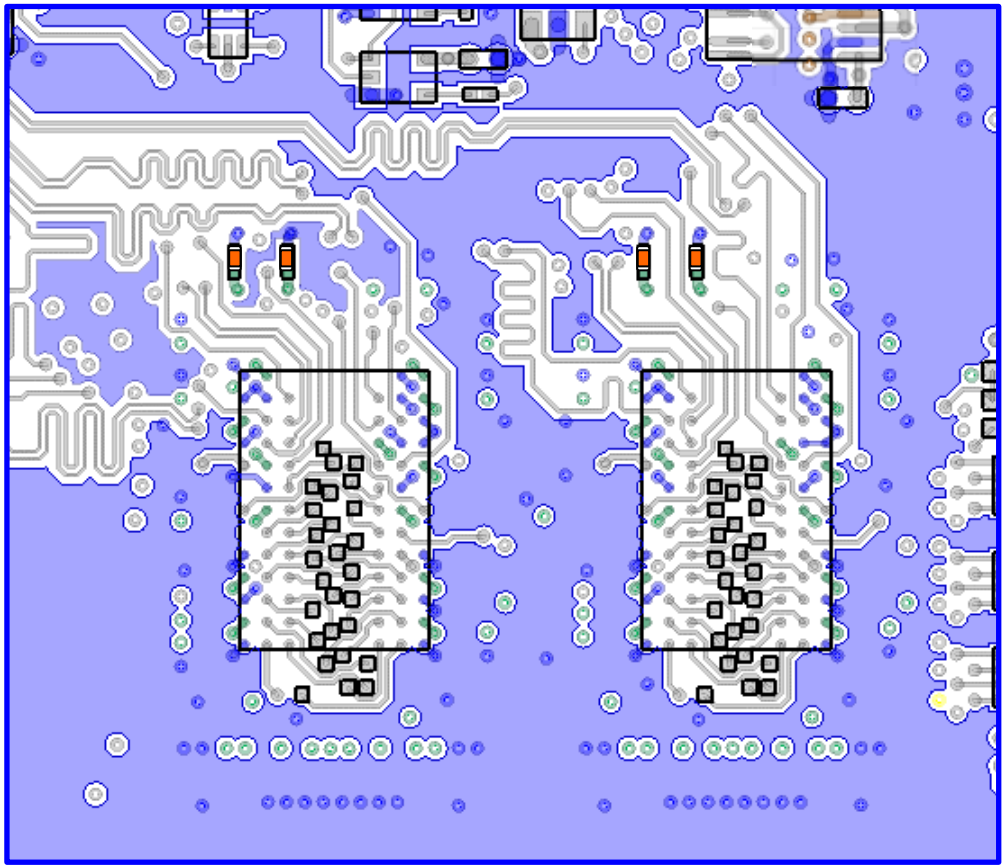
VDDR_MEM_1V35

※ We simulated with including
all capacitors on the target power lines.

2. Consideration of optimization

■ Cap. Layout : Replacement(Top) – DDR

4pcs Reduction



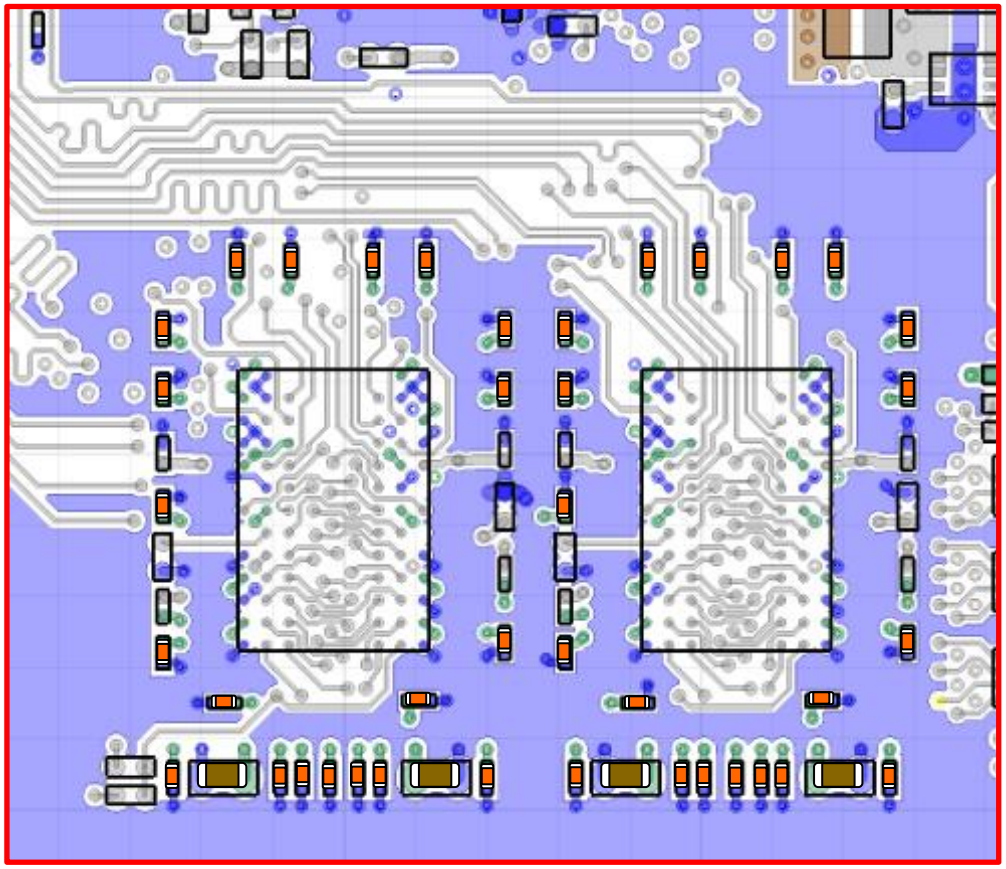
	0201/0.22uF GRT033C80J224	× 4 pcs
	0603/10uF GCM188D70J106	× 0 pcs
	0402/1uF NFM15HC105	× 0 pcs

VDDR_MEM_1V35

※ We simulated with including
all capacitors on the target power lines.

2. Consideration of optimization

■ Cap. Layout : Initial(Bottom) – DDR



	0201/0.22uF GRT033C80J224	× 40 pcs
	0603/10uF GCM188D70J106	× 4 pcs
	0402/1uF NFM15HC105	× 0 pcs

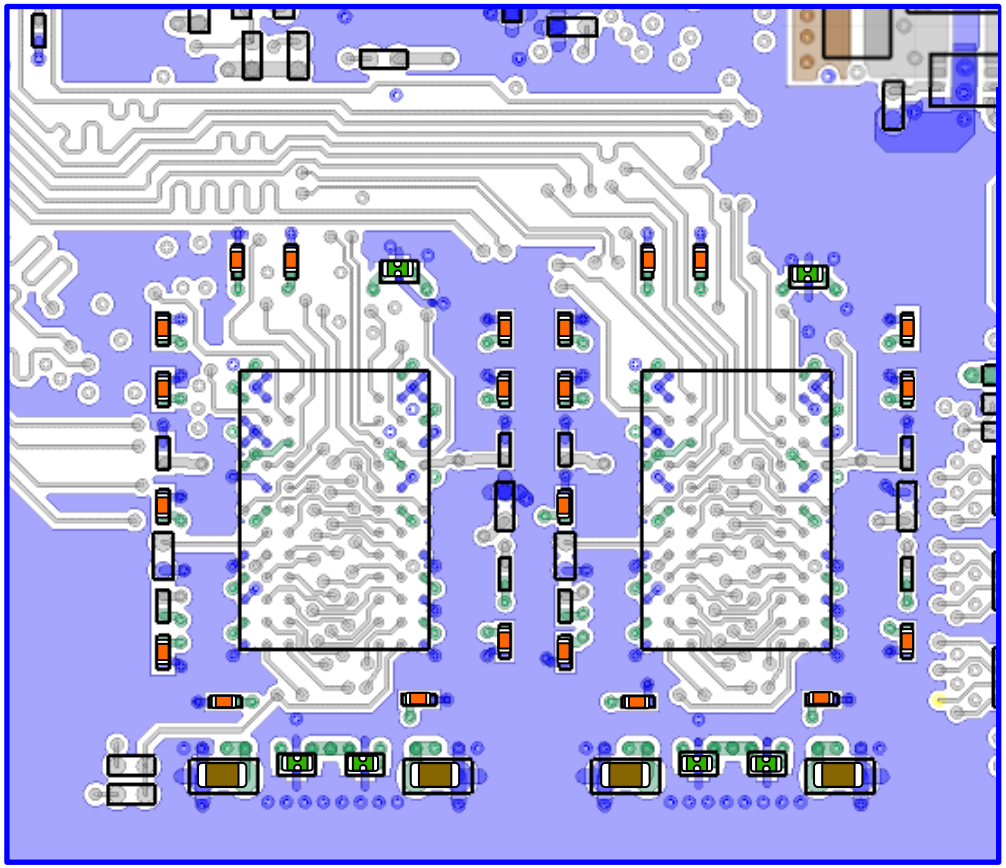
VDDR_MEM_1V35

※ We simulated with including
all capacitors on the target power lines.

2. Consideration of optimization

12pcs Reduction

■ Cap. Layout : Replacement(Bottom) – DDR



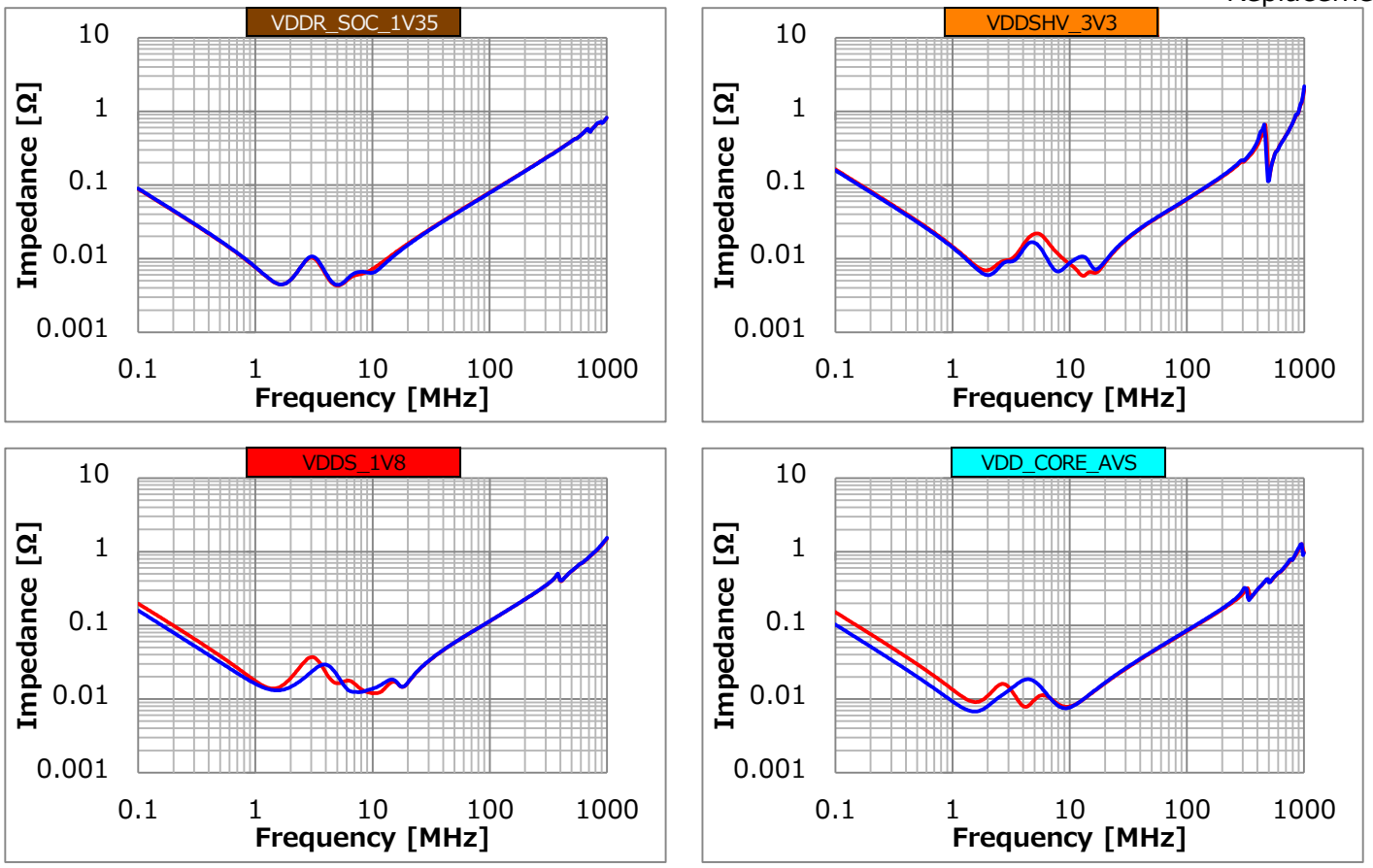
	0201/0.22uF GRT033C80J224	× 22 pcs
	0603/10uF GCM188D70J106	× 4 pcs
	0402/1uF NFM15HC105	× 6 pcs

VDDR_MEM_1V35

※ We simulated with including
all capacitors on the target power lines.

2. Consideration of optimization

■ Result of impedance simulation – U42

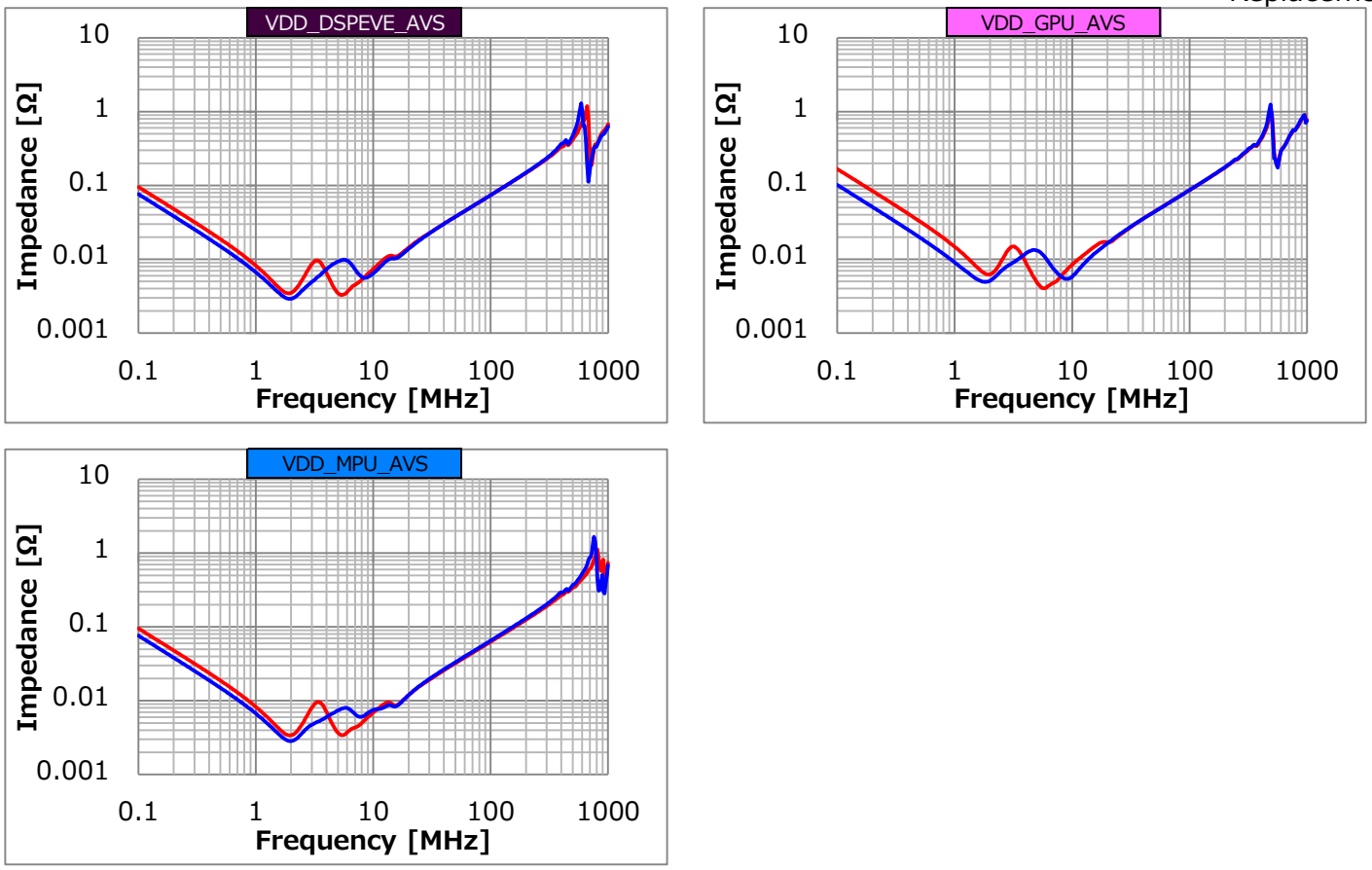


@100MHz

	Initial (mΩ)	Replacement (mΩ)	Effect (%)
VDDR_SOC_1V35	79.11	77.84	-1.62
VDDSHV_3V3	63.29	64.67	2.17
VDDS_1V8	113.6	114.1	0.44
VDD_CORE_AVS	83.42	85.43	2.41

2. Consideration of optimization

■ Result of impedance simulation – U42

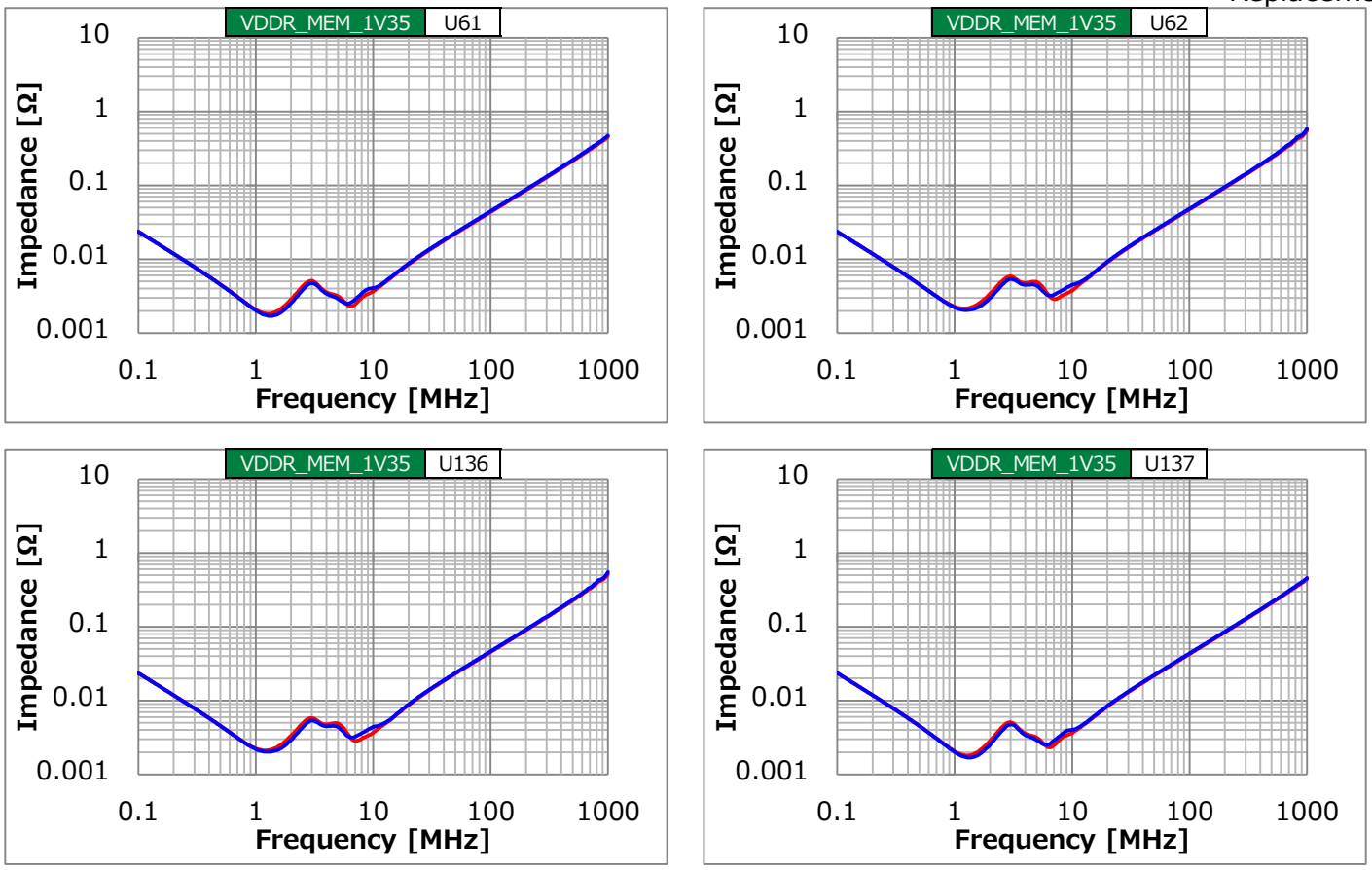


@100MHz

	Initial (mΩ)	Replacement (mΩ)	Effect (%)
VDD_DSPEVE_AVS	73.94	74.09	0.20
VDD_GPU_AVS	86.37	86.63	0.30
VDD_MPU_AVS	62.90	65.20	3.66

2. Consideration of optimization

■ Result of impedance simulation – U42



@100MHz

		Initial (mΩ)	Replacement (mΩ)	Effect (%)
VDDR_MEM_1V35	U61	43.52	44.68	2.67
VDDR_MEM_1V35	U62	47.13	48.21	2.29
VDDR_MEM_1V35	U136	42.67	43.55	2.07
VDDR_MEM_1V35	U137	45.59	46.58	2.18

Summary of Murata Proposal

<Qty> 38pcs Reduction!

Description	MPN	U42				DDR				Total	
		Top Side		Bottom Side		Top Side		Bottom Side		Initial	Proposal
		Initial	Proposal	Initial	Proposal	Initial	Proposal	Initial	Proposal		
0201 0.1uF	GCM033C70J104KE02	0	0	0	0	0	0	0	0	0	0
0201 0.22uF	GRT033C80J224KE01	0	0	0	0	8	4	40	22	48	26
0402 0.1uF	GCM155R71C104KA55	4	0	19	13	0	0	0	0	23	13
0402 0.47uF	GCM155C71A474KE36	8	5	30	24	0	0	0	0	38	29
0603 10uF	GCM188D70J106M***	0	0	0	0	0	0	4	4	4	4
0805 4.7uF	GCM21BR71C475KA73	1	1	0	0	0	0	0	0	1	1
0805 10uF	GCM21BR71A106KE22	10	8	0	1	0	0	0	0	10	9
0508 1uF	LLL215C70G105MA11	13	0	7	2	0	0	0	0	20	2
3T 0402 1uF	NFM15HC105D0G*	0	6	0	5	0	0	0	6	0	17
3T 0603 10uF	NFM18HC106D0G*	0	2	0	3	0	0	0	0	0	5
		36	22	56	48	8	4	44	32	144	106

<Space> 44.16mm2 Space Reduction!

Description	MPN	Area (mm2)	U42				DDR				Total	
			Top Side		Bottom Side		Top Side		Bottom Side		Initial	Proposal
			Initial	Proposal	Initial	Proposal	Initial	Proposal	Initial	Proposal		
0201 0.1uF	GCM033C70J104KE02	0.18	0	0	0	0	0	0	0	0	0	0
0201 0.22uF	GRT033C80J224KE01	0.18	0	0	0	0	1.44	0.72	7.2	3.96	8.64	4.68
0402 0.1uF	GCM155R71C104KA55	0.5	2	0	9.5	6.5	0	0	0	0	11.5	6.5
0402 0.47uF	GCM155C71A474KE36	0.5	4	2.5	15	12	0	0	0	0	19	14.5
0603 10uF	GCM188D70J106M***	1.28	0	0	0	0	0	0	5.12	5.12	5.12	5.12
0805 4.7uF	GCM21BR71C475KA73	2.4	2.4	2.4	0	0	0	0	0	0	2.4	2.4
0805 10uF	GCM21BR71A106KE22	2.4	24	19.2	0	2.4	0	0	0	0	24	21.6
0508 1uF	LLL215C70G105MA11	2.4	31.2	0	16.8	4.8	0	0	0	0	48	4.8
3T 0402 1uF	NFM15HC105D0G*	0.5	0	3	0	2.5	0	0	0	3	0	8.5
3T 0603 10uF	NFM18HC106D0G*	1.28	0	2.56	0	3.84	0	0	0	0	0	6.4
			63.6	29.66	41.3	32.04	1.44	0.72	12.32	12.08	118.66	74.5

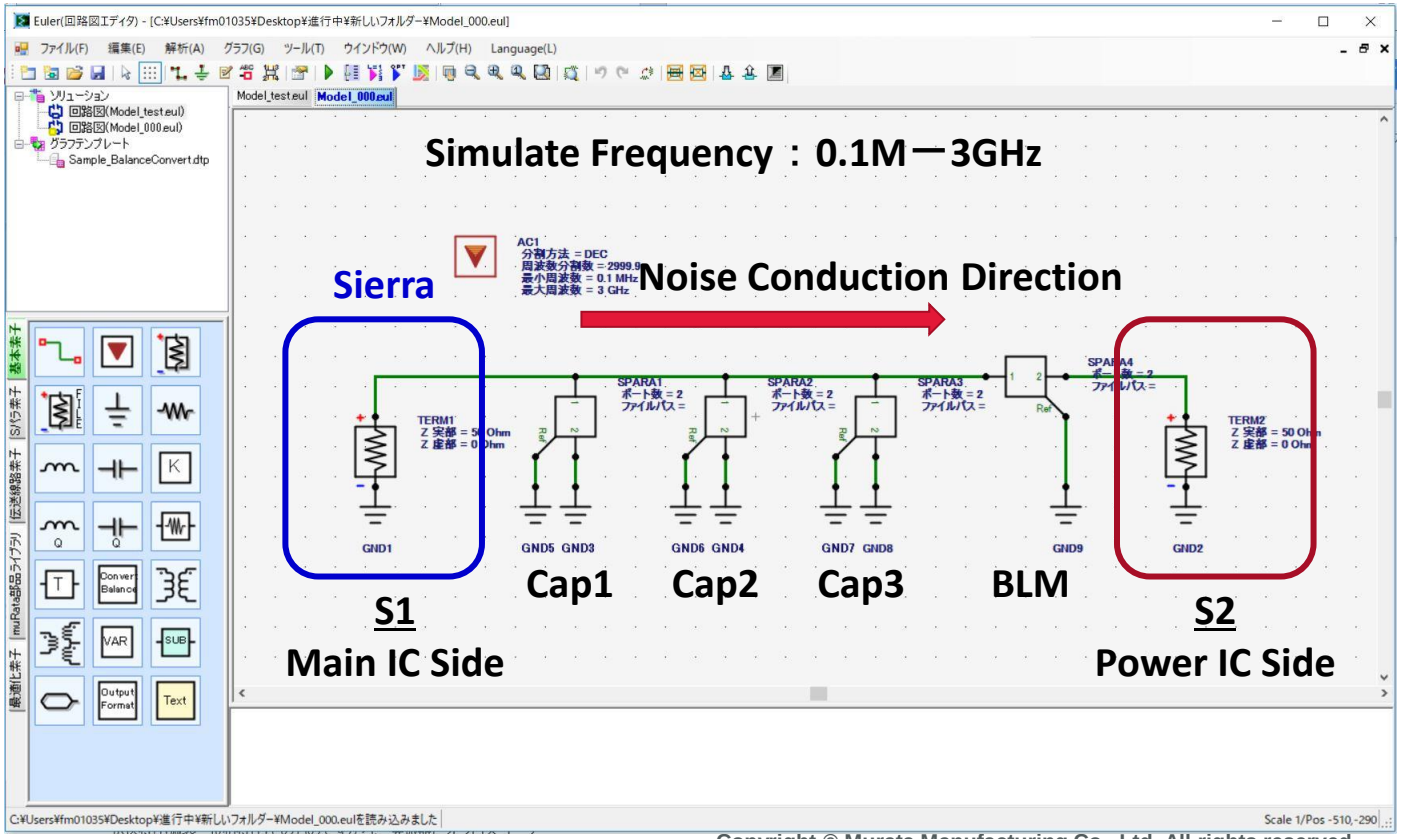
Agenda

1. Latest Murata's solution
2. Simulation result (Jacinto 6+)
3. Other topics

1. About Euler

■Simulation Method

- ▪50ohm terminal for both Input / Output
- ▪Use symbol for component in order to read Spara meter.
- ▪We estimate the noise from IC and set S21 in IC side.
  Then simulate S21 as I.L.(Insertion Loss)



2. P/N List for Simulation

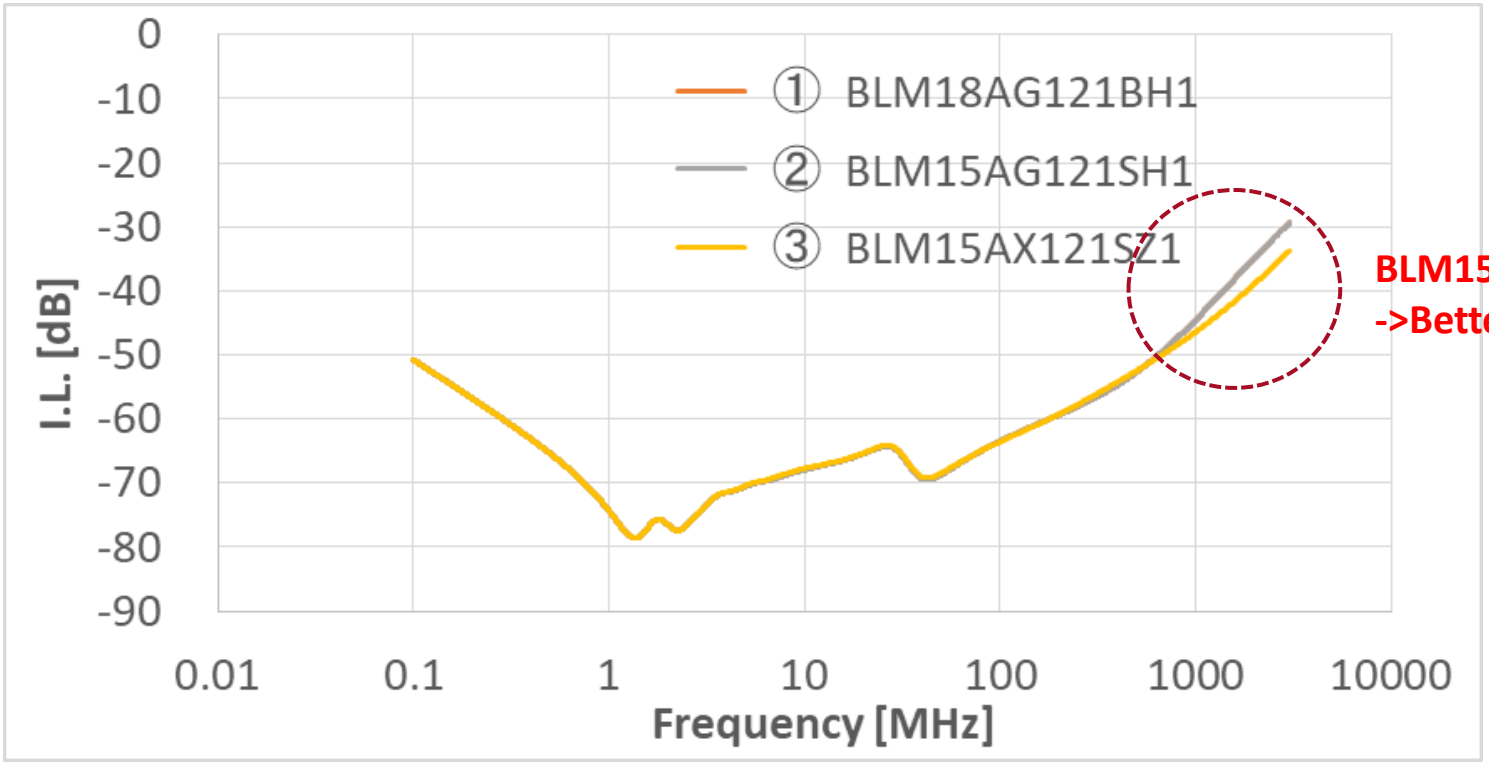
	Parts No.	Size [inch]	Characteristic
Chip Ferrite Beads	BLM18AG121BH1	0603	120ohm@100MHz
	BLM15AG121SH1	0402	120ohm@100MHz
	BLM15AX121SZ1	0402	120ohm@100MHz
MLCC	GCM033C70J104KE02	0201	0.1µF
	GCM155C71A105KE38	0402	1µF
	GCM188D70J106M	0603	10µF
	GCM21BD70J226M	0804	22µF
3-terminal LowESL MLCC	NFM15HC105D0J (*TBD)	0402	1µF
	NFM18HC106D0J (*TBD)	0603	10µF

We picked above P/Ns for the simulation.

3. Simulation Result 1)

■I.L Change Estimation by Chip Ferrite Beads

Chip Ferrite Beads			Capacitor	
Condition①	BLM18AG121BH1	×1	GCM033C70J104KE02	×1
Condition②	BLM15AG121SH1	×1	GCM188D70J106M	×1
Condition③	BLM15AX121SZ1	×1	GCM21BD70J226M	×1

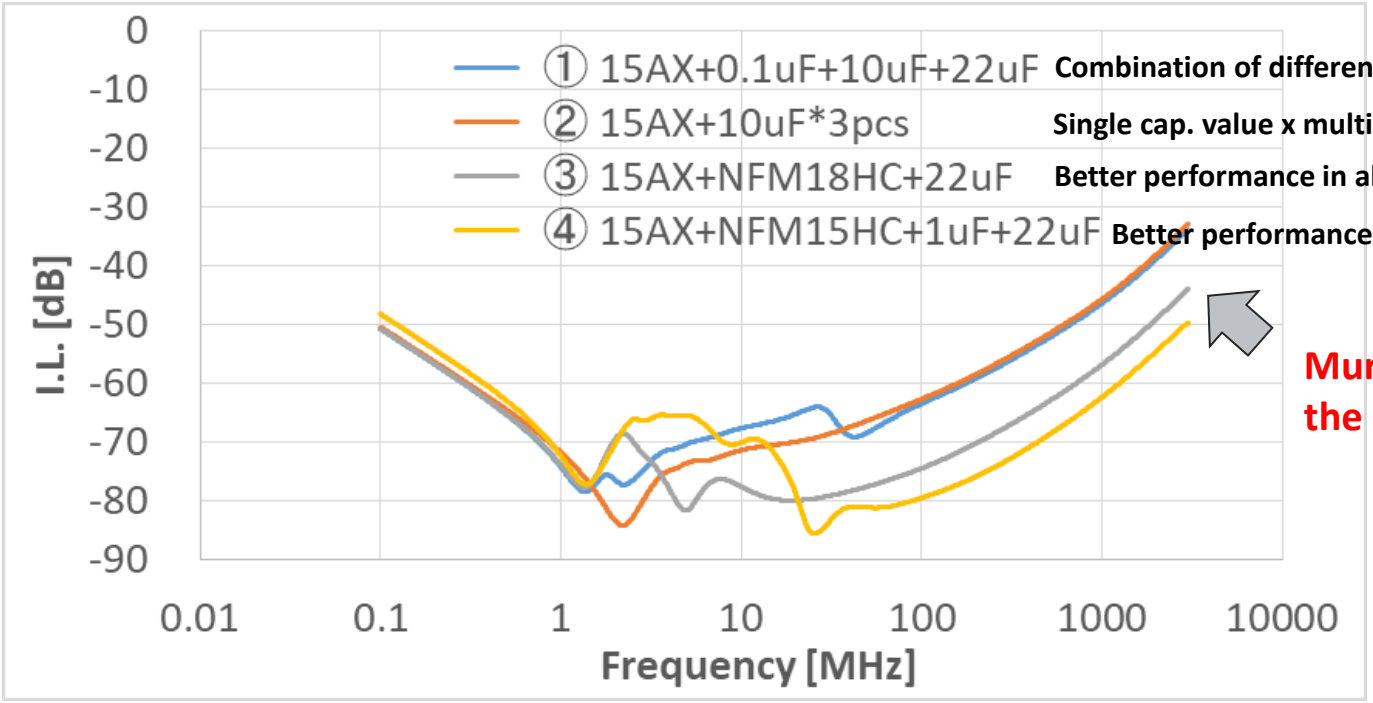


BLM15AX121SZ1
->Better I.L. around 1GHz.

3. Simulation Result 2)

■I.L Change Estimation by MLCC

Capacitor						Chip Ferrite Beads	
Condition①	GCM033C70J104KE02 GCM188D70J106M GCM21BD70J226M	×1 ×1 ×1	Condition③	NFM18HC106D0J GCM21BD70J226M	×1 ×1	BLM15AX121SZ1	×1
Condition②	GCM188D70J106M	×3	Condition④	NFM15HC105D0J GCM155C71A105KE38 GCM21BD70J226M	×1 ×1 ×1		



Combination of different cap. value creates anti-resonance.

Single cap. value x multi pcs will not create anti-resonance.

Better performance in all frequency range.

Better performance over 30MHz, but worse in 2M–30MHz.

Murata think this option is the best.

BEST PARTNER

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