

K2E SCHEMATIC

MAJOR REVISION HISTORY :

PCB REV.	SCH. REV.	DESCRIPTION	DATE
1.0	1.0	Proto Build	15-NOV-2013
2.0	2.0	Alpha Build	05-MAR-2014
2.0	2.01	Alpha ECNs Implemented	24-APR-2014
2.0	2.02	SATA ECN implemtead	06-AUG-2014
3.0	3.02	TI review comments implemented	03-NOV-2014
3.0	3.03	Top Avatar resistors value changed"	02-FEB-2015

I2C ADDRESS TABLE :

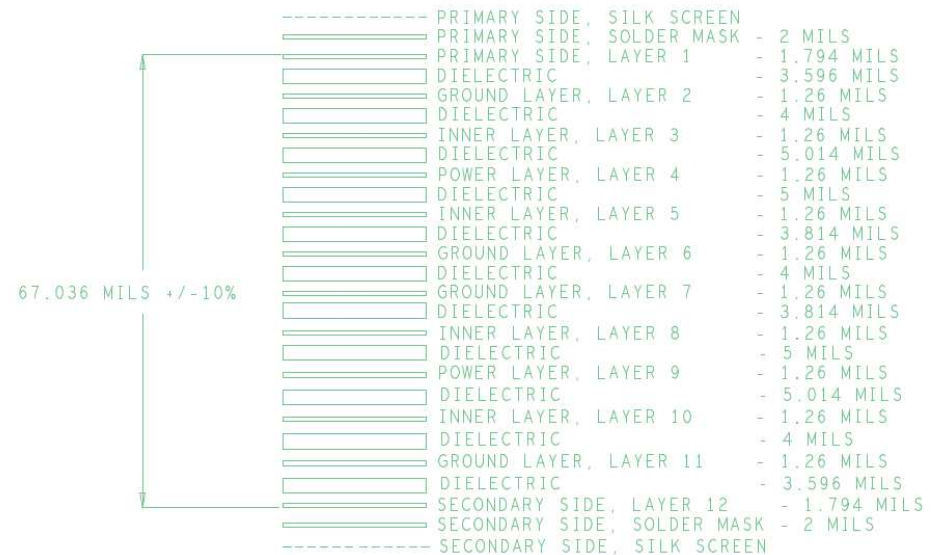
REF DES	DESCRIPTION	7 BIT ADDRESS
EEPROM1	1MBit I2C EEPROM	0x50
SODIMM	SODIMM EEPROM	0x53
U4	UCD9090	0x68

PCB MECHANICAL DETAILS :

1. PCB SIZE: 7.11" x 2.89" x 0.063"
3. NUMBER OF LAYERS: 12
4. IMPEDANCE CONTROL: YES

PCB LAYER STACK-UP DETAILS :

LAYER STACK-UP



NOTES, UNLESS OTHERWISE SPECIFIED :

1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. PARTS NOT INSTALLED ARE INDICATED WITH 'NU'.
4. SIGNAL NET NAMES WITH "#" SUFFIX, ARE ACTIVE LOW SIGNALS.


DISCLAIMER: THIS CIRCUIT DESIGN IS PROVIDED AS REFERENCE ONLY, WITHOUT WARRANTY EXPRESSED OR IMPLIED. THE USER IS ENCOURAGED TO PERFORM ALL DUE DILIGENCE WITH RESPECT TO DESIGN AND ANALYSIS. FOR COMMITTED PERFORMANCE AND FUNCTIONALITY, PLEASE REFER TO THE DEVICE DATA MANUAL.

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Title COVER PAGE			
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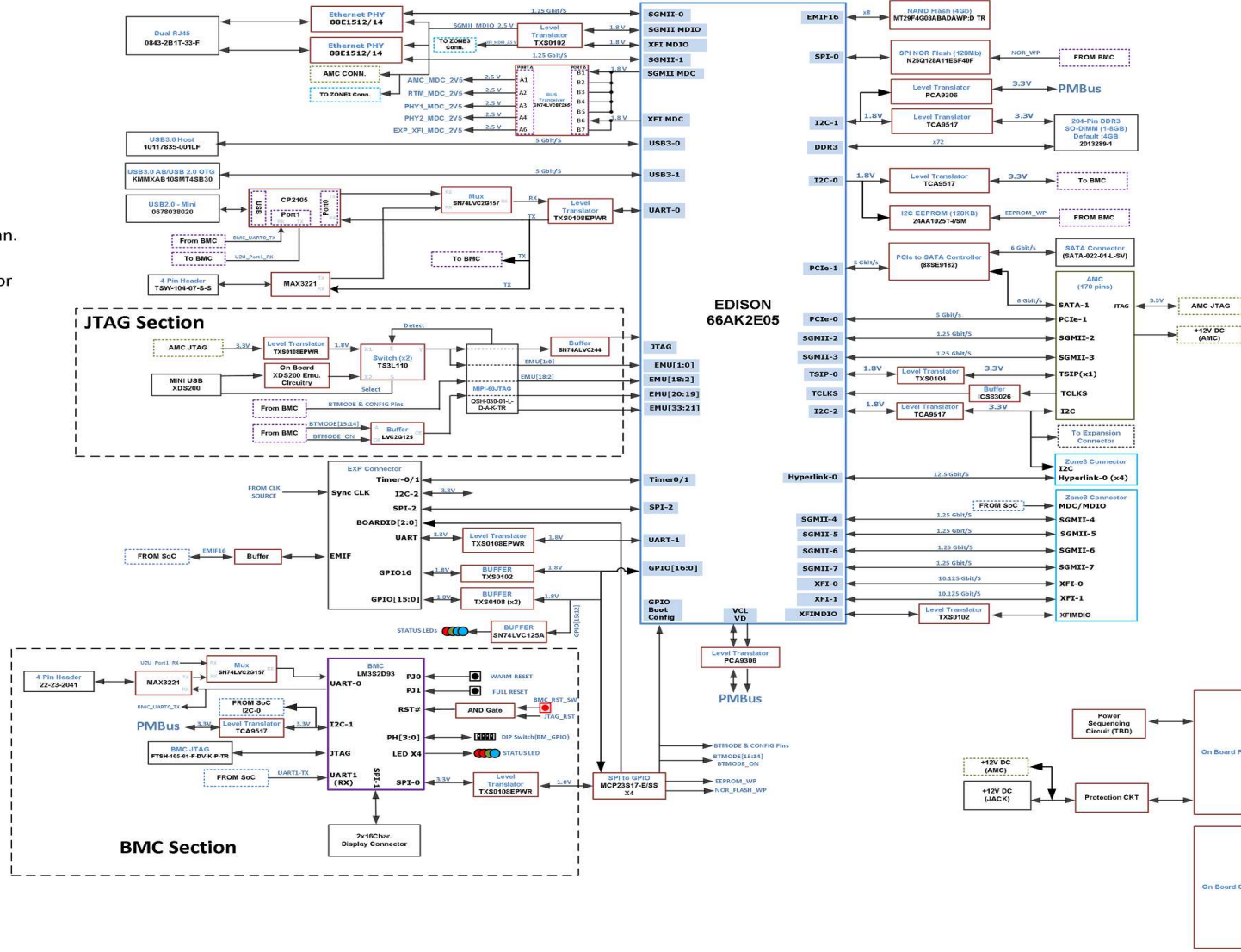
SCHEMATIC PAGE DESCRIPTION :

- 01 : COVER PAGE
- 02 : TABLE OF CONTENTS
- 03 : SYSTEM BLOCK DIAGRAM
- 04 : PLACEMENT
- 05 : POWER CONSUMPTION
- 06 : POWER SEQUENCE
- 07 : POWER DISTRIBUTION
- 08 : CLOCK DIAGRAM
- 09 : BMC BLOCK DIAGRAM
- 10 : AMC CONNECTOR
- 11 : SPI TO GPIO CONNECTOR
- 12 : SOC SGMII PCIE_MCM
- 13 : SOC XFI USB
- 14 : SOC DDR3
- 15 : EMU & JTAG
- 16 : PCIe to SATA
- 17 : SOC EMIF NAND
- 18 : MISC
- 19 : SOC CLOCK & Smart-Reflex
- 20 : SOC POWERA
- 21 : SOC POWERB
- 22 : SOC GND
- 23 : CLOCK SOURCE--1
- 24 : CLOCK SOURCE--2
- 25 : DDR3 SODIMM AND BMC LCD
- 26 : SGMII Ethernet PHY
- 27 : BMC LM3S2D93
- 28 : BMC MISC
- 29 : mTCA ZD3/120-pin Exp.
- 30 : POWER SUPPLY--1
- 31 : POWER SUPPLY-2
- 32 : XDS200_1
- 33 : XDS200_2
- 34 : XDS200_3
- 35 : XDS200_POWER
- 36 : XDS200_EMULATION
- 37 : REVISION HISTORY

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Title TABLE OF CONTENTS			
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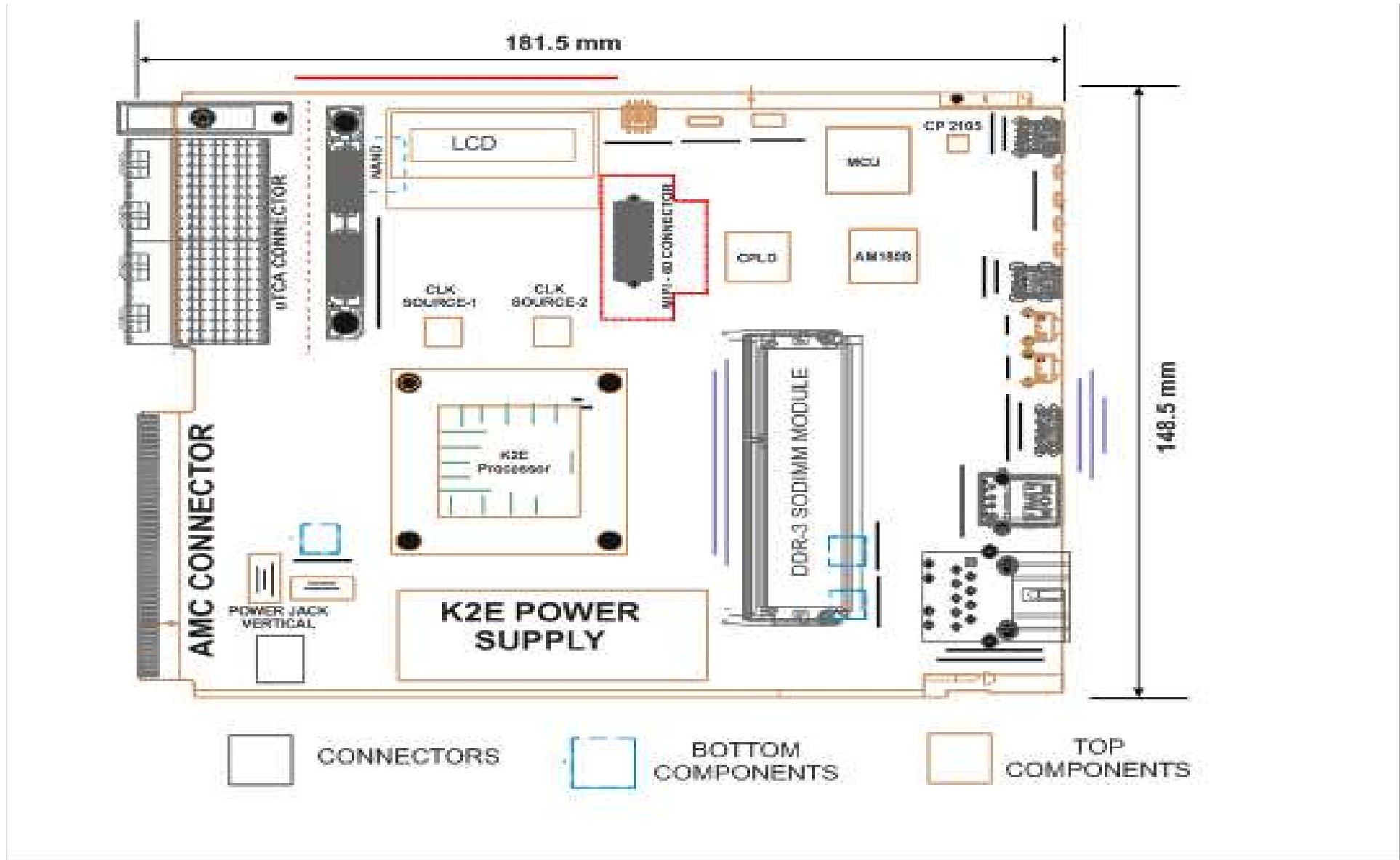
K2E EVM BLOCK DIAGRAM



- K2E SoC
- ICs
- Connectors
- Expansion Conn.
- AMC Connector
- BMC
- Zone 3 Conn.



Project K2E EVM		Designed for TI by elnfochips	
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PLACEMENT




Project		K2E EVB		Designed for TI by elfochips	
Title		PLACEMENT		  <small>The Solutions People</small>	
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POWER CONSUMPTION

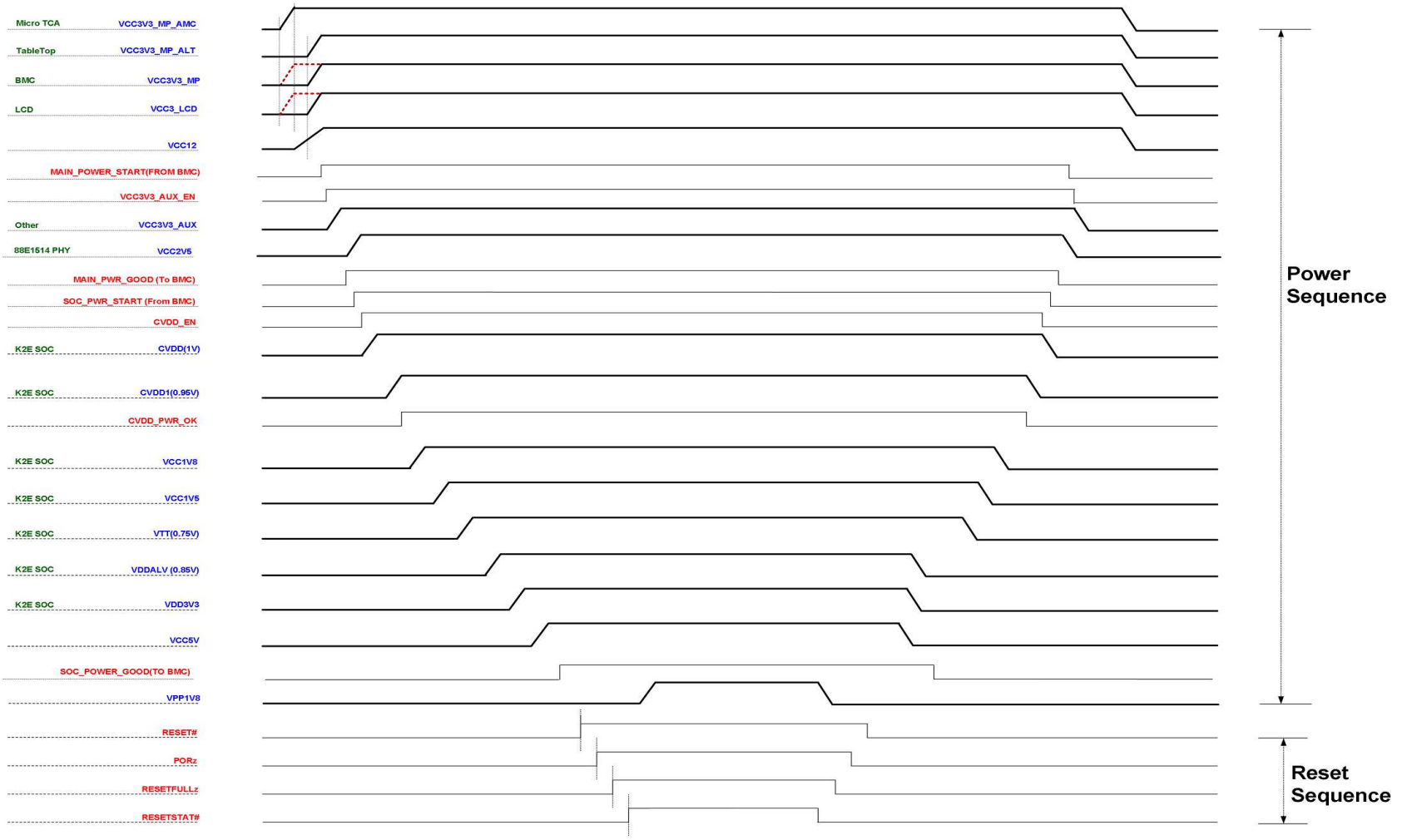
Approx Power Consumption for TI_EVM - EDISON														
Components Part No.	Description	Quantity Per Board	Current Consumed by corresponding device on power supply (mA)											Total Power (mW)
			0.75	0.85	0.95	1	1.5	1.8	2.5	3	3.3	3.3	5	
			VTT	AVDDS	CVDD1	CVDD	VCC1V5	VCC1V8	VCC2V5	VCC3V3_LCD	VCC3V3_ALT	VCC3V3_AUX, VDD3V3		
66AK2E05	Processor	1		800	1800	16000	800	400				50		20475
MT29F4G08ABDAHC-D	NAND flash	1						100						180
MT18KSF51272HZ-1G4	DDR3 SODIMM Module	1	600				2088					20		3648
LCD	LCD display	1								45				135
LM3S2D93	Microcontroller	1									136			448.8
88E1512	Gigabit ethernet phy	2						8			418			1379.4
88SE9182	PCIe to SATA controller	1						663						1193.4
CP2105	USB to UART Controller	1										20		66
N25Q128A11BSF40F	SPI EEPROM	1						20						36
MCP23S17T-E/SS	Microchip	4						3				1		8.7
CDCM6208	Reference Clock generator	2										640		2112
	XDS200 circuitry	1											130	650
USB	USB 3.0	1											908	4540
SATA	SATA 3.0 HDD	1											1400	7000
	FAN	1											100	1200
	Misc	1					100	100				100	100	1160
Total Current on individual power supply (mA)			600	800	1800	16000	2988	1286	8	45	554	831	2538	100
10% margin added over design (mA)			660	880	1980	17600	3286.8	1414.6	8.8	49.5	609.4	914.1	2791.8	110
Power Consumption in (mW)			495	748	1881	17600	4930.2	2546.28	22	148.5	2011.02	3016.53	13959	1320



TPS51200: 1.5V to 0.75V	660.00mA
LM26430: 12V to 0.85V	77.92mA
LM26430: 12V to 0.95V	195.94mA
TPS544B24: 12V to 1.0V	1725.49mA
TPS54620: 12V to 1.5V	573.66mA
LM26430: 12V to 1.8V	241.13mA
APL431: 3.3V to 3.0V	52.94mA
TPS73701: 3.3V to 2.5V	7.84mA
TLV1117-33CDCY: 12V to 3.3V	609.40mA
LM26430: 12V to 3.3V	289.06mA
TPS54620: 12V to 5.0V	1264.40mA
Total Current @ 3.3V :	
	0.97A
Total Current @ 5V :	
	2.79A
Total Current @ 12V :	
	5.09A
Total Power :	
	61.04W

Note :
1) Power consumption for 66AK2E05 is taken as TDP @ 90C & 1.4GHz* (worst case)

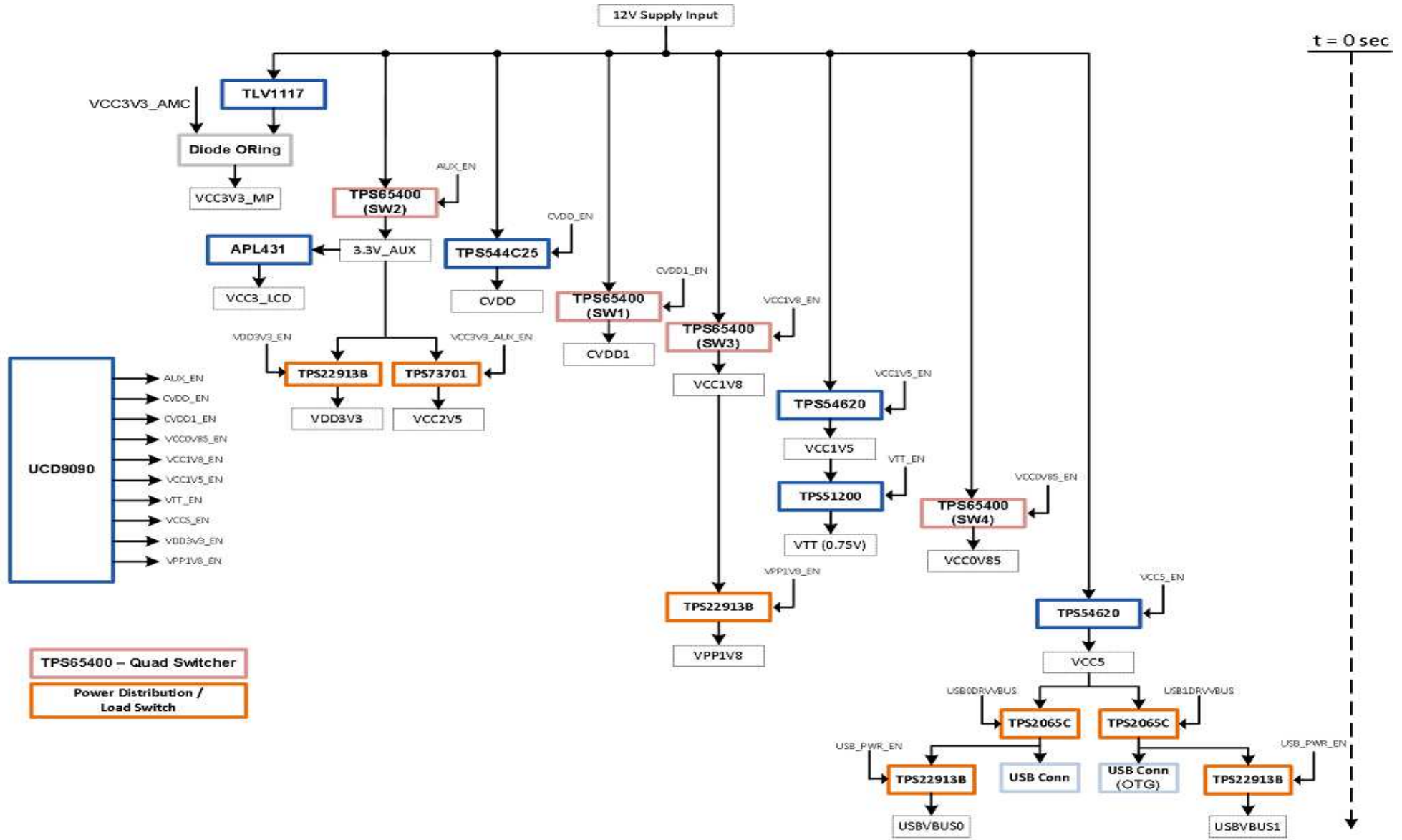
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Title POWER CONSUMPTION			
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K2E_EVM (EDISON) -- POWER SEQUENCE



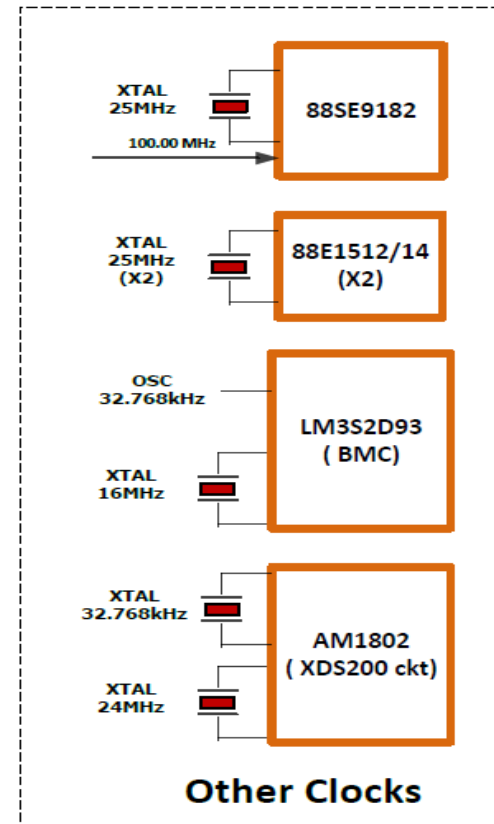
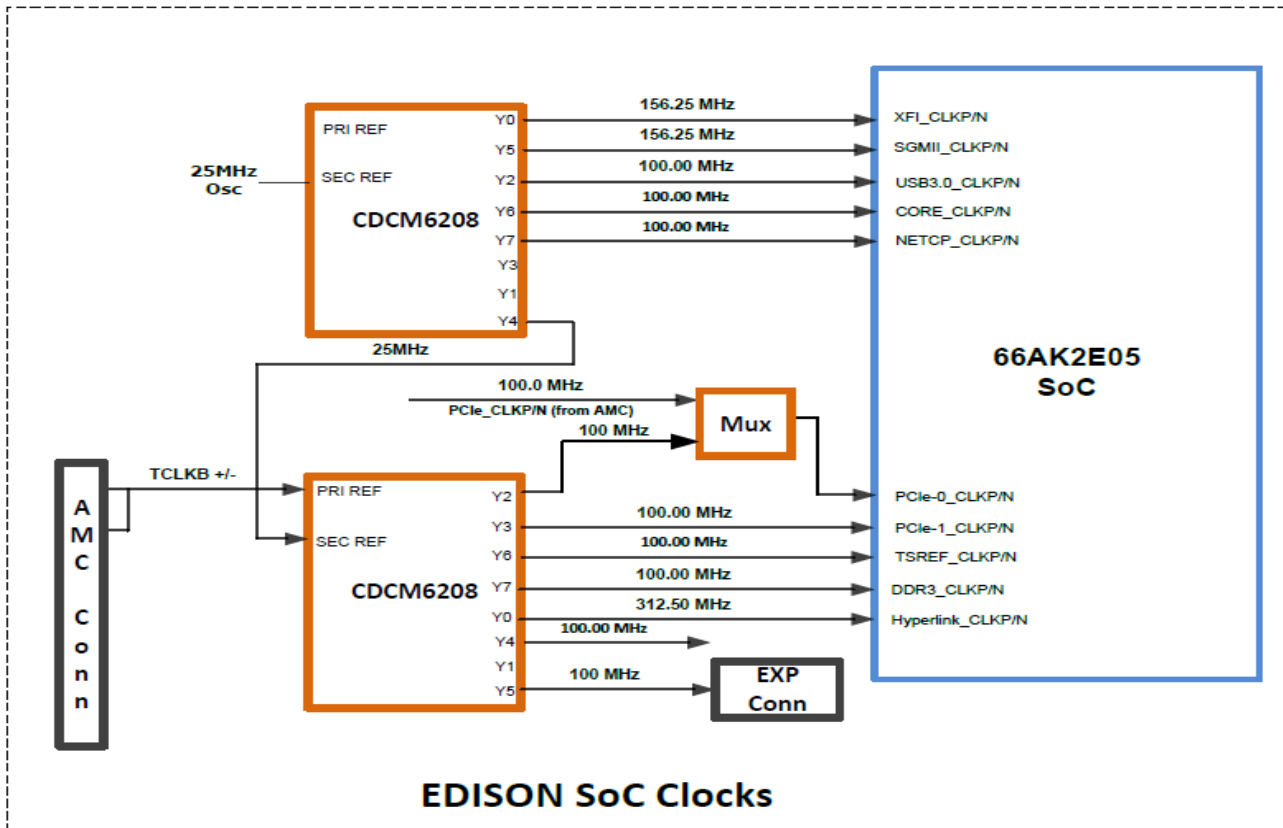
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Title POWER SEQUENCING		  <small>The Solutions People</small>	
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EDISON – Power Tree



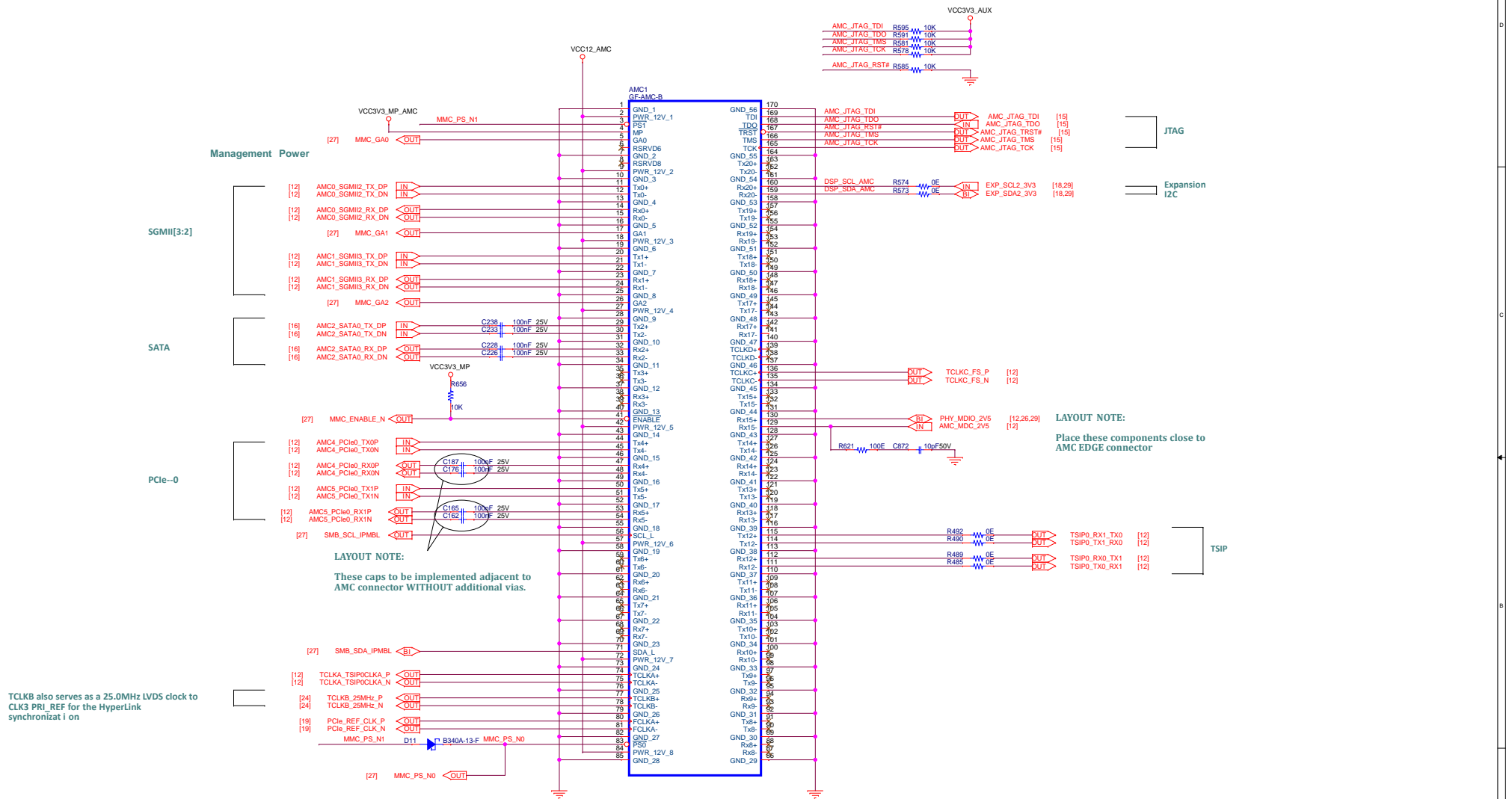
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Title POWER DISTRIBUTION			
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EDISON CLOCK GENERATION



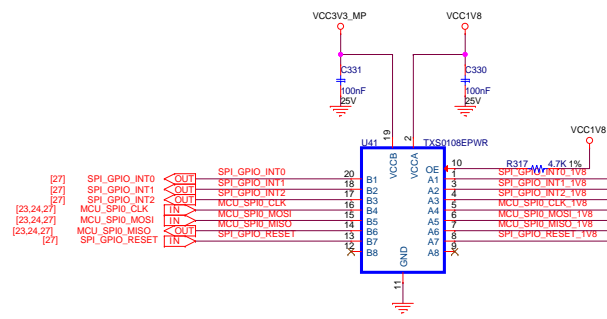
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Title CLOCK DIAGRAM			
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AMC EDGE CONNECTOR



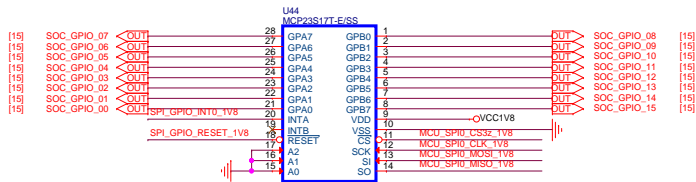
Project K2E EVM		Designed for TI by einfochips	
Title AMC INTERFACE			
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SPI LEVEL SHIFT 3V3 to 1V8



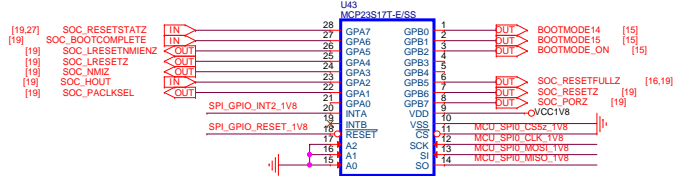
SPI TO GPIO

1.8V Level

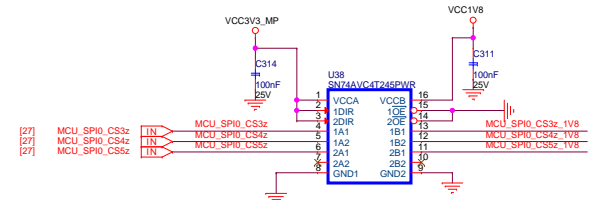
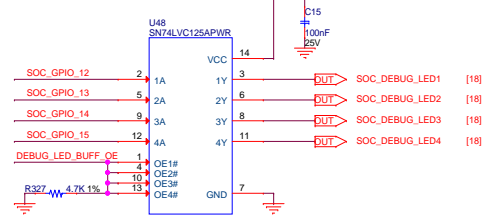
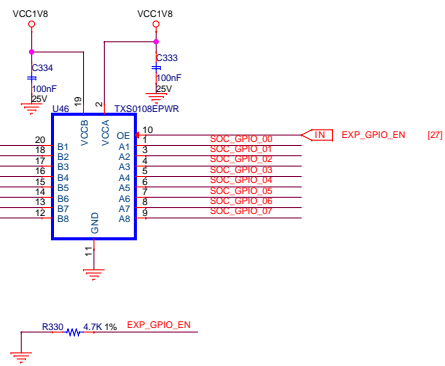
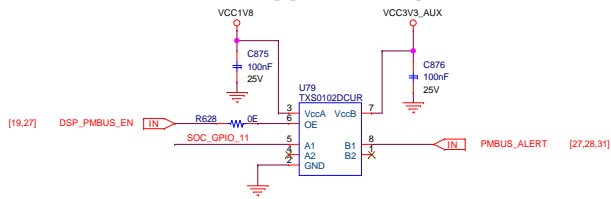


SPI TO GPIO

1.8V Level

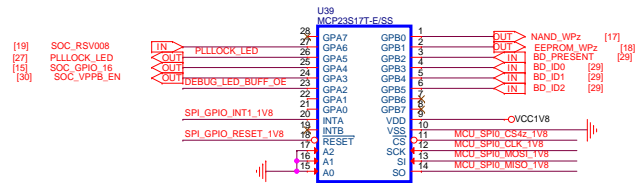


PMBUS ALERT BUFFER



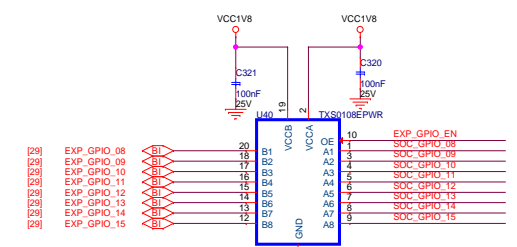
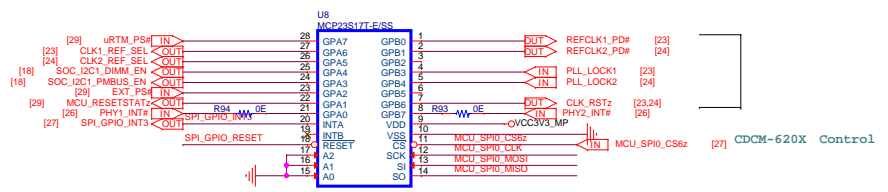
SPI TO GPIO

1.8V Level



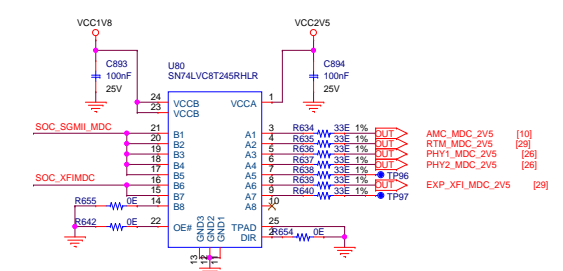
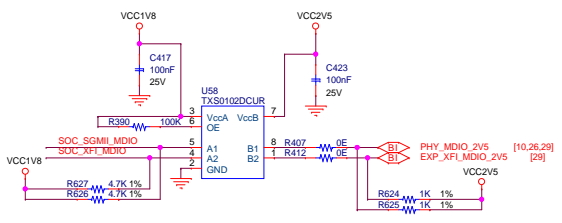
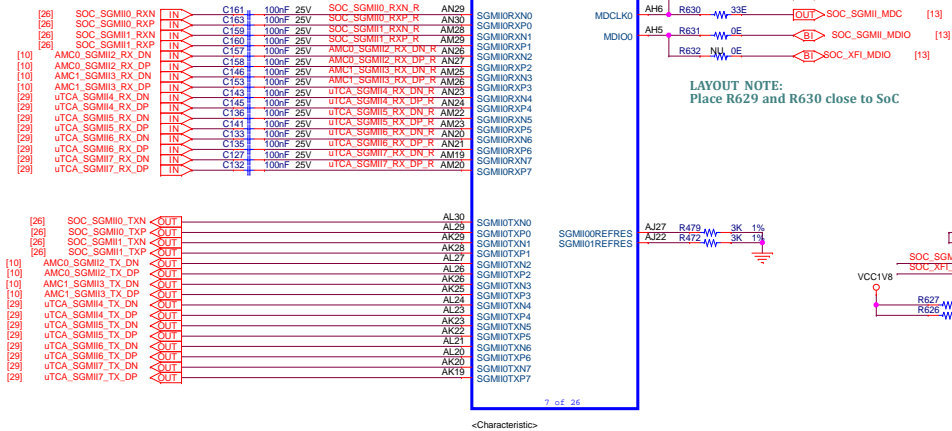
SPI TO GPIO

3.3V Level

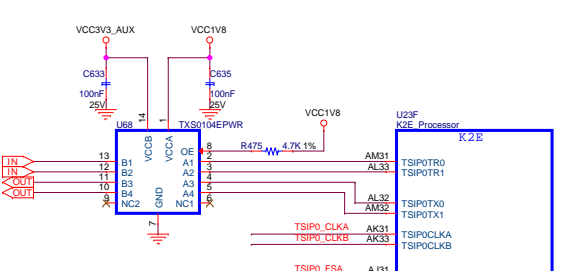
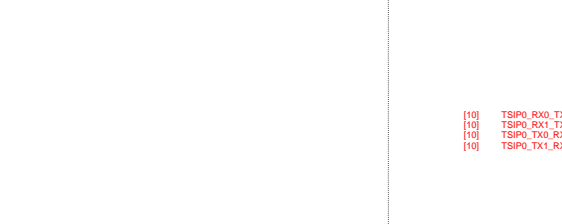
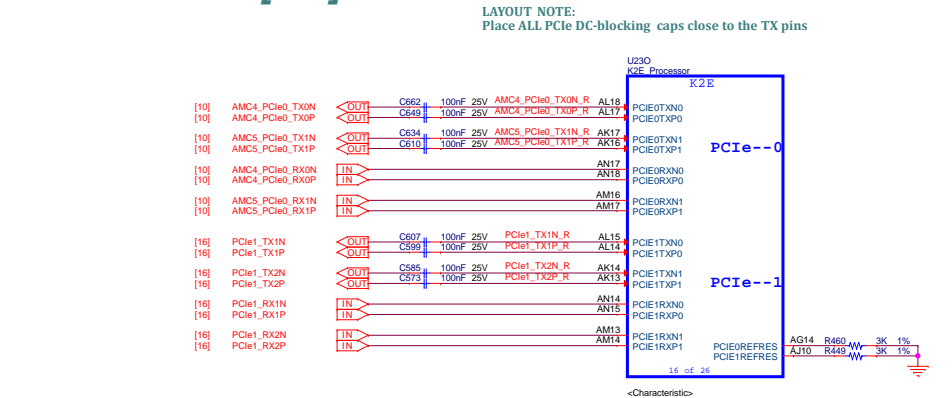


Project K2E EVM		Designed for TI by einfochips	
Title SPI to GPIO Converter			Rev 3.03
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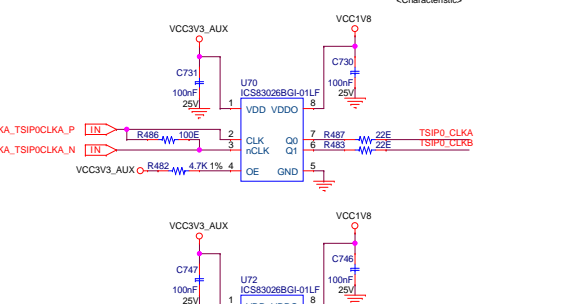
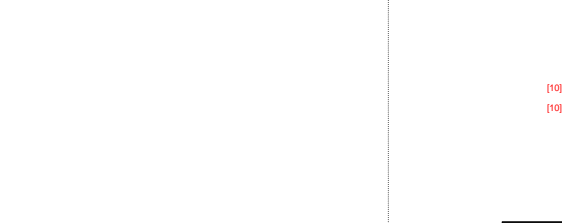
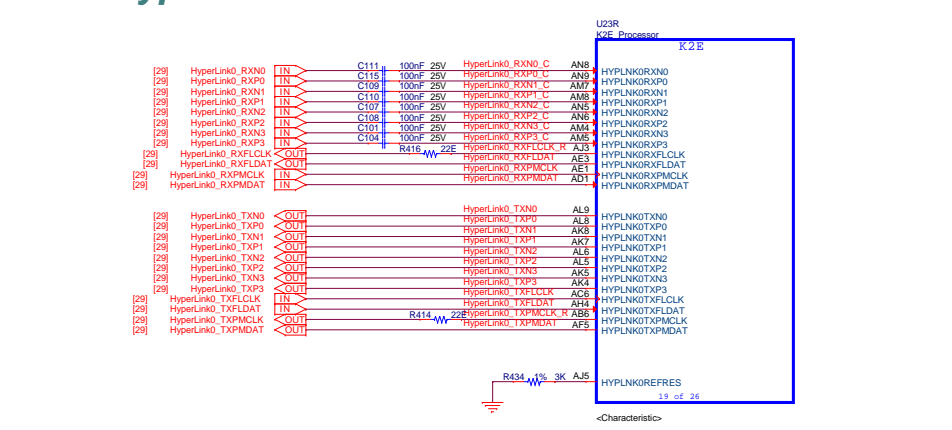
SGMII X8



PCIE[1:0] X2

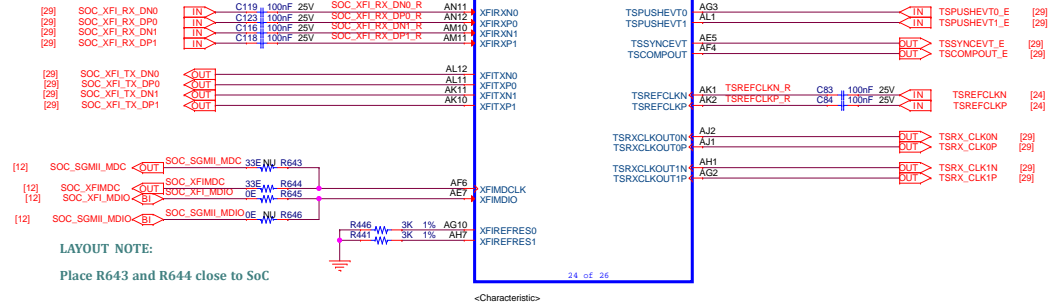


HyperLink X4

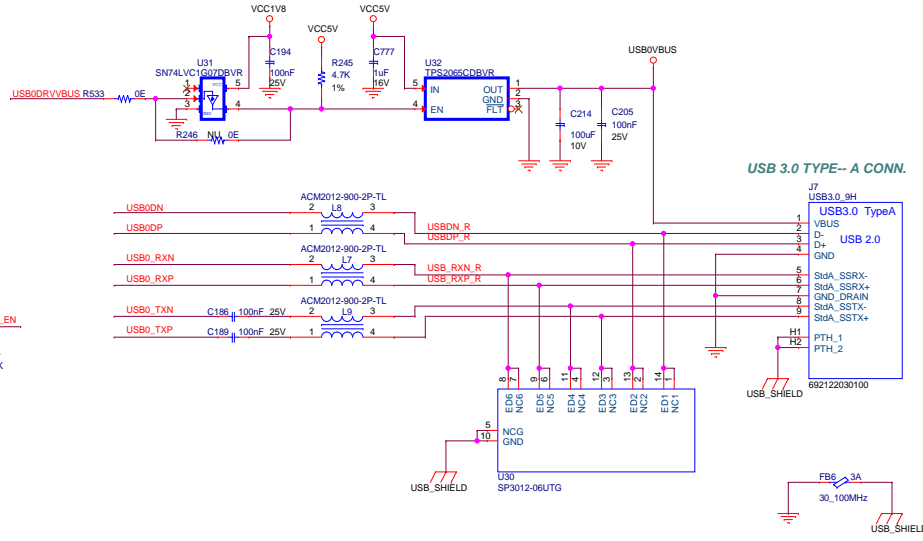
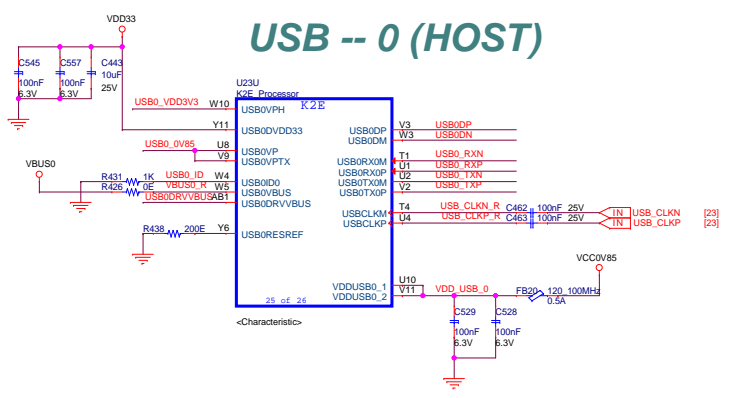


Project K2E EVM		Designed for TI by elfinohips	
Title SERDES INTERFACE			
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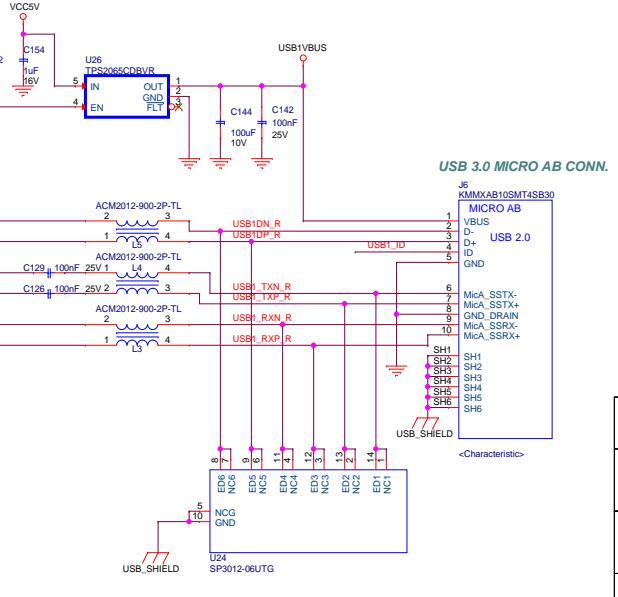
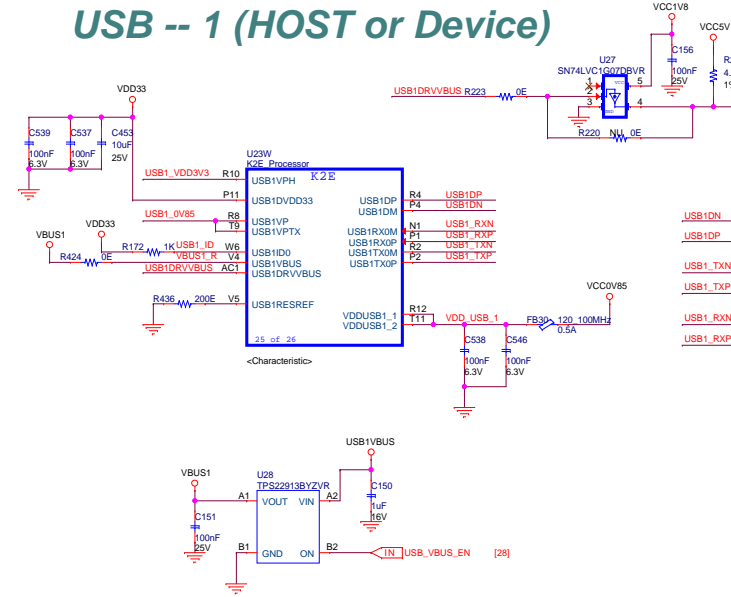
XFI X2



USB -- 0 (HOST)

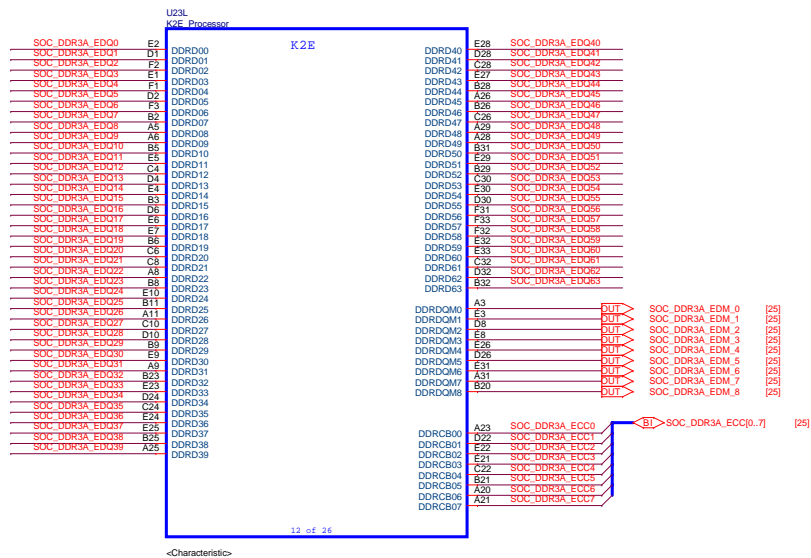
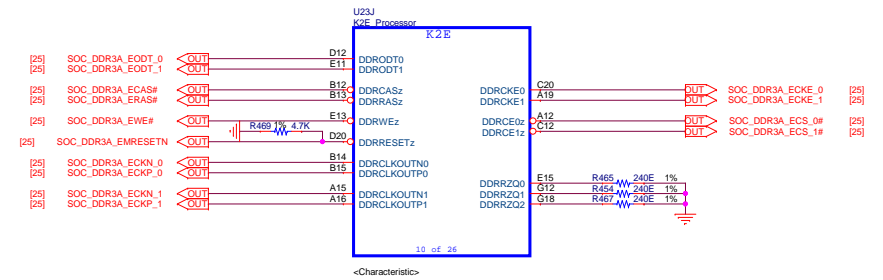
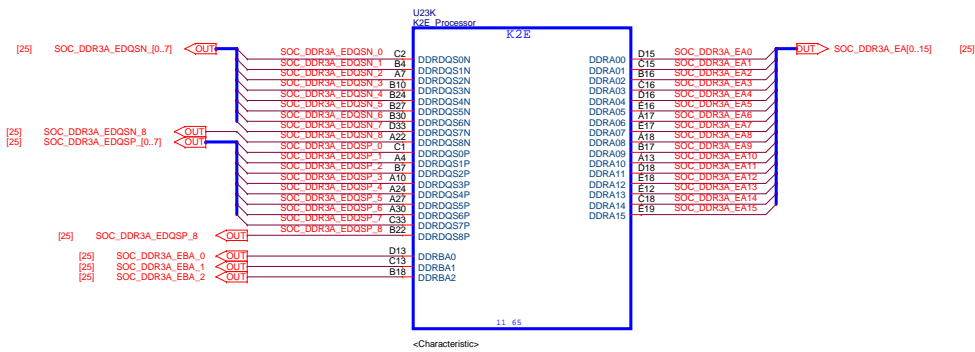


USB -- 1 (HOST or Device)



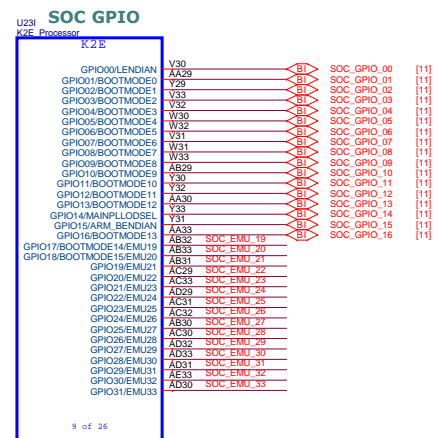
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Title SoC_XFI_USB			
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SOC DDR3

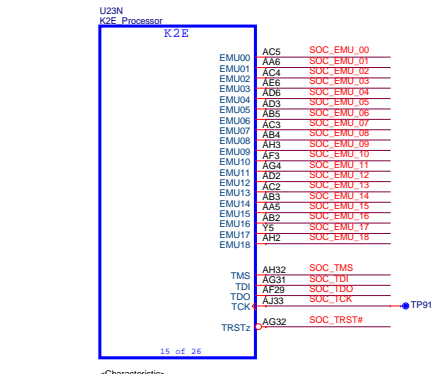
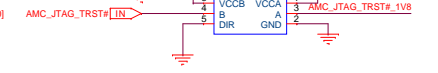
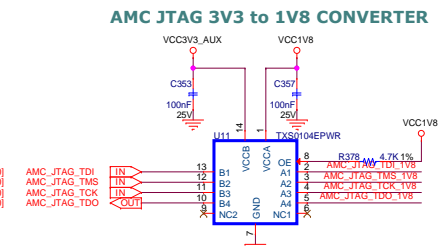


SOC_DDR3A_EDQ[0..63] [25]

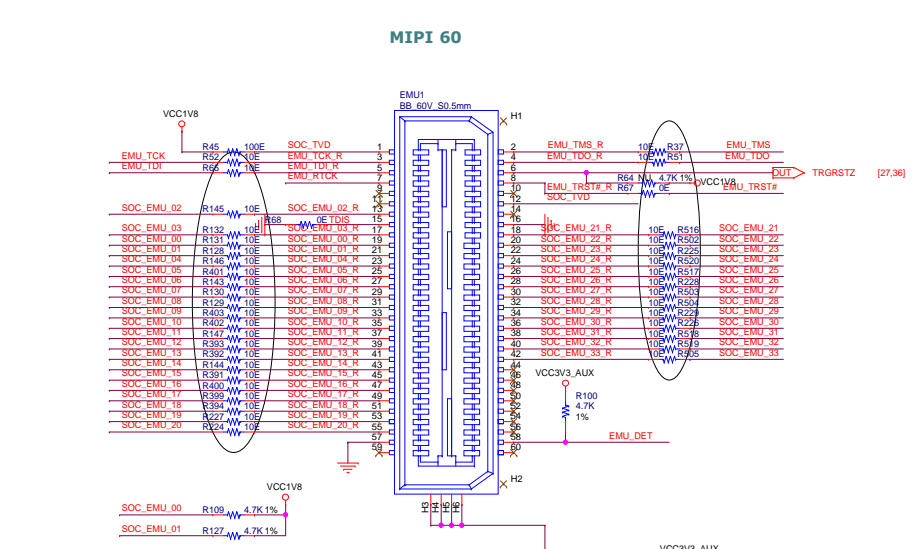
Project K2E EVM		Designed for TI by elfin chips	
Title SoC DDR3			
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<Characteristics>



<Characteristics>

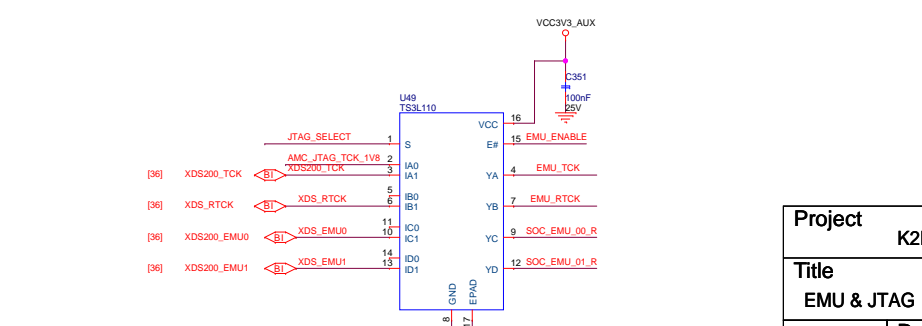
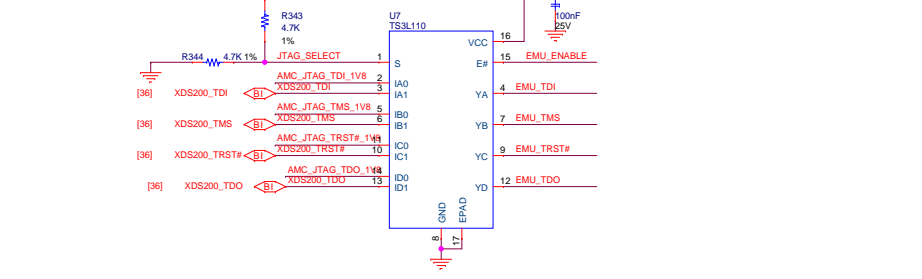


LAYOUT NOTE:

- Place termination resistors for EMU_TCK, TDI, TMS as close to MIPI-60 header as possible
- Place termination resistors for SOC_TDO and SOC_EMU* signals as close to the SoC as possible

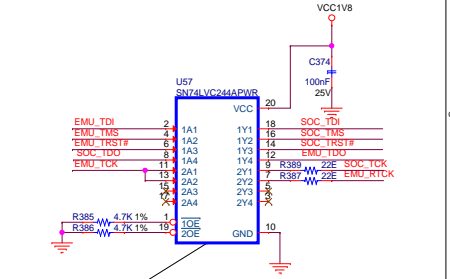
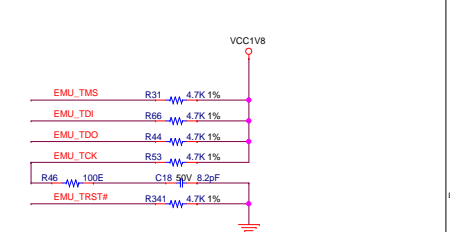
LAYOUT NOTE:

- Termination resistors for SOC_TCK and EMU_RTCK should be placed as close to U57 as possible



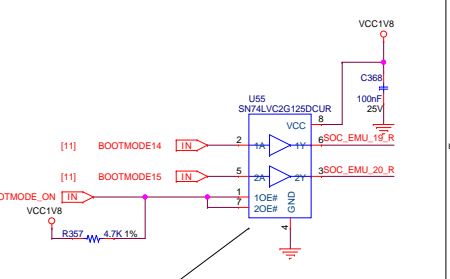
LAYOUT NOTE:

- Place U49 as close to MIPI-60 header as possible to minimize stubs on SOC_EMU_00_R and SOC_EMU_01_R



LAYOUT NOTE:

- Termination resistors for SOC_TCK and EMU_RTCK should be placed as close to U57 as possible

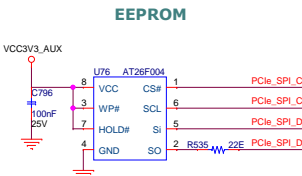
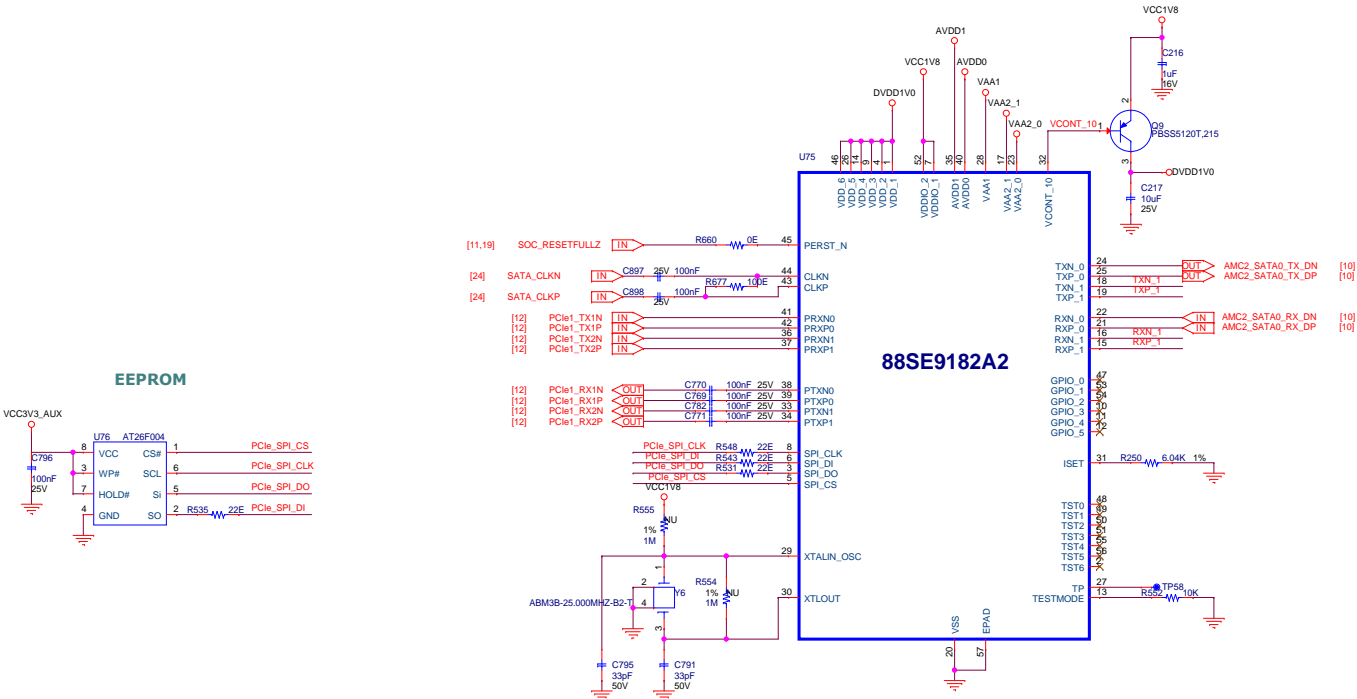


LAYOUT NOTE:

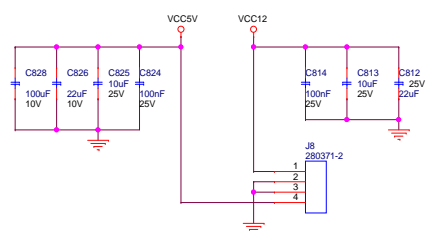
- Place U55 as close to MIPI-60 header as possible to minimize stubs on SOC_EMU_19_R and SOC_EMU_20_R

Project K2E EVM		Designed for TI by einfochips	
Title EMU & JTAG			
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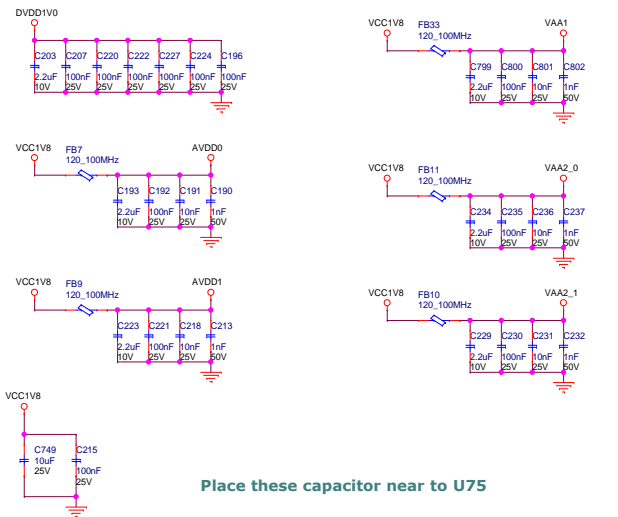
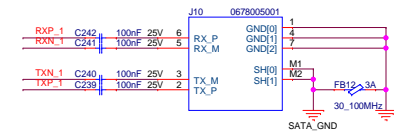
PCIe TO SATA CONTROLLER



SATA Power Connector



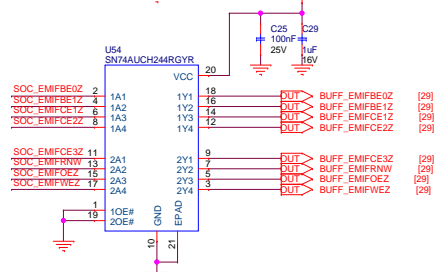
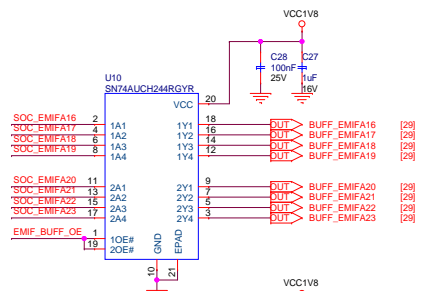
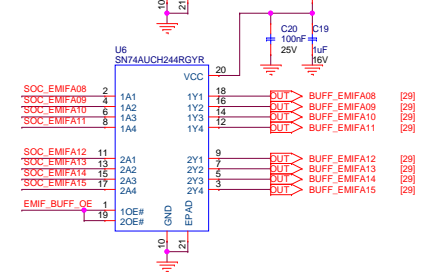
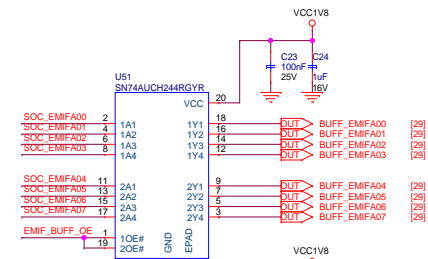
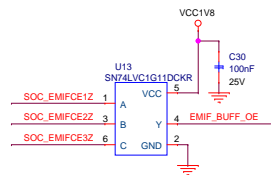
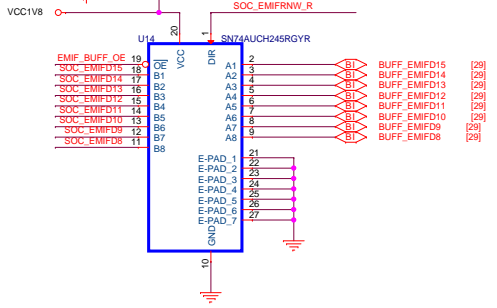
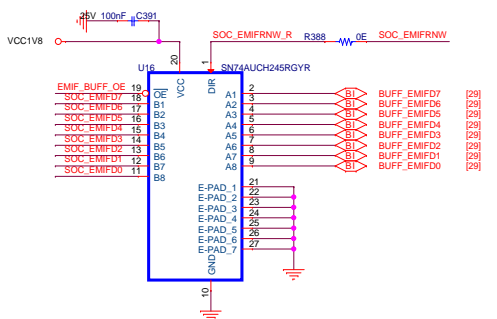
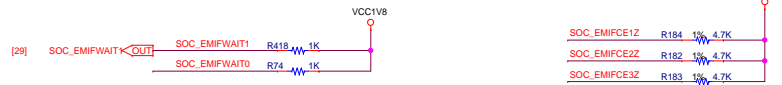
SATA DATA Connector



Place these capacitor near to U75

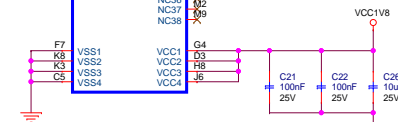
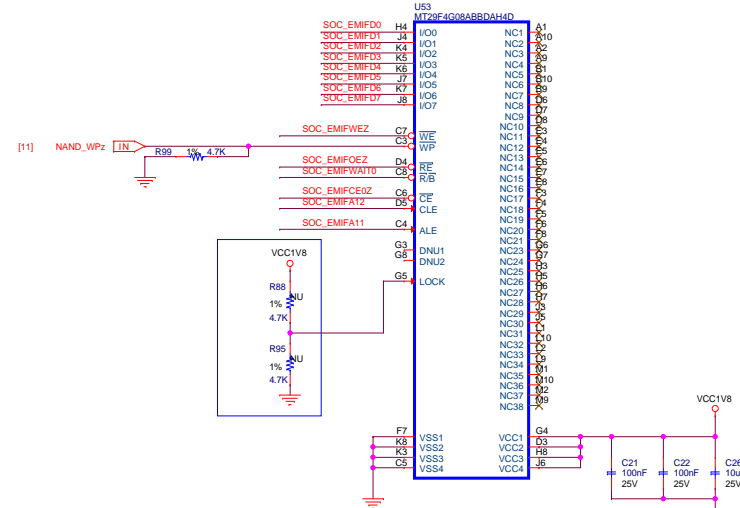
Project K2E EVM		Designed for TI by elnfochips	
Title PCIe to SATA		<small>The Solutions People</small>	
Size C	Document Number 16_00175_03	Rev 3.03	
Date: Monday, February 02, 2015		Sheet	16 of 37

SOC EMIF

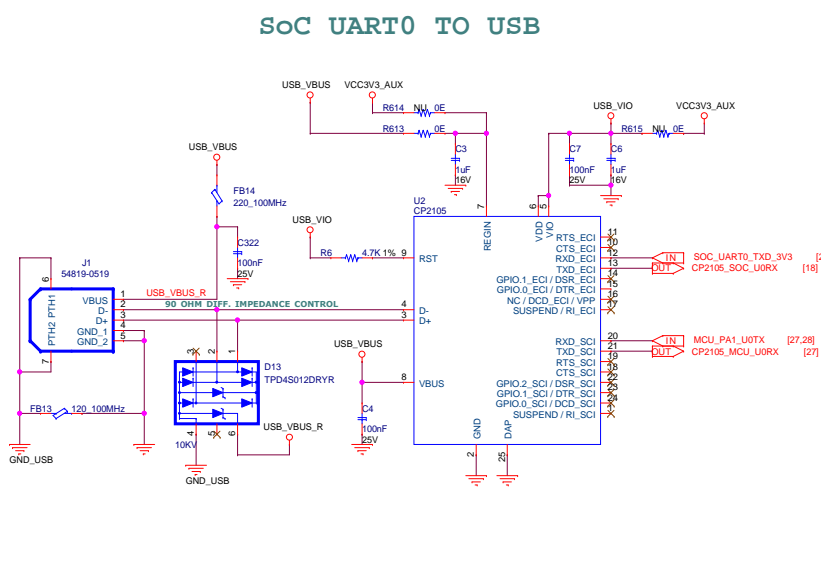
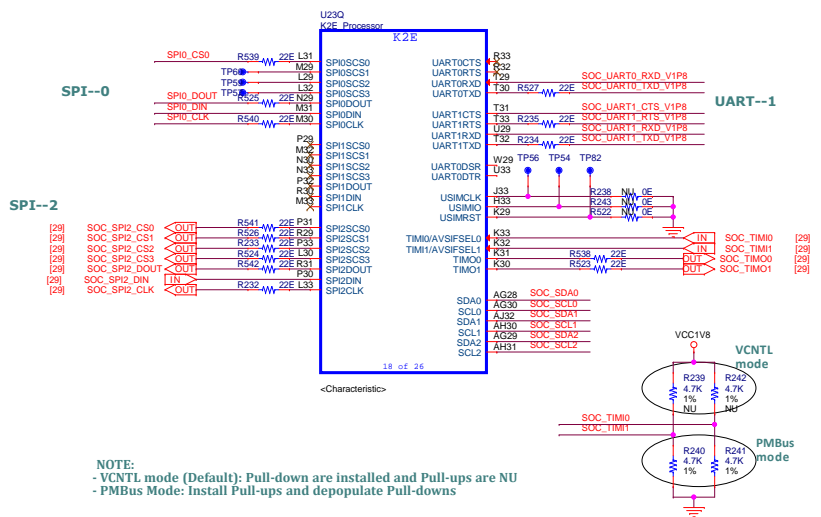


NAND FLASH

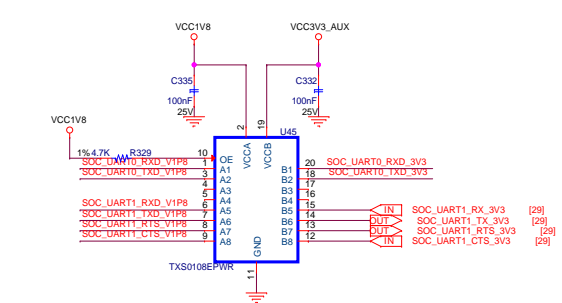
Note: NAND FLASH Device size is 4Gb.



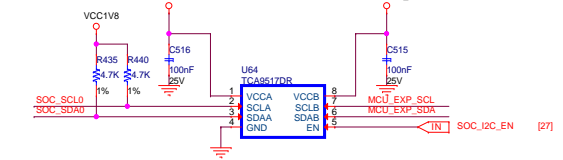
Project K2E EVM		Designed for TI by einfochips	
Title SoC_EMIF_NAND INTERFACE			
Size C	Document Number 16_00175_03	Rev 3.03	
Date: Monday, February 02, 2015		Sheet 17 of 37	



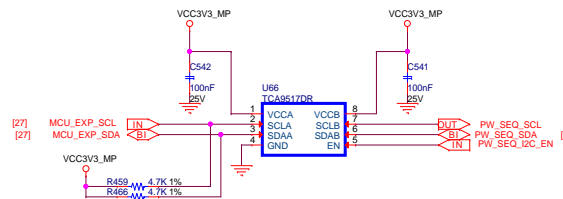
UART 1V8 to 3V3 CONVERTER



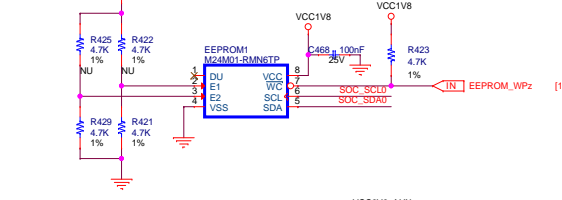
I2C--0 1V8 to 3V3 CONVERTER



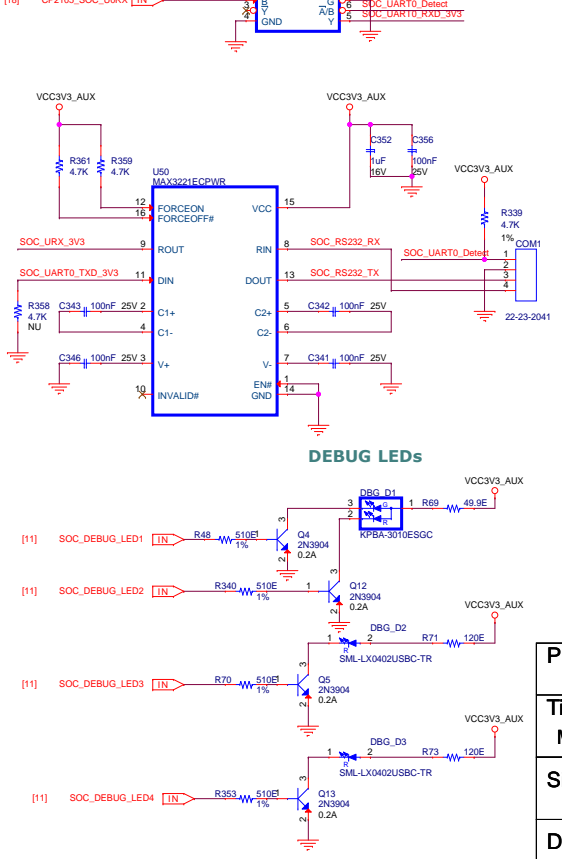
I2C--1 1V8 to 3V3 CONVERTER



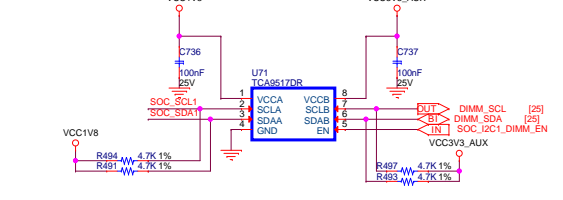
I2C EEPROM



DEBUB LEDs



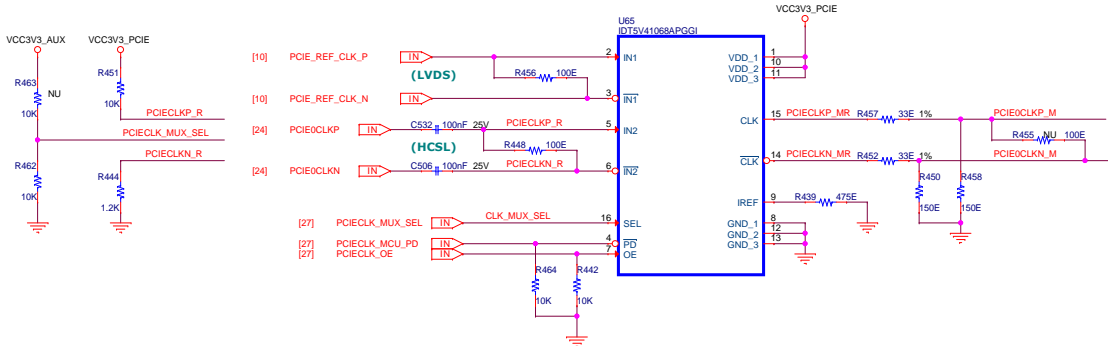
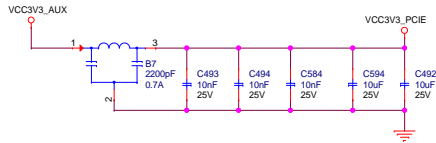
I2C--2 1V8 to 3V3 CONVERTER



Project		Designed for TI by einfochips	
Title			
MISC			
Size	Document Number	Rev	
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PCI CLOCK MUX

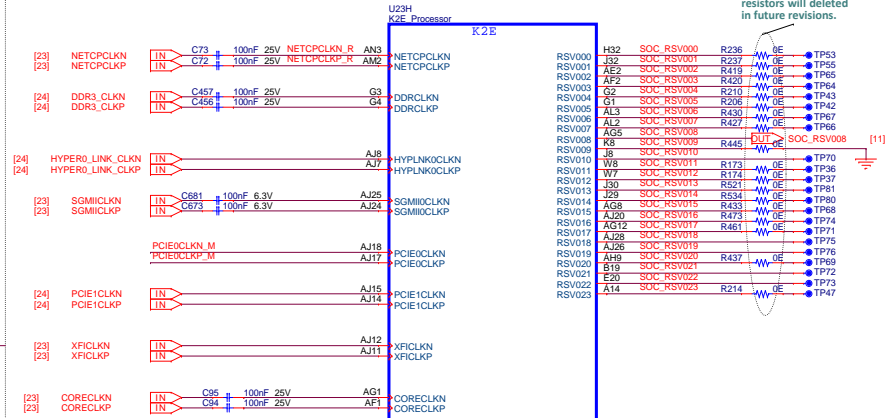
SEL	I/p PAIR SEL
LOW	IN2/IN2#
HIGH	IN1/IN1#



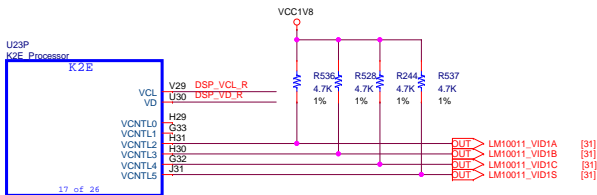
SOC REFERENCE CLOCK

All blocking capacitors should be placed near SOC to keep connect i ng routes short and minimize vias

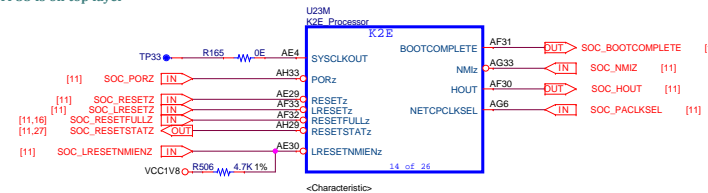
NOTE: These series resistors will be deleted in future revisions.



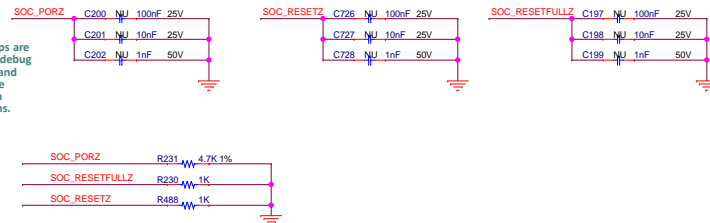
SMART REFLEX



LAYOUT NOTE:
Make sure that TP33 is on top layer

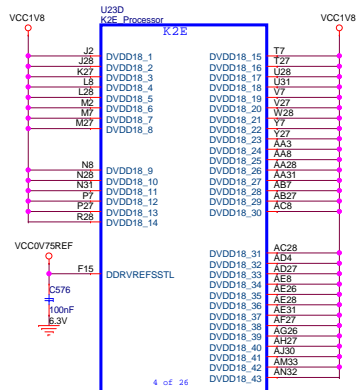


NOTE: These caps are for early silicon debug purposes ONLY and SHOULD NOT be implemented on customer designs.

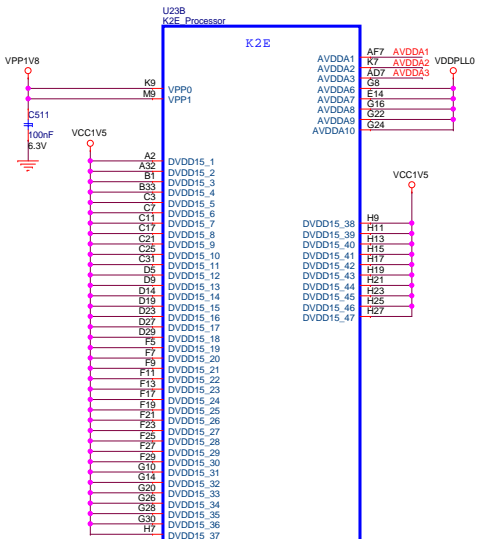
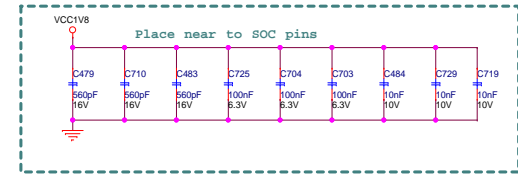
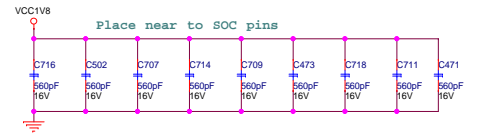
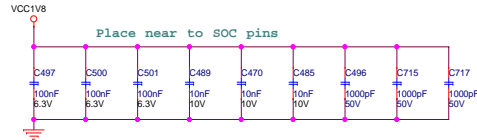
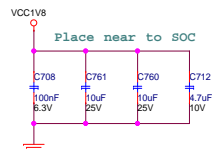


Project K2E EVM		Designed for TI by einfochips	
Title CLOCK and SMART REFLEX			
Size C	Document Number 16_00175_03	Rev 3.03	
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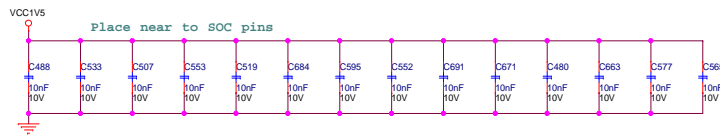
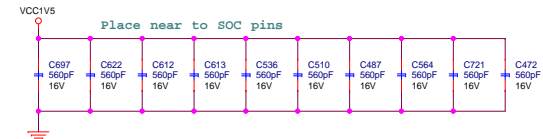
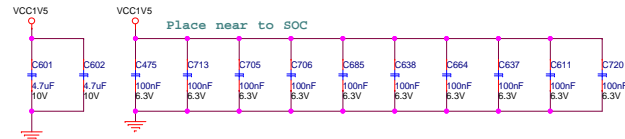
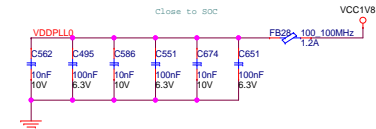
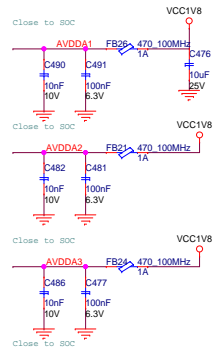
SOC POWER



<Characteristic>



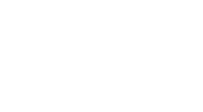
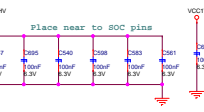
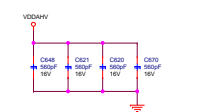
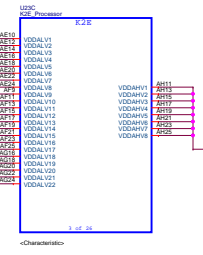
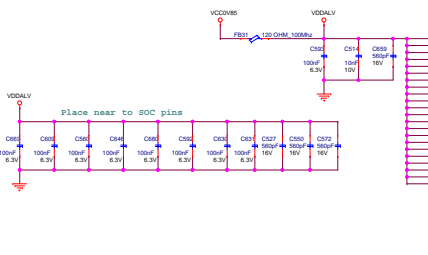
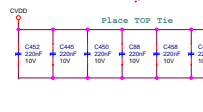
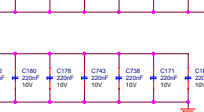
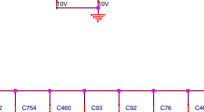
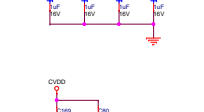
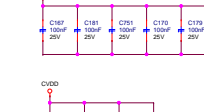
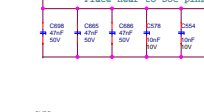
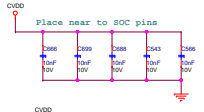
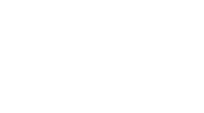
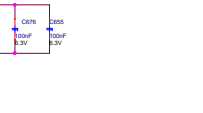
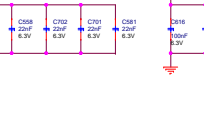
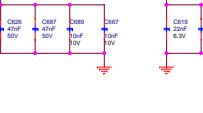
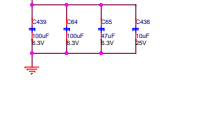
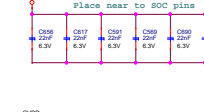
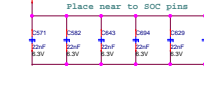
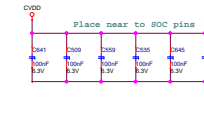
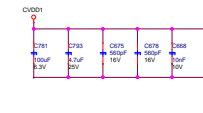
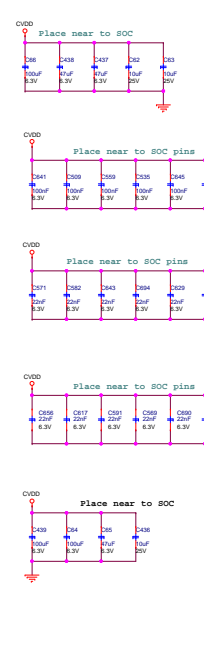
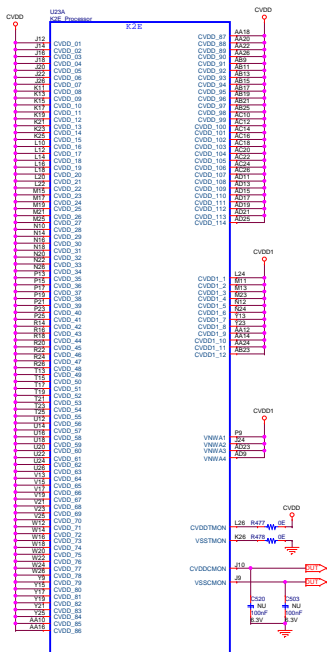
<Characteristic>



Project K2E EVM		Designed for TI by elnfochips	
Title SOC_POWERA			
Size C	Document Number 16_00175_03	Rev 3.03	
Date: Monday, February 02, 2015		Sheet 20 of 37	

0.85V - 1.05V (Smart Reflex)

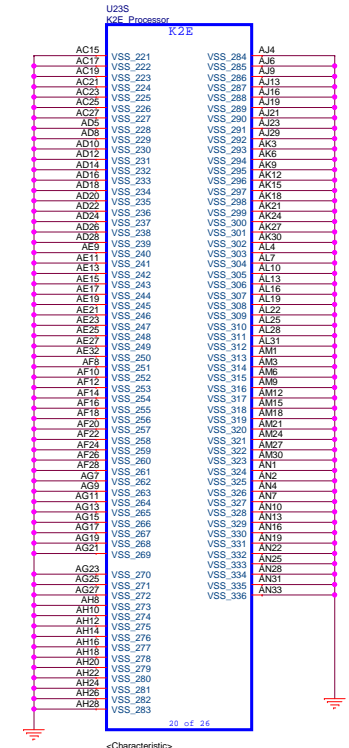
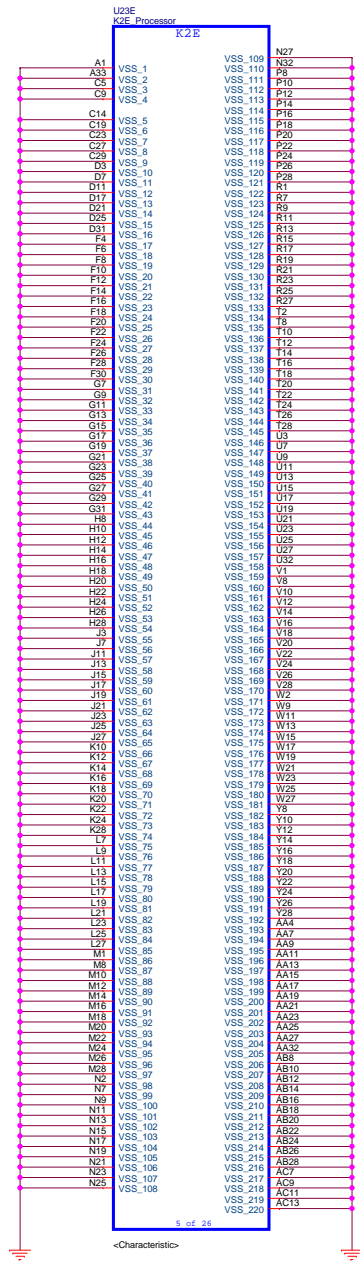
SOC POWER



THESE CAPS ARE ADDED FOR PROVISION ONLY. VALUES CAN BE CHANGED BASED ON PI ANALYSIS RESULT

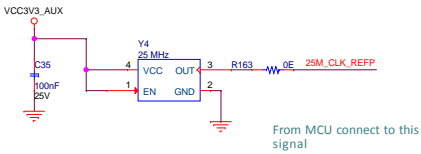
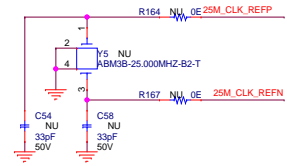
Project K2E EVM		Designed for TI by elnfochips	
Title SoC_POWERB			
Size D	Document Number 16_00175_03	Rev 3.03	
Date: Monday, February 02, 2015		Sheet 21 of 37	

SOC GROUND

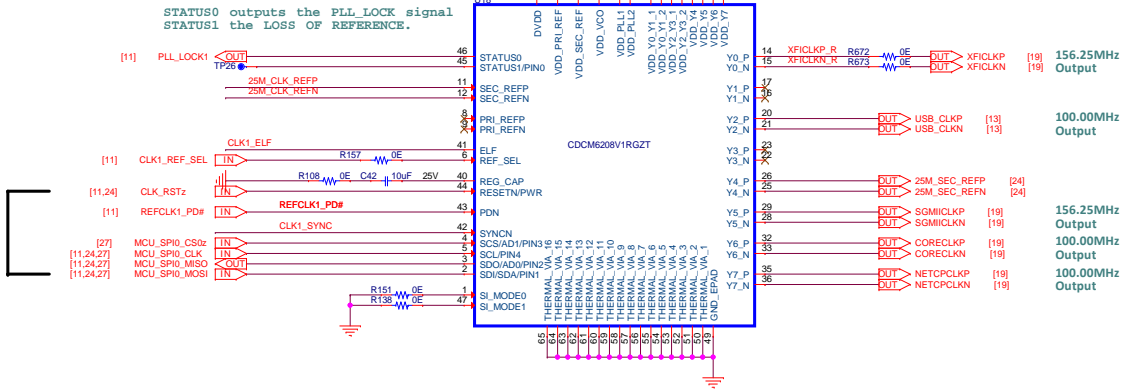


Project K2E EVM		Designed for TI by elfochips	
Title SoC Ground			
Size C	Document Number 16_00175_03	Rev 3.03	
Date: Monday, February 02, 2015		Sheet 22 of 37	

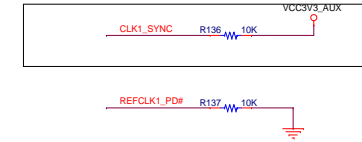
CLOCK SOURCE-- 1



From MCU connect to this signal



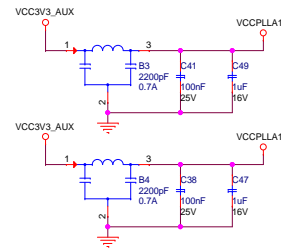
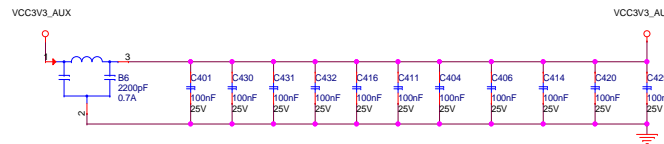
pull-up resistor



Synthesizer mode (high loop bandwidth)
CDCM6208V1
With C1=100pF, R2=500, C2=22nF and
Internal components R1=100, C3=42.2spF,
fFPD=25MHz, and ICP=2.5mA
Loop bandwidth = (337kHz)

Serial Interface Mode or Pin Mode Selection

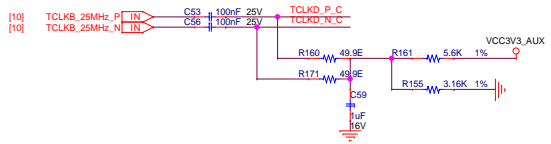
MCU_SI_MODE[1:0]	DESCRIPTION
00	SPI MODE (Default)
01	I2C MODE
10	PIN MODE (NO SERIAL PROGRAMMING)
11	RESERVED



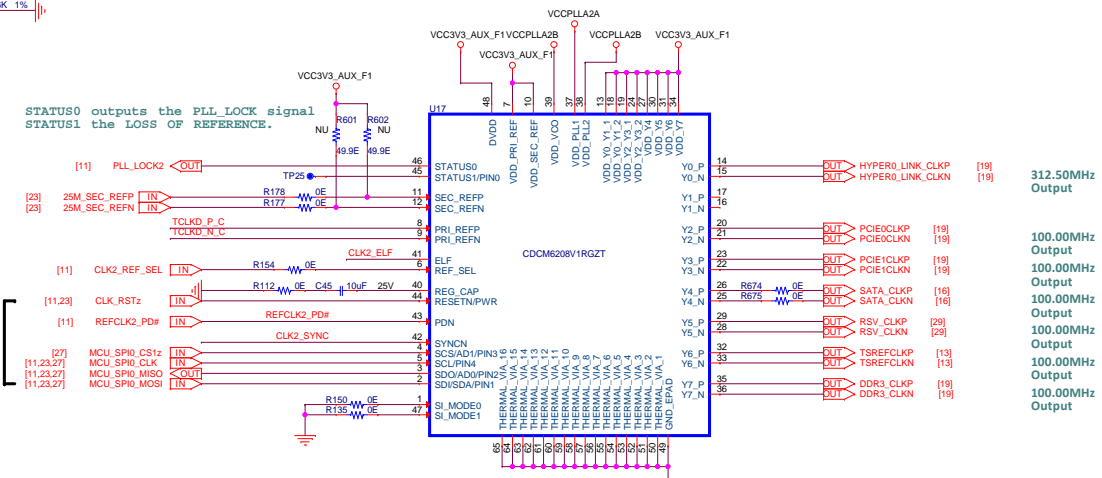
Project K2E EVM		Designed for TI by einfochips	
Title CLOCK SOURCE-- 1			
Size C	Document Number 16_00175_03	Rev 3.03	
Date: Monday, February 02, 2015		Sheet 23 of 37	

CLOCK SOURCE --2

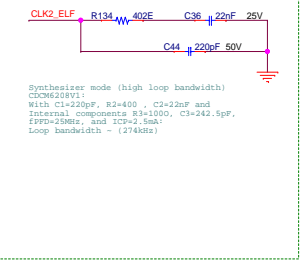
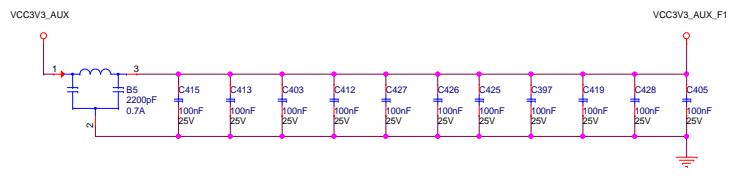
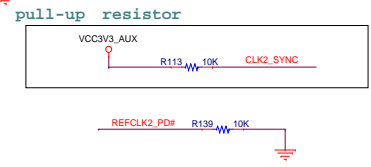
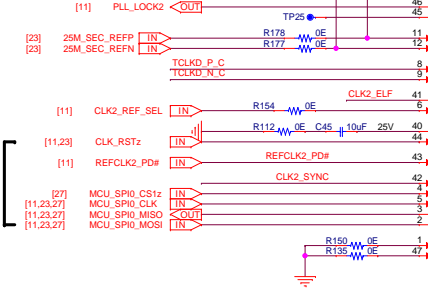
from AMC.0



from VCTCXO 25Mhz



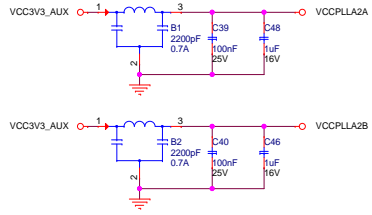
From MCU connect to this signal



Synthesizer mode (high loop bandwidth)
C3=308912
With C1=220pF, R2=400, C2=22nF and
Thermal components R3=1000, C3=242.5pF,
FFPD=25MHz, and ICP=2.5mA!
Loop bandwidth = (274kHz)

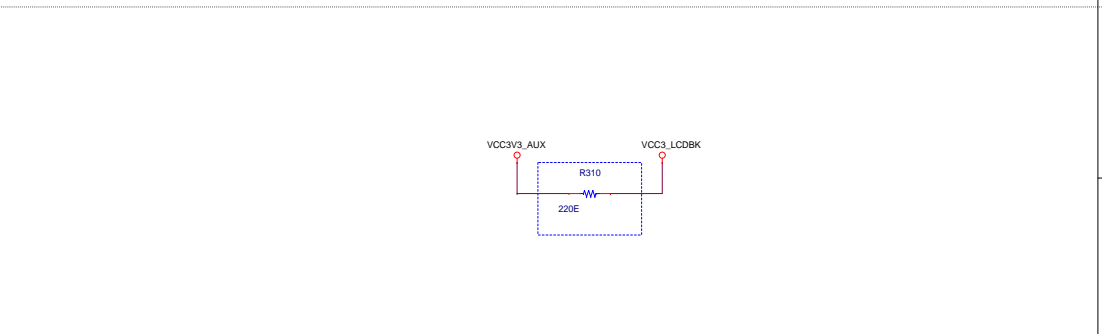
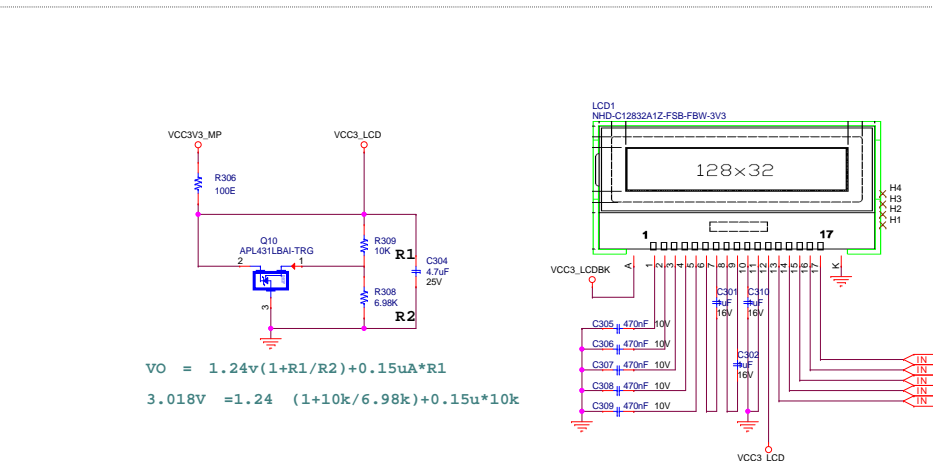
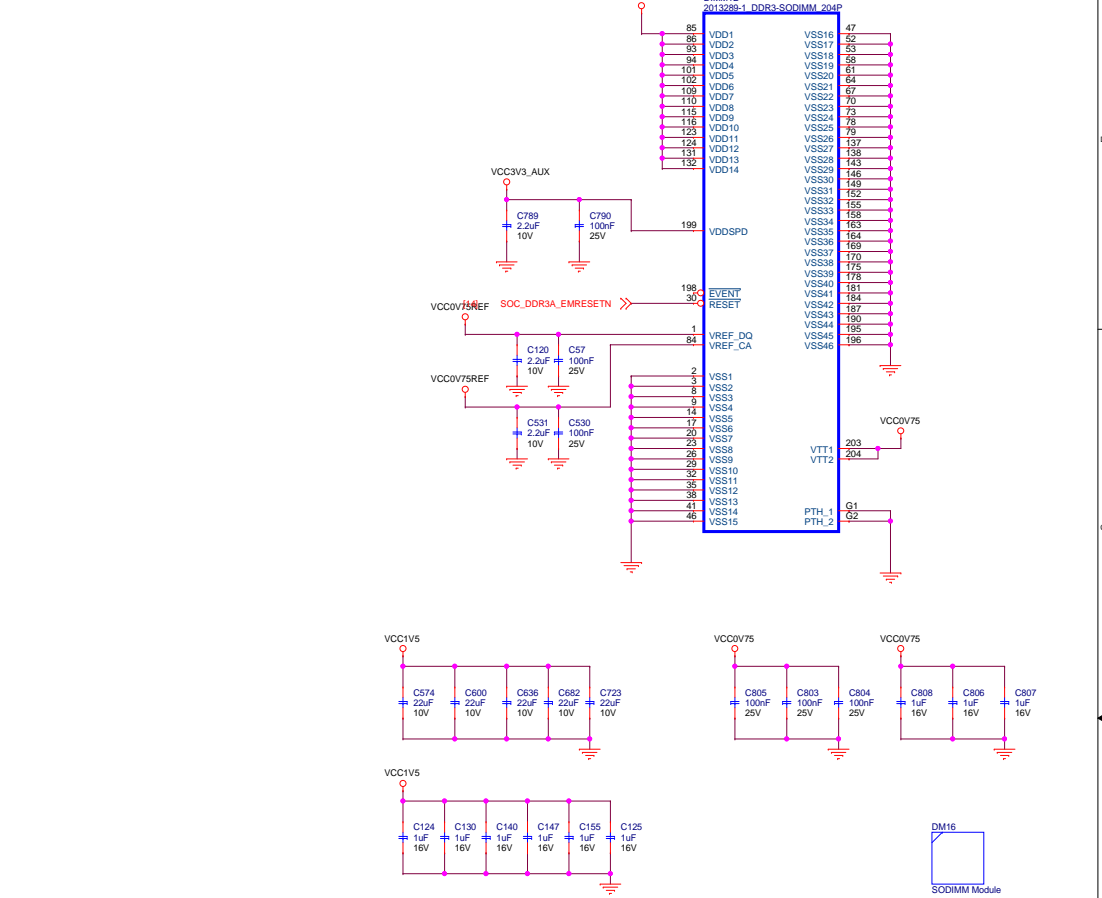
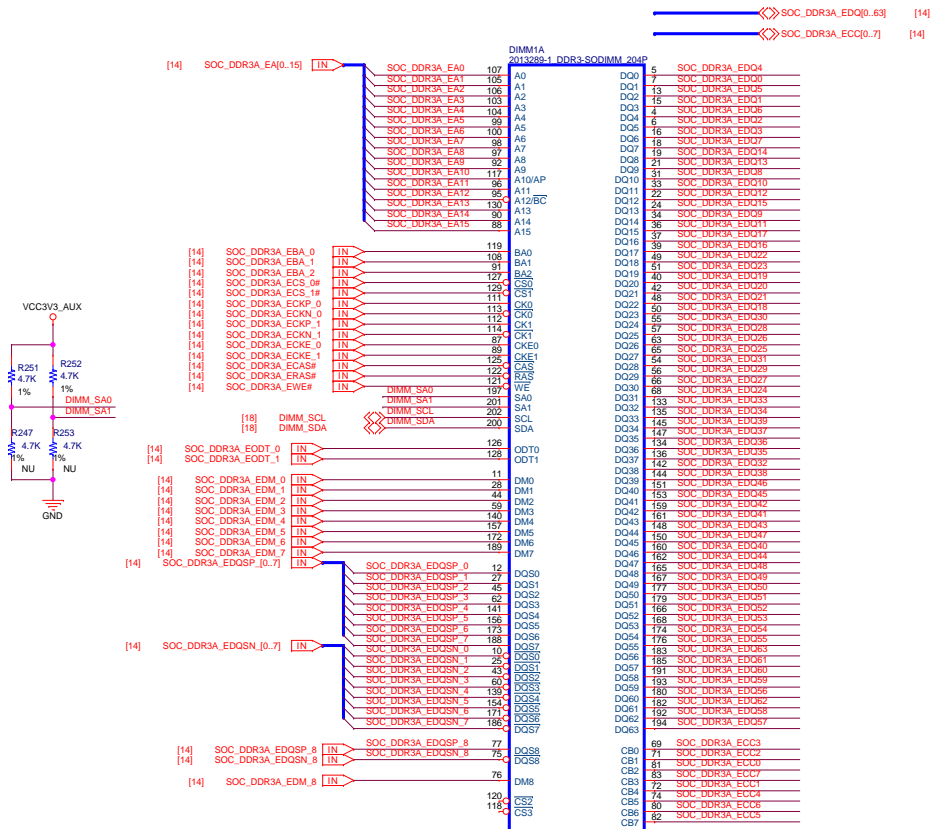
Serial Interface Mode or Pin Mode Selection

MCU_SI_MODE[1:0]	DESCRIPTION
00	SPI MODE (Default)
01	I2C MODE
10	PIN MODE (NO SERIAL PROGRAMMING)
11	RESEVED



Project K2E EVM		Designed for TI by einfochips	
Title CLOCK SOURCE-- 2			
Size C	Document Number 16_00175_03	Rev 3.03	
Date: Monday, February 02, 2015		Sheet 24 of 37	

DDR3 SODIMM



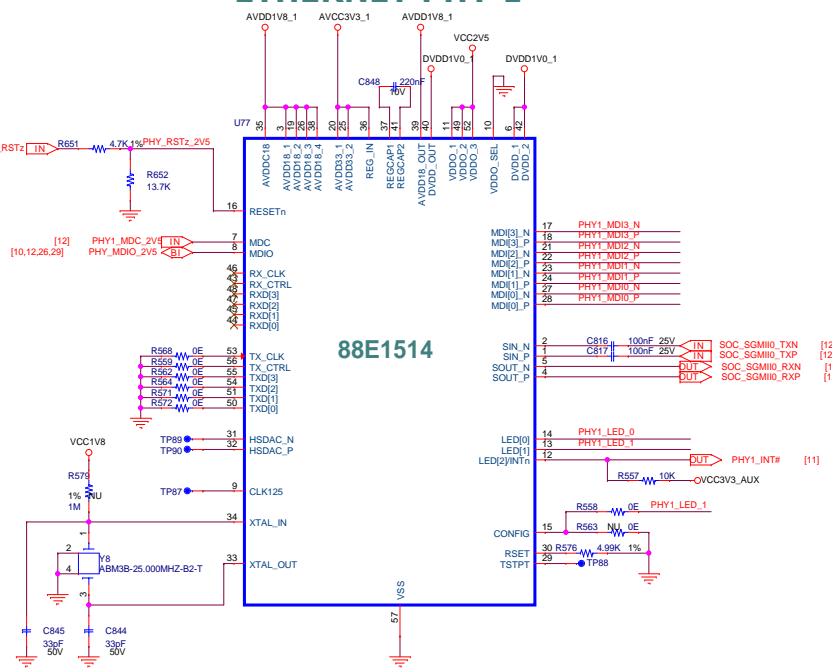
$$VO = 1.24v(1+R1/R2)+0.15uA*R1$$

$$3.018V = 1.24 (1+10k/6.98k)+0.15u*10k$$

SPI1 CS0
LCD control

Project K2E EVM		Designed for TI by einfchips	
Title DDR3- SODIMM AND LCD			
Size C	Document Number 16_00175_03	Rev 3.03	
Date: Monday, February 02, 2015		Sheet 25 of 37	

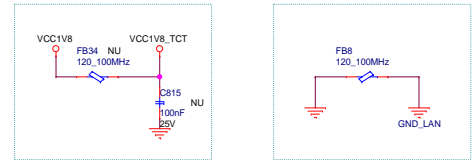
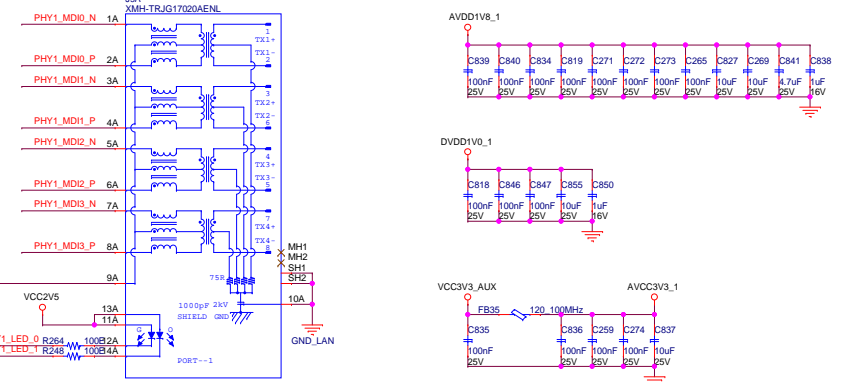
ETHERNET PHY 1



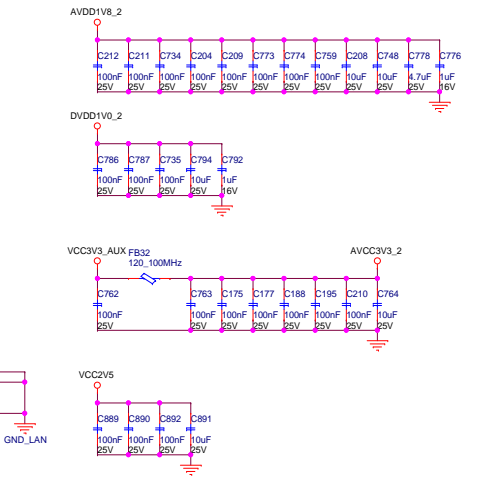
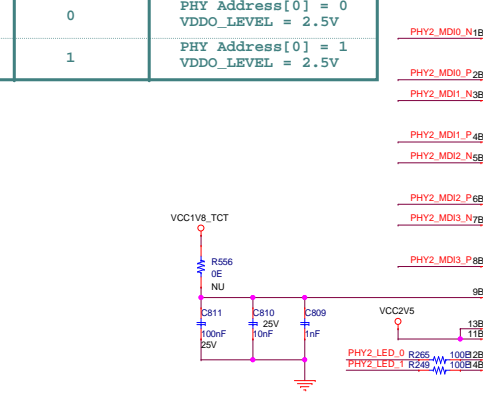
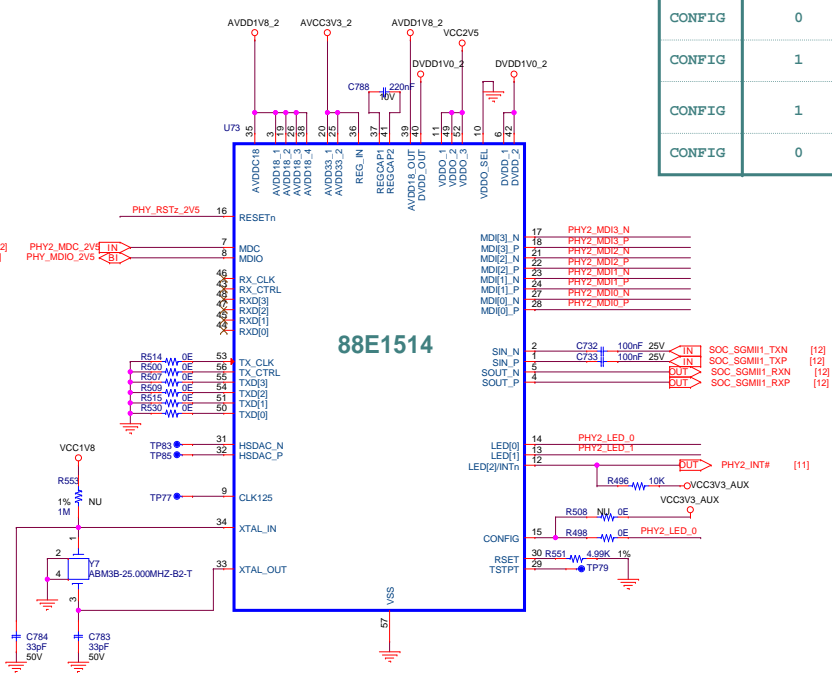
CONFIGURATION MAPPING

PIN	BIT 1,0
VSS	00
LED[0]	01
LED[1]	10
LED[2]	Unused
VDDO	11

PIN	CONFIG Bit1	CONFIG Bit0	Value Assignment
CONFIG	0	0	PHY Address[0] = 0 VDDO_LEVEL = 3.3V
CONFIG	1	1	PHY Address[0] = 1 VDDO_LEVEL = 3.3V
CONFIG	1	0	PHY Address[0] = 0 VDDO_LEVEL = 2.5V
CONFIG	0	1	PHY Address[0] = 1 VDDO_LEVEL = 2.5V



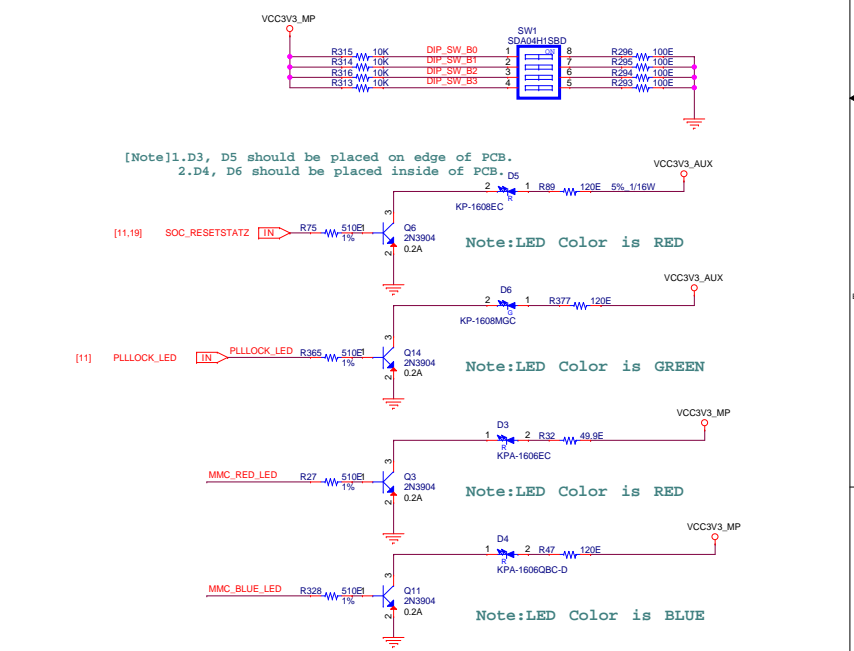
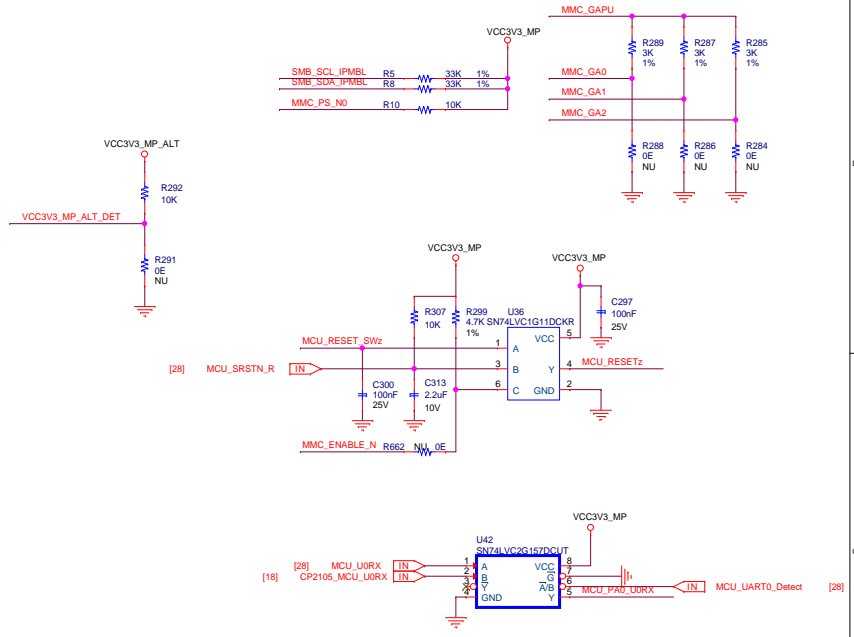
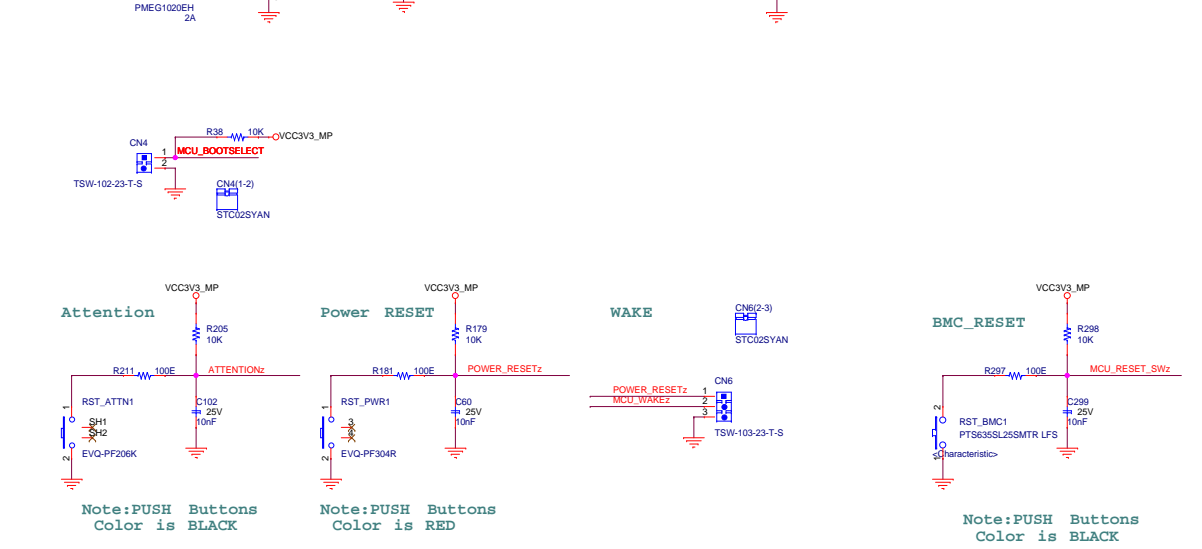
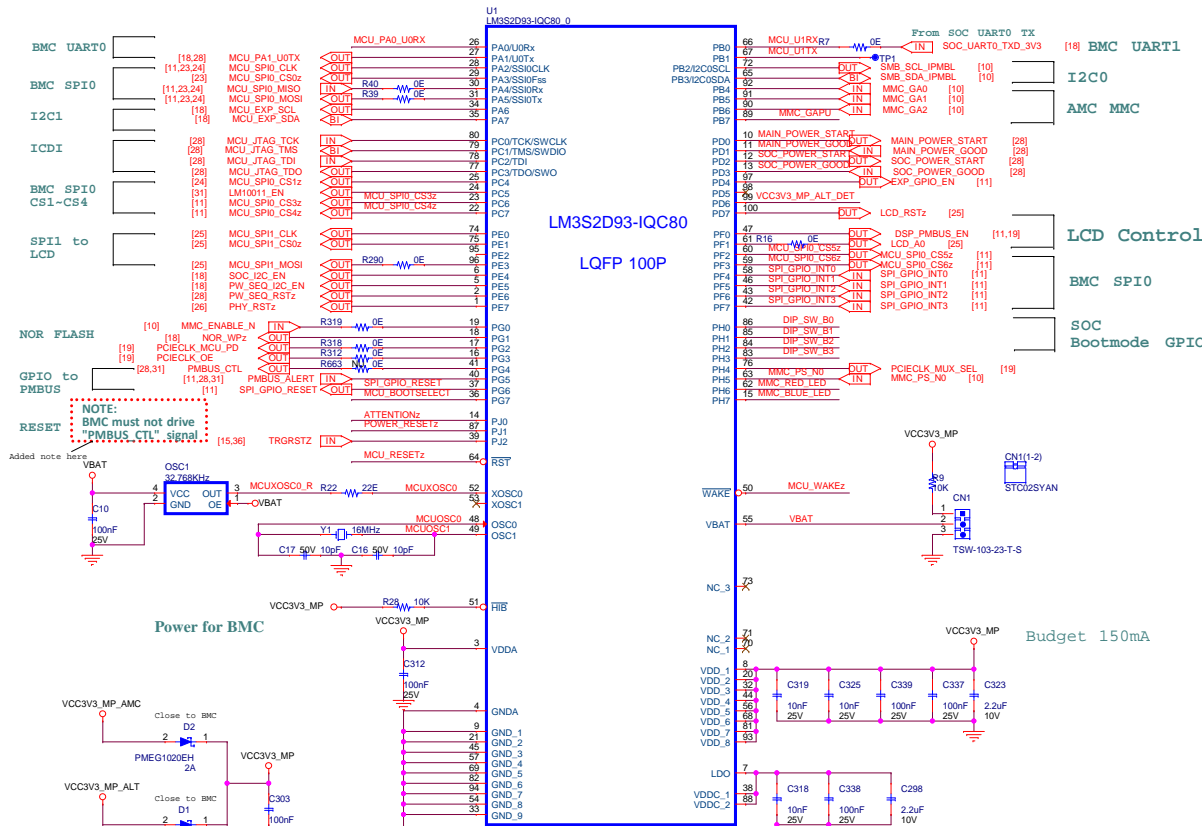
ETHERNET PHY 2



PHY ADDRESS :- 0X1

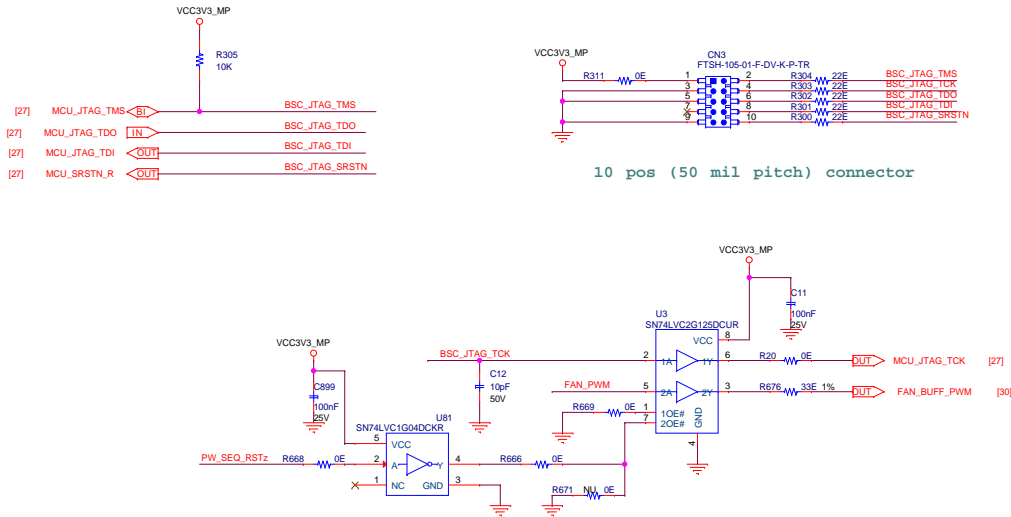
Project K2E EVM		Designed for TI by einfochips	
Title SGMII ETHERNET PHY			
Size C	Document Number 16_00175_03	Rev 3.03	
Date: Monday, February 02, 2015		Sheet 26 of 37	

BMC INTERFACE

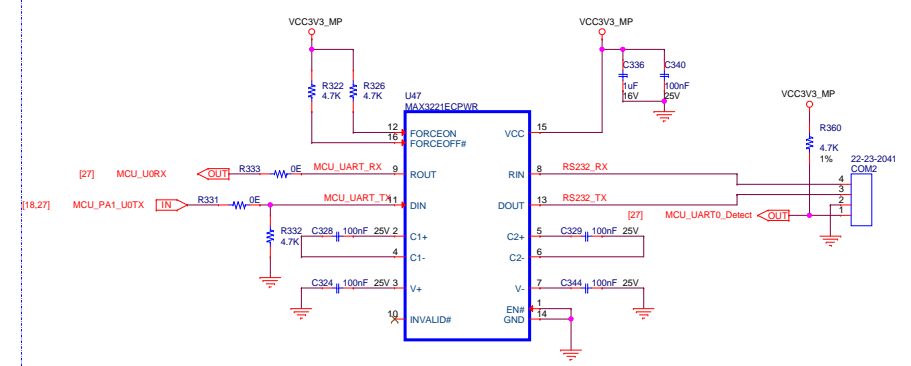


Project K2E EVM		Designed for TI by elnfochips	
Title BMC			
Size C	Document Number 16_00175_03	Rev 3.03	
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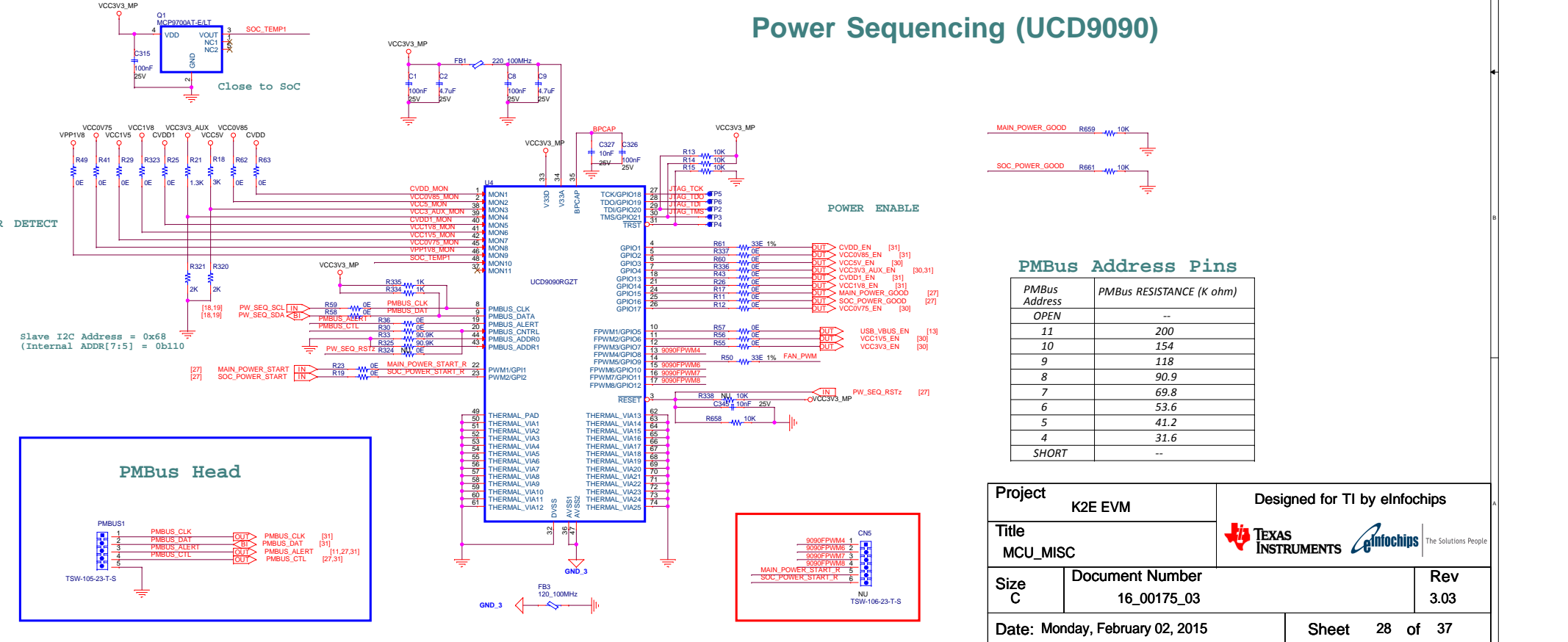
BMC JTAG



BMC UART



Power Sequencing (UCD9090)



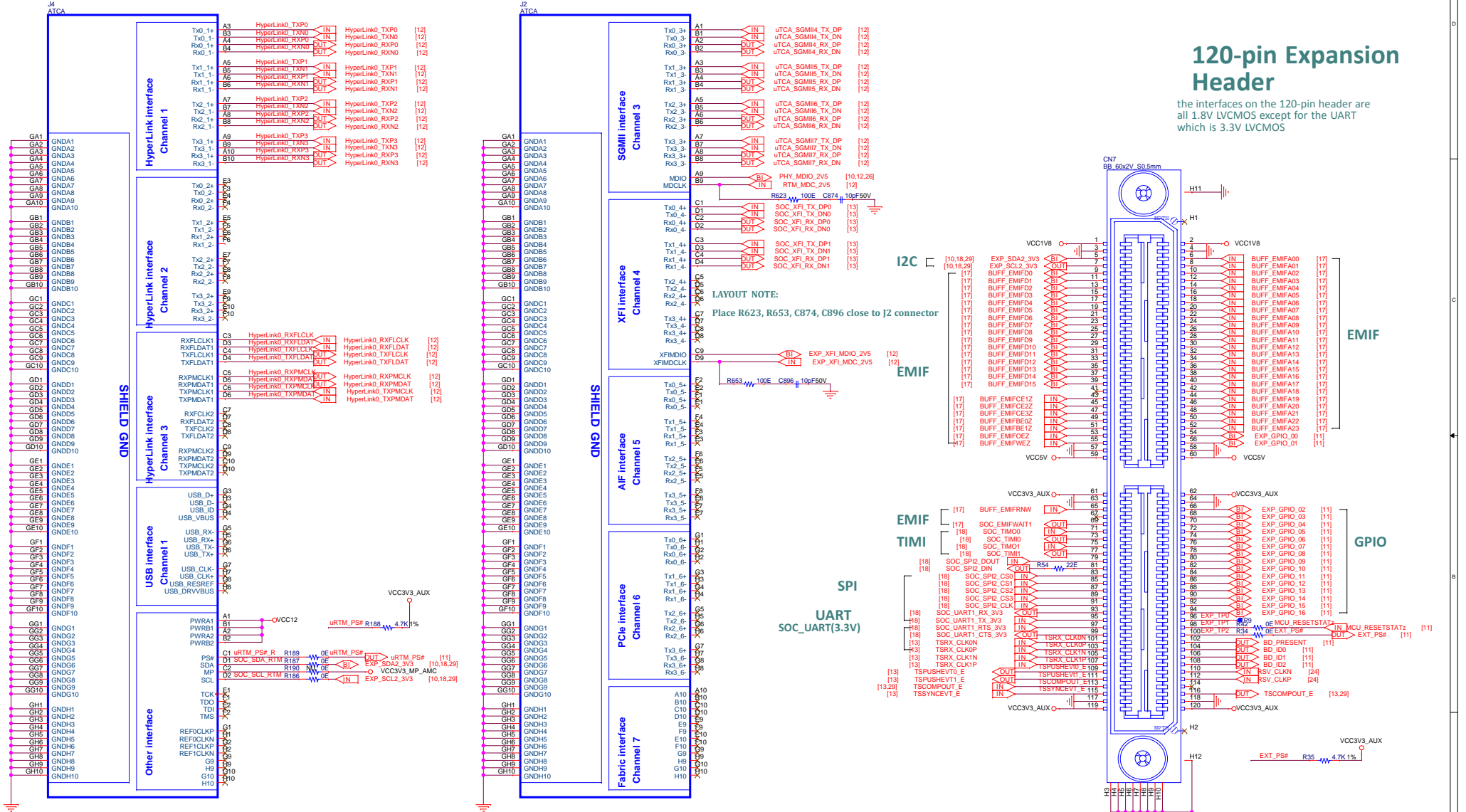
PMBus Address Pins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	200
10	154
9	118
8	90.9
7	69.8
6	53.6
5	41.2
4	31.6
SHORT	--

Project K2E EVM		Designed for TI by einfochips	
Title MCU_MISC			
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Note: J4 connector close to AMC Interface.

Note: J2 connector close to Key socket.

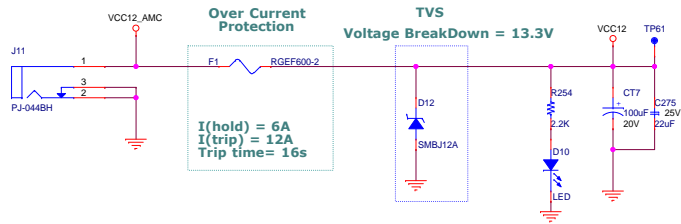


120-pin Expansion Header

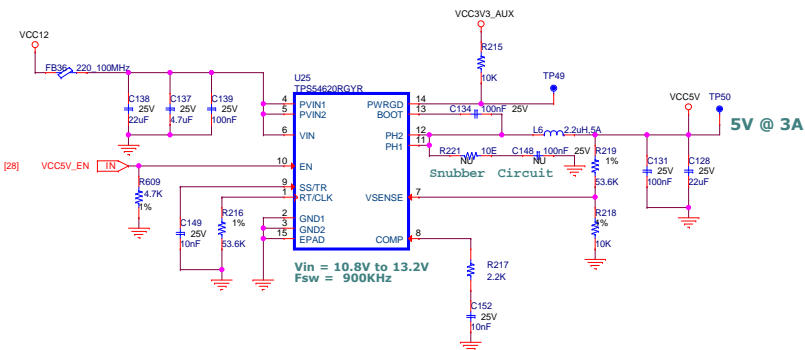
the interfaces on the 120-pin header are all 1.8V LVCMOS except for the UART which is 3.3V LVCMOS

Project K2E EVM		Designed for TI by einfochips	
Title uTCA AND EXPANSION			The Solutions People
Size C	Document Number 16_00175_03		
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VCC12@5A INPUT



12V to 5V Generation



$$V_{OUT} = 0.8 * (R1/R2 + 1)$$

$$= 0.8 * (53.6/10 + 1)$$

$$= \sim 5V$$

$$R_{rt} = 48000 * F_{sw}(kHz)^{-0.997} - 2$$

$$= 48000 * 900^{-0.997} - 2$$

$$= \sim 52.5 \text{ Kohms}$$

OUTPUT CAPACITOR CALCULATION

$$C_{out} = 2 * \Delta(I_{out}) / (F_{sw} * \Delta(V_{out}))$$

$$= 2 * 1 / (900kHz * 0.25)$$

$$= \sim 9\mu F$$

REFERENCE CAPACITOR = 22uF

INDUCTOR CALCULATION

$$L = (V_{in} - V_{out}) / (I_{out} * K_{ind}) * (V_{out} / (V_{in} * F_{sw}))$$

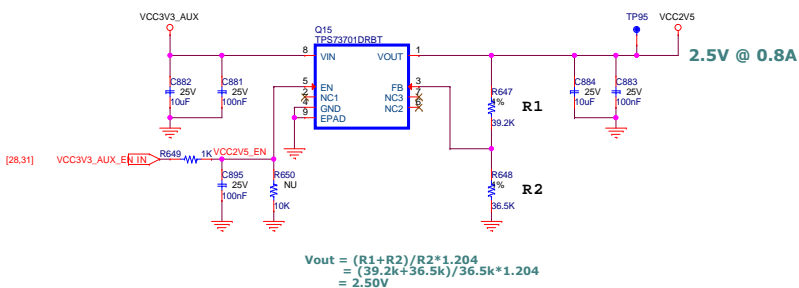
$$= (12 - 5) / (3 * 0.3) * (5 / (12 * 900kHz))$$

$$= 7.78 * 0.46\mu$$

$$= \sim 3.6\mu H$$

REFERENCE CAPACITOR = 2.2uH

3.3V_AUX to 2.5V Generation

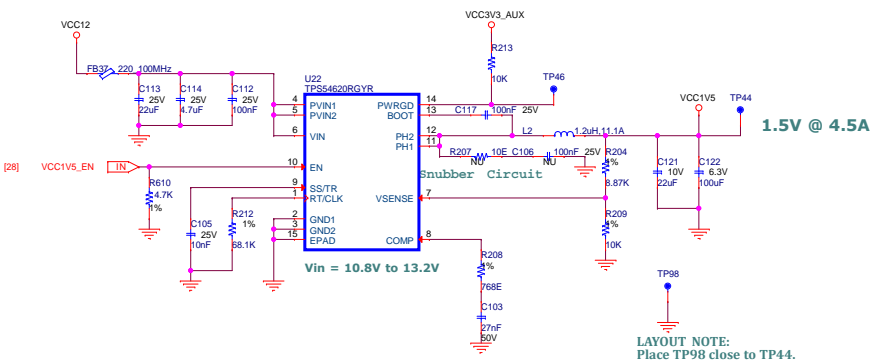


$$V_{out} = (R1+R2)/R2 * 1.204$$

$$= (39.2k+36.5k)/36.5k * 1.204$$

$$= 2.50V$$

12V to 1.5V Generation



$$V_{OUT} = 0.8 * (R1/R2 + 1)$$

$$= 0.8 * (8.87/10 + 1)$$

$$= \sim 1.5V$$

$$R_{rt} = 48000 * F_{sw}(kHz)^{-0.997} - 2$$

$$= 48000 * 700^{-0.997} - 2$$

$$= \sim 68 \text{ Kohms}$$

OUTPUT CAPACITOR CALCULATION

$$C_{out} = 2 * \Delta(I_{out}) / (F_{sw} * \Delta(V_{out}))$$

$$= 2 * 1 / (700kHz * 0.125)$$

$$= \sim 38\mu F$$

REFERENCE CAPACITOR = 100uF

INDUCTOR CALCULATION

$$L = (V_{in} - V_{out}) / (I_{out} * K_{ind}) * (V_{out} / (V_{in} * F_{sw}))$$

$$= (12 - 1.5) / (4.5 * 0.3) * (1.5 / (12 * 700kHz))$$

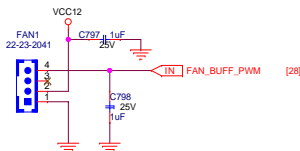
$$= 7.78 * 0.18\mu$$

$$= \sim 1.38\mu H$$

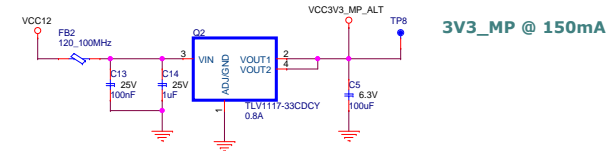
REFERENCE CAPACITOR = 1.2uH

LAYOUT NOTE:
Place TP98 close to TP44.

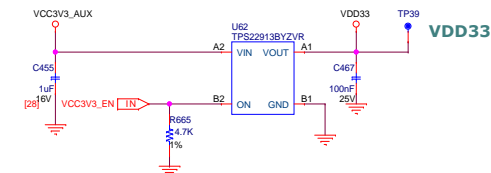
DC FAN Connector for SOC



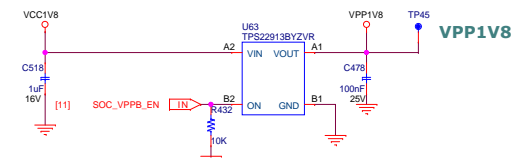
12V to VCC3V3_MP_ALT Generation



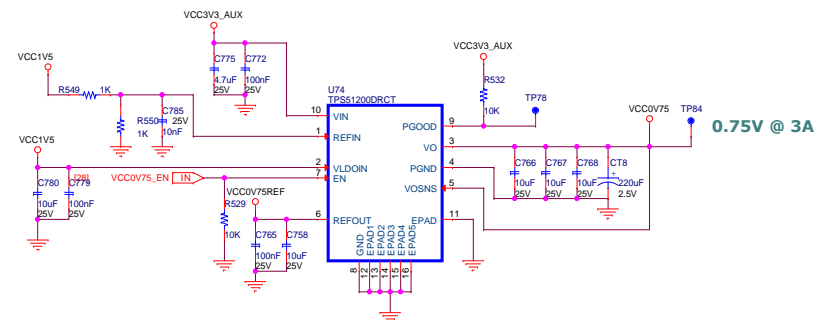
3V3_AUX to VDD33 Generation



VCC1V8 to VPP1V8 Generation



1.5V to 0.75V Generation



$$V_{OUT} = 0.8 * (R1/R2 + 1)$$

$$= 0.8 * (8.87/10 + 1)$$

$$= \sim 1.5V$$

$$R_{rt} = 48000 * F_{sw}(kHz)^{-0.997} - 2$$

$$= 48000 * 700^{-0.997} - 2$$

$$= \sim 68 \text{ Kohms}$$

OUTPUT CAPACITOR CALCULATION

$$C_{out} = 2 * \Delta(I_{out}) / (F_{sw} * \Delta(V_{out}))$$

$$= 2 * 1 / (700kHz * 0.125)$$

$$= \sim 38\mu F$$

REFERENCE CAPACITOR = 100uF

INDUCTOR CALCULATION

$$L = (V_{in} - V_{out}) / (I_{out} * K_{ind}) * (V_{out} / (V_{in} * F_{sw}))$$

$$= (12 - 1.5) / (4.5 * 0.3) * (1.5 / (12 * 700kHz))$$

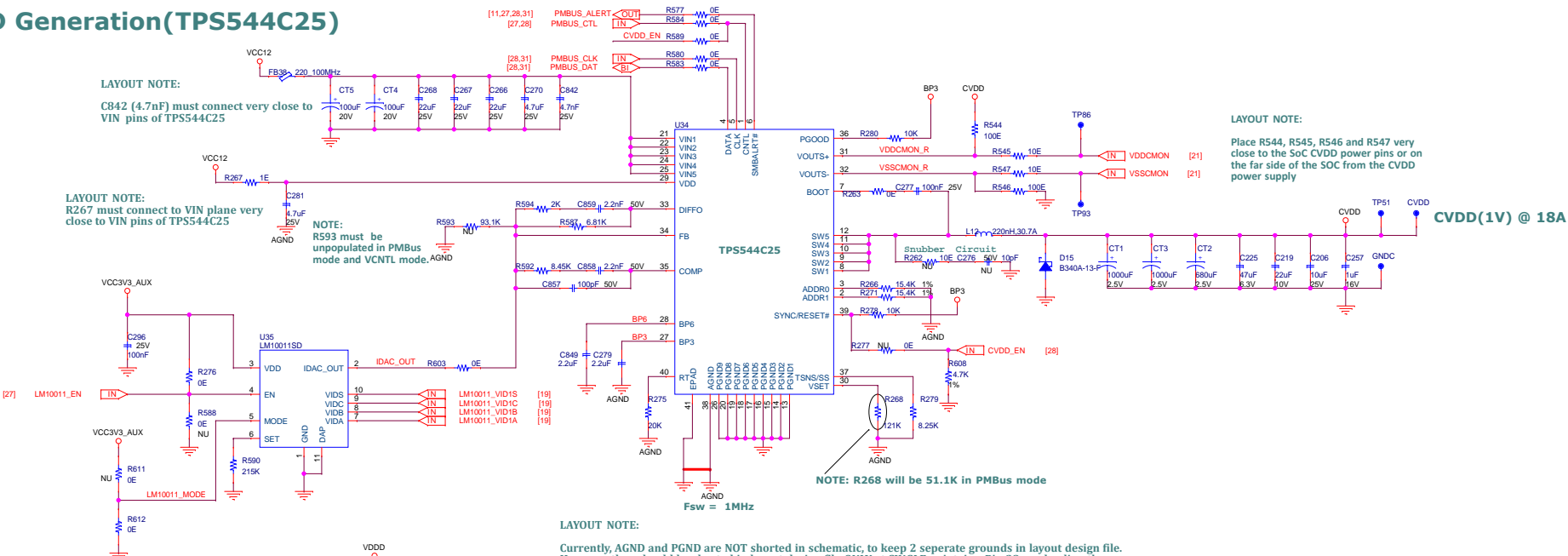
$$= 7.78 * 0.18\mu$$

$$= \sim 1.38\mu H$$

REFERENCE CAPACITOR = 1.2uH

Project K2E EVM		Designed for TI by elnfochips	
Title POWER SUPPLY--1			
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12V to CVDD Generation(TPS544C25)



LAYOUT NOTE:

C842 (4.7nF) must connect very close to VIN pins of TPS544C25

LAYOUT NOTE: R267 must connect to VIN plane very close to VIN pins of TPS544C25

NOTE: R593 must be unpopulated in PMBus mode and VCNTRL mode, AGND

LAYOUT NOTE:

Place R544, R545, R546 and R547 very close to the SoC CVDD power pins or on the far side of the SoC from the CVDD power supply

CVDD(1V) @ 18A

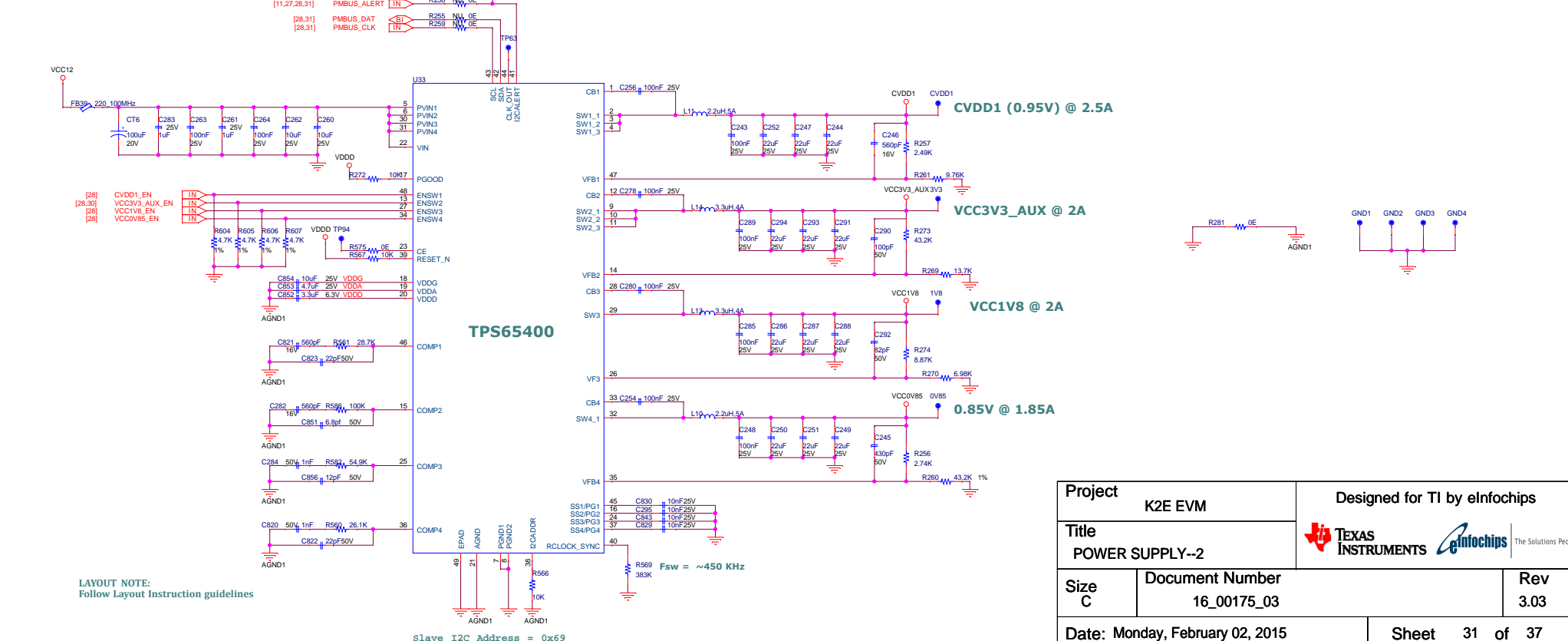
NOTE: R268 will be 51.1K in PMBus mode

Fsw = 1MHz

LAYOUT NOTE:

Currently, AGND and PGND are NOT shorted in schematic, to keep 2 separate grounds in layout design file. However, they should be shorted in layout design file ONLY at SINGLE point, i.e.: Pin 38 can be directly connected to Thermal Pad with thicker trace

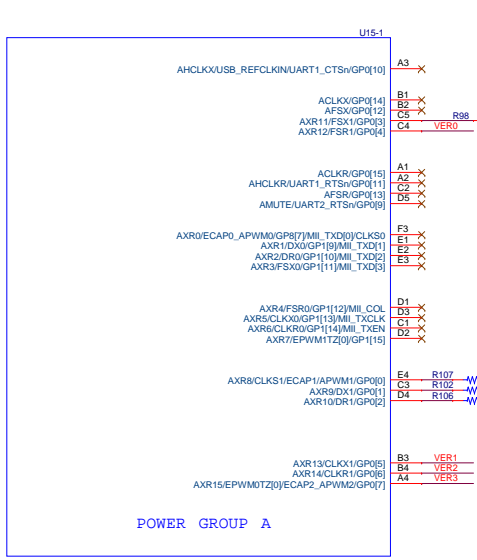
TPS65400(Quad Switcher)



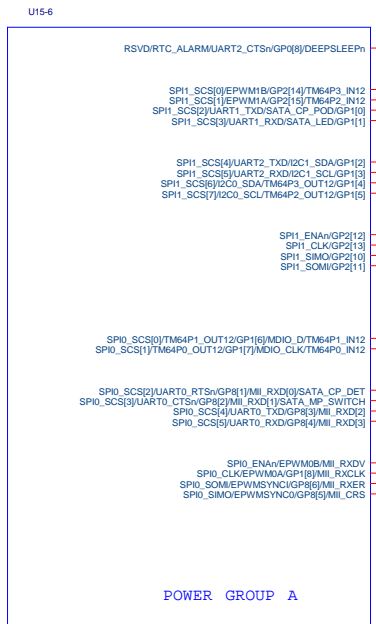
LAYOUT NOTE: Follow Layout Instruction guidelines

Slave I2C Address = 0x69

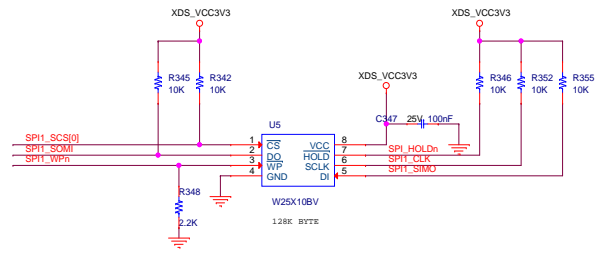
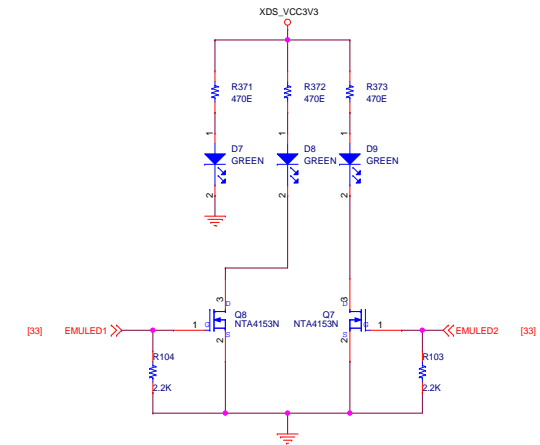
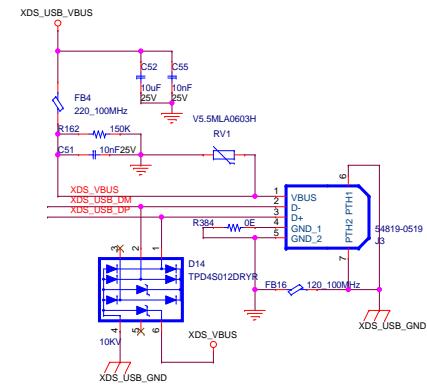
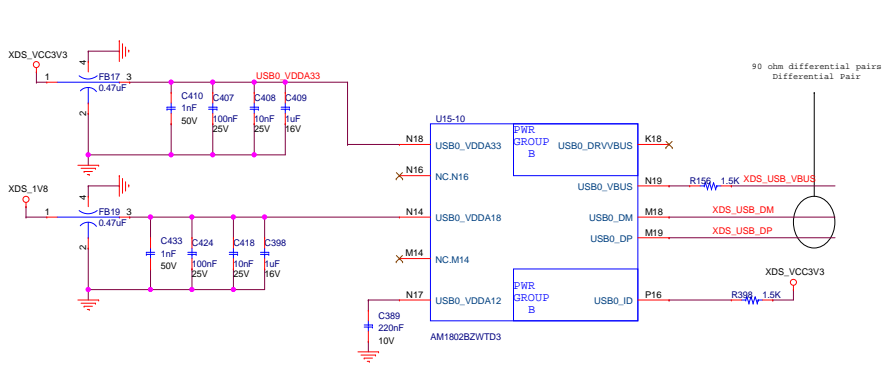
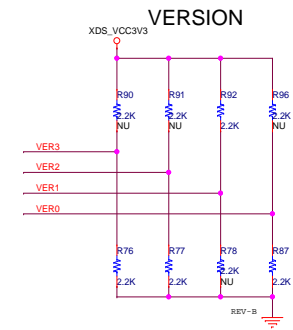
Project K2E EVM		Designed for TI by einfochips	
Title POWER SUPPLY--2			
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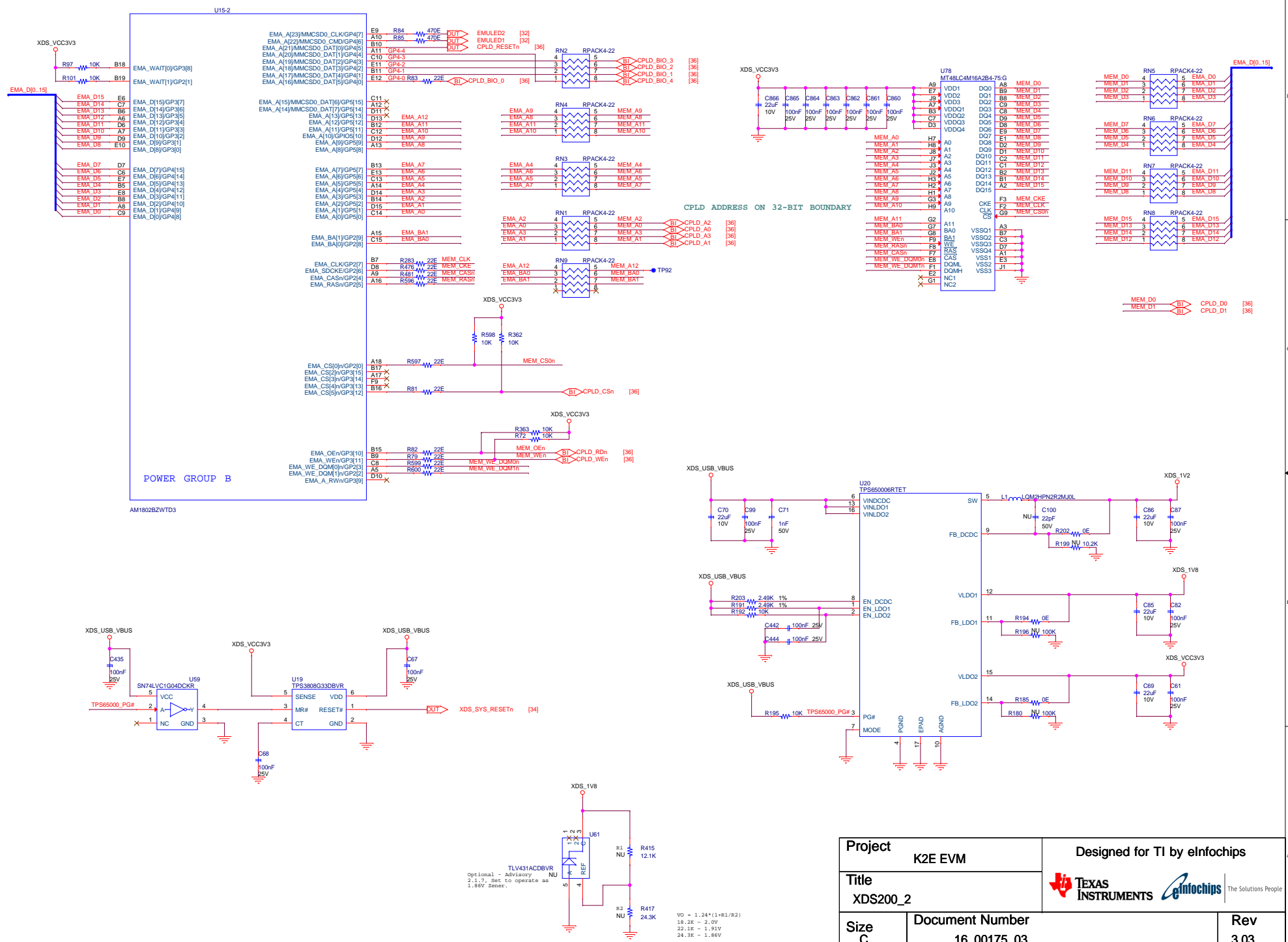
AM1802B2WTD3



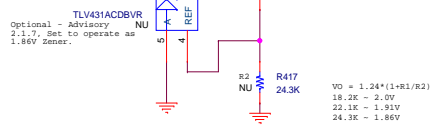
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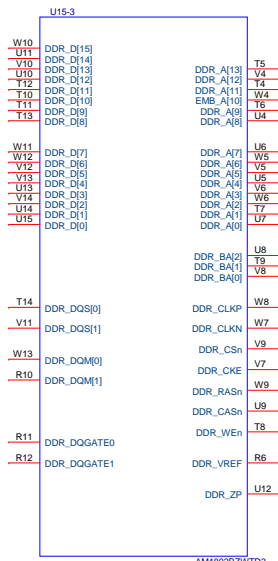


Project K2E EVM		Designed for TI by elnfochips	
Title XDS200_1			
Size C	Document Number 16_00175_03	Rev 3.03	
Date: Monday, February 02, 2015		Sheet 32 of 37	

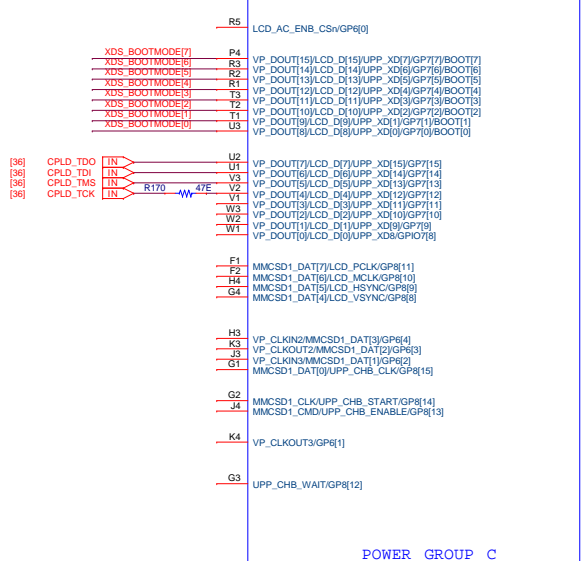


Project K2E EVM		Designed for TI by einfochips	
Title XDS200_2			
Size C	Document Number 16_00175_03	Rev 3.03	
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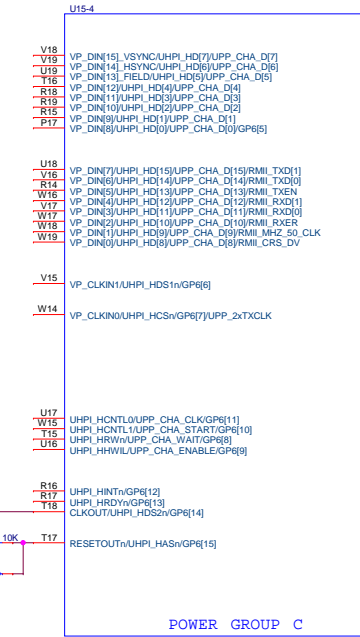


NOT USED



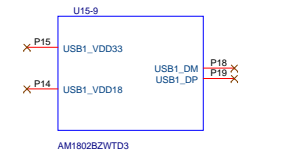
POWER GROUP C

AM1802B2WTD3



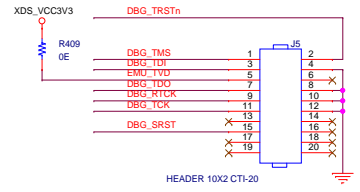
POWER GROUP C

AM1802B2WTD3

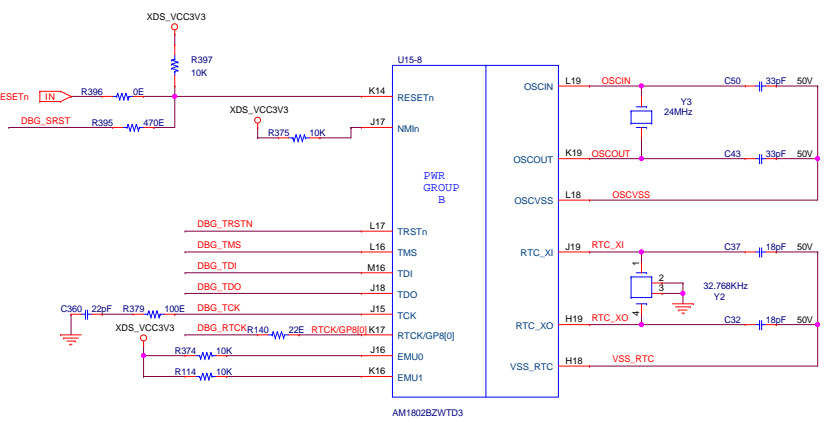


AM1802B2WTD3

NOT USED

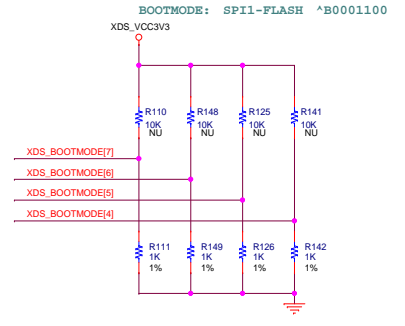
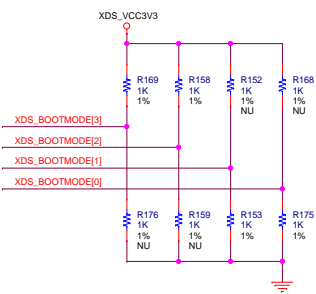


HEADER 10X2 CTI-20



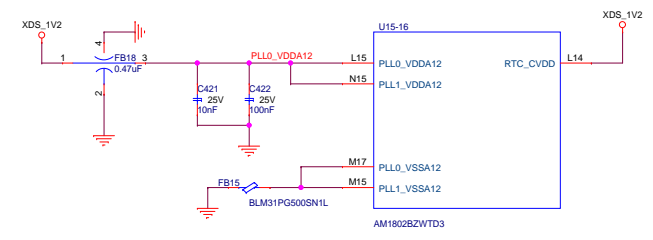
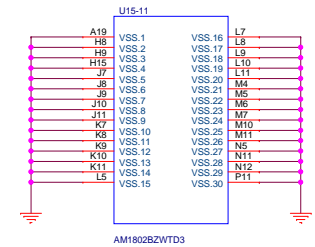
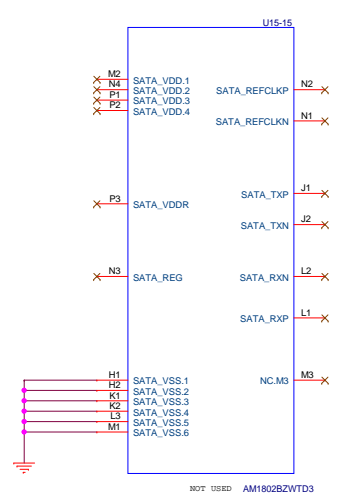
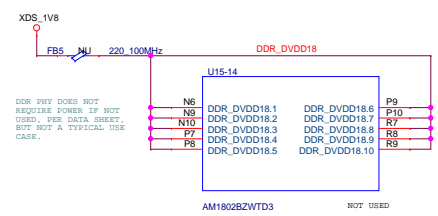
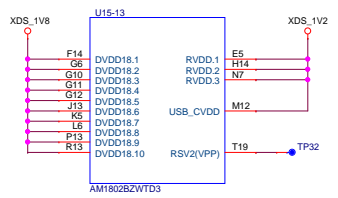
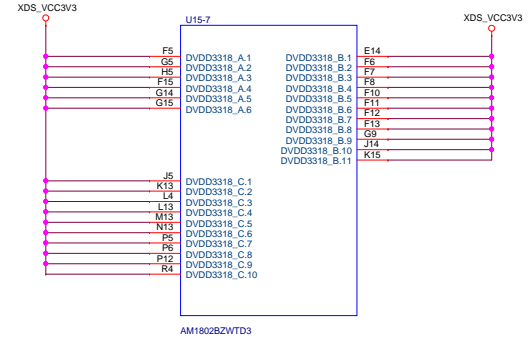
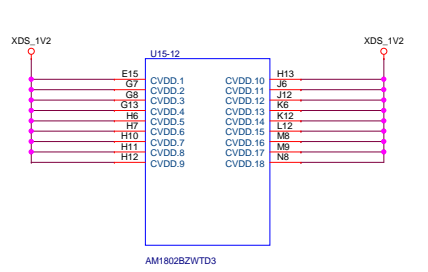
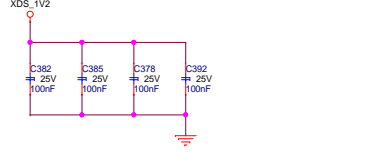
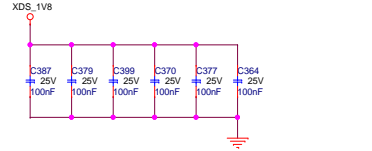
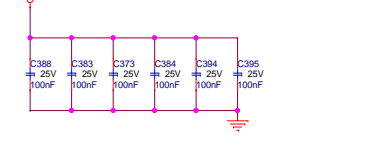
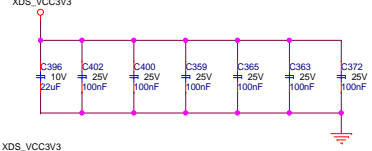
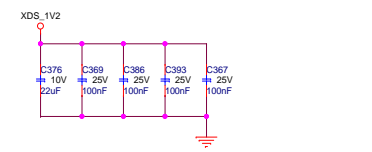
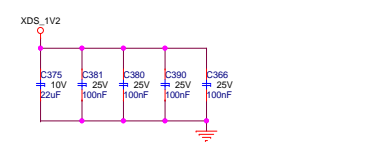
AM1802B2WTD3

BOOT MODE



BOOTMODE: SPI1-FLASH ^B0001100

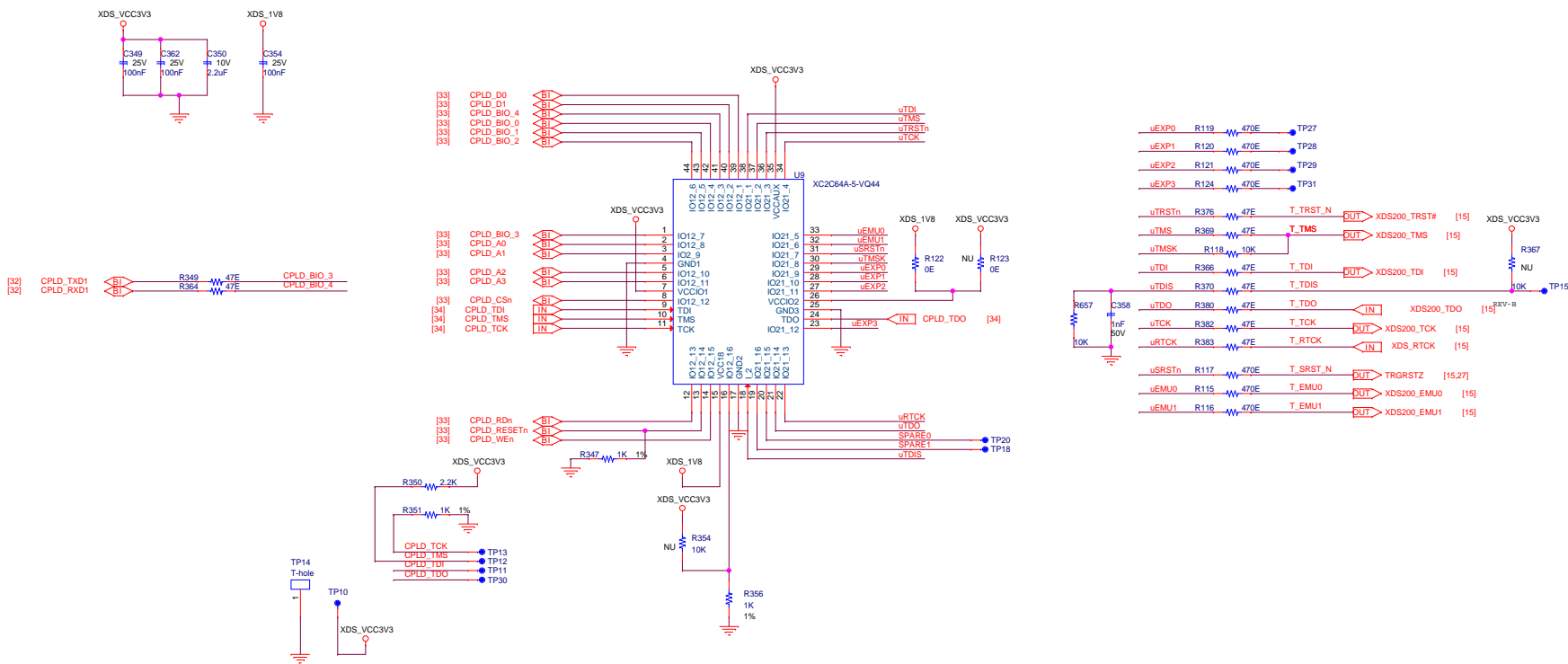
Project K2E EVM		Designed for TI by elnfochips	
Title XDS200_3			
Size C	Document Number 16_00175_03	Rev 3.03	
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DDR PHY DOES NOT REQUIRE POWER IF NOT USED, PER DATA SHEET, BUT NOT A TYPICAL USE CASE.

Project K2E EVM		Designed for TI by einfochips	
Title XDS200 POWER			
Size C	Document Number 16_00175_03	Rev 3.03	
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XDS200 CPLD

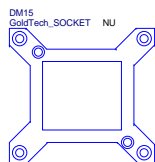
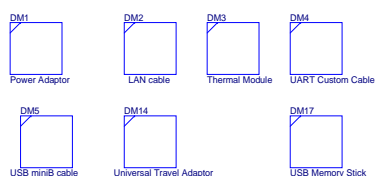


Project K2E EVM		Designed for TI by einfochips	
Title XDS EMULATION			
Size C	Document Number 16_00175_03	Rev 3.03	
Date: Monday, February 02, 2015		Sheet 36 of 37	

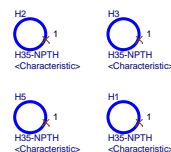
K2E EVM - REVISION HISTORY

PCB REV.	SCH. REV.	CHANGE DESCRIPTION	DATE	AUTHOR
1.0	1.0	Released to Fabrication	15-NOV-2013	eInfochips
2.0	1.01	1) LM26430: Pin#39 and #44 swapped - R575 marked as NU 2) CDCM6208V1: CLK_RSTz connection near to U17 is corrected - R601/R602 added on U17.Sec input - SGMIICLKP/N shifted to Y5 from Y1 3) BMC: DSP_PMBUS_EN changed to PF0 from PE2 4) XDS200: Added a SDRAM & related circuitry - U20 part# changed to TPS650006, fixed version of TPS65000, Changed R185, R194, R202 to 0E and Marked R180, R196, R199, C100 as NU 5) Power: R603 added, R604 - R610 added and marked them as NU	03-JAN-2014	eInfochips
	1.02	1) Power: R611, R612 (NU) added on LM10011 Mode pin 2) TA: IC part# changed to TPS544C24 in place of TPS544B24 - R268 changed to 127K, R590 changed to 215K, R587 changed to 6.81K - TP added near to R547 on VSSCOMON signal - RC Snubber package size changed 3) LM26430: TP added on CE pin 4) CP2105: Added support for Self-Power operation	21-JAN-2014	eInfochips
	1.03	1) LEDs: R47,R71 and R73 values changed to 120E 2) Added AC termination on MDC and MDIO (NU) signals near AMC EDGE connector and RTM connector 3) Configured PHY1 and PHY2 to operate at 2.5V I/O. 4) Added 2.5V LDO for PHY I/O 5) Added buffer on SGMII and XFI MDC signals and added pull-up on MDIO signals 6) U79 added for PMBUS_ALERT signal connection to SoC 7) SoC RSVxxx pin net names changed	25-FEB-2014	eInfochips
	1.04	- Released for Fabrication	05-MAR-2014	eInfochips
	2.0	- Block Diagram, aesthetical changes made	10-MAR-2014	eInfochips
	2.01	- Added 10K pull up resistor on "MMC_ENABLE_N" signal - Mounted 4.7K pull down resistors on R606,R607,R604,R609,R610,R608 - Removed 10K pull up resistor and added 10K pull down resistor on "UTDIS" signal at XDS200 CPLD. - Added 10K pull down resistor on "MAIN_POWER_GOOD" signal - Changed R590 resistor value to 182K - Changed part# of LM26430 to TPS65400 and Changed the part# of TPS544C24 to TPS544C25	06 Aug-2014	eInfochips
3.0	3.01	- Replaced R511 and R512 resistors with 100nF DC blocking capacitors on SATA clock lines. - Remove R510 Pull up resistor from SATA Chip Reset line and connect SATA reset with SOC fullreset line.	14 Aug-2014	eInfochips
	3.02	- Added Pulldown resistor on "SOC_POWER_GOOD" signal - Mounted Pulldown resistor on "VCC3V3_AUX_EN", VCC3V3_EN and "USB_VBUS_EN" signal. - Provided option to connect "MMC_ENABLE_N" signal to BMC reset line. - Updated power sequence and Power tree diagram - R266 and R271 resistors value changed to 15.1K as per updated datasheet of TPS544C25 - R279 resistor value changed to 8.25K as per updated datasheet of TPS544C25 - Changed R61 to 33E and added 0E NU resistor between BMC PMBUS_CTL and TPS544C25 enable pin. - TP98(GND) test point added near VCC1V5V testpoint - Added Ferrite beads on 12V input rail of VCC5V , VCC1V5 ,CVDD and Quad switchers. - Connect FAN_PWM signal with buffer and provide enable control - Added 0E resistors on XFI and SATA clock lines - Changed USB3.0 J7 connector to SMT - Changed pull up resistor value to 1K from 2.2K on PW_SEQ_SCL and PW_SEQ_SDA line - Added 100E resistor between SATA P and N lines	03 NOV-2014	eInfochips

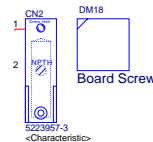
Dummy Components



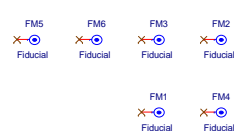
Mounting Holes



KEY ZONE

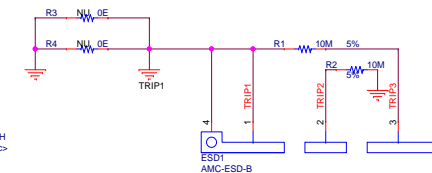
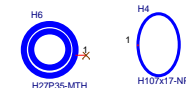


On Board Fiducials



Front panel and ESD Strip

AMC Hole



Project K2E EVM		Designed for TI by eInfochips	
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