

TDA4VM - DUAL TPS65941x PMICs

|       |                            |        |                     |   |       |
|-------|----------------------------|--------|---------------------|---|-------|
| Title |                            |        | CONTENTS OF CIRCUIT |   |       |
| Size  | Document                   | Number | Rev                 |   |       |
| C     | -                          |        | <1.0>               |   |       |
| Date: | Wednesday, August 26, 2026 |        | Sheet               | 1 | of 34 |

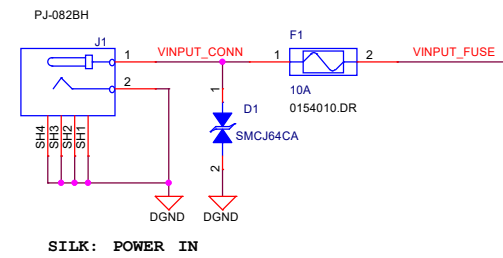
SYSTEM BLOCK DIAGRAM

|       |                          |        |                      |   |       |
|-------|--------------------------|--------|----------------------|---|-------|
| Title |                          |        | SYSTEM BLOCK DIAGRAM |   |       |
| Size  | Document                 | Number | Rev                  |   |       |
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| Date: | Tuesday, August 25, 2026 |        | Sheet                | 2 | of 34 |

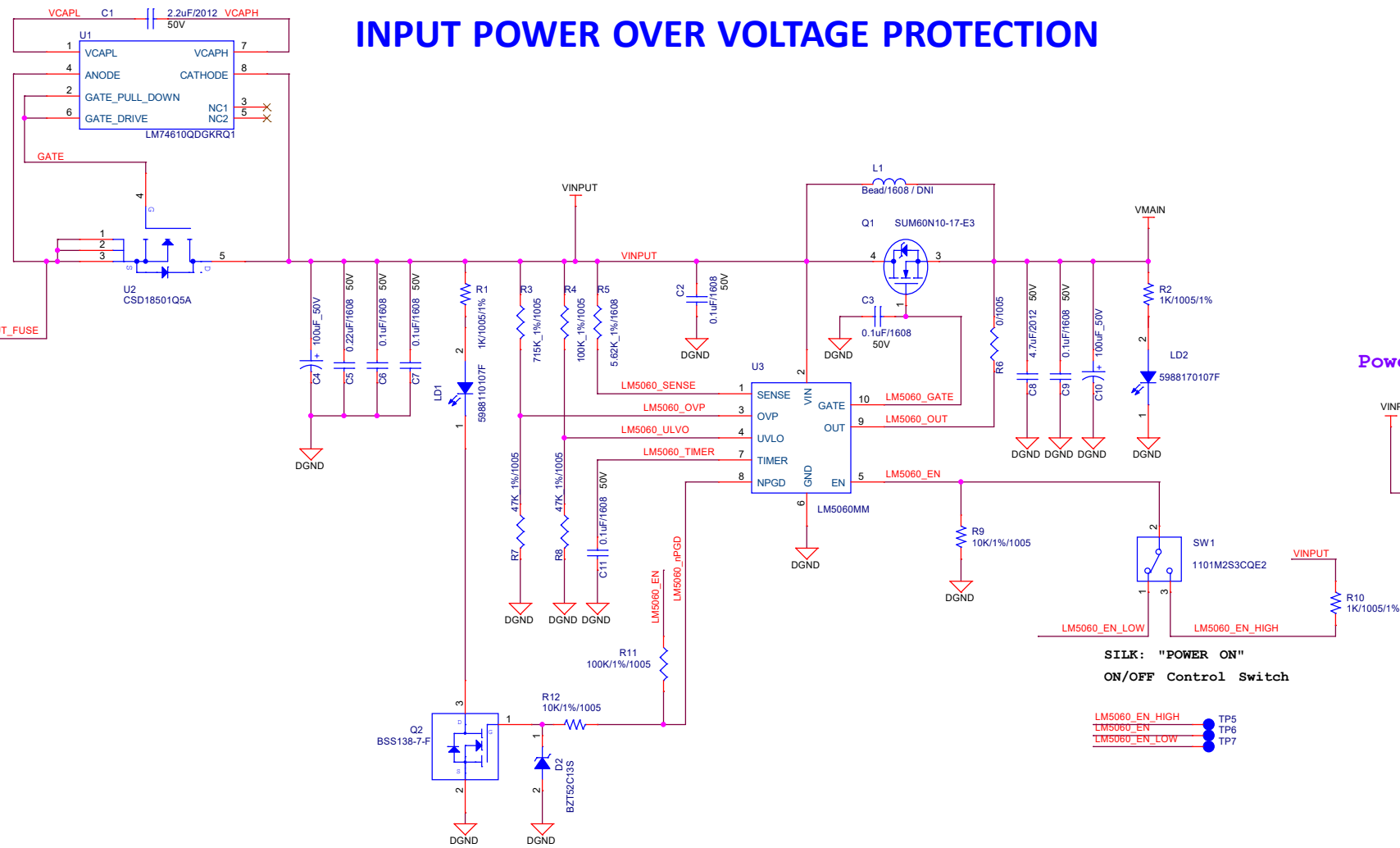
POWER TREE

|       |                          |        |            |   |       |
|-------|--------------------------|--------|------------|---|-------|
| Title |                          |        | POWER TREE |   |       |
| Size  | Document                 | Number | Rev        |   |       |
| C     | -                        |        | <1.0>      |   |       |
| Date: | Tuesday, August 25, 2026 |        | Sheet      | 3 | of 34 |

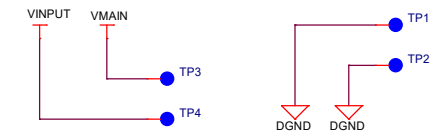
## Power Input



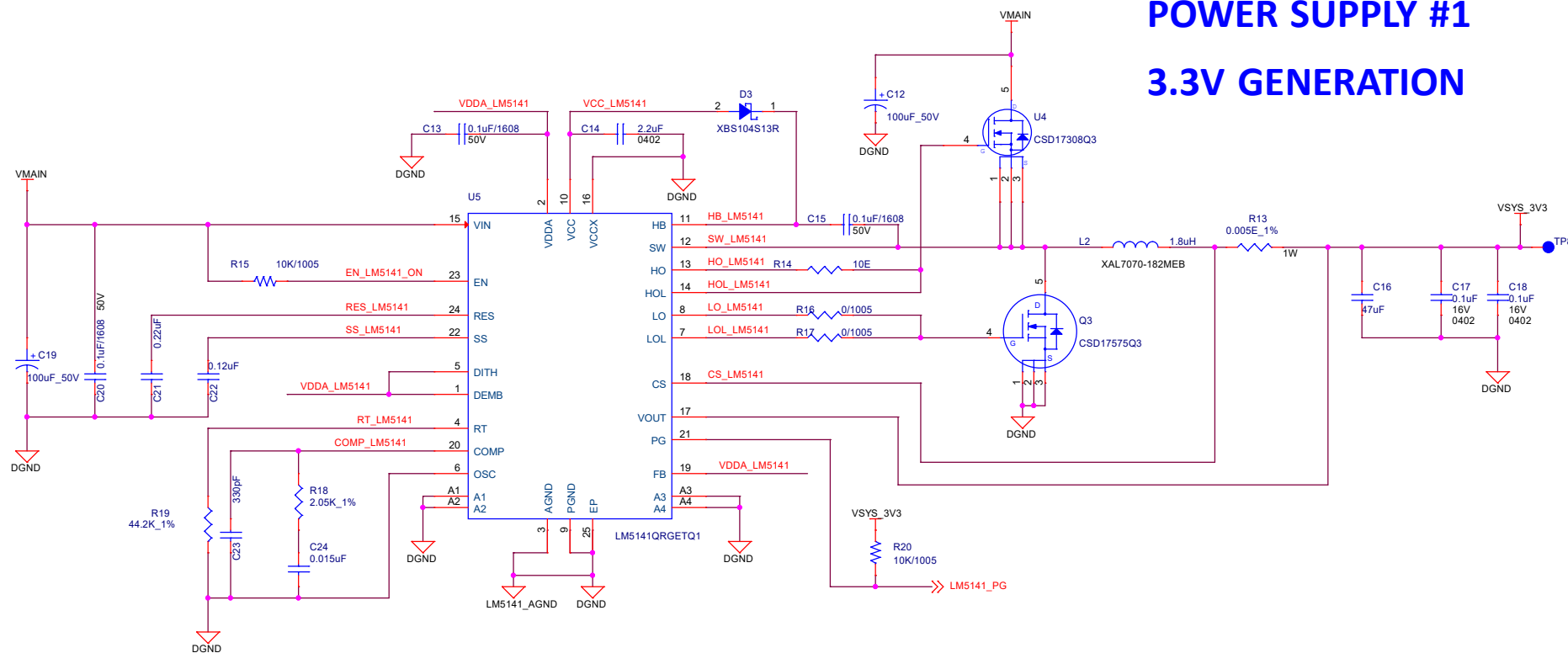
## INPUT POWER OVER VOLTAGE PROTECTION



## Power\_In/Ground test points



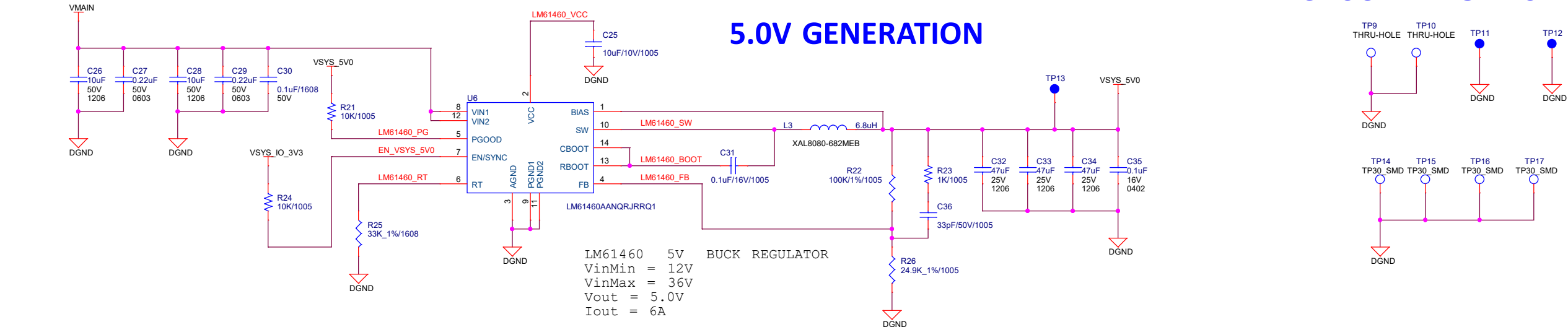
## POWER SUPPLY #1 3.3V GENERATION



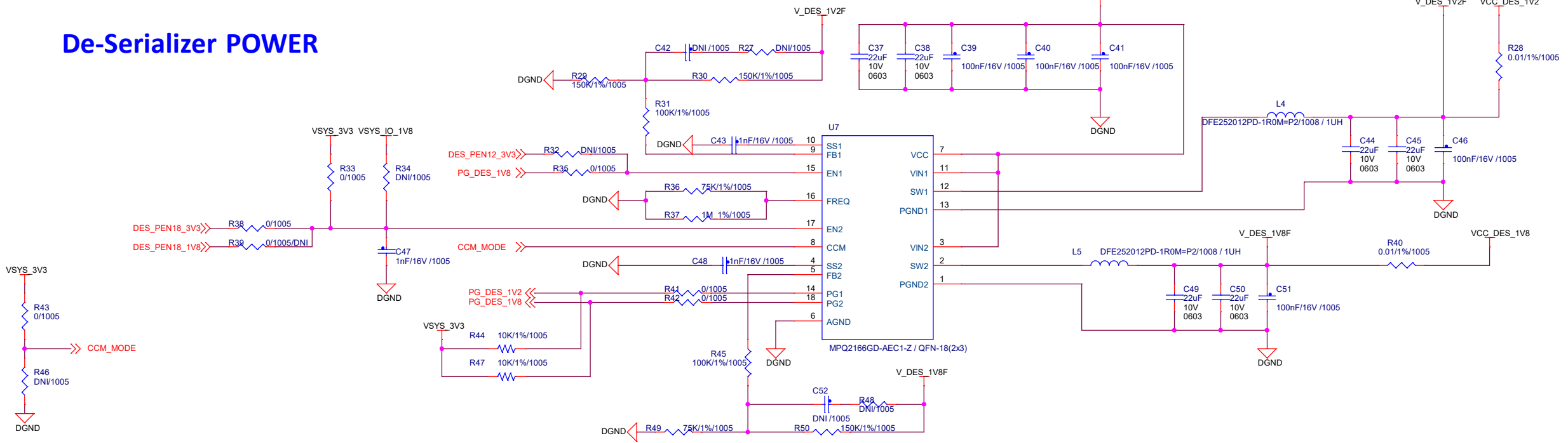
|                      |                          |               |
|----------------------|--------------------------|---------------|
| Title                |                          |               |
| PWR_IN_RANGE_GEN 3V3 |                          |               |
| Size                 | Document Number          | Rev           |
| A2                   | <Doc>                    | <RevCode>     |
| Date:                | Tuesday, August 25, 2026 | Sheet 4 of 34 |

POWER SUPPLY #2  
5.0V GENERATION

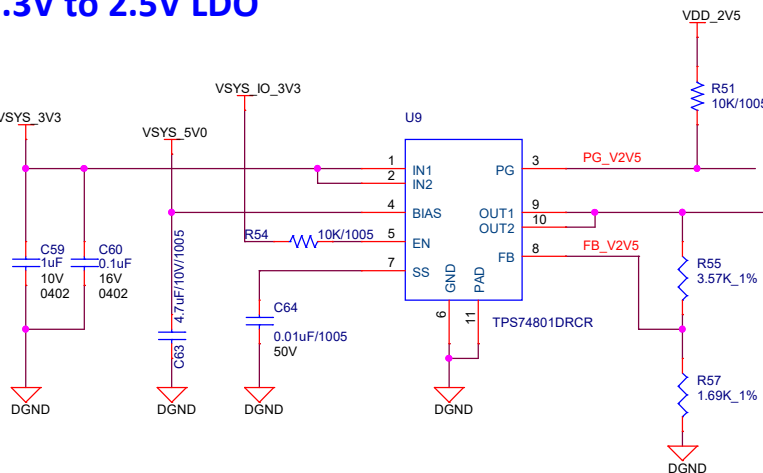
GROUND TEST POINTS



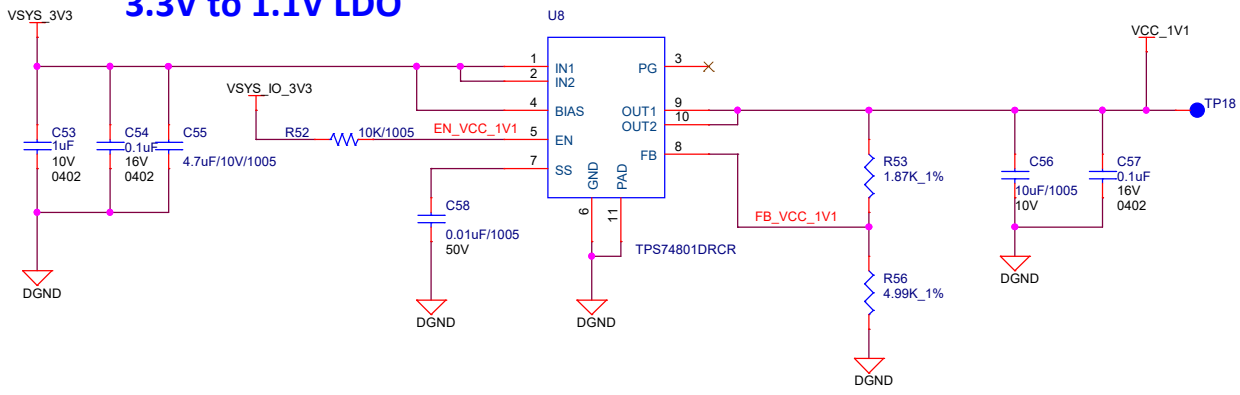
De-Serializer POWER



ETHERNET POWER  
3.3V to 2.5V LDO



USB HUB & ETHERNET POWER  
3.3V to 1.1V LDO



|       |                          |  |                          |   |       |
|-------|--------------------------|--|--------------------------|---|-------|
| Title |                          |  | PWR DES_ETHER_USB_GEN 5V |   |       |
| Size  | Document Number          |  |                          |   | Rev   |
| C     |                          |  |                          |   | <1.0> |
| Date: | Tuesday, August 25, 2026 |  | Sheet                    | 5 | of 34 |

PCB Notes:

For multi-phase Buck converter configs, route remote sense feedback as follows:

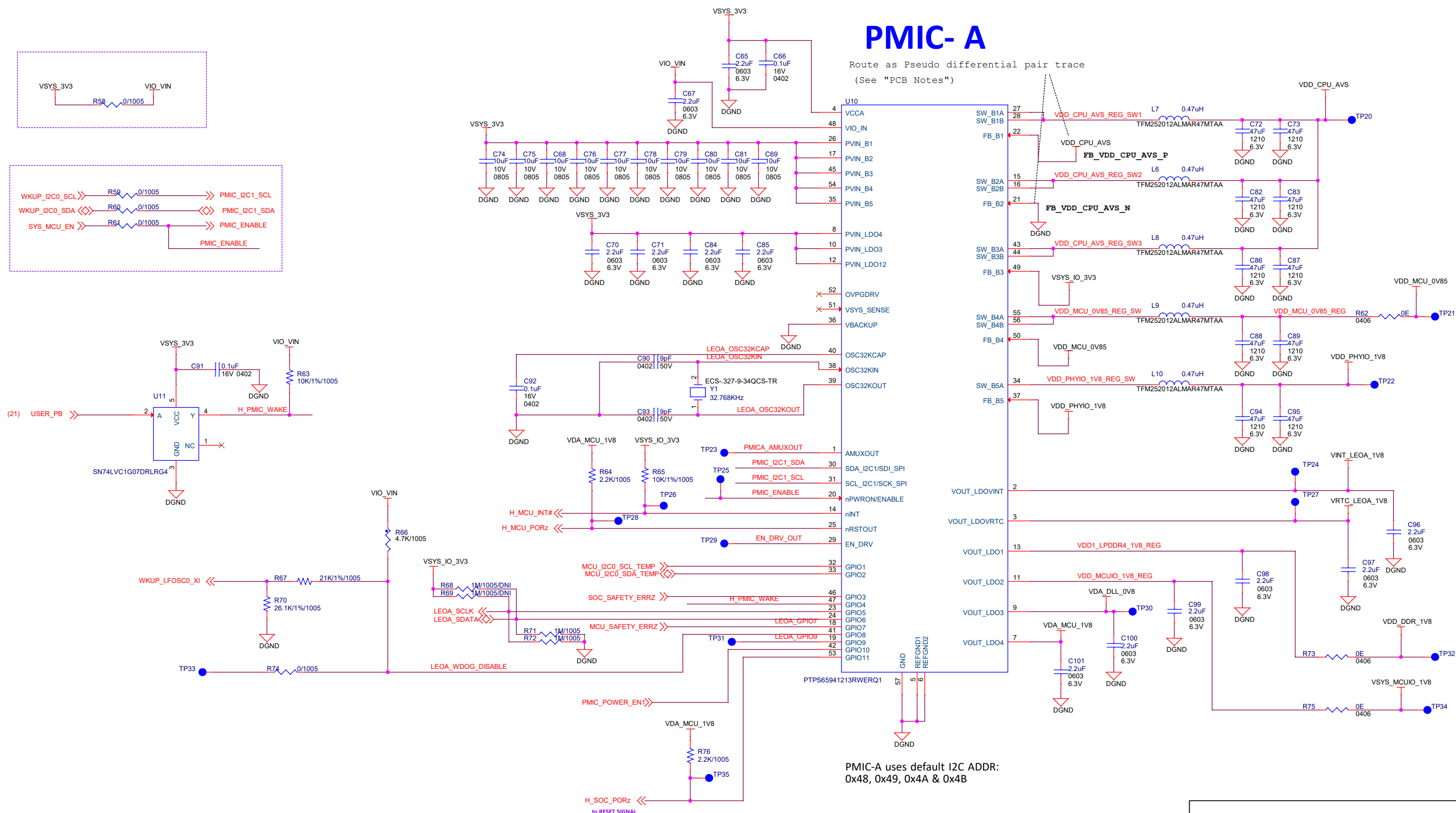
1. Pseudo differential pair traces on same layer& next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance =8-50mil, try to keep traces near each other as best as possible while

For single-phase Buck converters, route remote sense feedback as follows:

1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

## EVM's 3-Phase DUAL PMIC Power Distribution Network (PDN)

### (3-Phase Buck supplying VDD\_CPU)



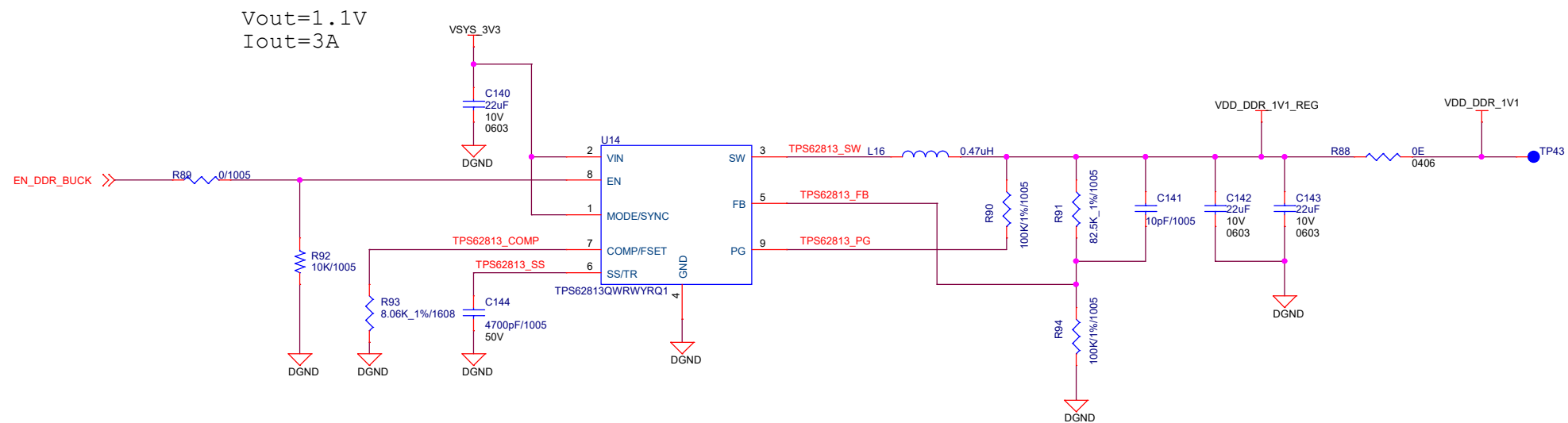
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|-------|--------------------------|-------|---------|
| Title |                          |       | PMIC A  |
| Size  | Document Number          | Rev   |         |
| C     | -                        | <1.0> |         |
| Date: | Tuesday, August 25, 2026 | Sheet | 6 of 34 |

For multi-phase Buck converter configs, route remote sense feedback as follows:

- For single-phase Buck converters, route remote sense feedback as follows:

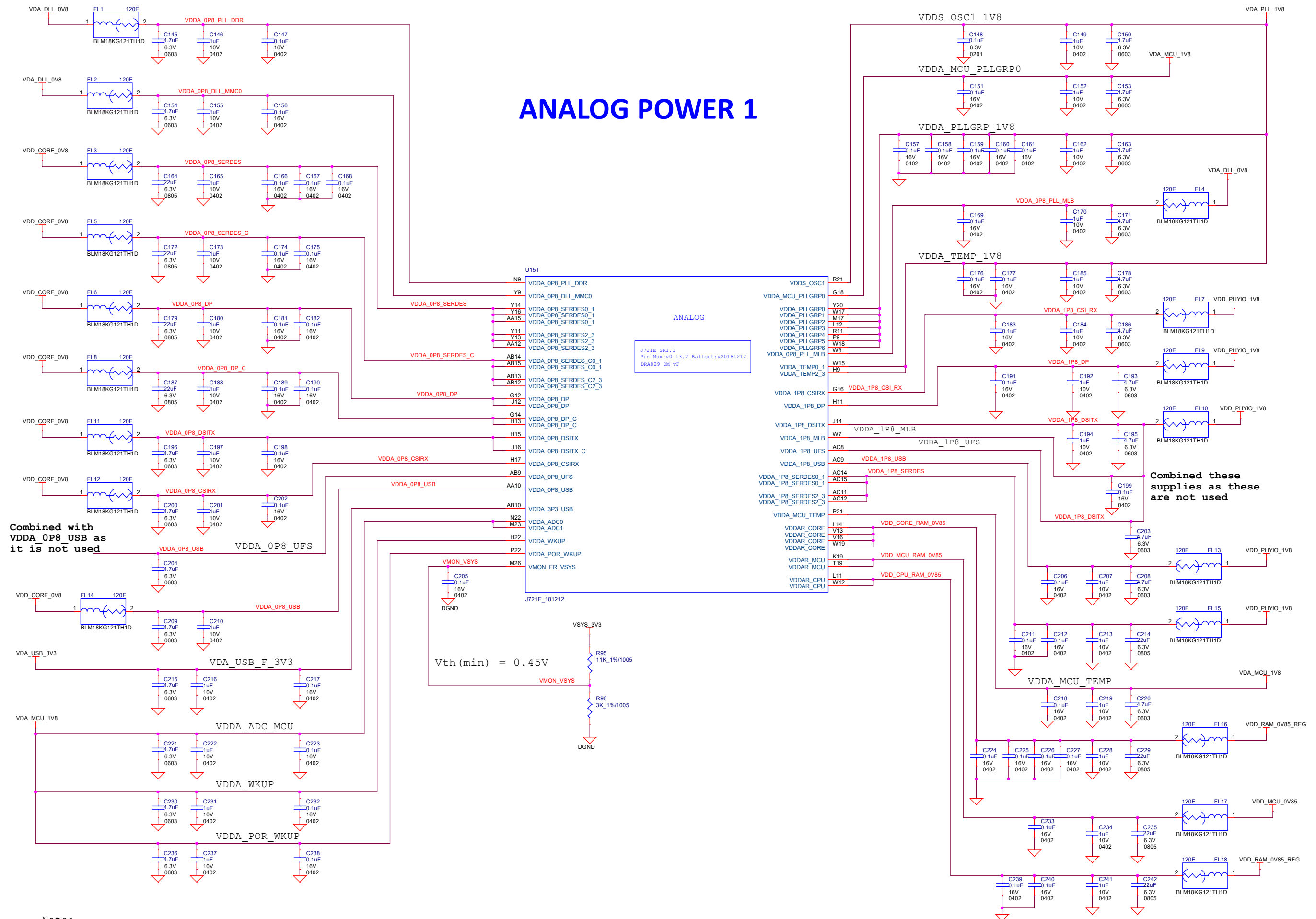
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|-----------|--------------------------|-------|--------------|
| Title     |                          |       |              |
| PMIC B    |                          |       |              |
| Size<br>C | Document Number<br>-     |       | Rev<br><1.0> |
| Date:     | Tuesday, August 25, 2026 | Sheet | 7 of 34      |

## VDD\_DDR\_1V1 BUCK REG



|                       |                          |       |              |
|-----------------------|--------------------------|-------|--------------|
|                       |                          |       |              |
| Title                 |                          |       |              |
| LOAD SWITCHES_DDR 1V1 |                          |       |              |
| Size<br>C             | Document Number          |       | Rev<br><1.0> |
| Date:                 | Tuesday, August 25, 2026 | Sheet | 8 of 34      |

# ANALOG POWER 1



- Combined these supplies as these are not used

Combined with  
VDDA\_0P8\_USB as  
it is not used

$$V_{th}(\min) = 0.45V$$

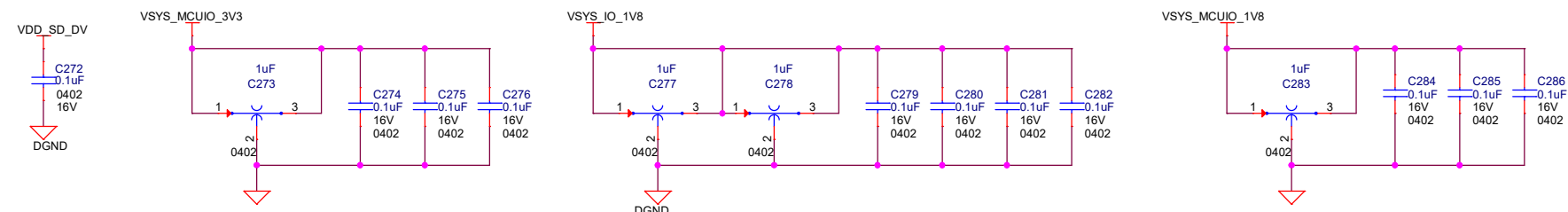
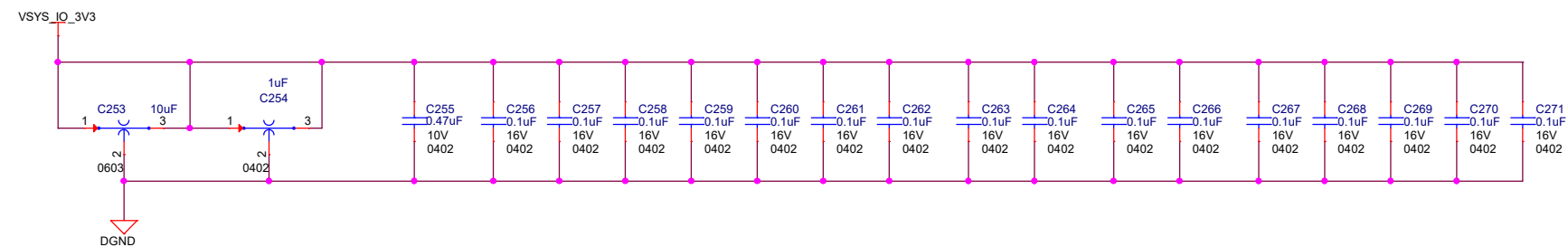
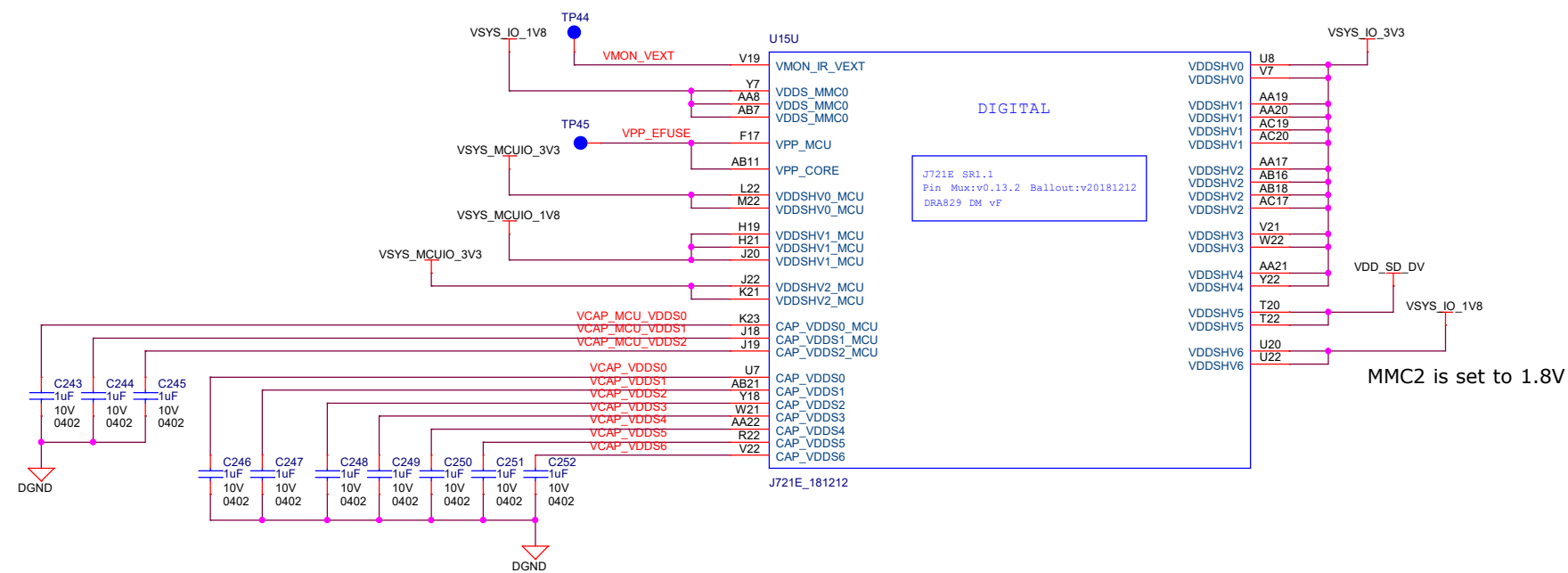
Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance ( $Z_t$ ).

|                  |                         |       |         |
|------------------|-------------------------|-------|---------|
|                  |                         |       |         |
| Title            |                         |       |         |
| SOC ANALOG POWER |                         |       |         |
| Size             | Document Number         |       | Rev     |
| A2               | -                       |       | <1.0>   |
| Date:            | Monday, August 24, 2026 | Sheet | 9 of 34 |

# DIGITAL POWER 1



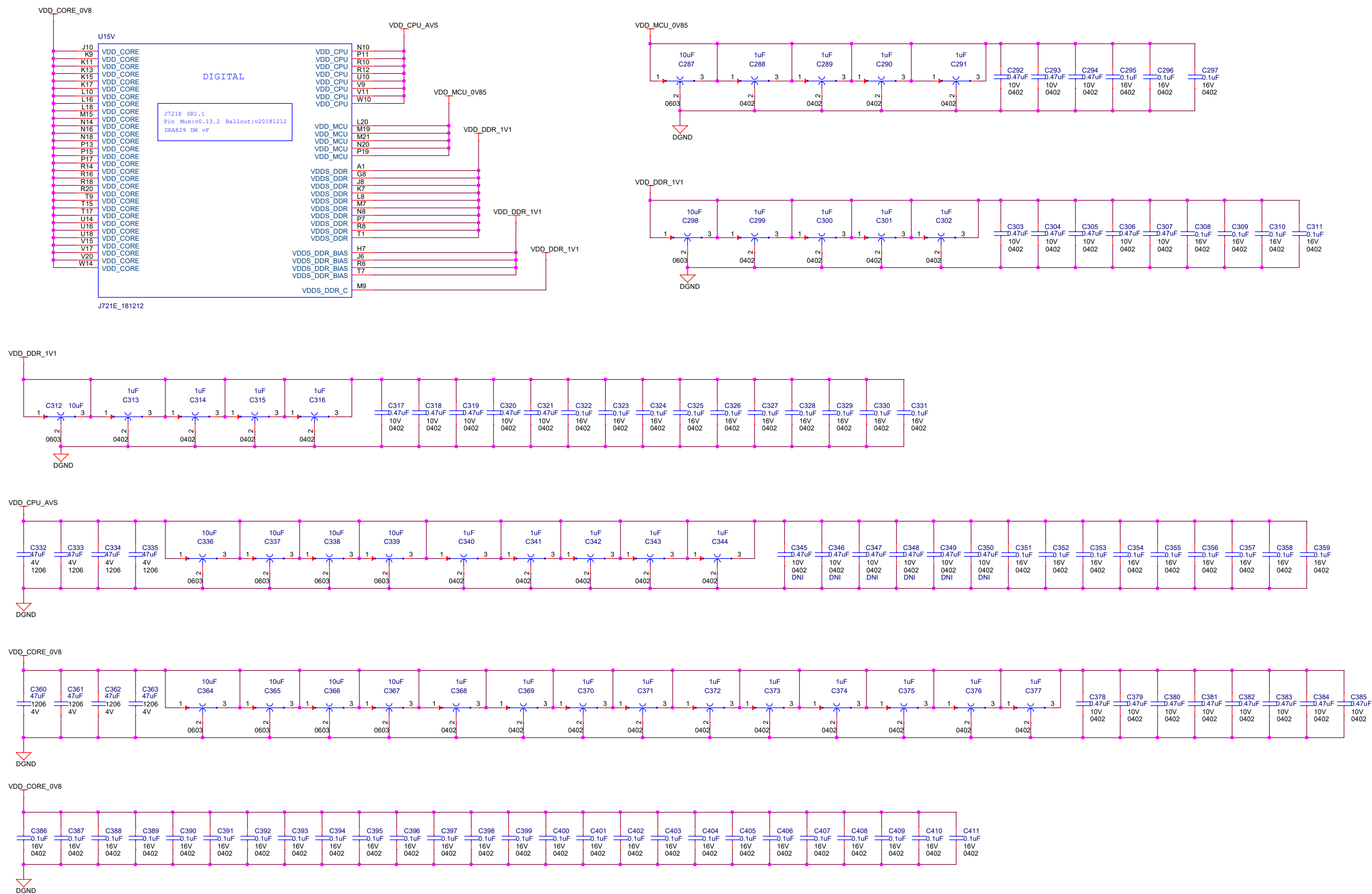
Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance ( $Z_t$ ).

|                              |                         |       |              |
|------------------------------|-------------------------|-------|--------------|
|                              |                         |       |              |
| Title<br>SOC DIGITAL POWER 1 |                         |       |              |
| Size<br>C                    | Document Number<br>-    |       | Rev<br><1.0> |
| Date:                        | Monday, August 24, 2026 | Sheet | 10 of 34     |

# DIGITAL POWER 2



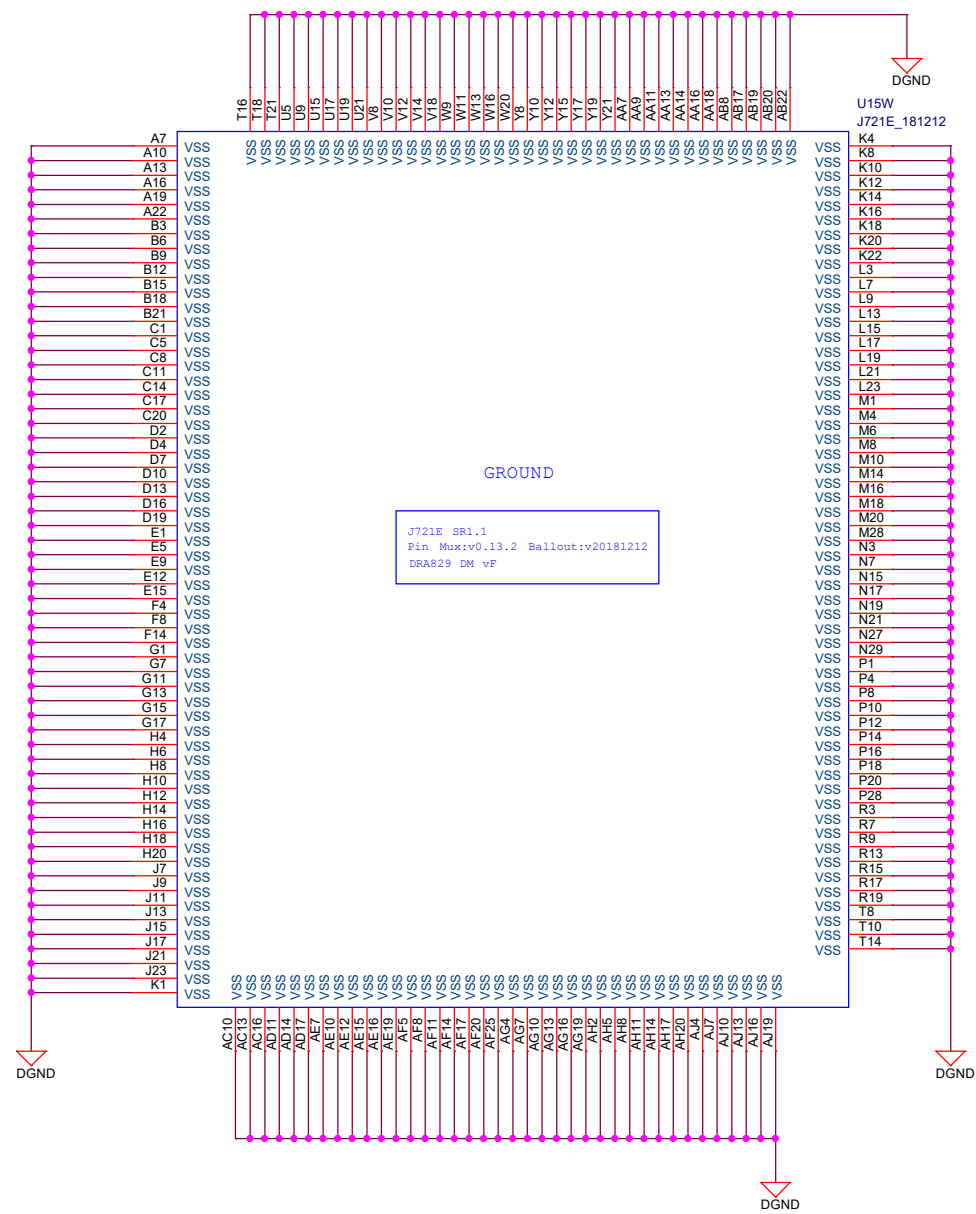
Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

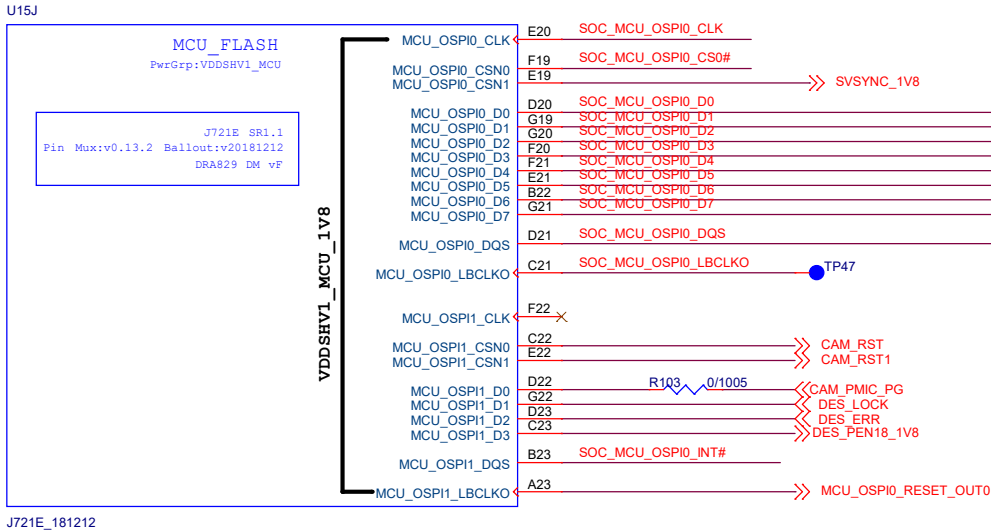
|                     |                         |       |          |
|---------------------|-------------------------|-------|----------|
|                     |                         |       |          |
| Title               |                         |       |          |
| SOC DIGITAL POWER 2 |                         |       |          |
| Size                | Document Number         |       | Rev      |
| C                   | -                       |       | <1.0     |
| Date:               | Monday, August 24, 2026 | Sheet | 11 of 34 |

SOC GROUND

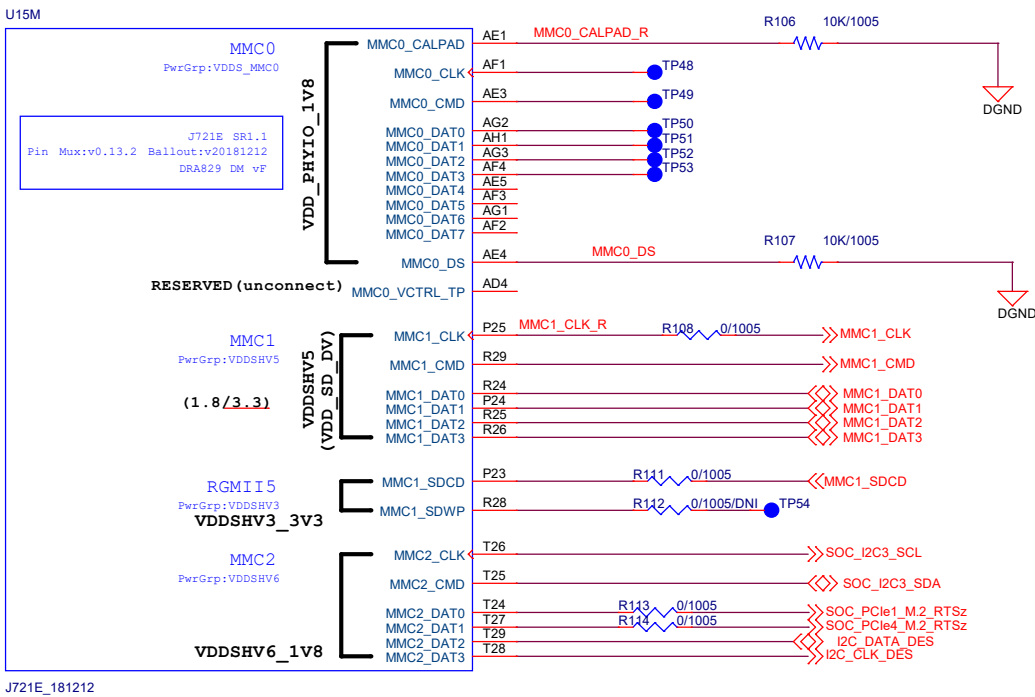


|       |                         |       |          |
|-------|-------------------------|-------|----------|
| Title |                         |       | SOC GND  |
| Size  | Document Number         | Rev   |          |
| C     | -                       | <1.0> |          |
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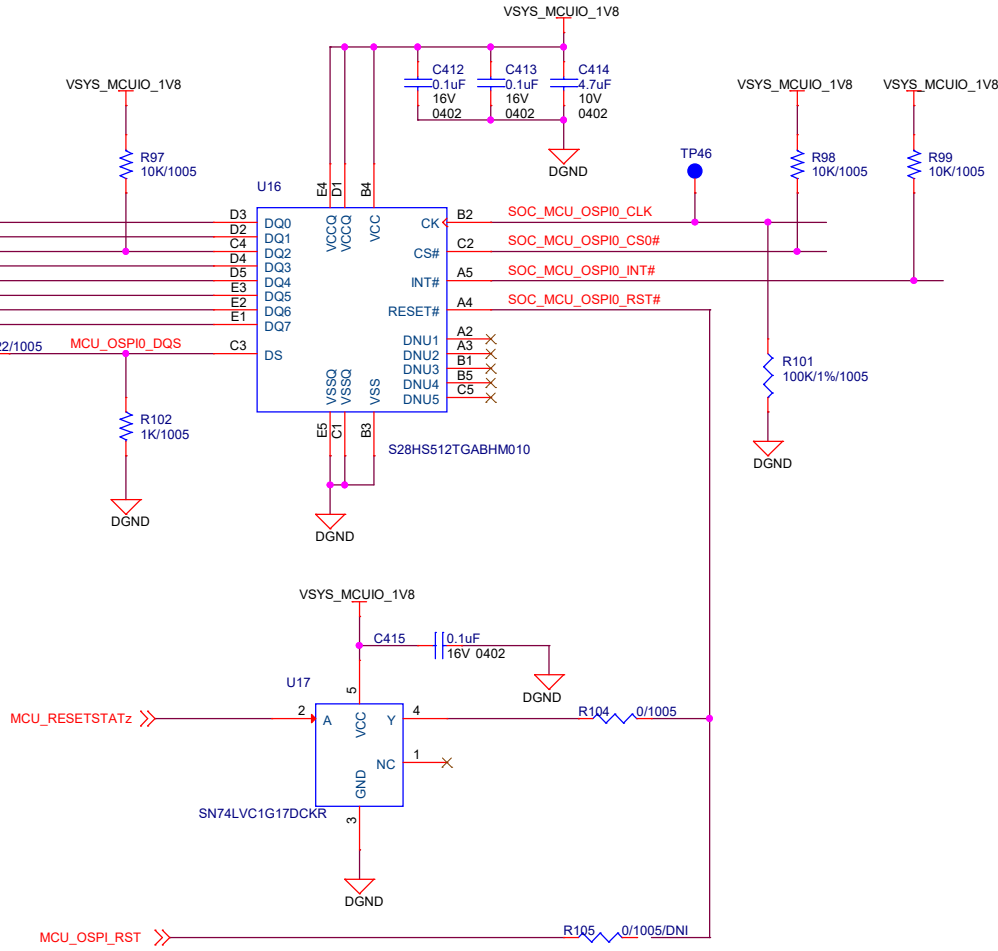
## MCU FLASH



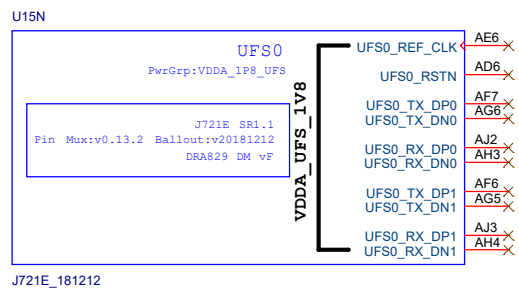
# MMC Interface



# OSPI FLASH

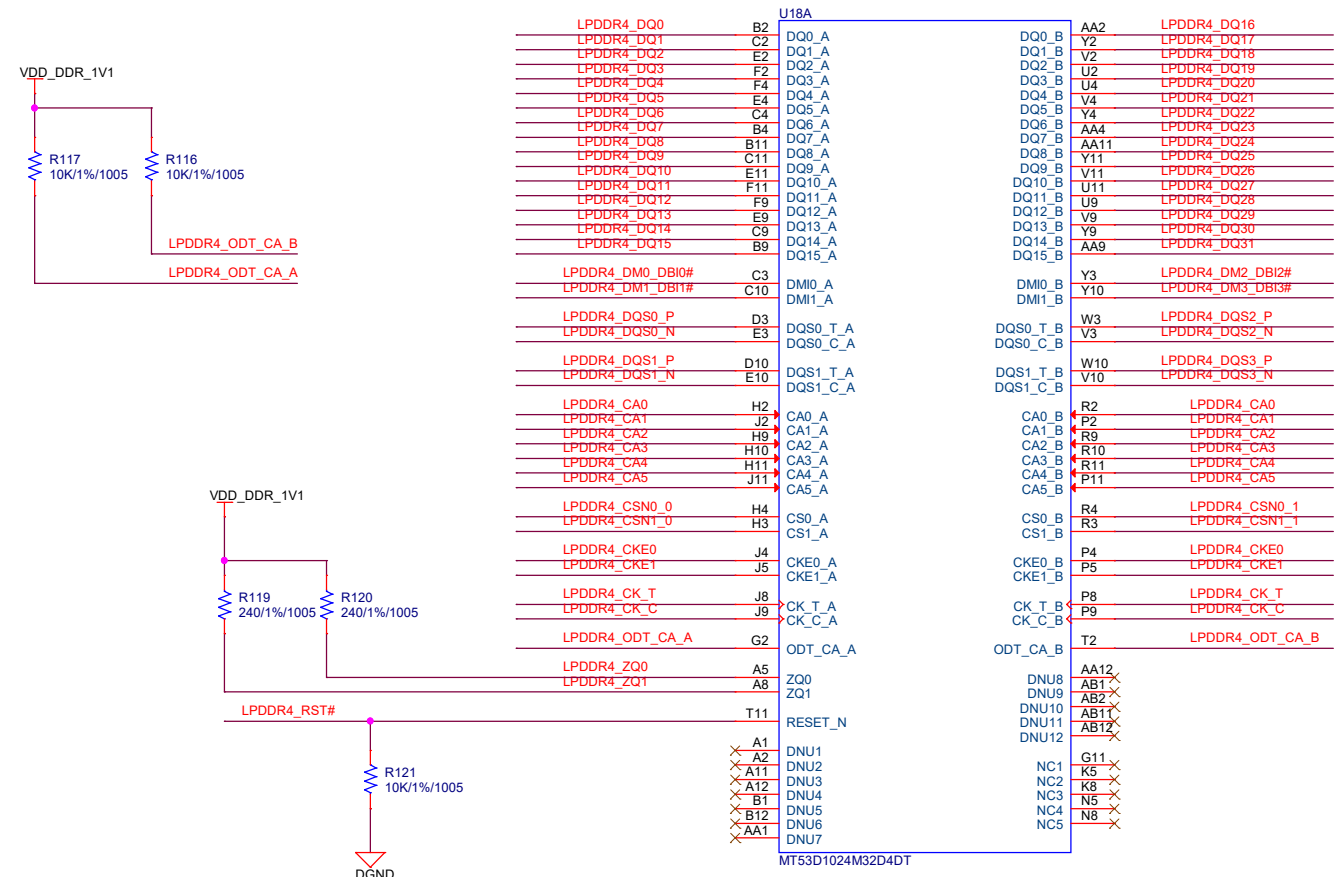


# UFS Interface

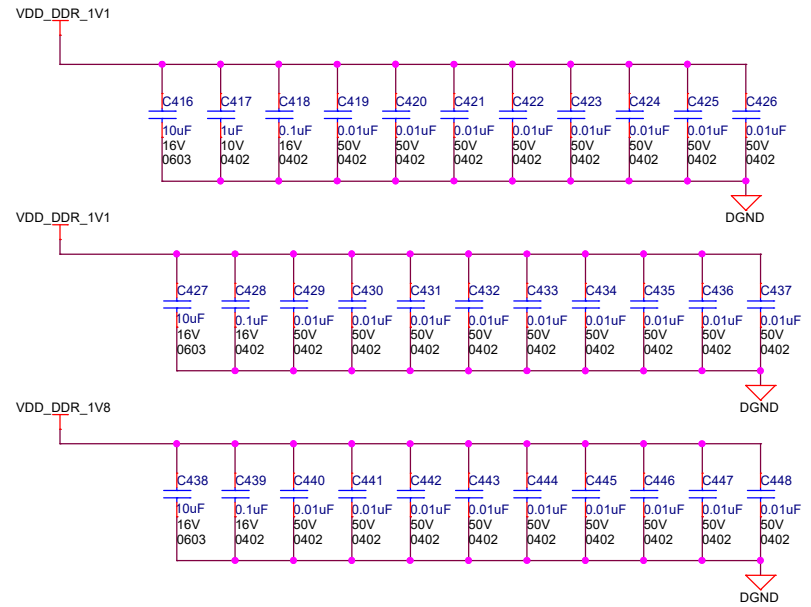
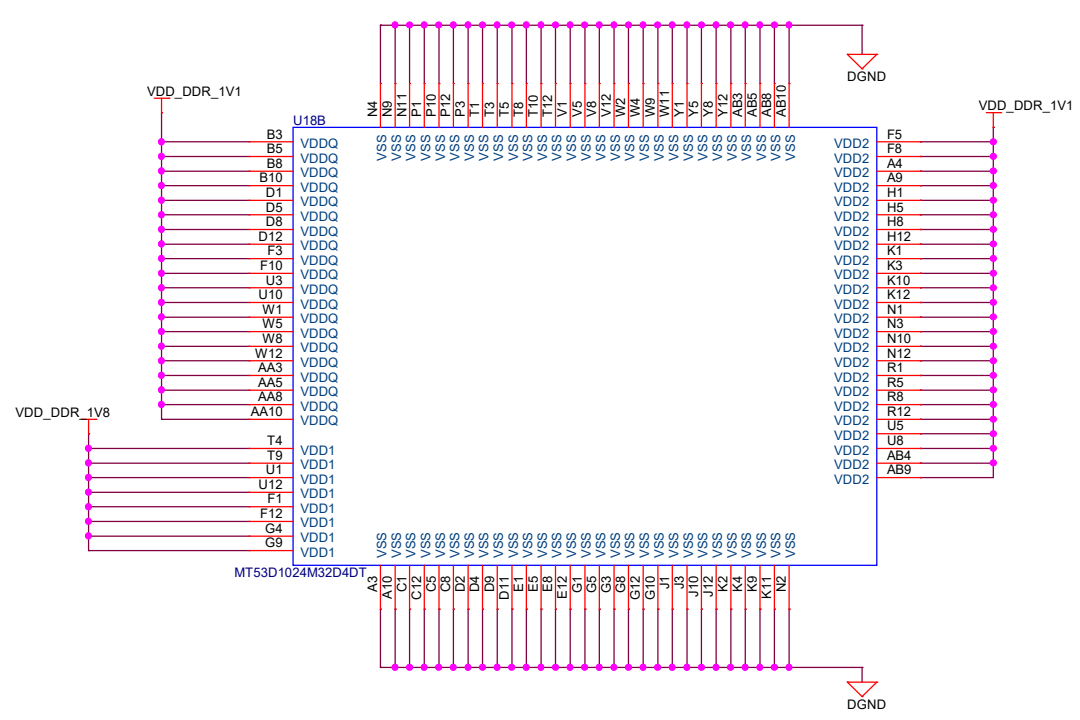
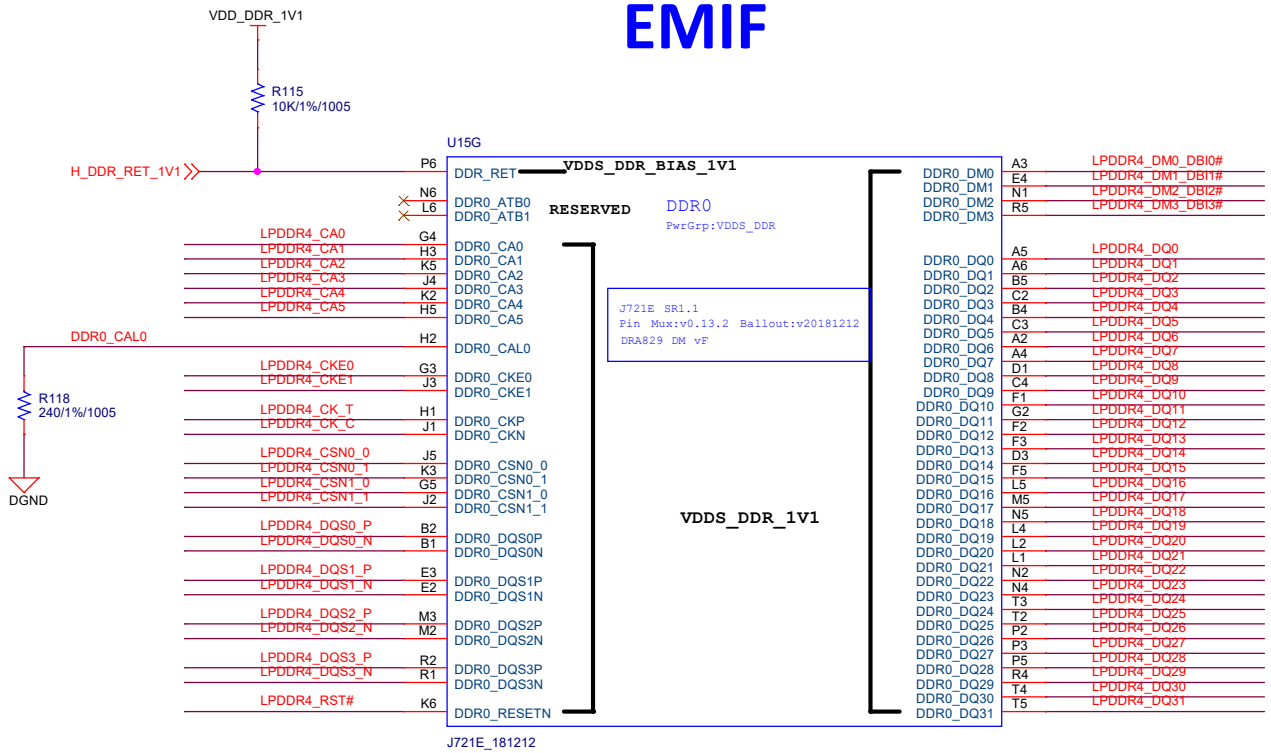


|                          |                          |                |             |
|--------------------------|--------------------------|----------------|-------------|
| Title                    |                          |                |             |
| SOC MCU FLASH_MMC_UFS IF |                          |                |             |
| Size<br>C                | Document Number<br>-     |                | Rev<br><1.0 |
| Date:                    | Tuesday, August 25, 2026 | Sheet 13 of 34 |             |

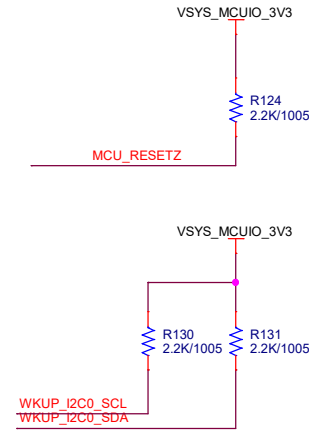
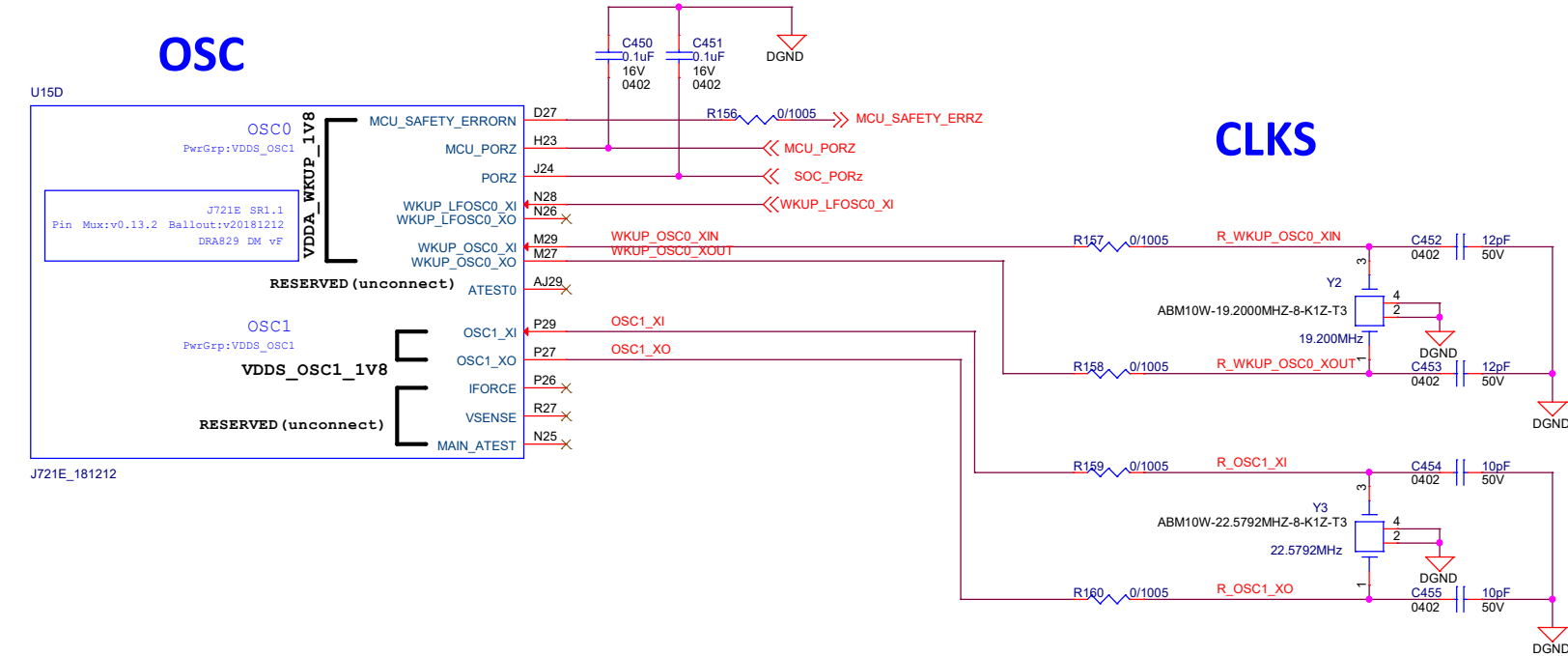
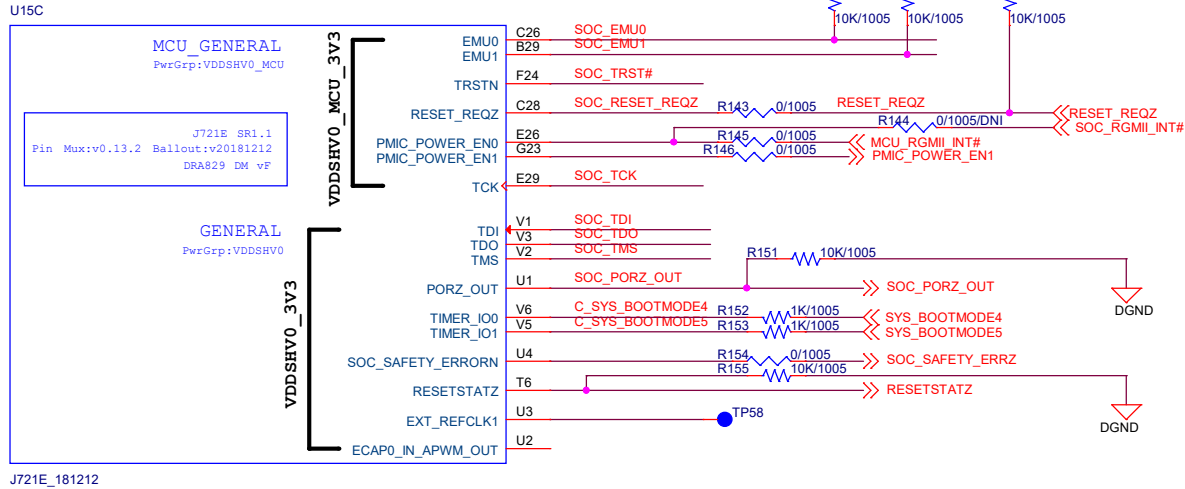
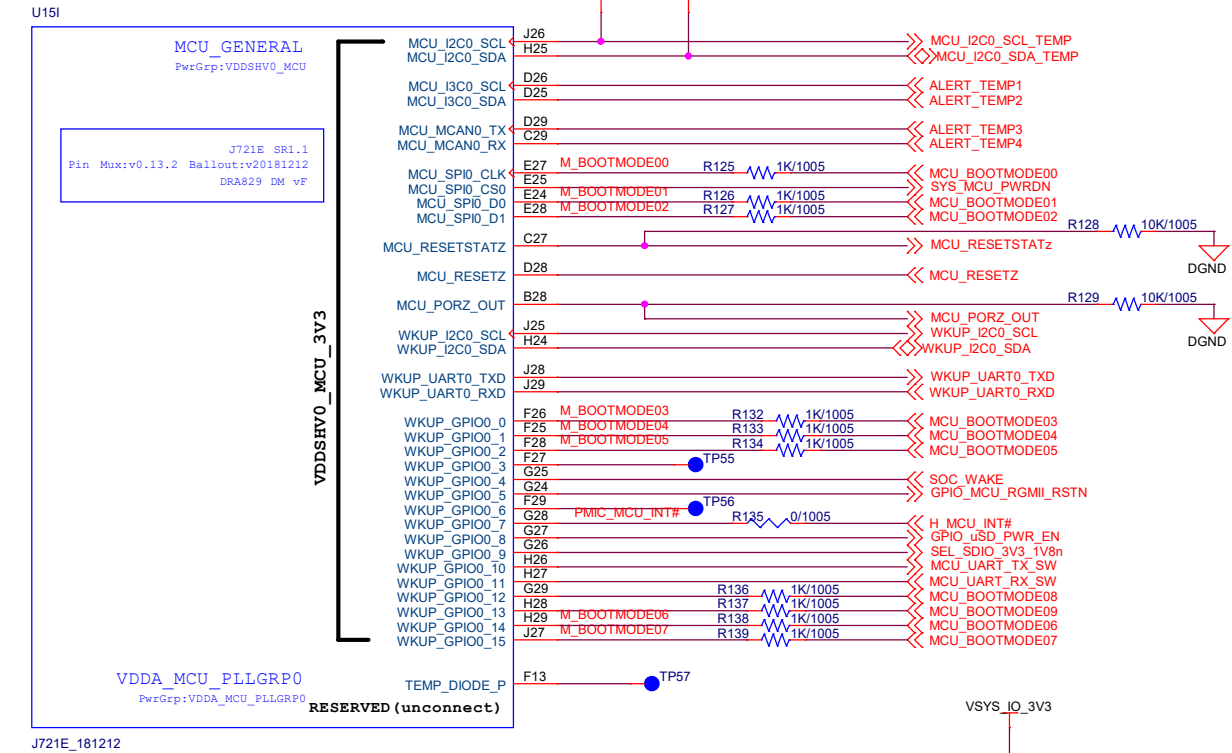
LPDDR4



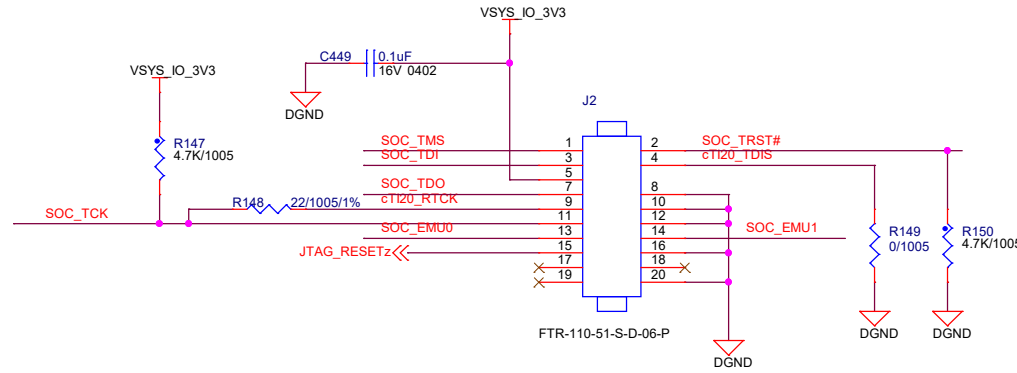
EMIF



# MCU & MAIN GENERAL IO, OSC CLKS

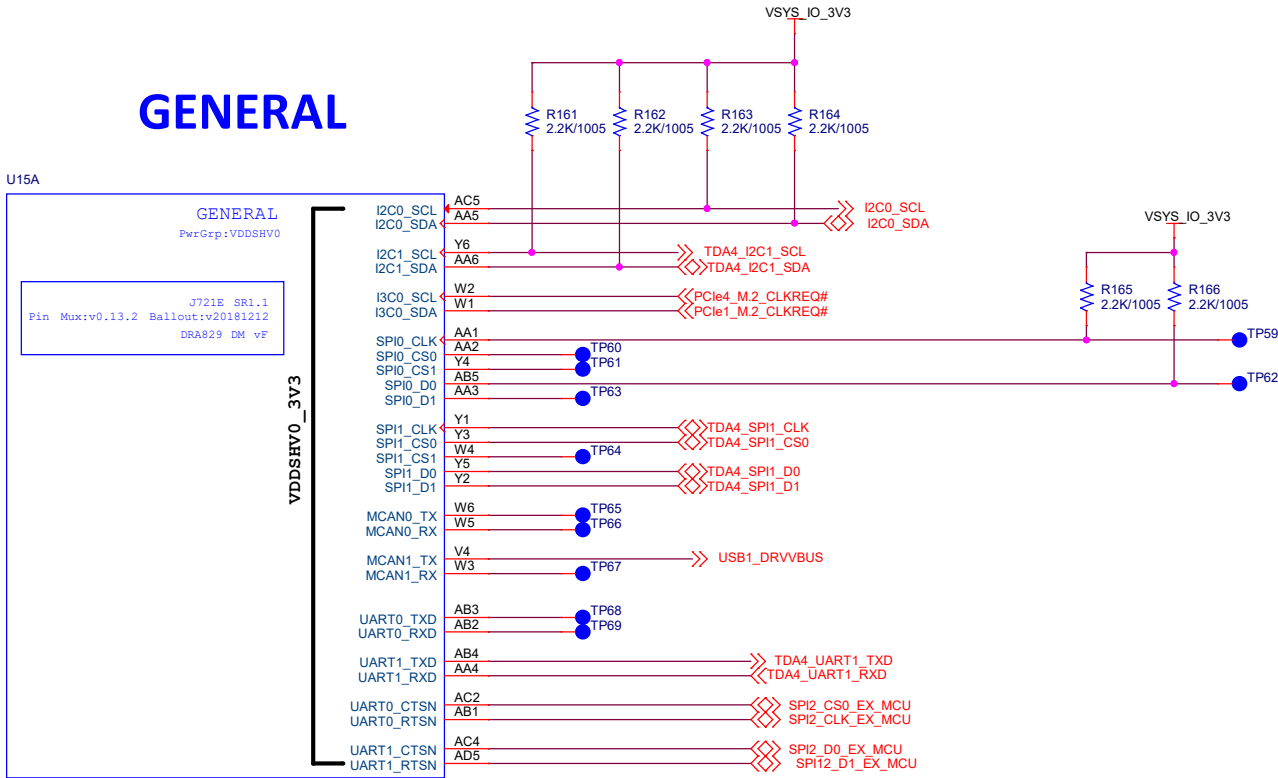


## cTI 20PIN JTAG HEADER

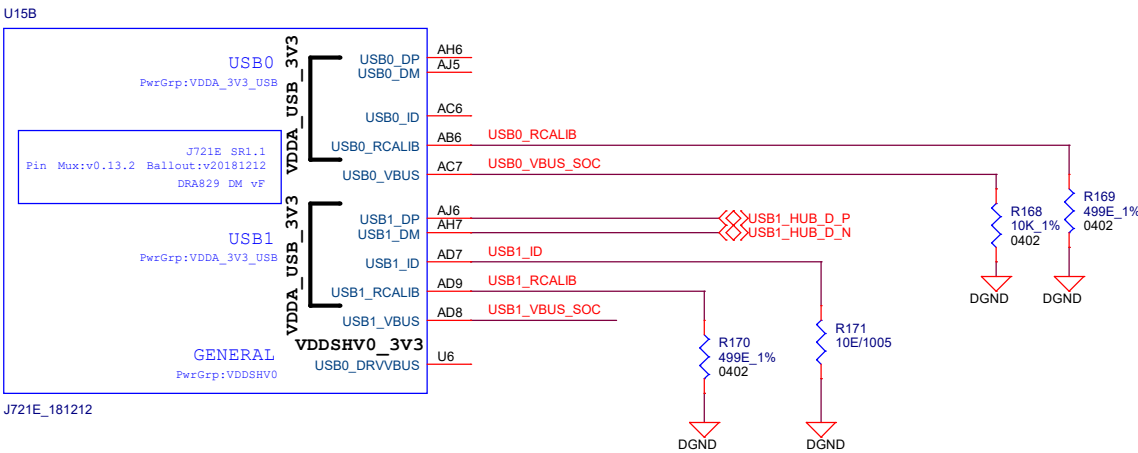


|                         |                          |       |          |
|-------------------------|--------------------------|-------|----------|
| Title                   |                          |       |          |
| SOC MCU&MAIN GEN IO,OSC |                          |       |          |
| Size                    | Document Number          |       | Rev      |
| C                       |                          |       | <1.0>    |
| Date:                   | Tuesday, August 25, 2026 | Sheet | 15 of 34 |

## GENERAL

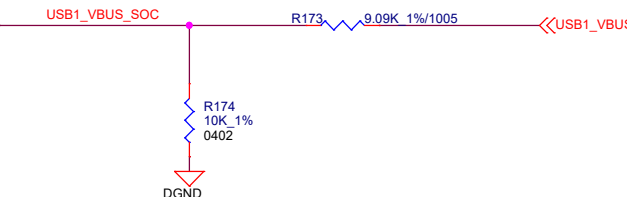


## USB



USB1 ID Pulled low. J7 SoC in Host Mode.

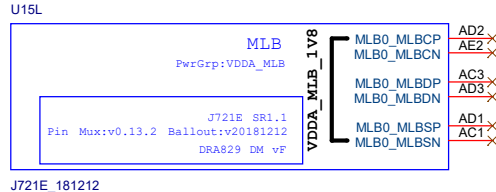
Note: Recommended VBUS circuit for embedded Hub



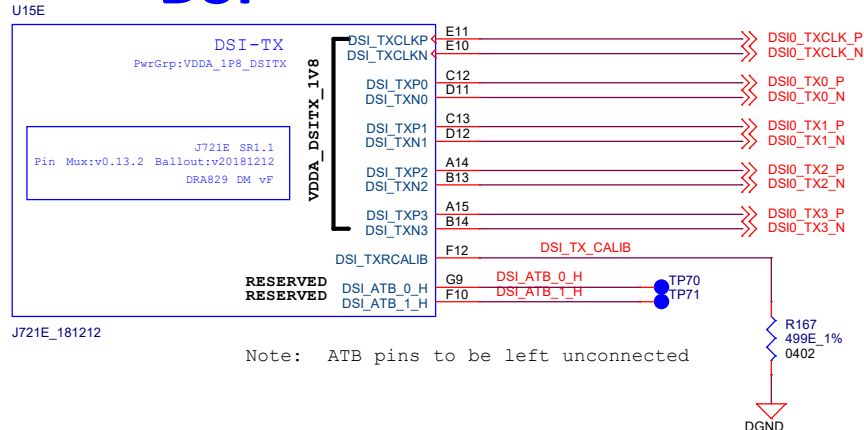
## USB VBUS Resistor divider circuit

Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS

MLB

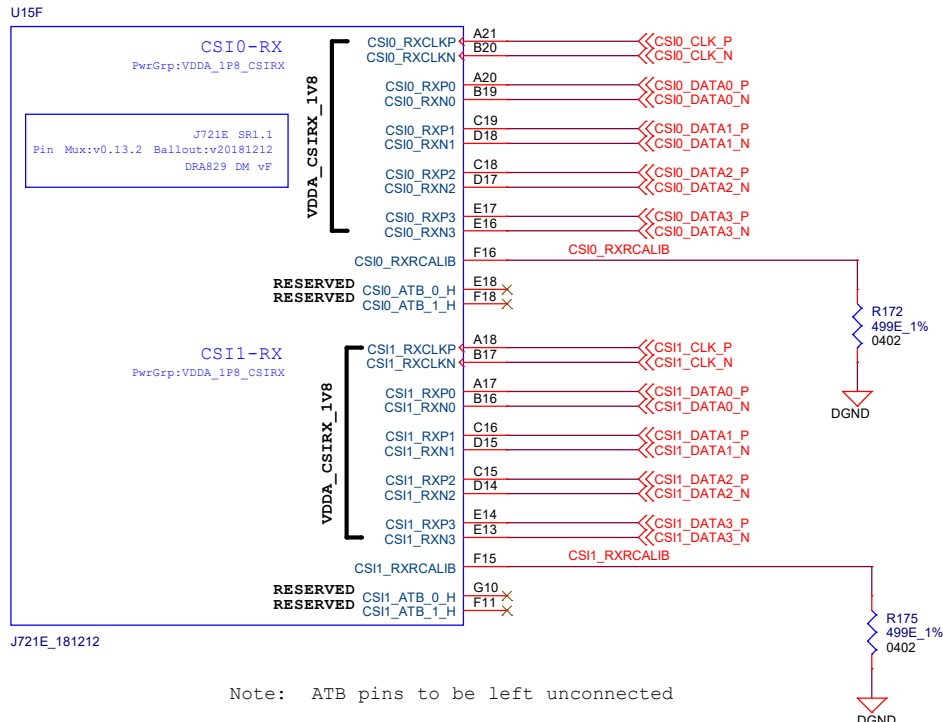


## DSI



Note: ATB pins to be left unconnected

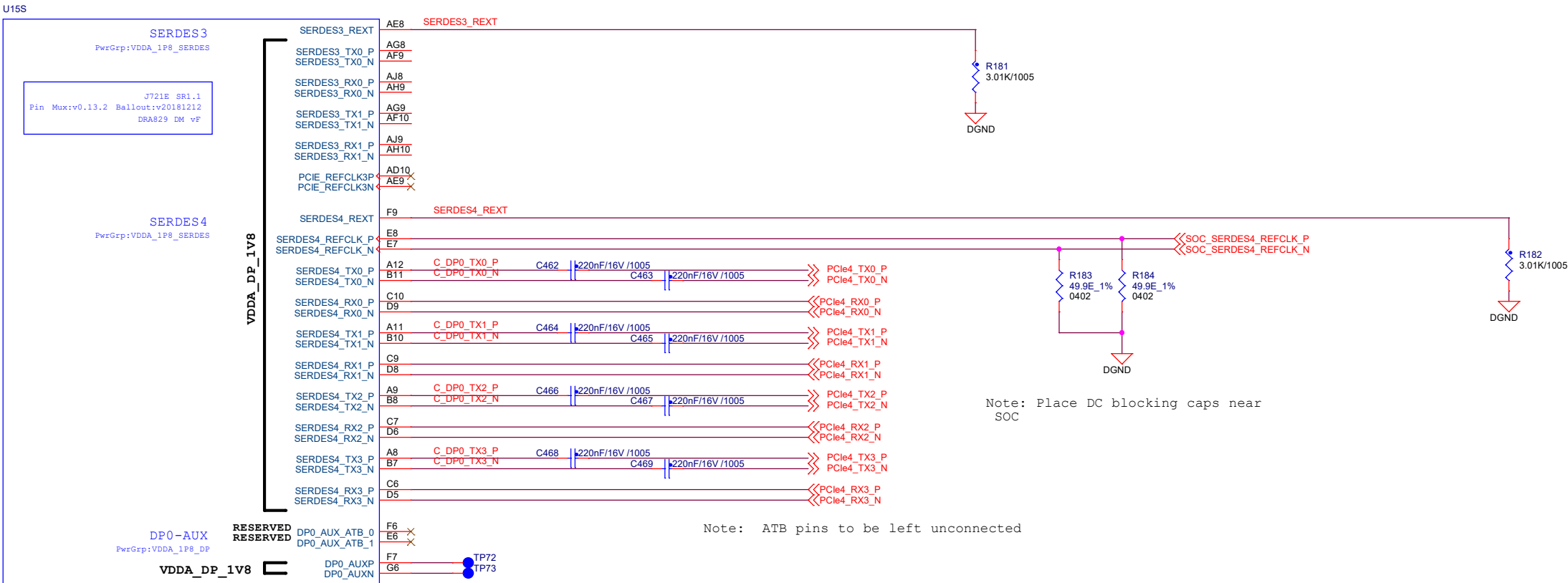
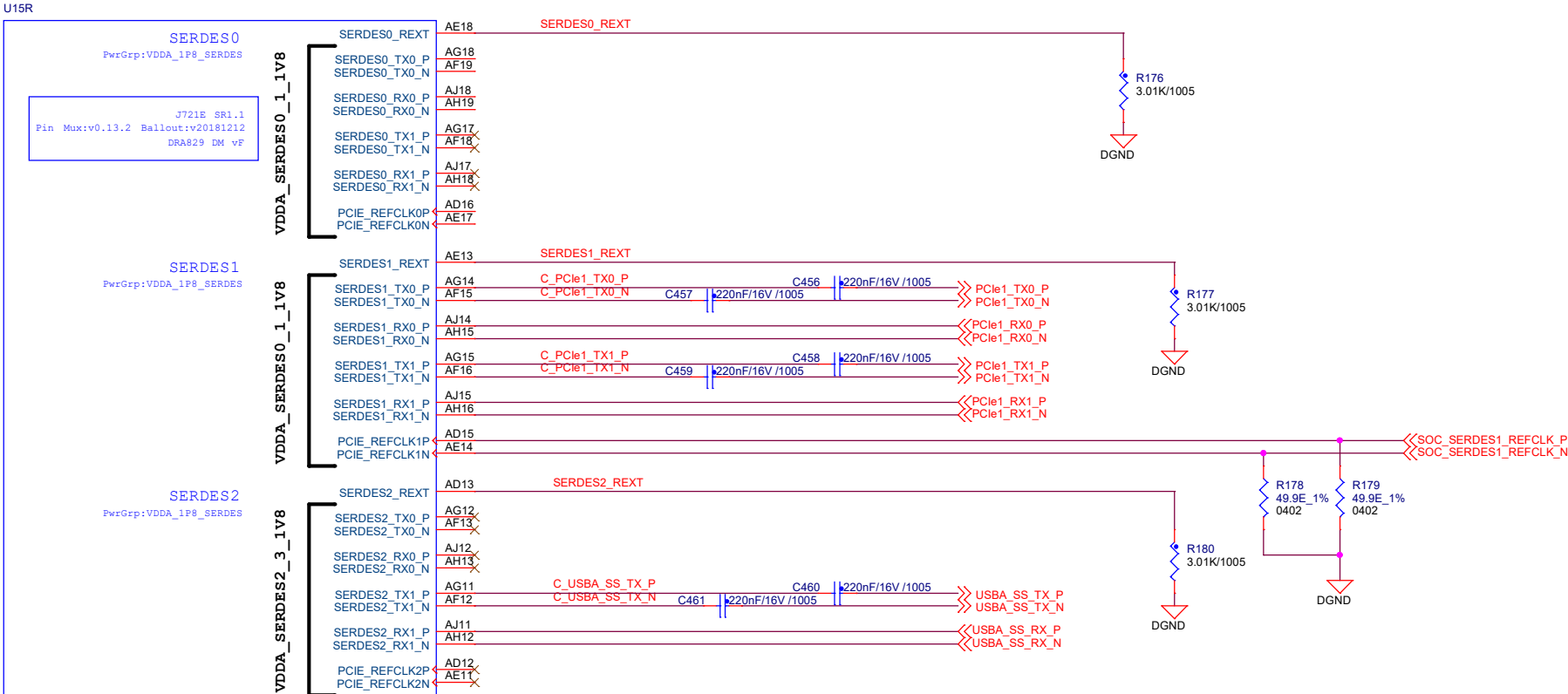
# CSI Interface



Note: ATB pins to be left unconnected

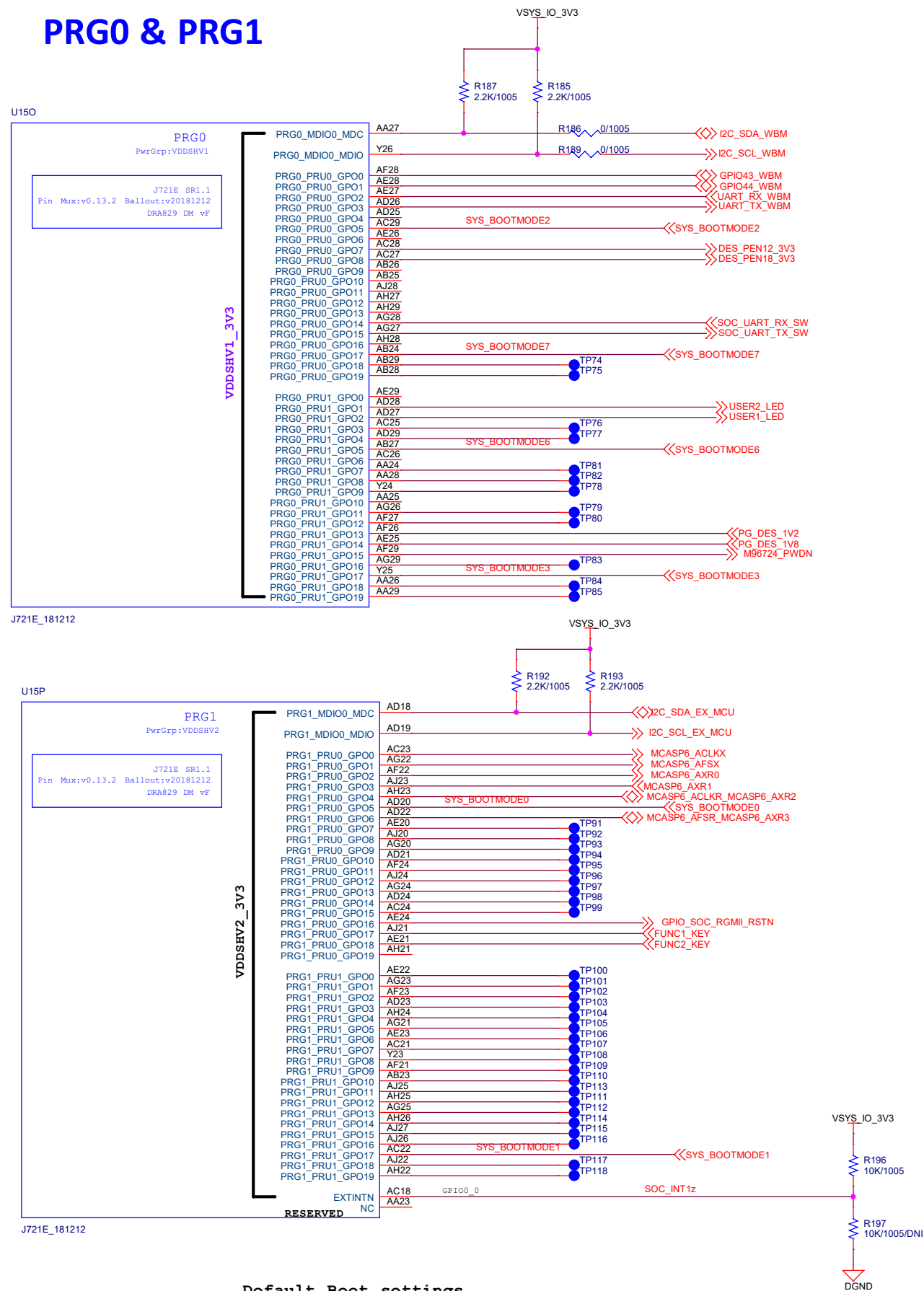
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| Title                   |                      |       |             |
| SOC GEN_USB_MLB_CSI_DSI |                      |       |             |
| Size<br>C               | Document Number<br>- |       | Rev<br>C1.0 |
| Date                    | Expiry/Amend Of      | Sheet | 46 of 94    |

# SERDES



|               |                          |                |             |
|---------------|--------------------------|----------------|-------------|
| Title         |                          |                |             |
| SOC SERDES IF |                          |                |             |
| Size<br>C     | Document Number<br>-     |                | Rev<br><1.0 |
| Date:         | Tuesday, August 25, 2026 | Sheet 17 of 34 |             |

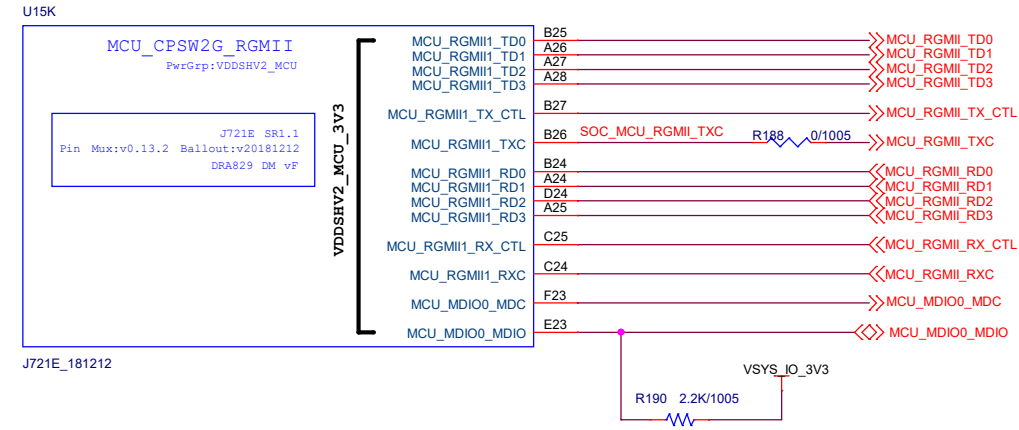
## PRG0 & PRG1



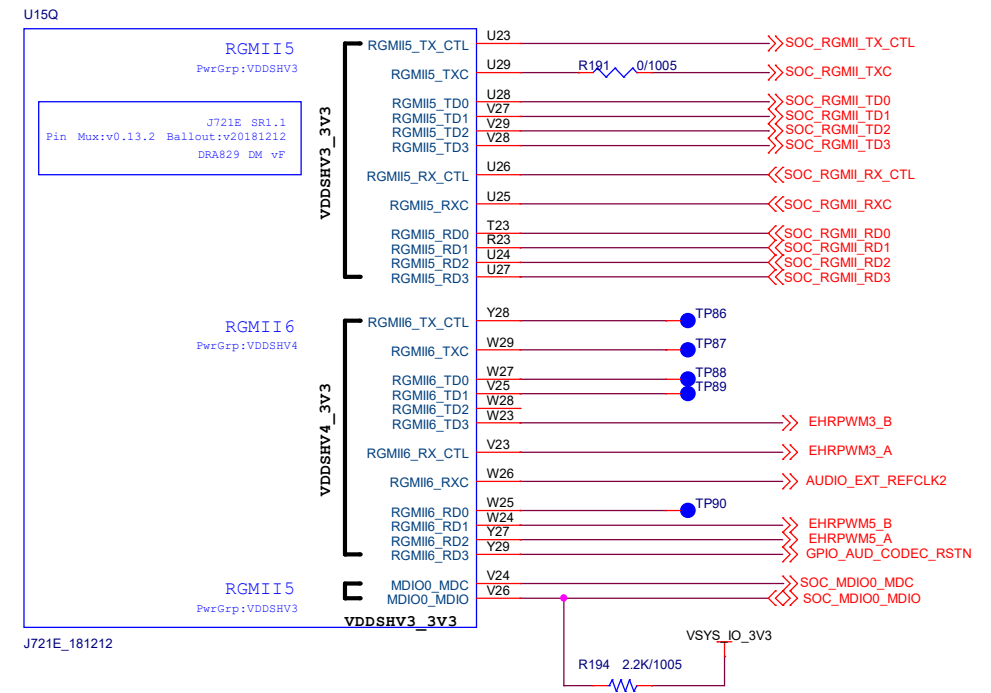
Default Boot settings  
set to SD boot

SYS\_BOOTMODE0 : H  
SYS\_BOOTMODE6 : H

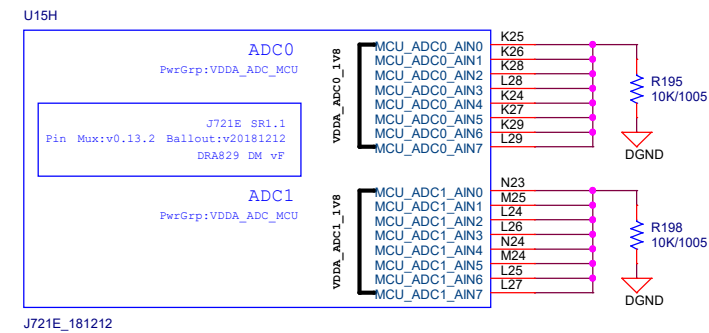
## MCU\_RGMII



## MAIN RGMII

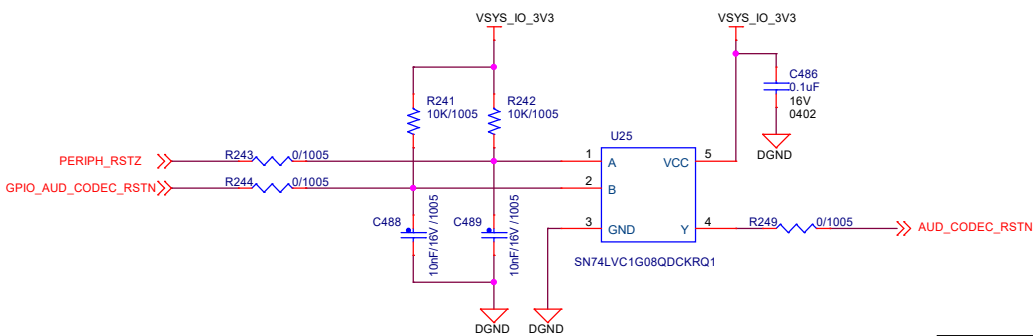
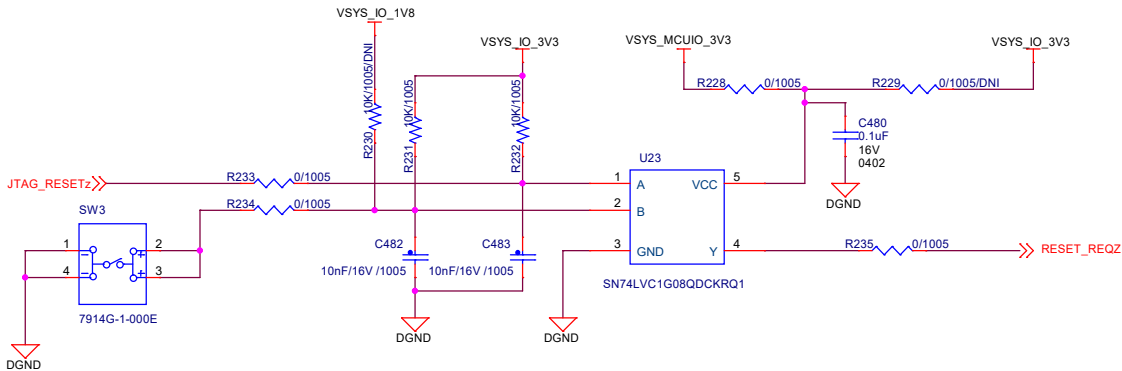
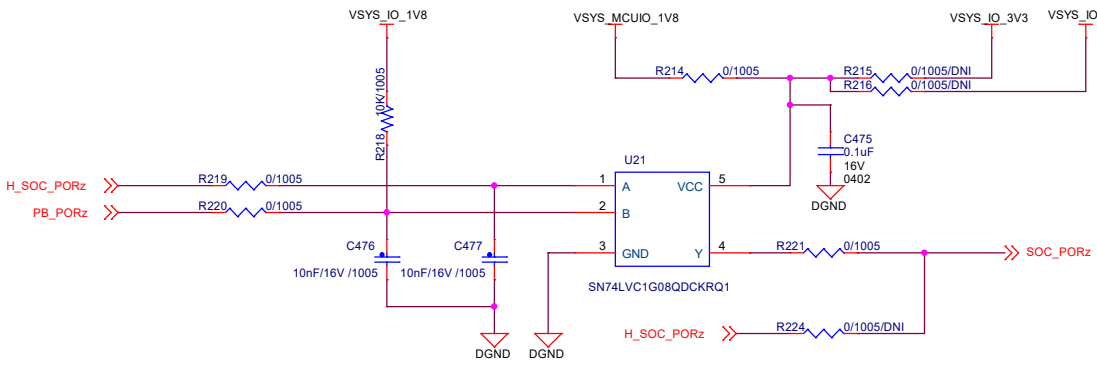
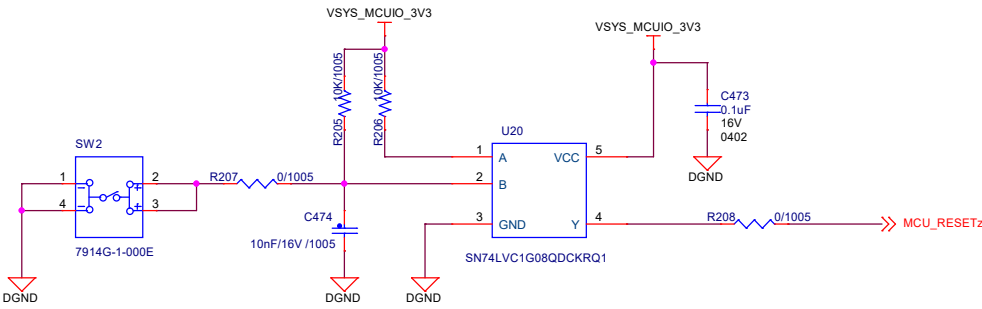
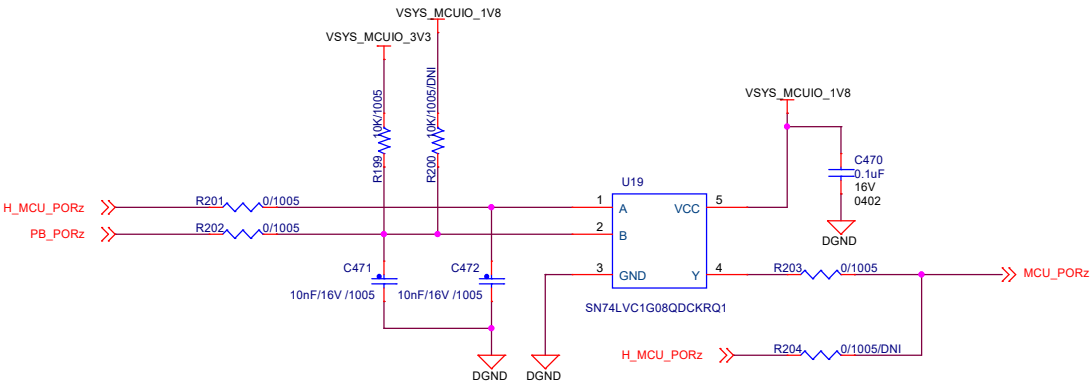
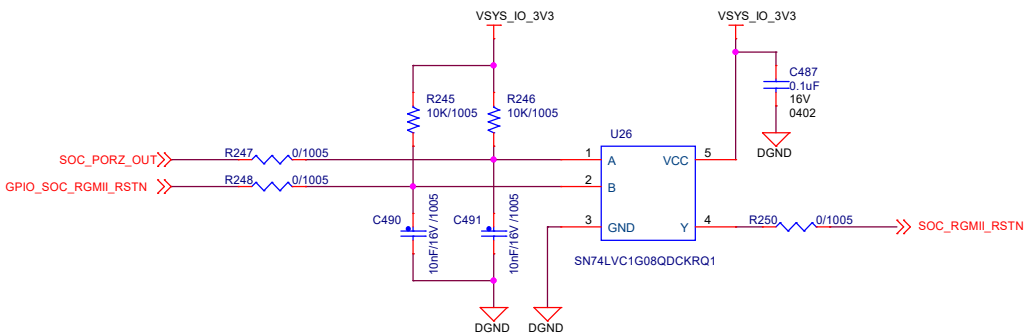
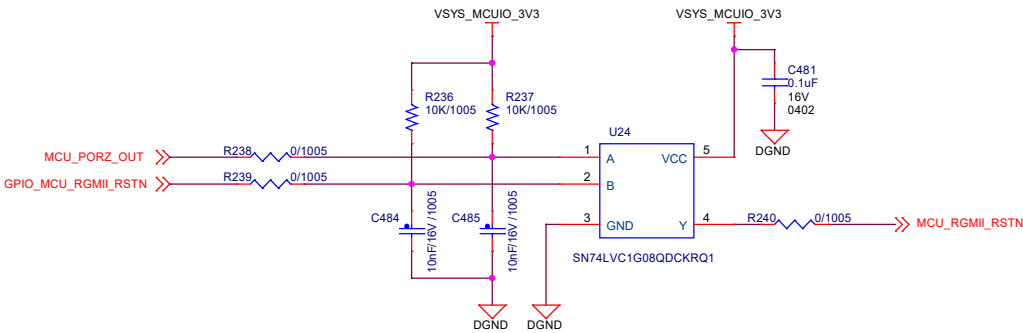
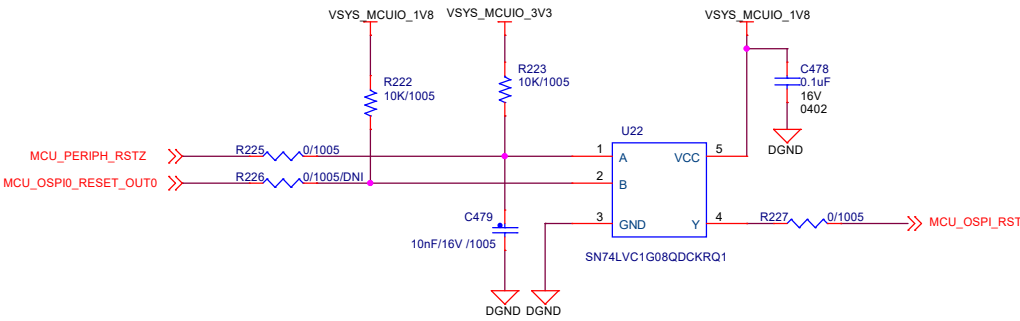
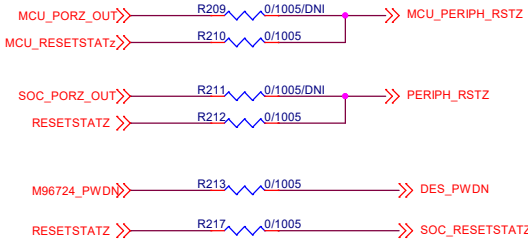


## MCU ADCs



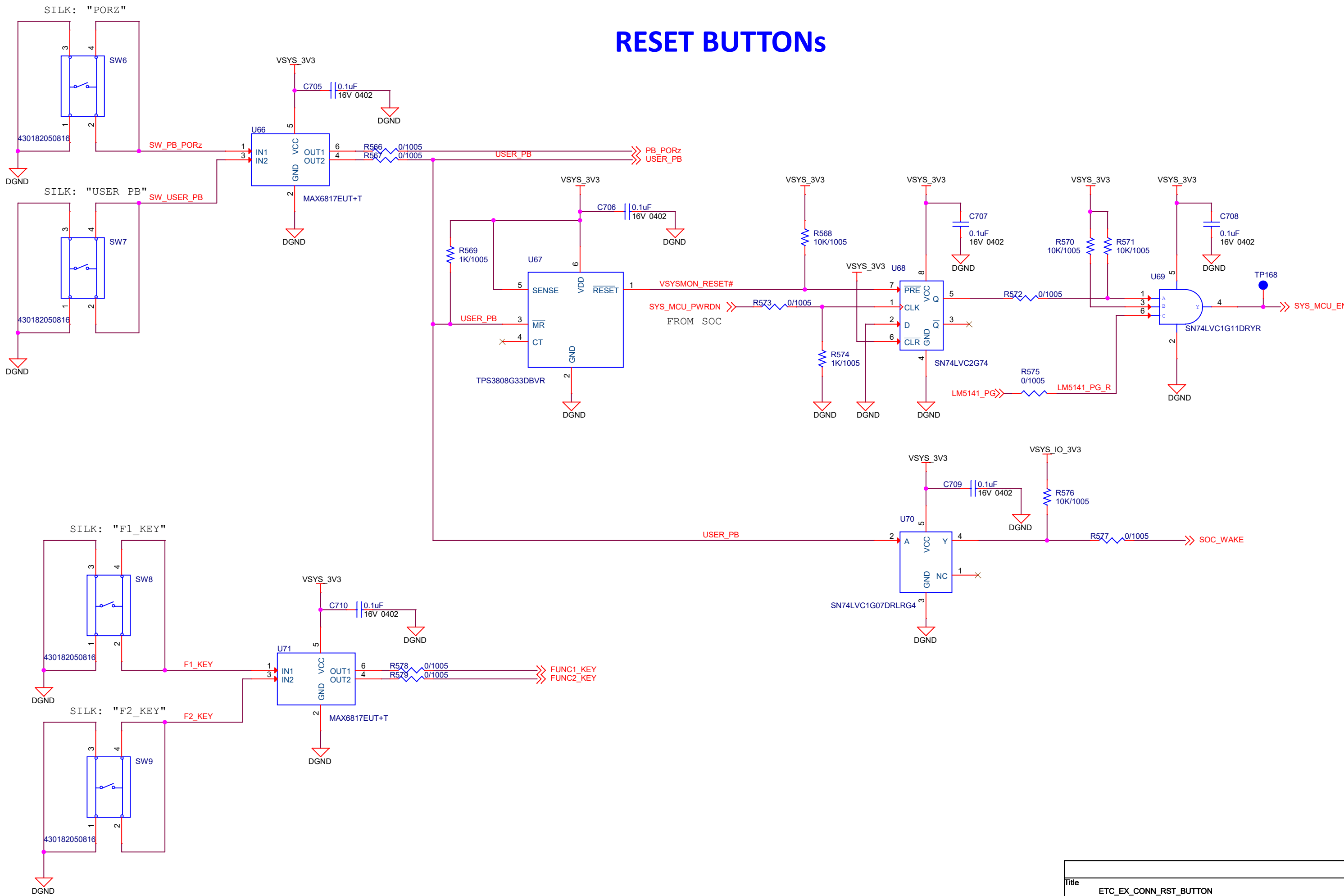
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|-------|--------------------------|-------|---------------------------|-------|
| Title |                          |       | SOC_MCU_RGMII_ADC_PROG0_1 |       |
| Size  | Document Number          |       | Rev                       |       |
| C     |                          |       | <1.0>                     |       |
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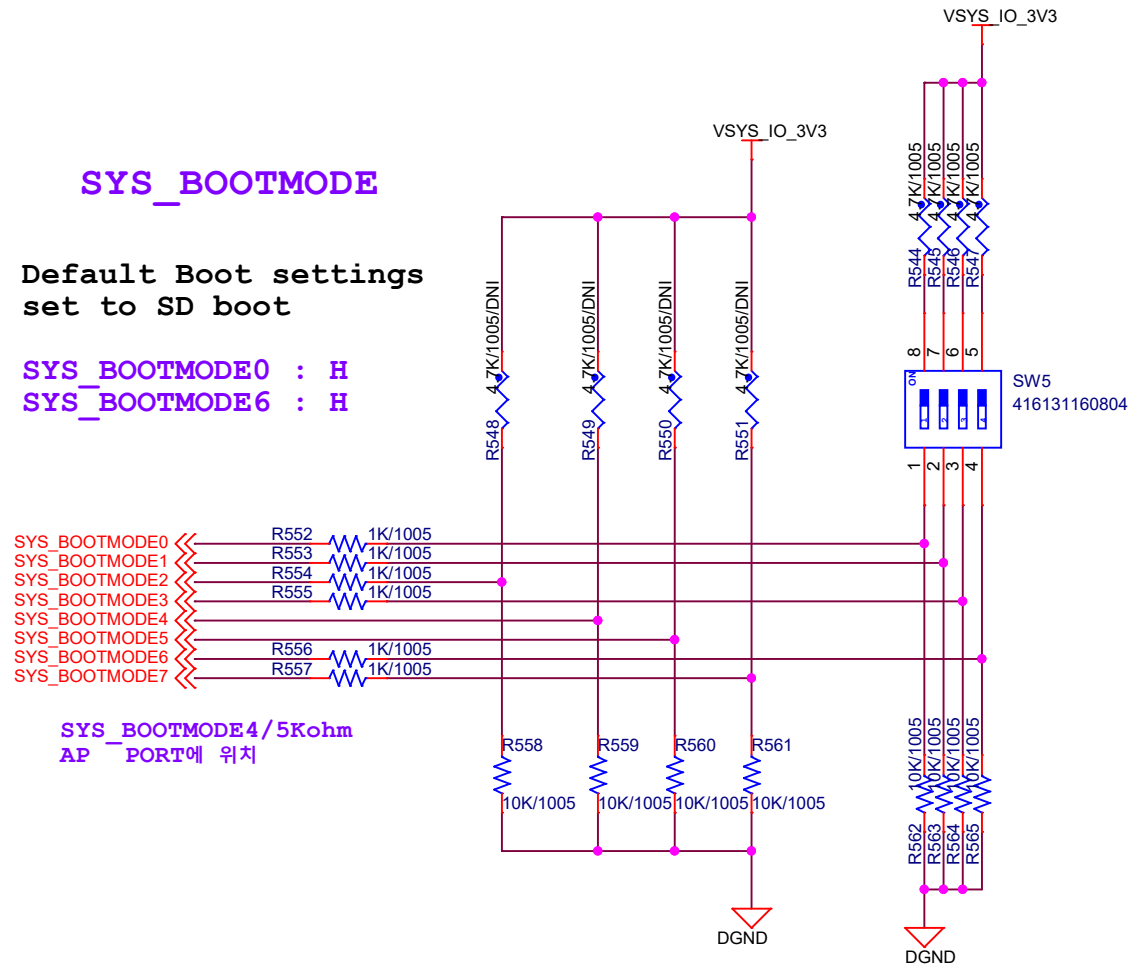
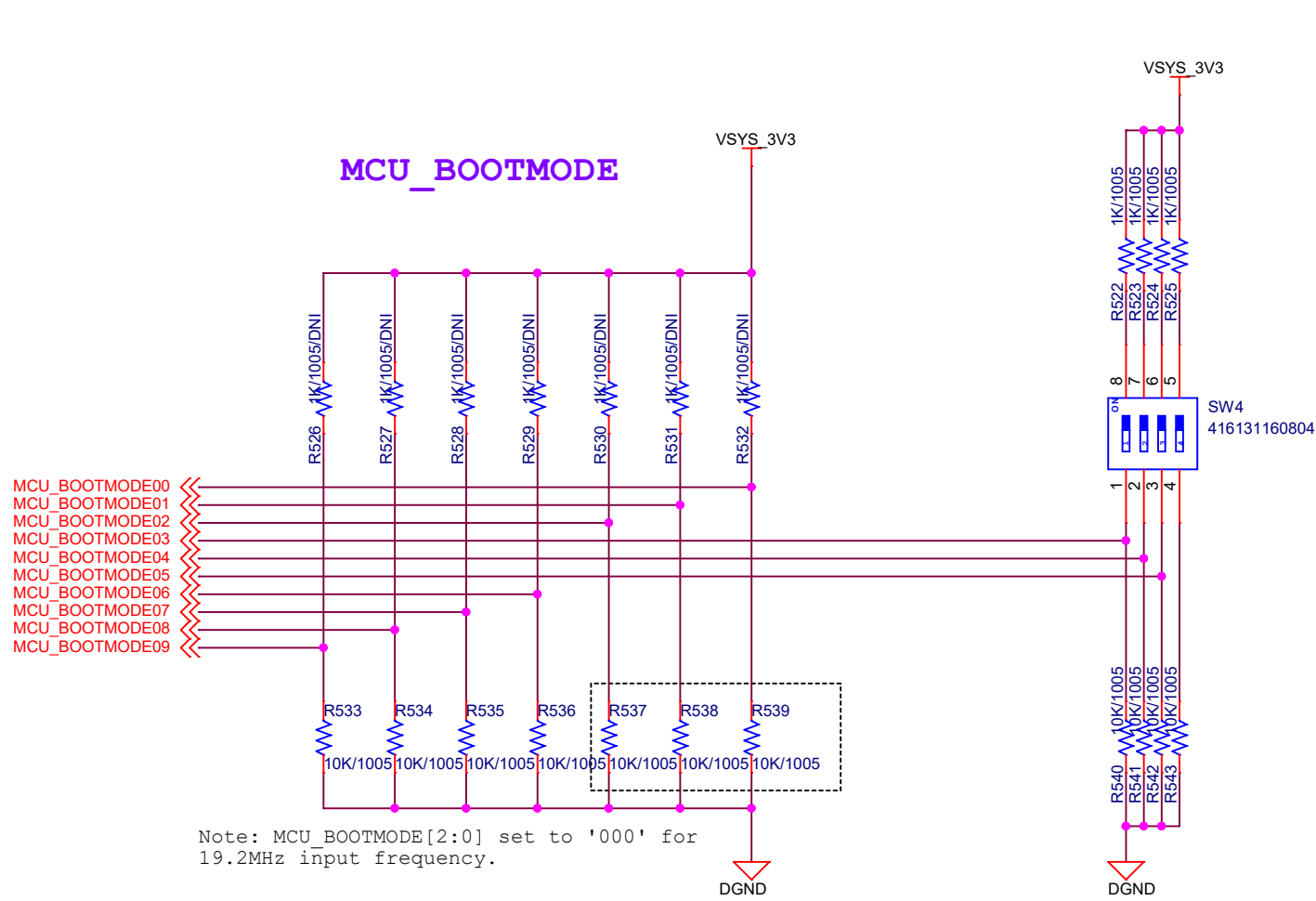
RESET SIGNAL



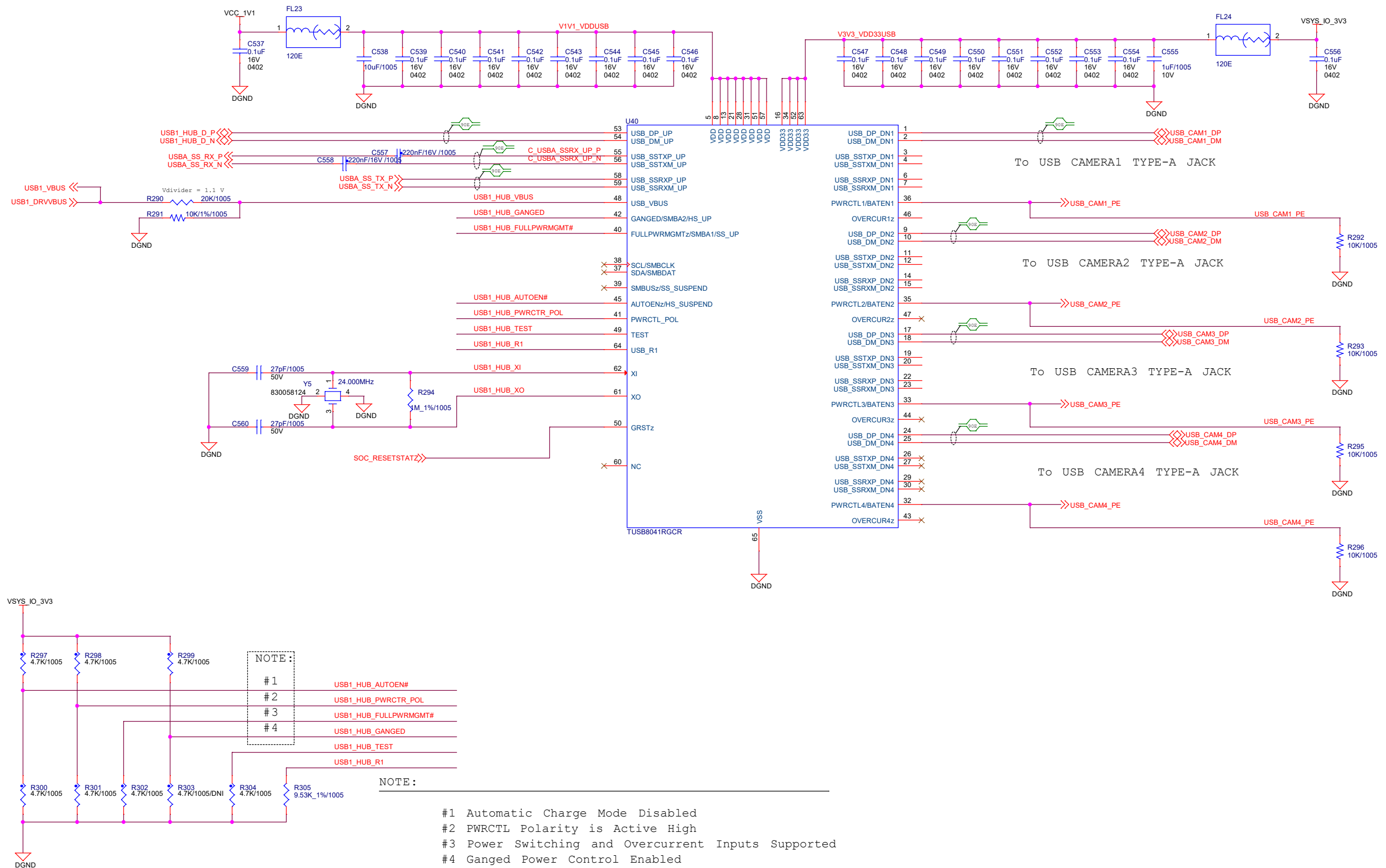
|                                |                 |       |
|--------------------------------|-----------------|-------|
| Title                          |                 |       |
| RESET                          |                 |       |
| Size                           | Document Number | Rev   |
| A2                             | -               | <1.0> |
| Date: Tuesday, August 25, 2026 |                 |       |
| Sheet 19 of 34                 |                 |       |

# RESET BUTTONs



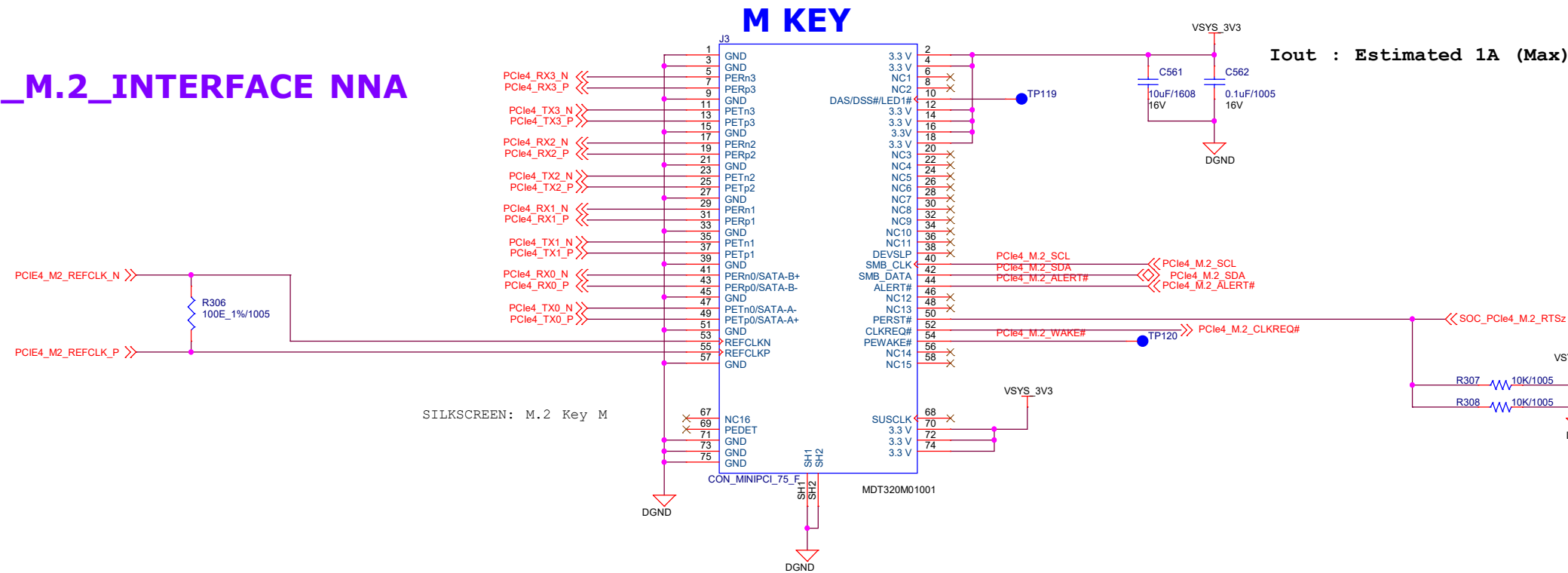


# USB3.0 HUB

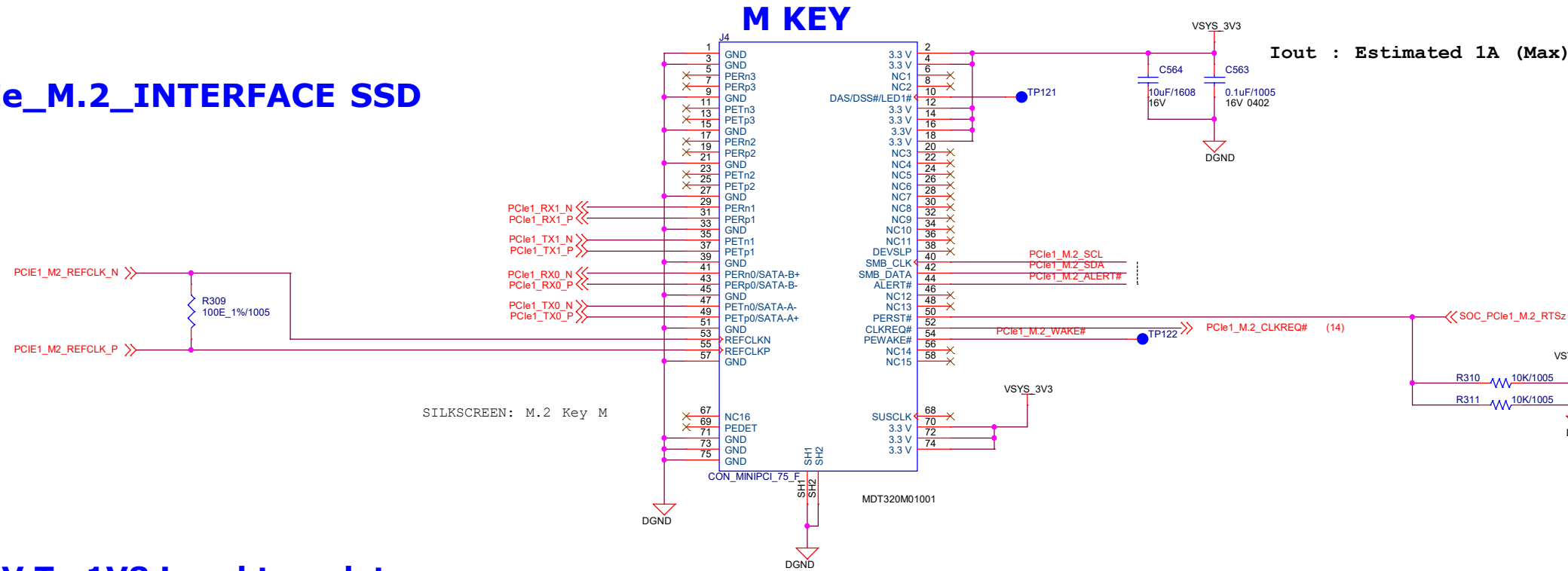


|       |                          |                 |                   |    |       |
|-------|--------------------------|-----------------|-------------------|----|-------|
| Title |                          |                 | USB3.0 HUB_USB2.0 |    |       |
| Size  | C                        | Document Number |                   |    | Rev   |
|       |                          | -               |                   |    | <1.0> |
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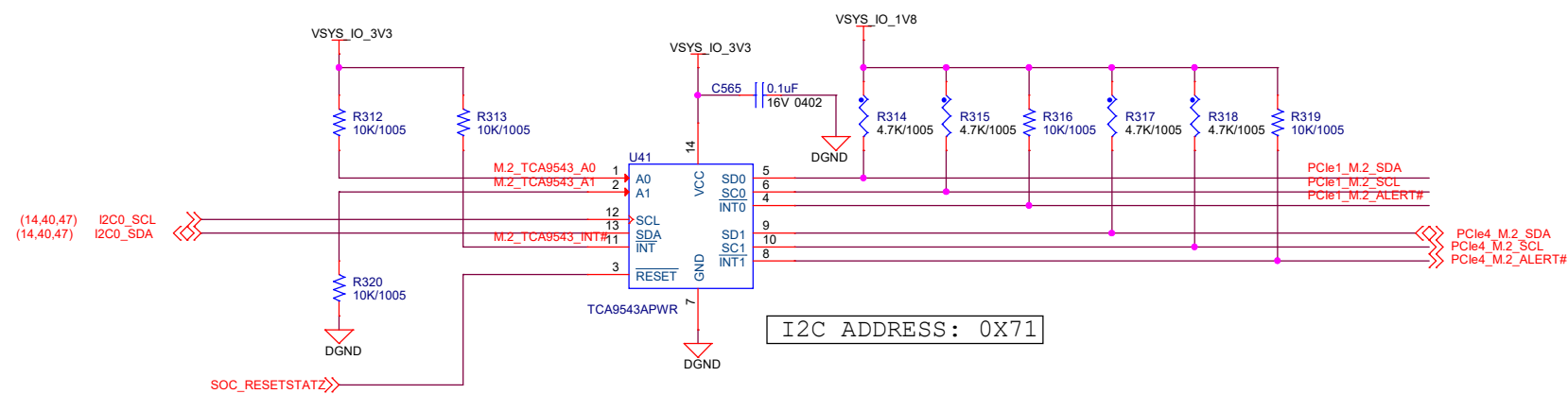
PCIe\_M.2\_INTERFACE NNA



PCIe\_M.2\_INTERFACE SSD

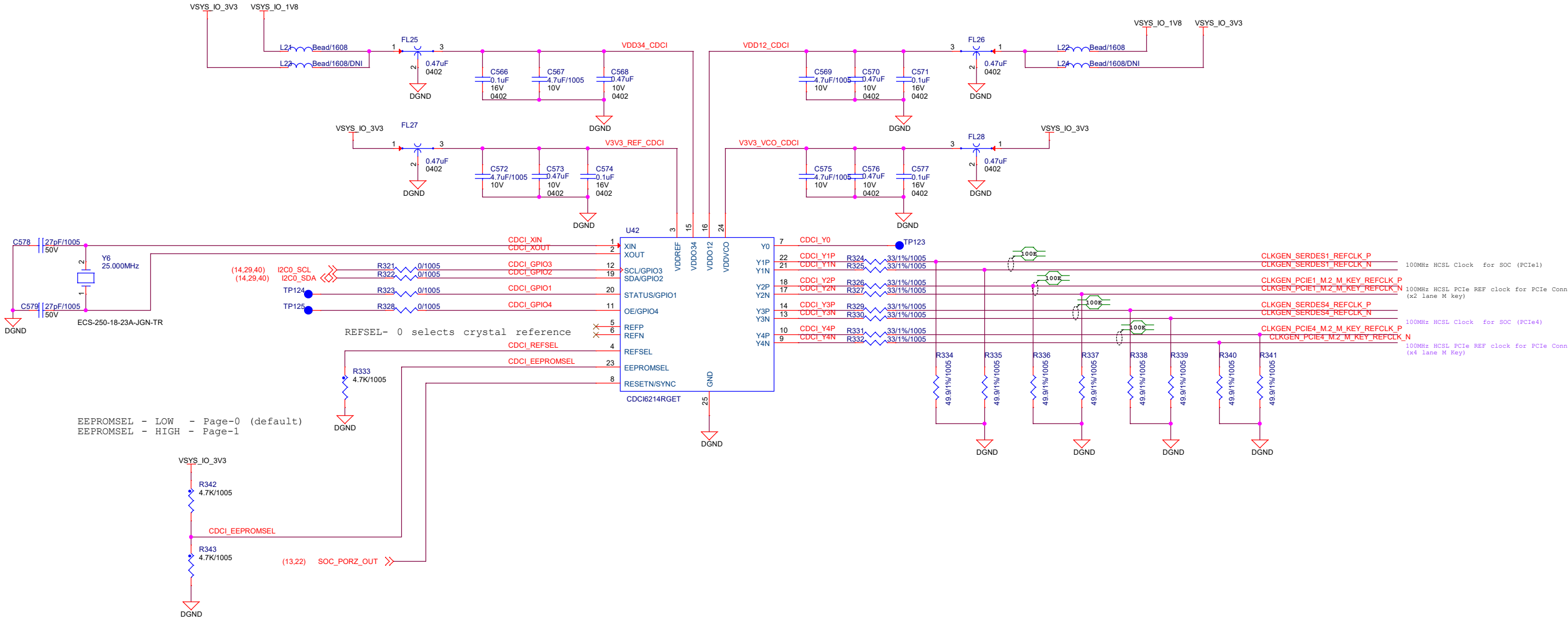


3.3V To 1V8 Level translator

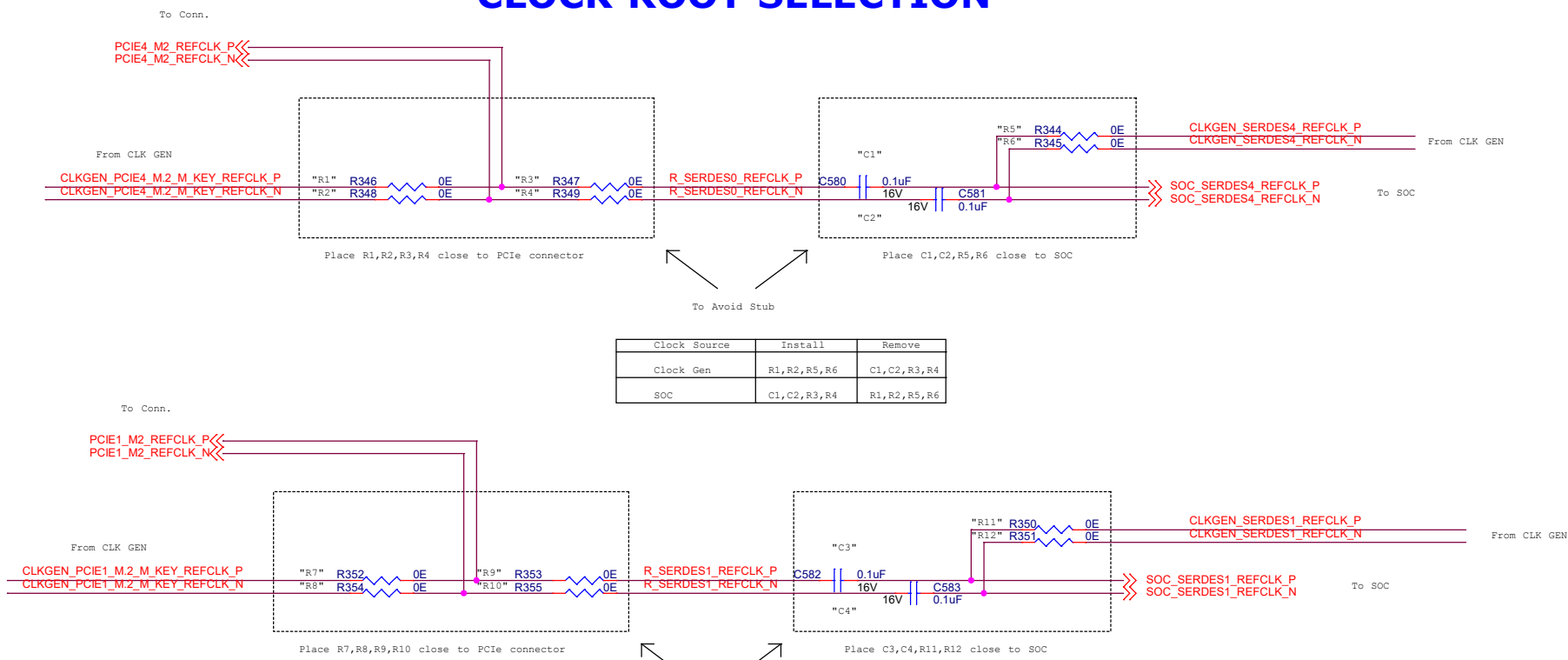


|       |                          |  |                            |    |       |
|-------|--------------------------|--|----------------------------|----|-------|
| Title |                          |  | PCIe_M.2_INTERFACE NNA/SSD |    |       |
| Size  | Document Number          |  |                            |    | Rev   |
| C     | -                        |  |                            |    | <1.0> |
| Date: | Tuesday, August 25, 2026 |  | Sheet                      | 23 | of 34 |

# SERDES CLOCK GENERATOR

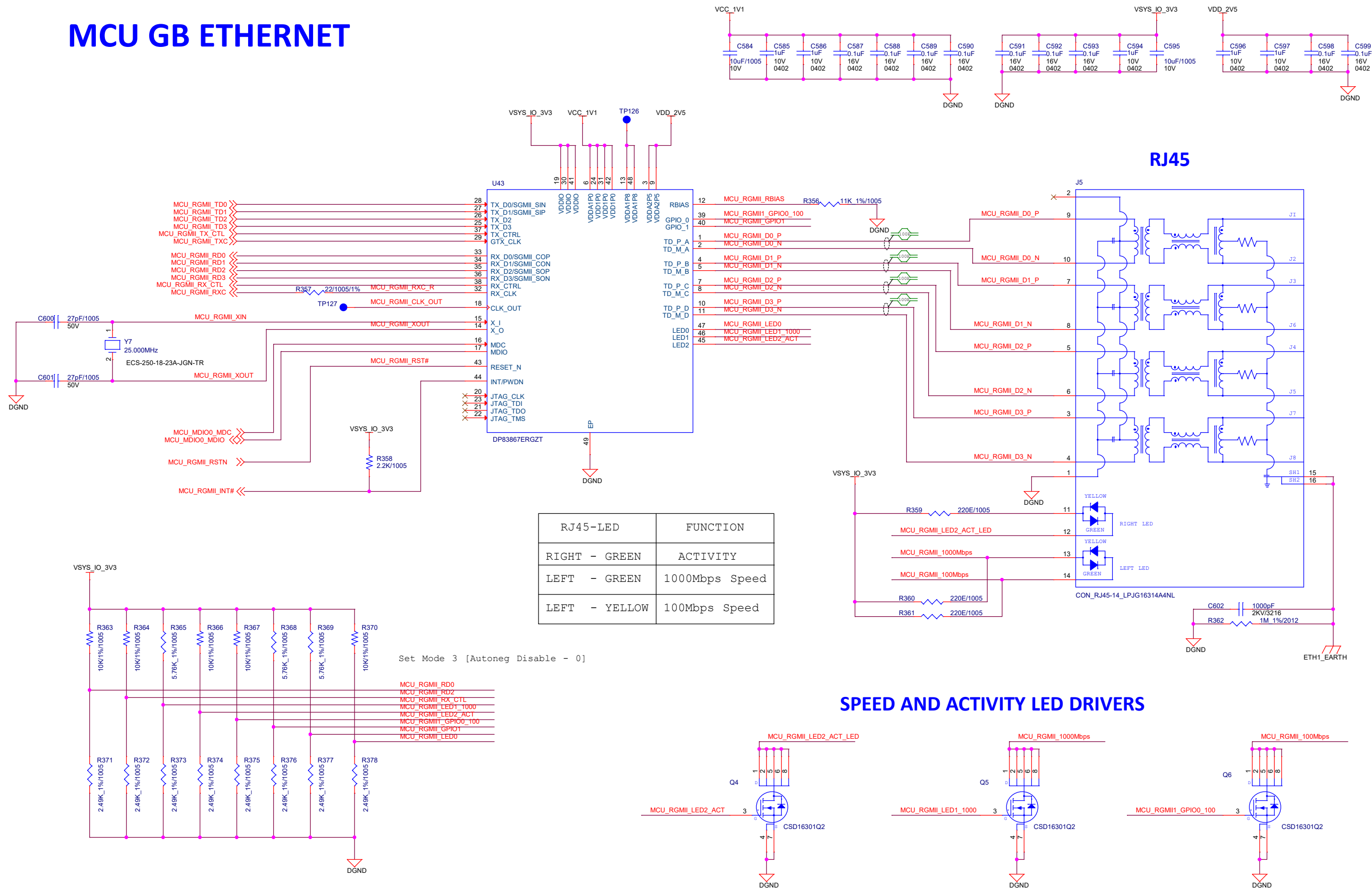


## CLOCK ROOT SELECTION



|                |                          |                |
|----------------|--------------------------|----------------|
| Title          |                          |                |
| SERDES CLK GEN |                          |                |
| Size           | Document Number          | Rev            |
| C              | -                        | <1.0>          |
| Date:          | Tuesday, August 25, 2026 | Sheet 24 of 34 |

# MCU GB ETHERNET

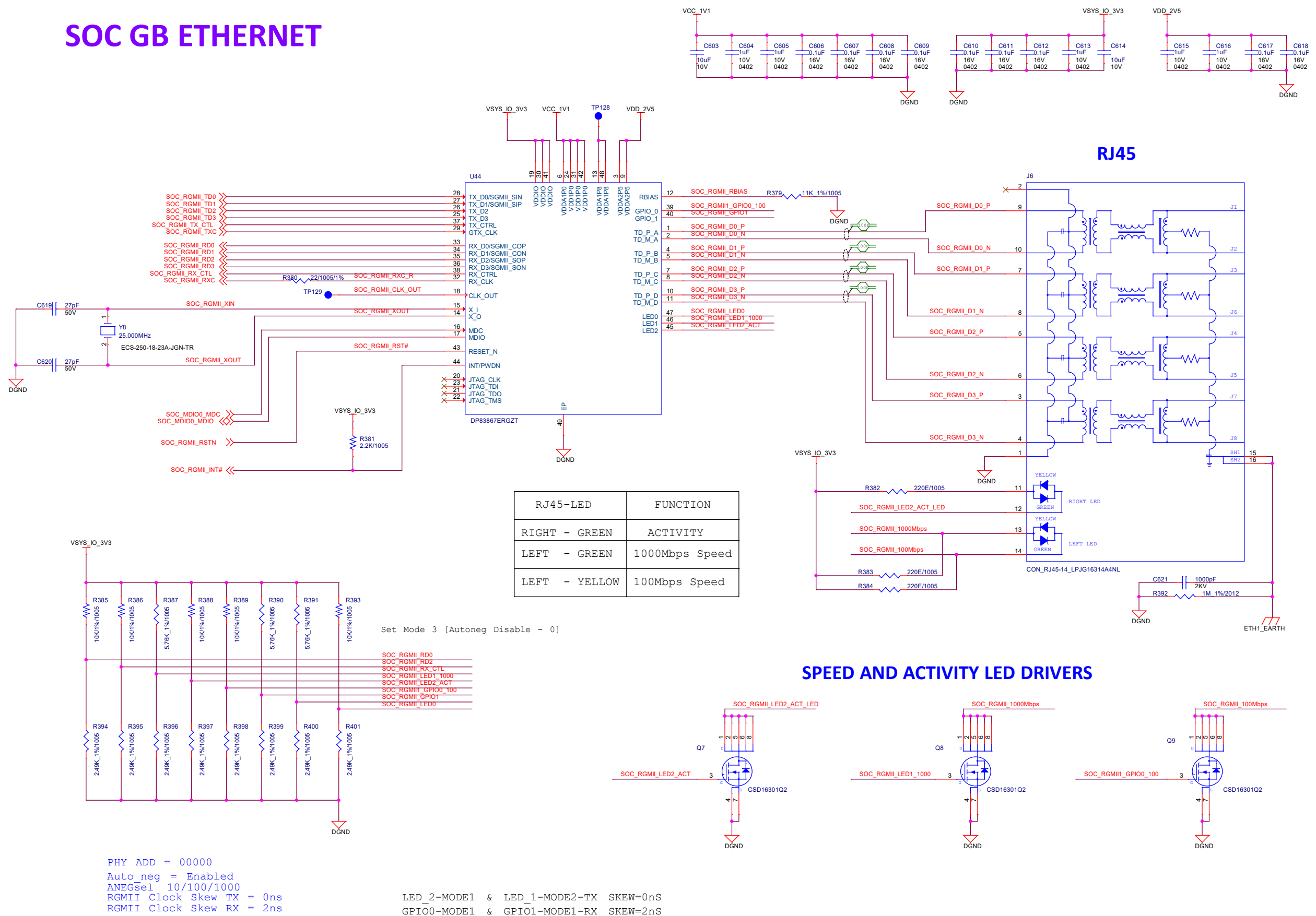


PHY ADD = 00000  
Auto\_neg = Enabled  
ANEGsel 10/100/1000  
RGMII Clock Skew TX = 0ns  
RGMII Clock Skew RX = 2ns

LED\_2-MODE1 & LED\_1-MODE2-TX SKEW=0ns  
GPIO0-MODE1 & GPIO1-MODE1-RX SKEW=2ns

## SPEED AND ACTIVITY LED DRIVERS

# SOC GB ETHERNET



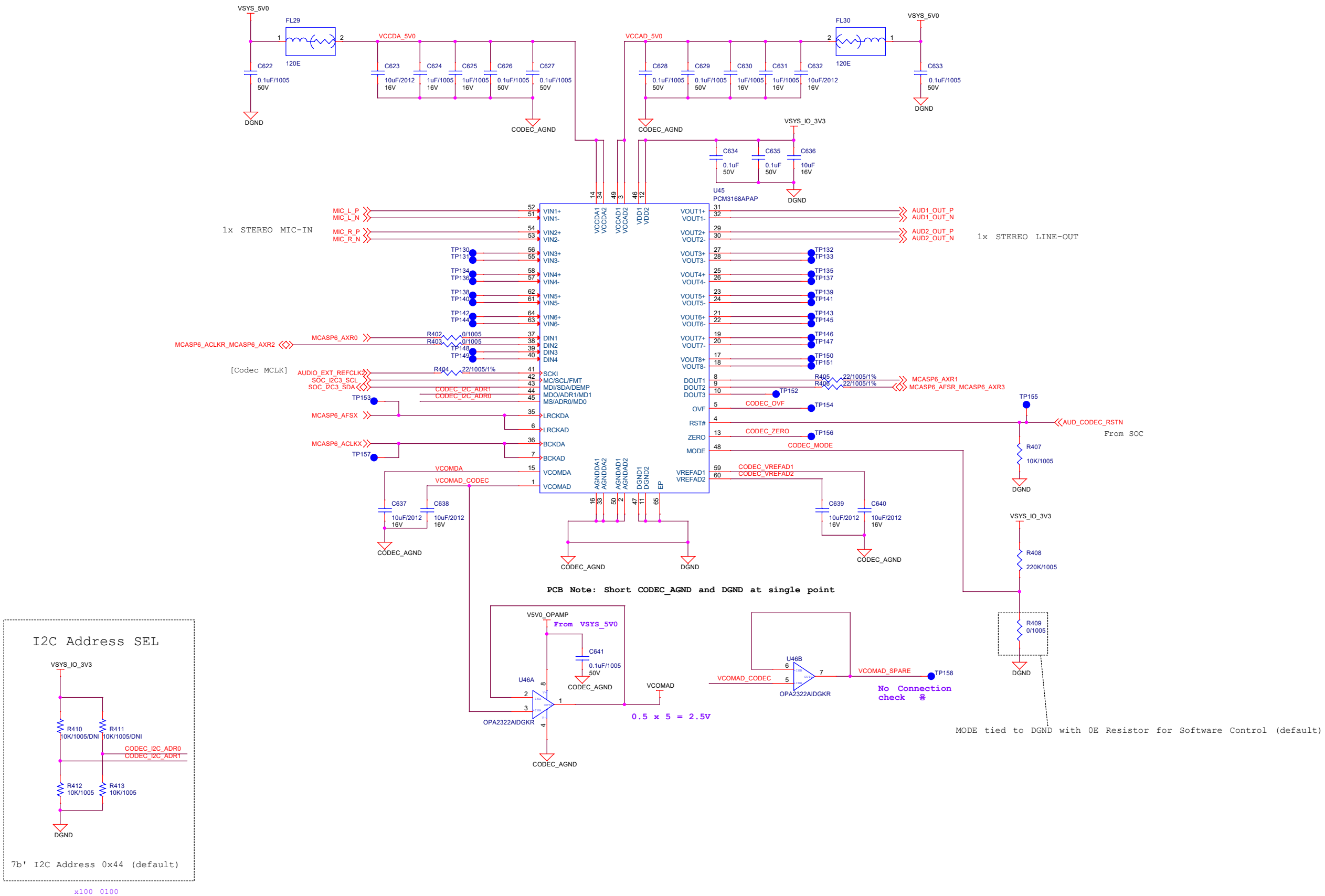
|               |                |
|---------------|----------------|
| RJ45-LED      | FUNCTION       |
| RIGHT - GREEN | ACTIVITY       |
| LEFT - GREEN  | 1000Mbps Speed |
| LEFT - YELLOW | 100Mbps Speed  |

```
Set Mode 3 [Autoneg Disable - 0]
```

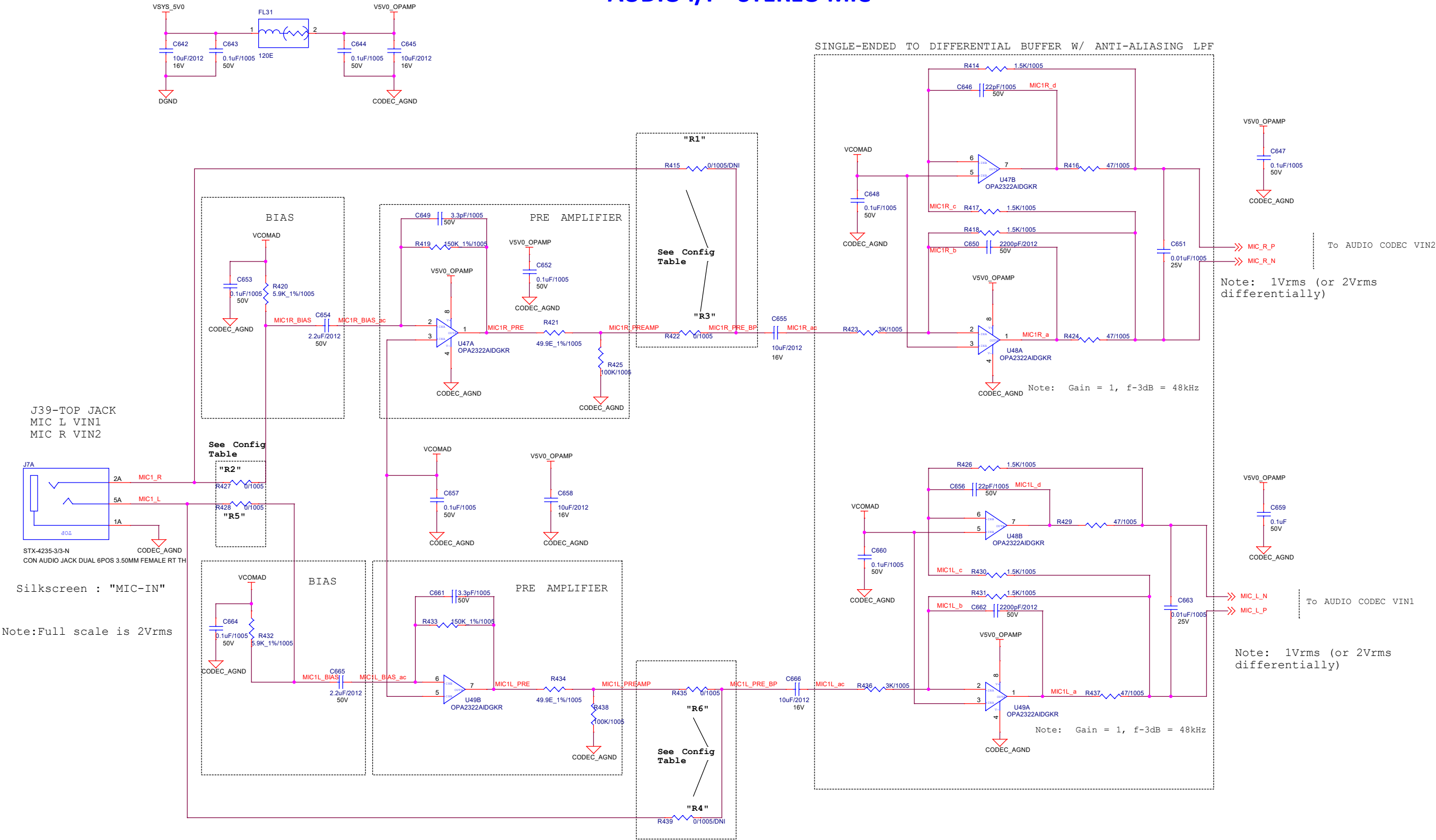
```
PHY ADD = 00000
Auto_neg = Enabled
ANEGsel 10/100/1000
RGMII Clock Skew TX = 0ns
RGMII Clock Skew RX = 2ns
```

```
LED_2-MODE1    & LED_1-MODE2-TX  SKEW=0nS
GPIO0-MODE1    & GPIO1-MODE1-RX  SKEW=2nS
```

# AUDIO I/F CODEC



AUDIO I/F - STEREO MIC



Config Table

|                       |                | Install        | Remove         |
|-----------------------|----------------|----------------|----------------|
| PASSIVE-MIC (default) | BIAS + PREAMP  | R2, R3, R5, R6 | R1, R4         |
| ACTIVE-MIC            | BIAS ONLY      | R1, R2, R4, R5 | R3, R6         |
| LINE-INPUT            | NO BIAS/PREAMP | R1, R4         | R2, R3, R5, R6 |

R2, R5 : Remove???  
문 의 할 것

AUDIO I/F - STEREO LINE OUT # 1

8Vpp Differential

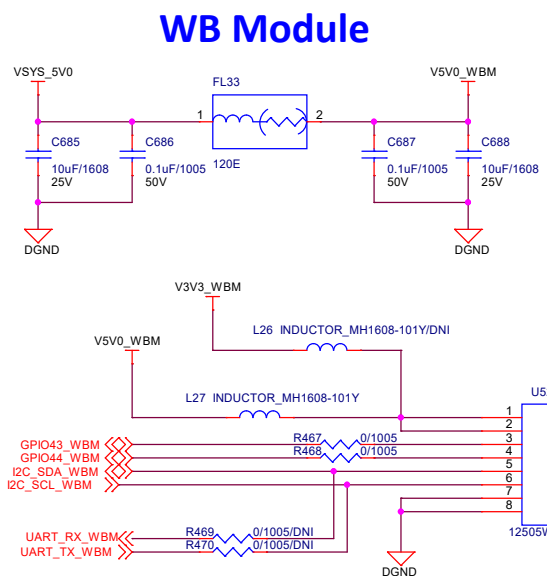
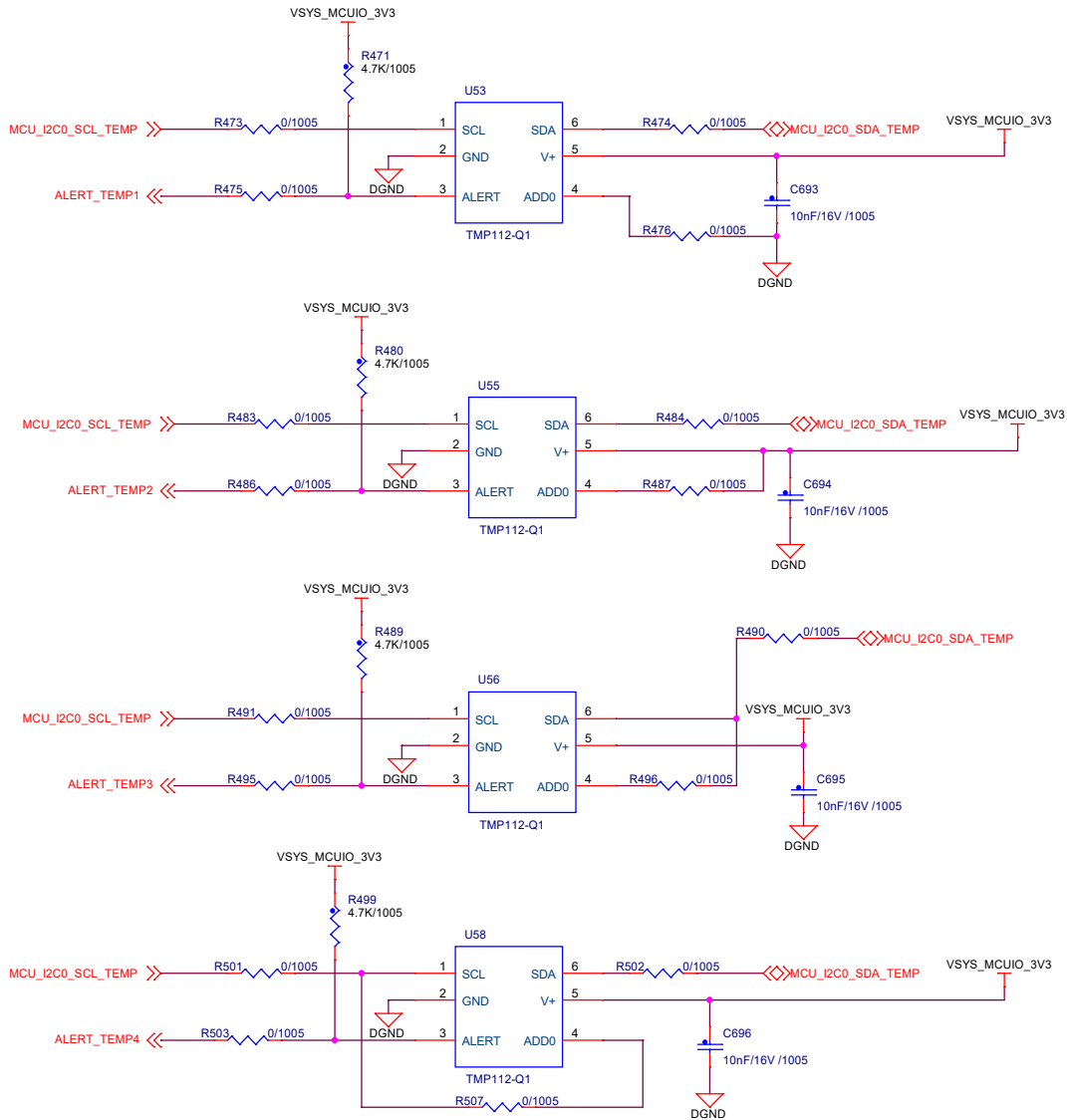
8Vpp Differential

J40-BOTOMM JACK  
Line-OUT L VOUT1  
Line-OUT R VOUT2

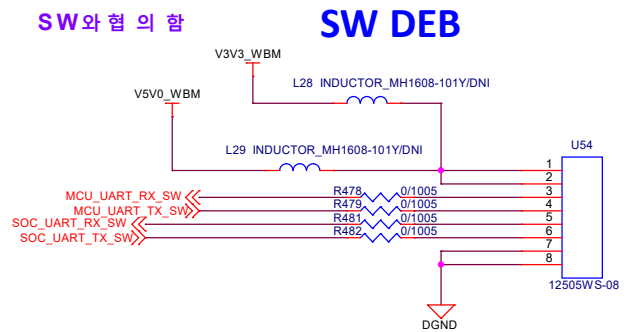
2 Vrms  
CON AUDIO JACK DUAL 6POS 3.50MM FEMALE RT TH  
STX-4235-3/3-N

Silkscreen for J40: "  
LINE OUT/HEADPHONE"

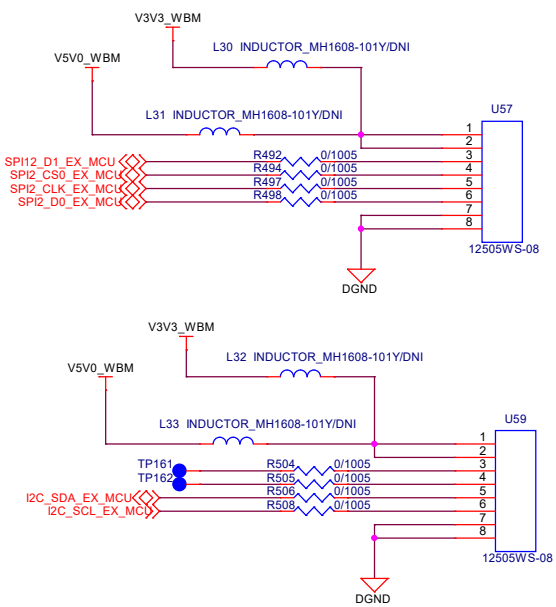
|                                 |                          |                |
|---------------------------------|--------------------------|----------------|
| Title                           |                          |                |
| AUDIO I/F STEREO LINE OUT #1 #2 |                          |                |
| Size                            | Document Number          | Rev            |
| A2                              | -                        | <1.0>          |
| Date:                           | Tuesday, August 25, 2026 | Sheet 29 of 34 |



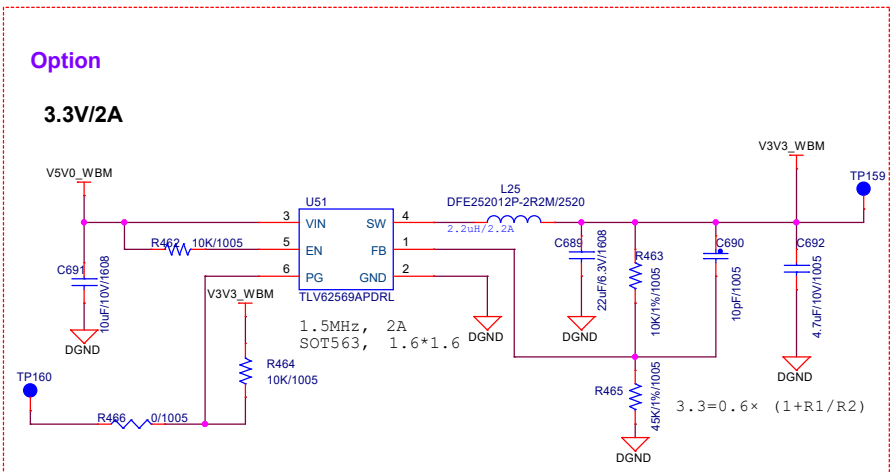
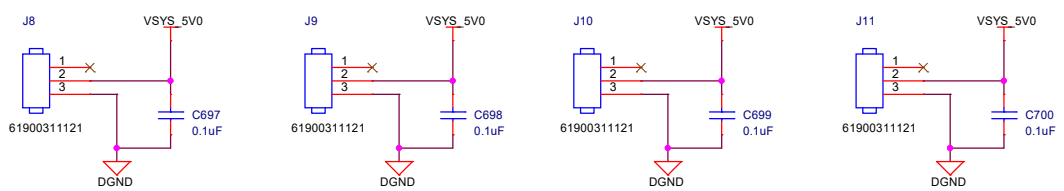
SW와 협 의 함



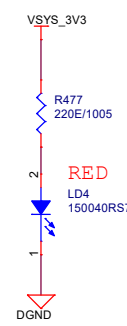
### EX MCU FOR LCD(DISPLAY)



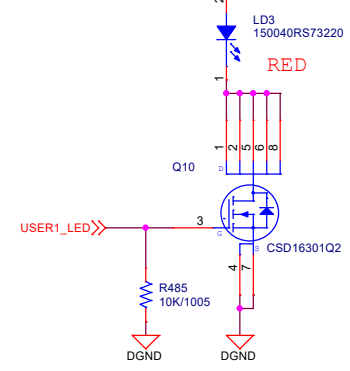
### FAN HEADER



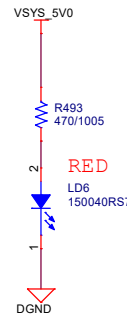
#### POWER LED (3.3V)



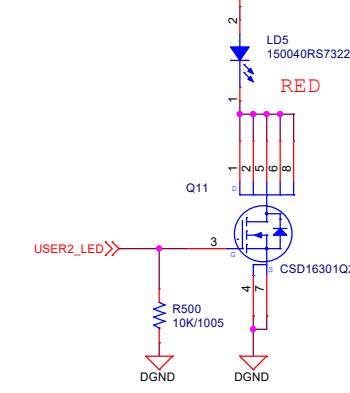
#### USER1 LED



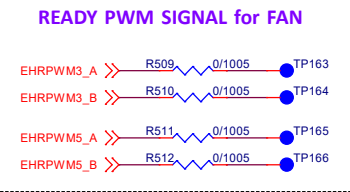
#### POWER LED (5.0V)



#### USER2 LED

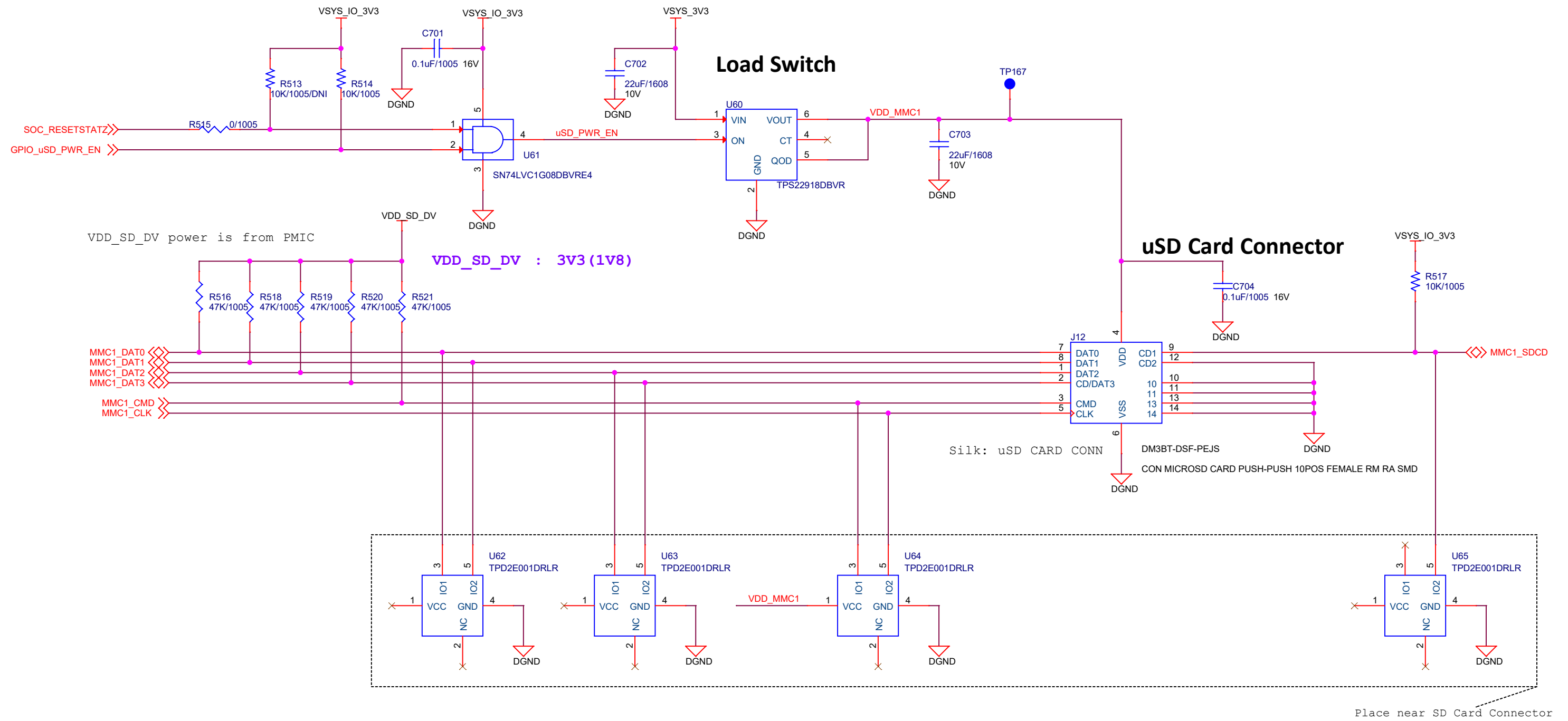


$R = (V_{cc} - V_f) / I$   
 $I = (3.3 - 2.0) / 220 = 5.9\text{mA}(6\text{mA})$   
 $R = (5 - 2) / 0.006 = 500(470 \text{ or } 510)$



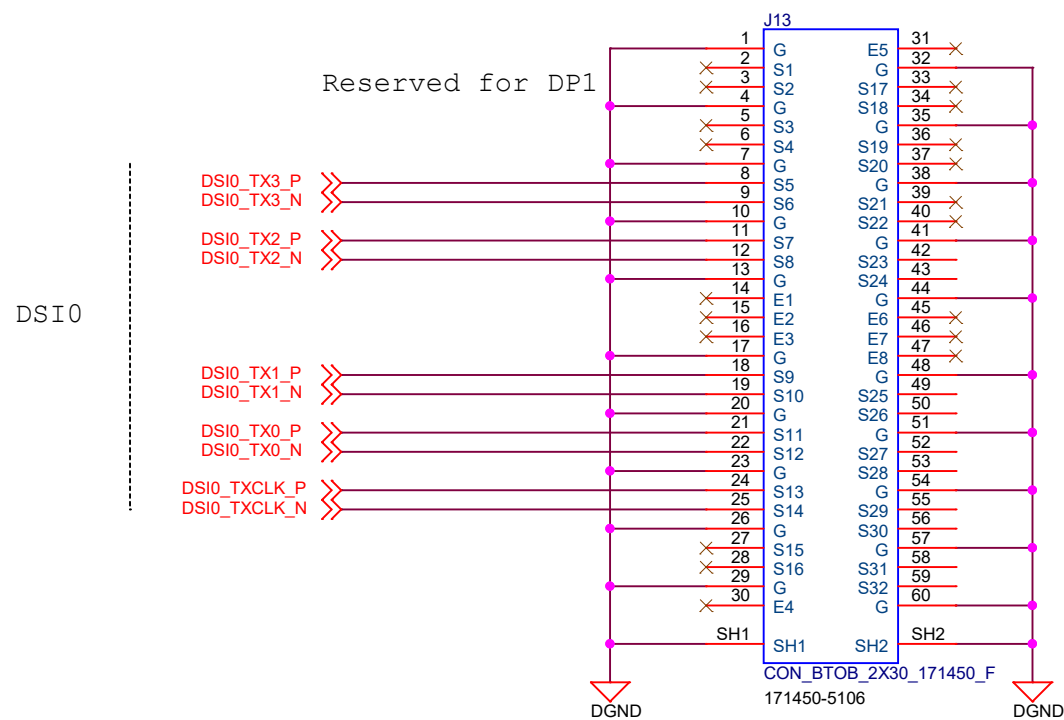
|                 |                          |                |
|-----------------|--------------------------|----------------|
| Title           |                          |                |
| TEMP SENSOR_WBM |                          |                |
| Size            | Document Number          | Rev            |
| A2              |                          | <1.0>          |
| Date:           | Tuesday, August 25, 2026 | Sheet 30 of 34 |

# Micro SD CARD INTERFACE

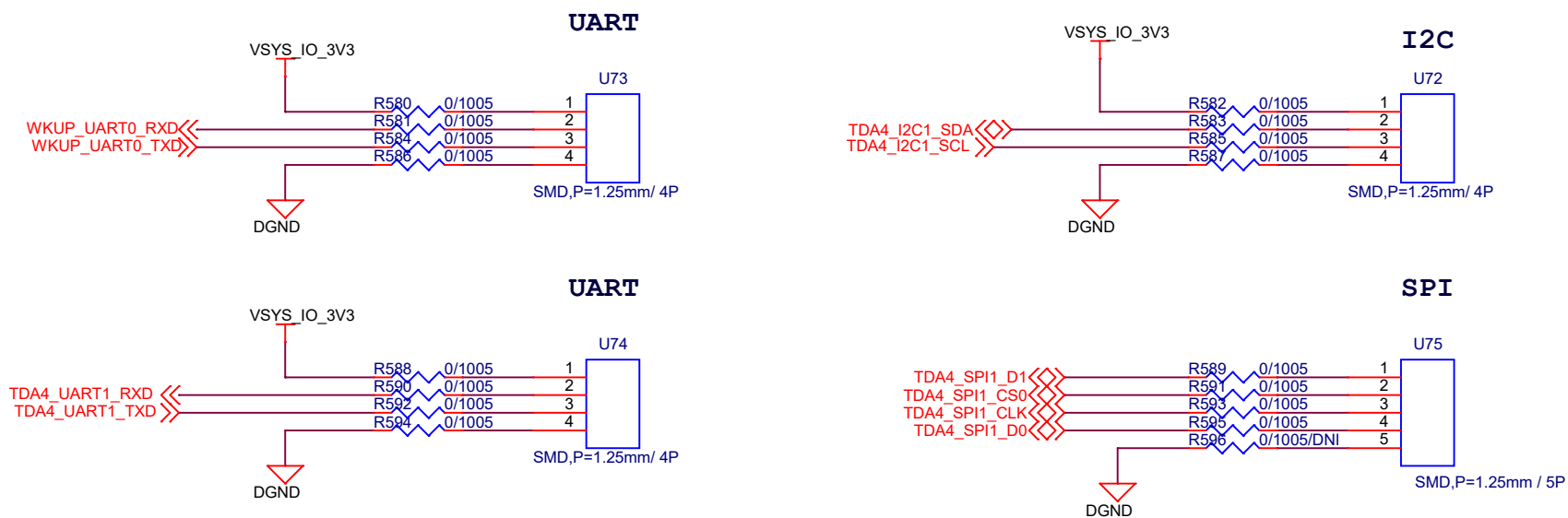


|               |                         |             |          |
|---------------|-------------------------|-------------|----------|
| Title         |                         |             |          |
| MICRO SD CARD |                         |             |          |
| Size<br>A3    | Document Number<br>-    | Rev<br><1.0 |          |
| Date:         | Monday, August 24, 2026 | Sheet       | 31 of 34 |

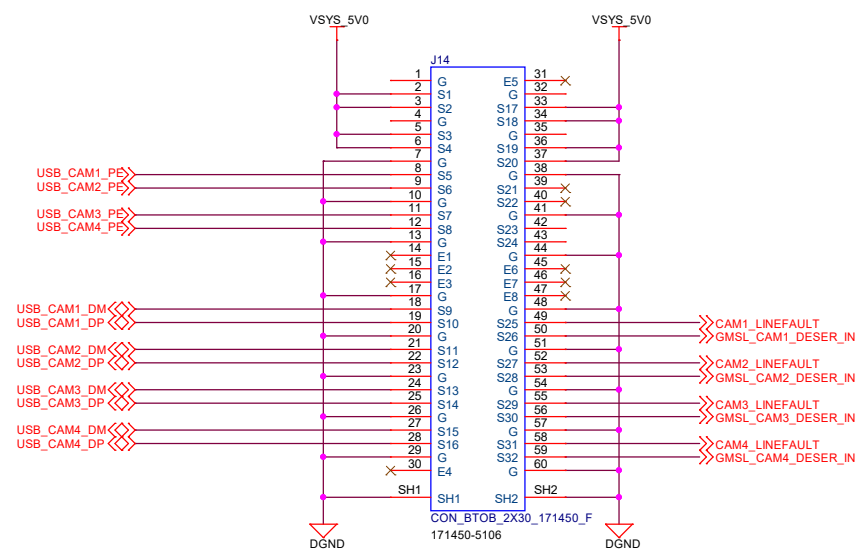
DSI Connector



External Connector



CAMERA INTERFACE



|              |                            |        |           |
|--------------|----------------------------|--------|-----------|
| Title        |                            |        |           |
| CAMERA INPUT |                            |        |           |
| Size         | Document                   | Number | Rev       |
| A2           | <Doc>                      |        | <RevCode> |
| Date:        | Wednesday, August 26, 2026 |        |           |
| Sheet        | 33                         | of     | 34        |

DES SIGNAL

