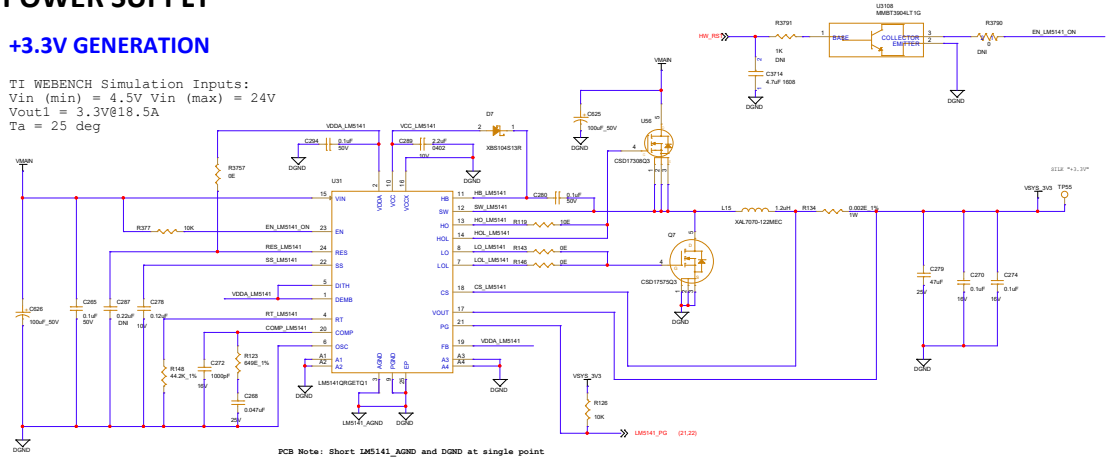
POWER SUPPLY

+3.3V GENERATION

TI WEBENCH Simulation Inputs:
Vin (min) = 4.5V Vin (max) = 24V
Vout1 = 3.3V@18.5A
Ta = 25 deg

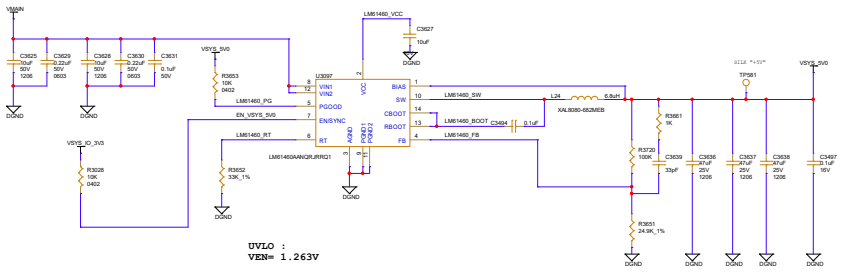


PCB Note: Short LM5141_AGND and DGND at single point

UVLO : 3.4V
VIL : 0.8V / VIH : 2.0V

+5.0V GENERATION

LM61460 5V BUCK REGULATOR
VinMin = 12V
VinMax = 36V
Vout = 5.0V
Iout = 6A

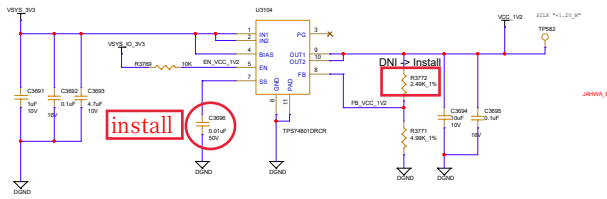


UVLO :
VEN= 1.263V

DESERIALIZER POWER

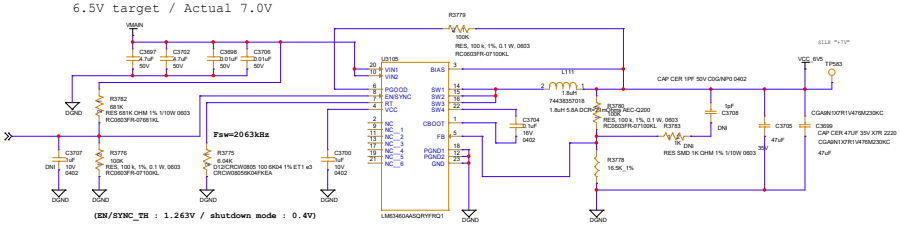
3.3V to 1.2V LDO

Iout=550mA



+7.0V Camera Module POWER

6.5V/4.2A
6.5V target / Actual 7.0V

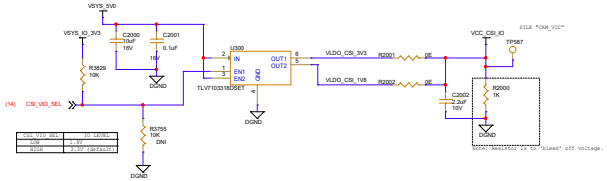


(EN/SYNC_TH : 1.263V / shutdown mode : 0.4V)

UVLO
turn on : 9.9V /turn off : 7.128V

EN/SYNC Level
VMAIN : 24V -> 3.072V / 12V -> 1.53V

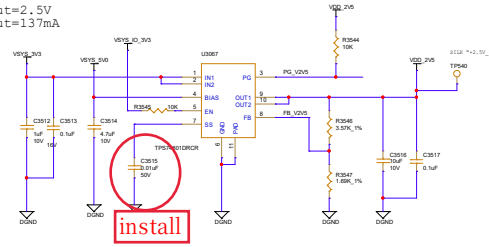
CAMERA IO SUPPLY SELECTION



ETHERNET POWER

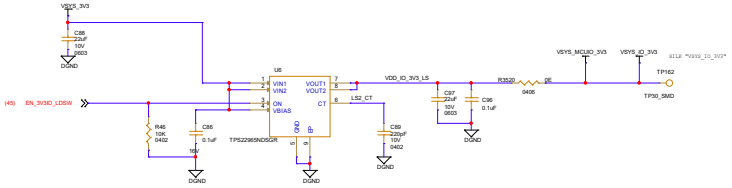
3.3V to 2.5V LDO

Vout=2.5V
Iout=137mA



+3.3V LOAD SWITCH

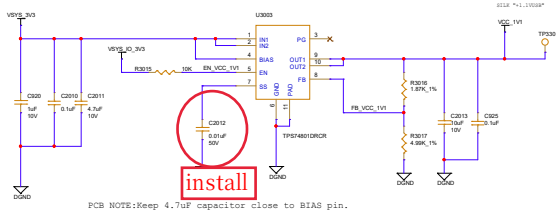
USB HUB / PHY / HDMI / CPLD / Clock Gen / TDA4VM



USB HUB & ETHERNET POWER

3.3V to 1.1V LDO

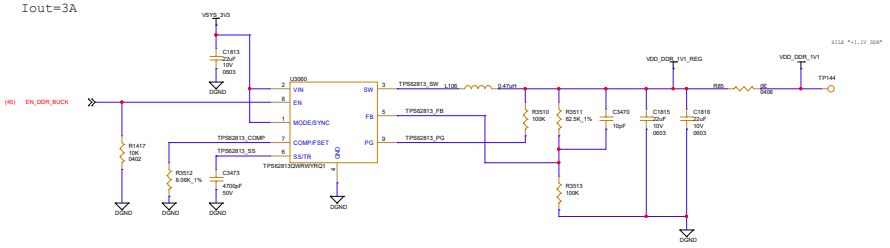
Vout=1.1V
Iout=888mA



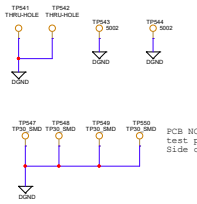
PCB NOTE:Keep 4.7uF capacitor close to BIAS pin.

+1.1V LPDDR4 & TDA4VM EMIF POWER

Vout=1.1V
Iout=3A



GROUND TEST POINTS



PCB NOTE: Spread the SMD test points Top and Bottom Side of PCB

DX SOLUTION	PROJECT	TI_1_DVKIT
	PCB CODE (REV)	DX-S2-001-A0(O)
PAGE 8 OF 35		

EVM's 3-Phase DUAL PMIC Power Distribution Network (PDN)

(3-Phase Buck supplying VDD_CPU)

"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

PMIC- A

Route as Pseudo differential pair trace
(See "PCB Notes")

Programming Header

J15 — 62000311121 CON HDR 1X3 2.00MM PITCH ST TH

U60 — CCBTLV3257MPWREP

OEn	S	Bit State
0	0	A = B1
0	1	A = B2
1	X	Open

Install Shunt/Jumpers while programming PMIC on J21

0ohm DNI to gnd for next rev

U17 — PTPS65941213RWERQ1

U21 — SN74LVC1G07DRLRG4

(EVM Bd Setting Default):

LEOA_WDOG_DISABLE	PD (Low)	Enable WDOG
	PU (High)	Disable WDOG

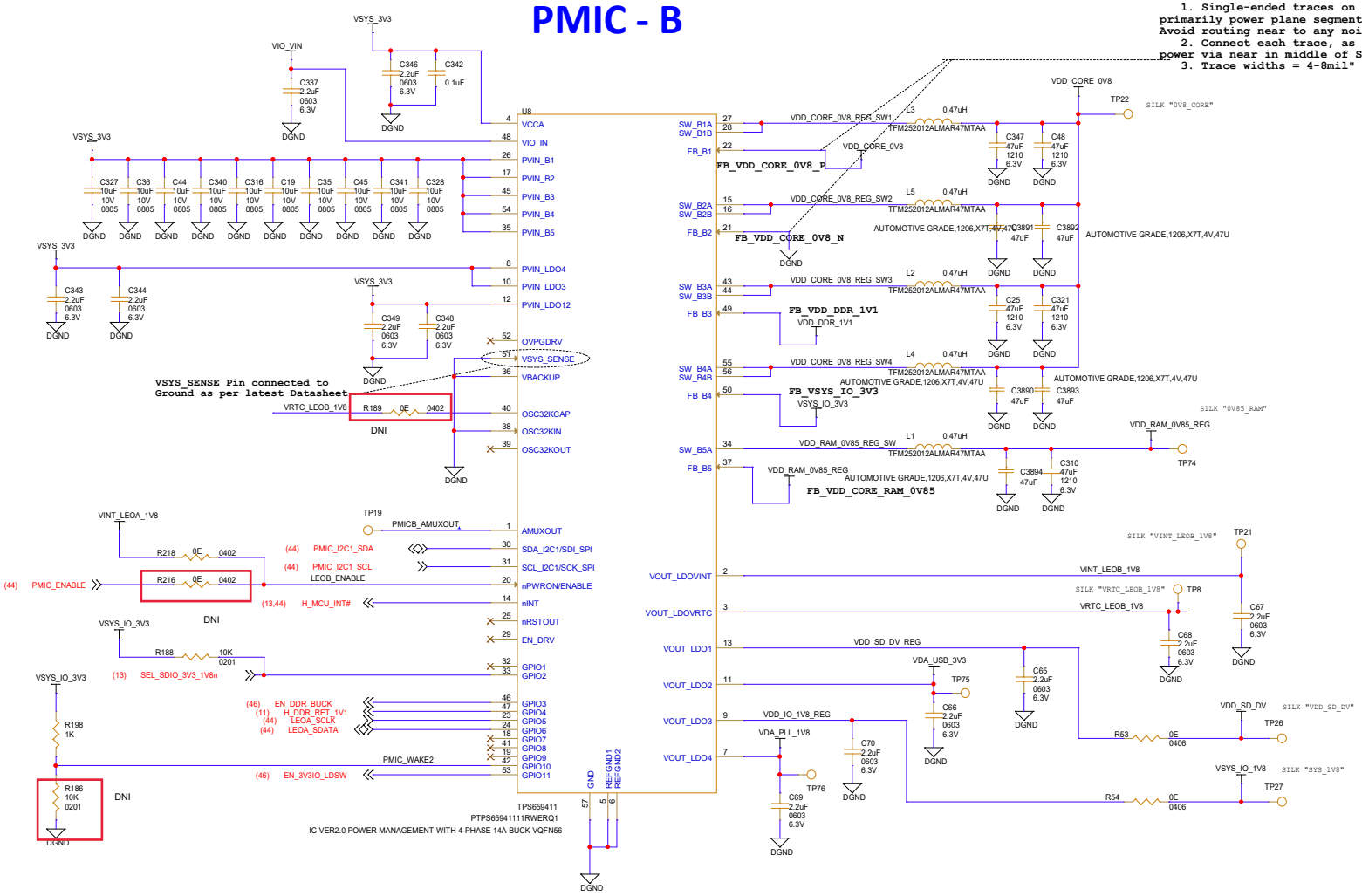
PMIC-A uses default I2C ADDR:
0x48, 0x49, 0x4A & 0x4B

DX SOLUTION	PROJECT TI_1_DVKIT
PAGE 9 OF 35	PCB CODE (REV) DX-S2-001-A0(O)

PMIC - B

"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

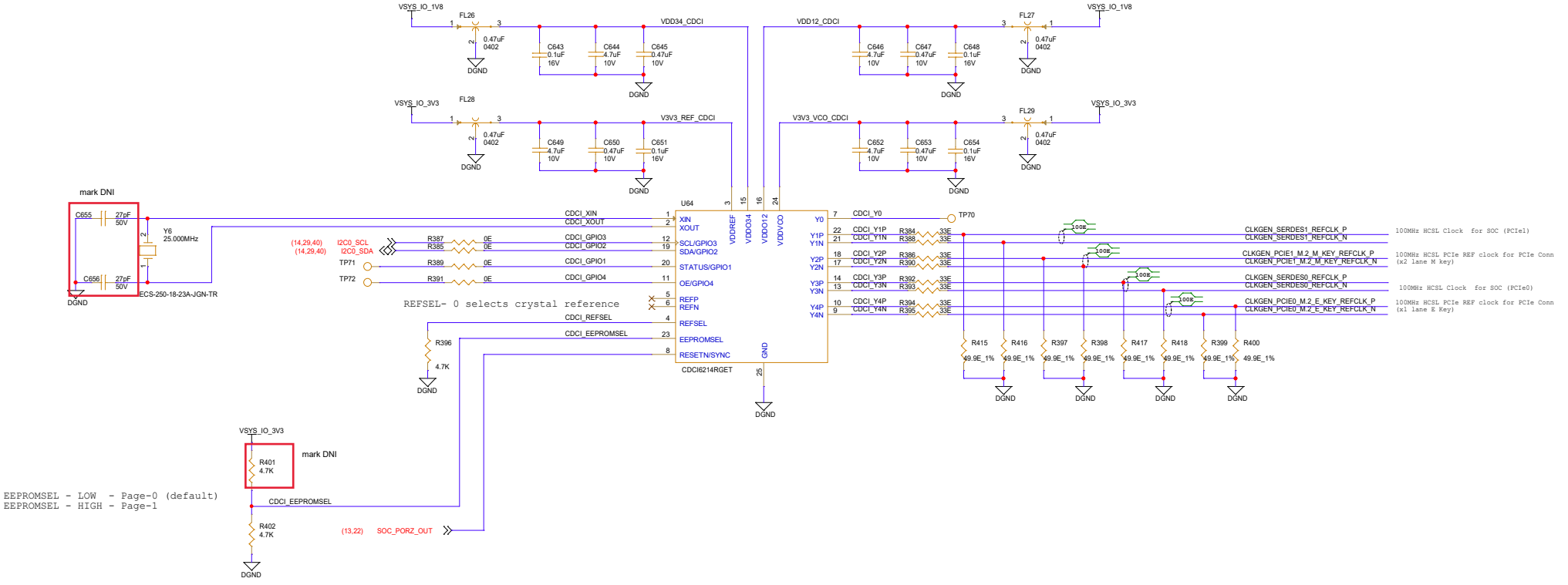
For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"



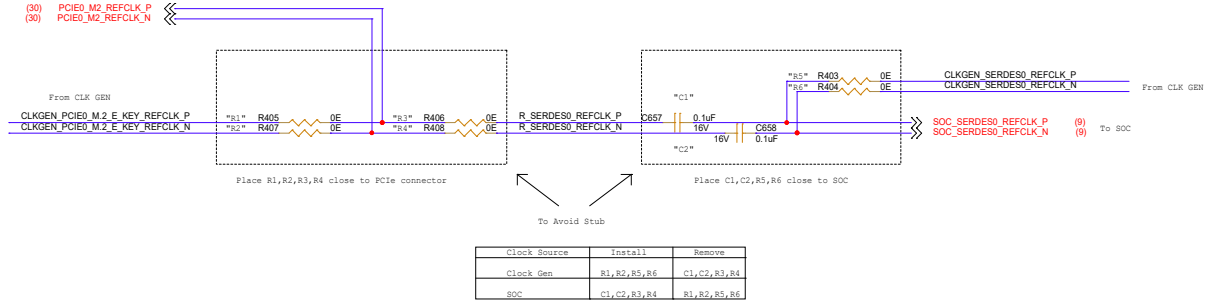
PMIC-B uses NVM to set I2C ADDR:
0x4C, 0x4D, 0x4E & 0x4F

DX SOLUTION	PROJECT	TI_1_DVKIT
PAGE 10 OF 35	PCB CODE (REV)	DX-S2-001-A0(O)

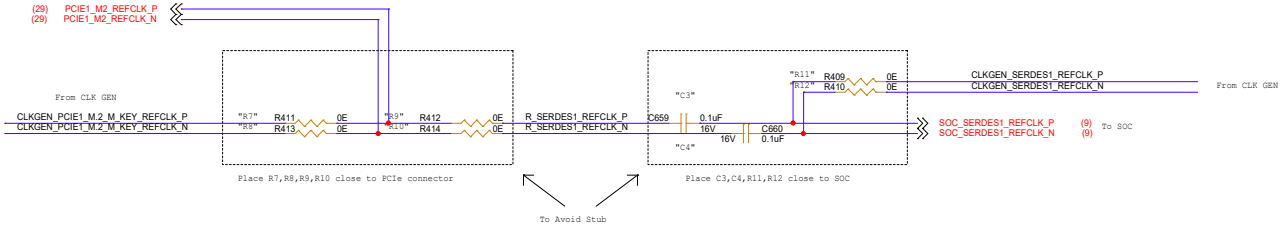
SERDES CLOCK GENERATOR



CLOCK ROOT SELECTION



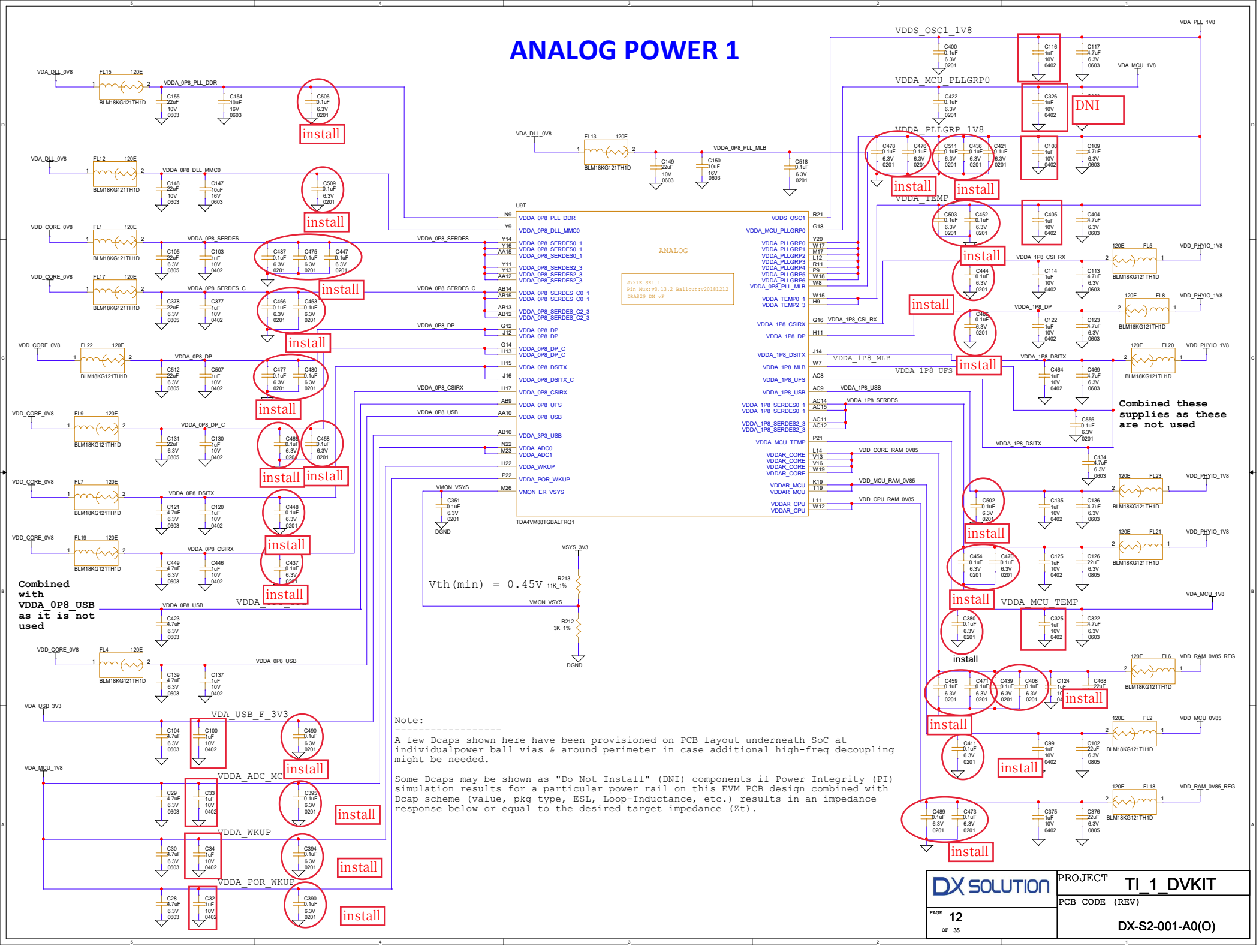
Clock Source	Install	Remove
Clock Gen	R1,R2,R5,R6	C1,C2,R3,R4
SOC	C1,C2,R3,R4	R1,R2,R5,R6



Clock Source	Install	Remove
Clock Gen	R7,R8,R11,R12	C3,C4,R9,R10
SOC	C3,C4,R9,R10	R7,R8,R11,R12

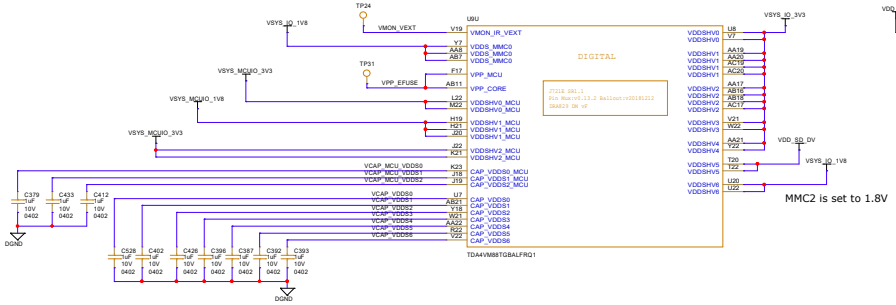
DX SOLUTION	PROJECT TI_1_DVKIT
PAGE 11 OF 35	PCB CODE (REV) DX-S2-001-A0(O)

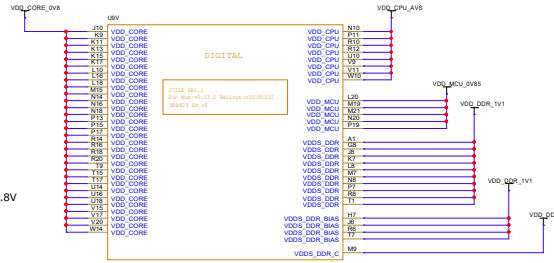
ANALOG POWER 1



DX SOLUTION	PROJECT TI_1_DVKIT
PAGE 12 OF 35	PCB CODE (REV) DX-S2-001-A0(O)

DIGITAL POWER

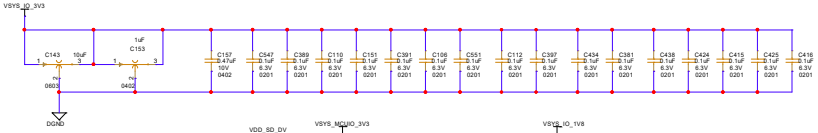


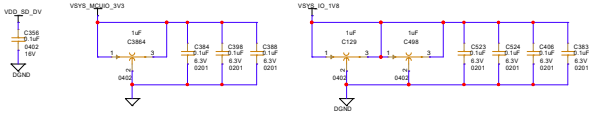


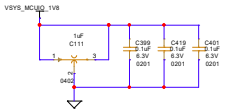
Note:

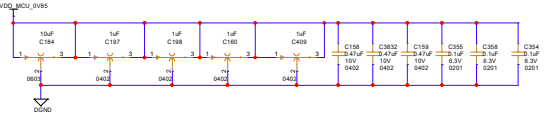
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individualpower ball vias & around perimeter in case additional high-freq decoupling might be needed.

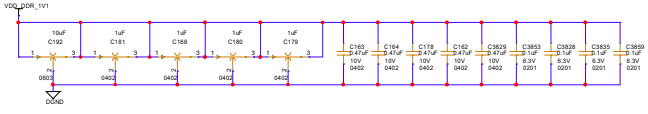
Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

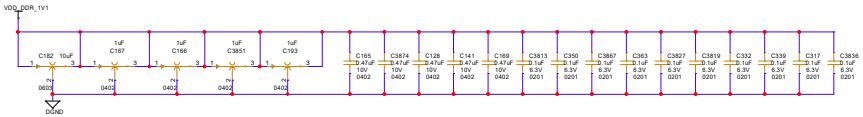


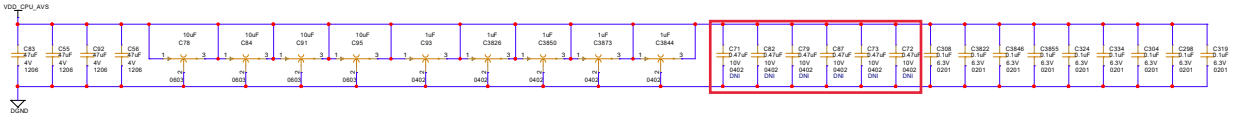


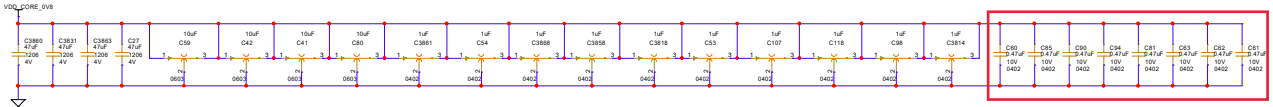


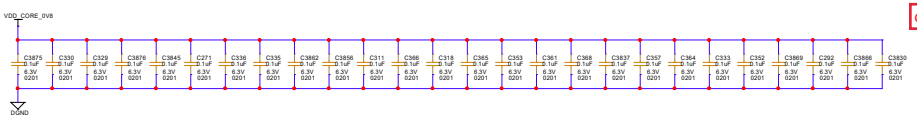








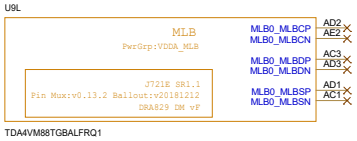




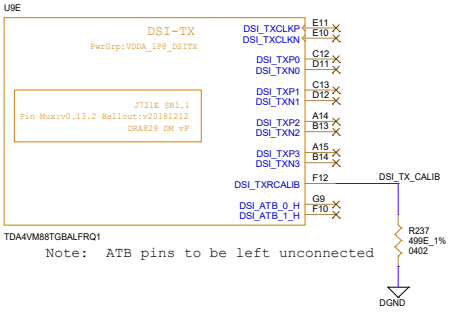
DX SOLUTION	PROJECT: TI_1_DVKIT
PAGE 13 OF 35	PCB CODE (REV): DX-S2-001-A0(O)

UNUSED BLOCK

MLB

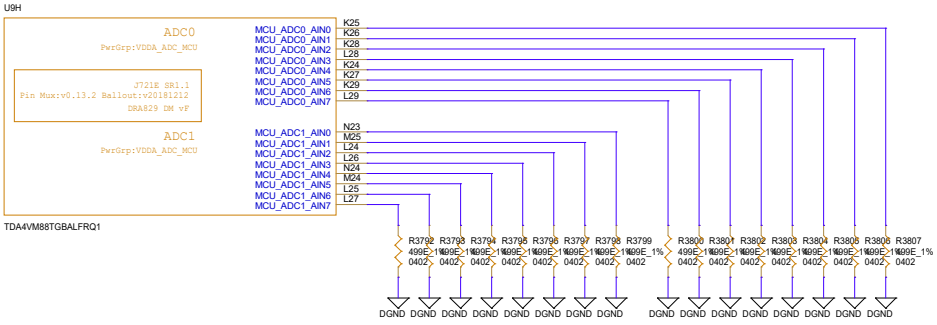


DSI

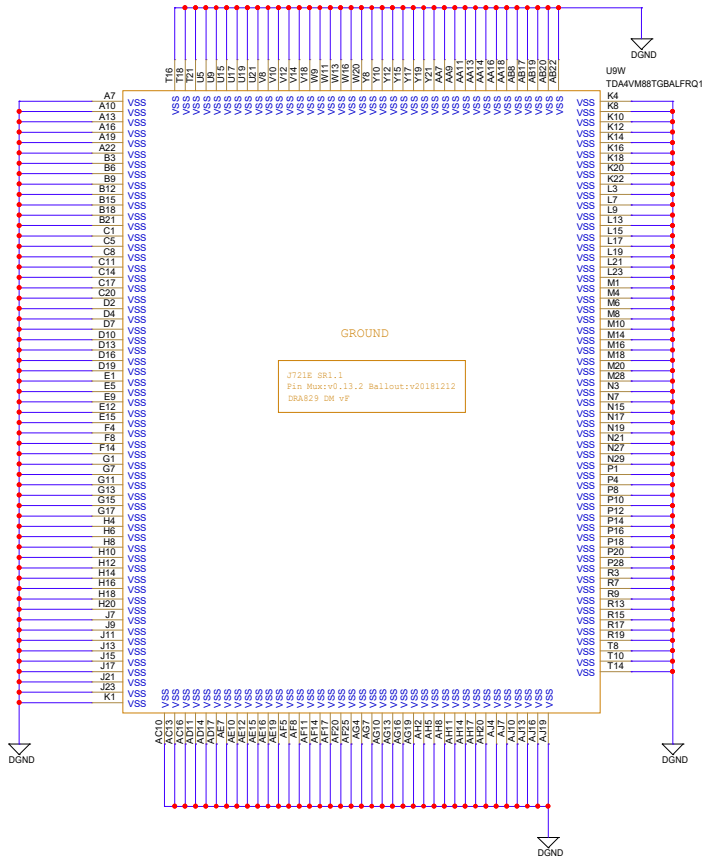


Note: ATB pins to be left unconnected

MCU ADCs



SOC GROUND



DX SOLUTION	PROJECT TI_1_DVKIT
PAGE 14 OF 35	PCB CODE (REV) DX-S2-001-A0(O)