Keystone II Power Supplies and Power Sequencing

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ABSTRACT

This application note is intended to provide early information regarding power sequencing requirements for the Keystone II family of DSP's. This document will be replaced by a more formal document when it becomes available and will be incorporated into the data manual in the near future.

This application note is not intended to be a design guide and will not provide power related requirements beyond the identification of the various rails and sequencing requirements. This application note does not identify the details for ramping after a reset is applied – this information will be provided at a later date.

The following information is provided and considered to be correct at the printing of this application note and will be replaced by actual design guides or data manuals as they become available.

BACKGROUND

Texas Instruments' has developed a new generation of high performance DSP's in a 28nm process to meet demanding market requirements. This family of DSP's is collectively referred to as the "Keystone II" family. This new family of processors has many of the same power requirements as its predecessor did (Keystone I or Keystone family of DSP's) with regards to power rails and power sequencing. Due to new IP's, process node, and added features; there exists additional power rails and power sequencing requirements.

GENERAL CONSIDERATIONS

The Keystone II family of processors still supports both concepts of power sequencing (Core before I/O and I/O before Core. This document will cover both concepts of power sequencing,

There are multiple devices within this family and not all rails, peripherals, or features are present in all devices (due to various interfaces and peripherals being included or excluded). This application note addresses all power rails and requirements, should the Keystone II device you intend to use not include or require a specific rail(s), then it can be omitted from the design (unless additional notes or comments are provided).

In many cases, if a peripheral is not used the power supply must still be connected; however filtering for the unused rails may not be required.

Unused clocks should still be properly terminated to prevent noise from entering the DSP, or for reducing power levels where possible. IO's on your DSP are not failsafe, as such no signal inputs to the DSP are allowed before the DSP is fully powered.

POWER RAILS

The following table (Table 1) provides a listing of the required power rails for the entire Keystone II family of DSP's. As previously stated, not all DSP's will require every rail. In many cases some rails can be tied together, some rails must originate from the same source, and some rails may have variations in tolerances.

Table 1: Keystone II Rail Definitions

Ref.	Common Name	Description	Voltage
1	CVDDT	ARM Core SmartReflex Supply	0.80 – 1.05V[A]
2	CVDD	DSP[B] Core SmartReflex Supply	0.80 – 1.05V[A]
3	VDDALV	SerDes Analog Power Supply	0.85V
4	VDDAHV	SerDes I/O Power Supply	1.8V
5	CVDD1	DSP Fixed Core Supply	0.95V
6	CVDDT1	ARM Fixed Core Supply	0.95V[C]
7	AVDDA15:01	DDR3 DLL & PLL Supply	1.8V[AK]
8	DVDD1V5A	I/O Power Supply for DDR3A	1.5V
9	DVDD1V5B	I/O Power Supply for DDR3B	1.5V
10	DVDD1V8	Power Supply for 1.8V I/O's	1.8V
11	VDDA18	PLL Supplies	1.8V
12	USBVDD3V3	3.3V USB High Voltage Supply	3.3V[D AH]
13	USB0V85	USB LV PHY Power Supply	0.85V[D]
14	VPPB	Customer FUSEFARM	1.8V[AI]

NOTE A: The value indicated is intended to cover the entire possible voltage range for all process variations. Each Keystone II processor will typically operate at a subset of the entire range which will be hardcoded into each device prior to shipping. Powers supplies should be designed to support a 400mV range between 0.700 and 1.1V so that the respective voltage steps are aligned with the intended values.

NOTE B: The term "DSP Core" refers to the entire scaled SoC excluding the ARM

NOTE C: The value of this rail is subject to change and is currently under evaluation

NOTE D: If the USB3.0 peripheral is not required or used, all non 3.3V power supply connections must be connected through a zero ohm resistor to ground.

NOTE AH: If the USB3.0 peripheral is not required or used, the 3.3V supply pins should be connected to ground through a zero ohm resistor.

NOTE AI: The VPPB 1V8 supply has specific sequencing and slew rate requirements that must be followed in order to prevent erroneous or incorrect programming of this fuse farm. The 1V8 supply listed is a minimum supply voltage necessary to program the fuse farm (maximum 1V9. The power supply driving this pin must not be intermittent or decrease below the 1V8 rail after programming – otherwise the efuse will become unpredictable.

NOTE AK: The AVDDA10:06 pins support the DDR3A DLL's; the AVDDA15:11 pins support the DDR3B DLL's; and the AVDDA05:01 pins support the PLL supplies.

COMBINING POWER RAILS

The following table (Table 2) provides a listing of the possible rails to be tied together and relative impact to the customer for the entire Keystone II family of DSP's.

Refer to Appendix A for additional important consideration details

Table 2: Power Rail Combining

Ref.	Common Name	Grouping	Description	Voltage
1	CVDDT	1	ARM Core SmartReflex Supply	0.80 – 1.05V
2	CVDD	1	DSP Core SmartReflex Supply	0.80 – 1.05V
3	VDDALV	5	SerDes Analog Power Supply	0.85V
4	VDDAHV	4	SerDes Analog Power Supply	1.8V
5	CVDD1	2	DSP Fixed Core Supply	0.95V
6	CVDDT1	2	ARM Fixed Core Supply	0.95V
7	AVDDA15:1	4	DDR3 DLL & PLL Supply	1.8V[AK]
8	DVDD1V5A	3	I/O Power Supply for DDR3A	1.5V
9	DVDD1V5B	3	I/O Power Supply for DDR3B	1.5V
10	DVDD1V8	4	Power Supply for 1.8V I/O's	1.8V
11	VDDA18	4	PLL Supplies	1.8V
12	USBVDD3V3	6	3.3V USB Supply	3.3V
13	USB0V85	5	Internal PHY Power Supply	0.85V
14	VPPB	7	Customer FUSEFARM	1.8V

NOTE AK: The AVDDA10:06 pins support the DDR3A DLL's; the AVDDA15:11 pins support the DDR3B DLL's; and the AVDDA05:01 pins support the PLL supplies.

Texas Instruments offers to customers the option of combining certain power rails to aid in the general reduction of power supply components. Like numbers as identified in Table 2 can be combined with the following comments.

Grouping 1: Grouping 1 consists of the AVS or SmartReflex supplies for both the DSP and ARM cores. Combining these two supply rails will have an impact on which power control interface is used and the amount of power consumed by the DSP.

When these two rails are tied together, the core requiring a lower voltage will be presented with the higher voltage of the other core (thus a higher overall power may be noted). When combining the two AVS rails together it will be necessary to connect the correct DSP power management

interface to your power controller (VCNTL/VID or Power I2C). When these are tied together – only one SmartReflex power management interface will be used.

It is strongly recommended that when group 1 is tied together that group 2 also be tied together (but connected to a separate and correct voltage supply). When tying this group together, the VCNTL or i2c interface used should always be the DSP and not the ARM interface.

Grouping 2:Grouping 2 consists of the fixed core power rails for both the DSP and ARM cores. When combining the two AVS rails together it will be necessary to tie together the fixed core rails also (not to the AVS supply).

NOTE: *Texas Instruments is looking at the impact of tying the two separate fixed core supply rails together when the AVS supply rails are not tied together, if this becomes a feasible option or alternative – this application note and subsequent data manuals or hardware design guides will also be updated*

Grouping 3:Grouping 3 consists of the fixed 1.5V DDR3 IO power rails for both DDR3 A and DDR3 B interfaces. These two rails may be tied together regardless any other rail being tied together.

Grouping 4:Grouping 4 consists of the fixed 1.8V SerDes and IO power rails. These two rails may be tied together regardless any other rail being tied together. Several of these rails will require independent and separate filters.

Grouping 5:Grouping 5 consists of the fixed 0.85V inputs to the DSP; these rails can originate from the same power source but may have separate filtering requirements.

Grouping 6:Grouping 6 consists of the fixed 3.3V input supply power rails to the DSP; these rails can originate from the same power source but may have separate filtering requirements.

Grouping 7:Group 7 is a single input power pin to your processor. This input is a 1.8V supply and can be derived from group 4 supply if necessary, however this input pin has specific sequencing requirements and must be sequenced after de-assertion of PORz.

NOTE: The comments in this application note pertain to a single DSP. When multiple DSP's are used the combination of power rails must also take into consideration the impact on sequencing, total amperage requirements and impact on both AC and DC tolerances.

FILTERING REQUIREMENTS

The following table (Table 3) provides a preliminary listing of the filtering requirements by power rails for the entire Keystone II family of DSP's. In all cases the ferrite must go close to the pin.

Table 3: Power Rail Filter Definition

Ref.	Common Name	Note	Filter Required	Filter Description	No. Filters
1	CVDDT		No	N/A	0
2	CVDD		No	N/A	0
3	VDDALV		No	N/A	0
4	VDDAHV		No	N/A	0
5	CVDD1		No	N/A	0
6	CVDDT1		No	N/A	0
7	AVDDA15:6	F, F2	Yes[E]	Ferrite: 100MHz; 75Ω – 150Ω	10/2
8	DVDD1V5A		No	N/A	0
9	DVDD1V5B		No	N/A	0
10	DVDD1V8		No	N/A	0
11	AVDDA5:1	F, E1,F3	Yes[E]	150Ω@10MHz, DCR≤130mohms	5
12	VPH	F, F1, F2	Yes[E]	Ferrite: 100MHz; 75Ω – 150Ω	1
13	VP/VPTX/VDDUSB	F, F1, F2	Yes[E]	Ferrite: 100MHz; 75Ω – 150Ω	2
14	VPPB		No	N/A	0

NOTE E: Texas Instruments is still evaluating the need for filters on unused peripherals, therefore refer to your data manual or available pin list for specific details on which interfaces are necessary for your application. At the re-release of this document each ferrite should be rated a minimum of 150-200mA unless they are combined as with AVDDA10:6 and AVDDA15:11 and then the single ferrite should be rated for 1.5A – minimum.

NOTE E1: Texas Instruments allows the use of a ferrite bead rated at 200mA minimum and 150Ω@10MHz with a DCR of ≤130mΩ. Optionally; the ferrite may have the same ratings at a different frequency provided it meets the following values: 470Ω @ 100MHz or 180Ω@1GHz. The recommended part is a Murata BLM18KG471SN1D.

NOTE F: Not all devices will incorporate the same peripherals, power interfaces, or require every clock; therefore refer to your data manual or available pin list for specific details on which interfaces and clocks are necessary for your application

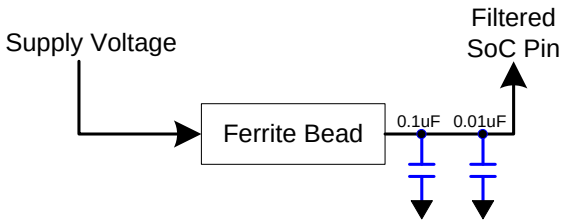
NOTE F1: If the peripheral is used, connect the pin to VDDALV (0.85V) through a ferrite bead; if peripheral is unused remove ferrite and tie (short trace) to ground through 0Ω resistor.

NOTE F2: The recommended part should be a Murata BLM18EG101TN1 rated for 2A if AVDDA10:6 are tied together, a separate BLM18EG101TN1 should also be used for AVDDA15:11. If individual ferrites

are used for AVDDA15:6 are used the recommended part should be a Murata BLM15AG121SN1 for each pin. The DCR should be ≤250mΩ

The following figure (Figure 1) illustrates the intended filter connection between the ferrite bead and respective input power pins. The bulk capacitors required in the supply side of the input voltage are not illustrated in this figure but are required.

Figure 1: Power Rail Filter Implementation Example



It is recommended that the capacitors located between your ferrite bead and the input power pins on your DSP be ceramic and be placed close to the pins on the input side.

AC RIPPLE AND DC TOLERANCE REQUIREMENTS

The following table (Table 4) provides a preliminary listing of the maximum AC ripple and DC tolerance requirements by power rails for the entire Keystone II family of DSP's.

Table 4: AC Ripple & DC Tolerances

Ref.	Common Name	Description	Voltage	Tolerance[I]
1	CVDDT	ARM Core SmartReflex Supply	0.80 – 1.05V	±5%
2	CVDD	DSP Core SmartReflex Supply	0.80 – 1.05V	±5%
3	VDDALV	SerDes Analog Power Supply	0.85V	±5%[G]
4	VDDAHV	SerDes Analog Power Supply	1.8V	±5%[H]
5	CVDD1	DSP Fixed Core Supply	0.95V	±5%
6	CVDDT1	ARM Fixed Core Supply	0.95V	±5%
7	AVDDA15:01	DDR3 DLL & PLL Supply	1.8V[AK]	±5%
8	DVDD1V5A	I/O Power Supply for DDR3A	1.5V	±5%
9	DVDD1V5B	I/O Power Supply for DDR3B	1.5V	±5%
10	DVDD1V8	Power Supply for 1.8V I/O's	1.8V	±5%
11	VDDA18	PLL Supplies	1.8V	±5%
12	USBVDD3V3	3.3V USB Supply	3.3V	±5%
13	USB0V85	Internal PHY Power Supply	0.85V	±5%
14	VPPB	Customer FUSEFARM	1.8V	±5%[AG]

NOTE AK: The AVDDA10:06 pins support the DDR3A DLL's; the AVDDA15:11 pins support the DDR3B DLL's; and the AVDDA05:01 pins support the PLL supplies.

NOTE G: VDDALV should have a maximum of 20mVpp AC power-supply noise superimposed on the 0.85V nominal DC value. The supply ramp-up slew rate limit is 19mV/1.0µs for VDDHA in order to avoid triggering the PHY ESD clamps and causing excess current draw.

NOTE H: VDDAHV should have a maximum of 50mVpp AC power-supply noise superimposed on the 1.8V nominal DC value. The supply ramp-up slew rate limit is 40mV/1.0µs for VDDHA in order to avoid triggering the PHY ESD clamps and causing excess current draw.

NOTE I: The absolute maximum tolerance is listed as ±5%, this includes the AC ripple levels indicated. As an example (using the VDDAHV 1.8V supply rail); if the AC ripple is +42mV p-p and the total tolerance is ±90mV, the maximum DC variation cannot exceed +48mV or -90mV. Texas Instruments only guarantees the performance of its DSP's under these conditions.

NOTE AG: VPPB pin(s) have an absolute maximum ramp-up slew rate of 1.8V/100µs.

NOTE: The comments in this application note pertain to a single DSP. When multiple DSP's are used the combination of power rails must also take into consideration the impact on sequencing, total amperage requirements and impact on both AC and DC tolerances.

POWER RAIL SEQUENCING REQUIREMENTS

The following section defines the sequencing requirements for all power and clock rails including resets for the entire Keystone II family of DSP's. TI DSP's are intended to support both I/O before Core and Core before I/O methods of power sequencing. The following two options assume that respective cores supply rails are tied together. Refer to the rightmost column in both tables (Table 5 & 6) for sequencing order.

Table 5: Sequencing - Core before I/O

Ref.	Common Name	Description	Voltage	Sequence
1	CVDDT	ARM Core SmartReflex Supply	0.80 – 1.05V	1
2	CVDD	DSP Core SmartReflex Supply	0.80 – 1.05V	1
3	VDDALV	SerDes Analog Power Supply	0.85V	3
4	VDDAHV	SerDes Analog Power Supply	1.8V	4
5	CVDD1	DSP Fixed Core Supply	0.95V	2
6	CVDDT1	ARM Fixed Core Supply	0.95V	2
7	AVDDA15:01	DDR3 DLL & PLL Supply	1.8V[AK]	4
8	DVDD1V5A[K]	I/O Power Supply for DDR3A	1.5V	5
9	DVDD1V5B[K]	I/O Power Supply for DDR3B	1.5V	5
10	DVDD1V8	Power Supply for 1.8V I/O's	1.8V	4
11	VDDA18	PLL Supplies	1.8V	4
12	USBVDD3V3	3.3V USB Supply	3.3V	6
13	USB0V85	Internal PHY Power Supply	0.85V	3
14	Clocks[J]	SYSCLK / CORECLK / ALTCORECLK / ARMCLK / RP1CLK	-	7
15	Resets[L]	Reset➔PORz➔Resetfullz	-	8
16	VPPB	Customer FUSEFARM	1.8V	9

NOTE J: Not all devices will incorporate the same peripherals, power interfaces, or require every clock; therefore refer to your data manual or available pin list for specific details on which interfaces and clocks are necessary for your application. All clocks should be present and stable before deassertion of reset.

NOTE K: The combination of both DVDD1V5 rails is being considered internally. Should these rails be tied together this application note and respective data manuals and hardware design guide will be updated.

NOTE AK: The AVDDA10:06 pins support the DDR3A DLL's; the AVDDA15:11 pins support the DDR3B DLL's; and the AVDDA05:01 pins support the PLL supplies.

Table 6: Sequencing - I/O before Core

Ref.	Common Name	Description	Voltage	Sequence[AC]
1	CVDDT	ARM Core SmartReflex Supply	0.80 – 1.05V	3
2	CVDD	DSP Core SmartReflex Supply	0.80 – 1.05V	3
3	VDDALV	SerDes Analog Power Supply	0.85V	5
4	VDDAHV	SerDes Analog Power Supply	1.8V	1
5	CVDD1	DSP Fixed Core Supply	0.95V	4
6	CVDDT1	ARM Fixed Core Supply	0.95V	4
7	AVDDA15:01	DDR3 DLL & PLL Supply	1.8V[AK]	1
8	DVDD1V5A[K]	I/O Power Supply for DDR3A	1.5V	2
9	DVDD1V5B[K]	I/O Power Supply for DDR3B	1.5V	2
10	DVDD1V8	Power Supply for 1.8V I/O's	1.8V	1
11	VDDA18	PLL Supplies	1.8V	1
12	USBVDD3V3	3.3V USB Supply	3.3V	6
13	USB0V85	Internal PHY Power Supply	0.85V	5
14	Clocks[J]	SYSCLK / CORECLK / ALTCORECLK / ARMCLK / RP1CLK	-	7
15	Resets[L, AD]	Reset➔PORz➔Resetfullz	-	8
16	VPPB	Customer FUSEFARM	1.8V	9

NOTE J: Not all devices will incorporate the same peripherals, power interfaces, or require every clock; therefore refer to your data manual or available pin list for specific details on which interfaces and clocks are necessary for your application.

NOTE K: The combination of both DVDD1V5 rails is being considered internally. Should these rails be tied together this application note and respective data manuals and hardware design guide will be updated.

NOTE L: The reset sequence may change from what is indicated; refer to the respective data manual for the final definition. Your application should be flexible enough to alter this if needed.

NOTE AC: Each power rail should be at a valid level prior to the next rail starting to ramp.

NOTE AD: Upon a successful and correct power sequencing, and proper deassertion of resets, the RESETSTATz pin is considered valid. Incorrect power sequencing or deassertion of resets prior to proper power rail sequencing will leave the RESETSTAz pin in an intermittent state and unusable.

NOTE AK: The AVDDA10:06 pins support the DDR3A DLL's; the AVDDA15:11 pins support the DDR3B DLL's; and the AVDDA05:01 pins support the PLL supplies.

SMARTREFLEX AND EXTERNAL AVS POWER SUPPLY CONTROL

The Keystone II family of DSP's requires the use of an external variable voltage supply commonly referred to as a SmartReflex or AVS power controller[Y]. Similar to the Keystone I family of DSP's, Keystone II DSP's support Class 0 and Class 3 SmartReflex. Each Keystone II DSP shall support both a VCNTL and I2C interface as a SmartReflex or AVS control mechanism.

The VCNTL (Voltage Control) interface of your DSP, also referred to as a VID (or Voltage ID) is a parallel interface which conveys the appropriate voltage setting to the associated power supply. The following three tables define the possible configurations available when using the VCNTL interface.

The following tables (7-9) describe the interface connection between the currently used UCD9222 or UCD9244 digital controller and Keystone II devices (not all rails may apply).

Table 7: VCNTL 4 Pin 4 Bit Parallel Interface

VCNTL Config.	4 pin 4 bit[Z]		
DSP VCNTL INTERFACE	**DSP PIN USED**	**DSP PIN DESCRIPTION**	**UCD9222/44 PIN INTERFACE[AA]**
VCNTL0	VCNTL0	DSP AVS Parallel Voltage Control Pin 0	VID1A
VCNTL1	VCNTL1	DSP AVS Parallel Voltage Control Pin 1	VID1B
VCNTL2	VCNTL2	DSP AVS Parallel Voltage Control Pin 2	VID1C
VCNTL3	VCNTL3	DSP AVS Parallel Voltage Control Pin 3	VID1S
VCNTL4	**Not Used**	-	-
VCNTL5	**Not Used**	-	-
VCNTLT0	VCNTLT0	ARM AVS Parallel Voltage Control Pin 0	VID2A
VCNTLT1	VCNTLT1	ARM AVS Parallel Voltage Control Pin 1	VID2B
VCNTLT2	VCNTLT2	ARM AVS Parallel Voltage Control Pin 2	VID2C
VCNTLT3	VCNTLT3	ARM AVS Parallel Voltage Control Pin 3	VID2S
VCNTLT4	**Not Used**	-	-
VCNTLT5	**Not Used**	-	-

Table 8: VCNTL 4 Pin 6 Bit Serial Interface

VCNTL Config.	4 pin 6 bit		
DSP VCNTL INTERFACE	**DSP PIN USED**	**DSP PIN DESCRIPTION**	**UCD9222/44 PIN INTERFACE[AA]**
VCNTL0	-	DSP AVS Parallel Voltage Control Pin 0	-
VCNTL1	-	DSP AVS Parallel Voltage Control Pin 1	-
VCNTL2	VCNTL2	DSP AVS Parallel Voltage Control Pin 2	VID1A
VCNTL3	VCNTL3	DSP AVS Parallel Voltage Control Pin 3	VID1B
VCNTL4	VCNTL4	DSP AVS Parallel Voltage Control Pin 4	VID1C

Continued

VCNTL Config.	4 pin 6 bit		Con't from above
DSP VCNTL INTERFACE	**DSP PIN USED**	**DSP PIN DESCRIPTION**	**UCD9222/44 PIN INTERFACE[AA]**
VCNTL5	VCNTL5	DSP AVS Parallel Voltage Control Pin 5	VID1S (Select)
VCNTLT0	-	ARM AVS Parallel Voltage Control Pin 0	-
VCNTLT1	-	ARM AVS Parallel Voltage Control Pin 1	-
VCNTLT2	VCNTLT2	ARM AVS Parallel Voltage Control Pin 2	VID2A
VCNTLT3	VCNTLT3	ARM AVS Parallel Voltage Control Pin 3	VID2B
VCNTLT4	VCNTLT4	ARM AVS Parallel Voltage Control Pin 4	VID2C
VCNTLT5	VCNTLT5	ARM AVS Parallel Voltage Control Pin 5	VID2S (Select)

Table 9: VCNTL 6 Pin 6 Bit Parallel Interface

VCNTL Config.	6 pin 6 bit[AL]			
DSP VCNTL INTERFACE	**DSP PIN USED**	**DSP PIN DESCRIPTION**	**UCD9222 PIN INTERFACE[AA]**	**UCD9244 PIN INTERFACE[AA]**
VCNTL0	VCNTL0	DSP AVS Parallel Voltage Control Pin 0	VID1A	VID1A
VCNTL1	VCNTL1	DSP AVS Parallel Voltage Control Pin 1	VID1B	VID1B
VCNTL2	VCNTL2	DSP AVS Parallel Voltage Control Pin 2	VID1C	VID1C
VCNTL3	VCNTL3	DSP AVS Parallel Voltage Control Pin 3	VID1S	VID1S
VCNTL4	VCNTL4	DSP AVS Parallel Voltage Control Pin 4	VID2A	VID2A
VCNTL5	VCNTL5	DSP AVS Parallel Voltage Control Pin 5	VID2B	VID2B
VCNTLT0	VCNTLT0	ARM AVS Parallel Voltage Control Pin 0	-	VID3A
VCNTLT1	VCNTLT1	ARM AVS Parallel Voltage Control Pin 1	-	VID3B
VCNTLT2	VCNTLT2	ARM AVS Parallel Voltage Control Pin 2	-	VID3C
VCNTLT3	VCNTLT3	ARM AVS Parallel Voltage Control Pin 3	-	VID3S
VCNTLT4	VCNTLT4	ARM AVS Parallel Voltage Control Pin 4	-	VID4A
VCNTLT5	VCNTLT5	ARM AVS Parallel Voltage Control Pin 5	-	VID4B
			Note AE	
				Note AF

NOTE Y: Depending on design, processor selection, or implementation, more than one AVS/SmartReflex power supply may be required. Not all DSP's will contain for example a ARM core, which if not included can be omitted.

NOTE Z: The 4 pin 4 bit interface supported by your Keystone II DSP may not be supported in released silicon. The basic 4 pin 4 bit interface, which is very similar to that implemented in earlier Texas Instruments' DSP's is intended to also support up to a 400mV voltage control range but doesn't offer the lower resolution of other interface options.

NOTE AA: Pin assignments are based on common existing power supplies; e.g. UCD9222 and UCD9244. Refer to the respective data manual for verification of interconnectivity.

NOTE AB: When using the UCD9222 in a 6 pin 6 bit VCNTL parallel interface two pins are borrowed from the 2nd rail. The second rail in this instance can only be used as a fixed rail controller

NOTE AE: When using the UCD9222 in a 6 pin, 6 bit parallel configuration the VID2C and VID2S pins must be grounded. Parallel VID interfaces wider than 4 bits are supported on odd-numbered rails by utilizing the VID pins from the next-higher even-numbered rail. The even-numbered rail can still be used as a fixed-voltage rail.

NOTE AF: When using the UCD9244 in a 6 pin, 6 bit parallel configuration the VID2C, VID2S, VID4C, and VID4S pins must be grounded. Parallel VID interfaces wider than 4 bits are supported on odd-numbered rails by utilizing the VID pins from the next-higher even-numbered rail. The even-numbered rail can still be used as a fixed-voltage rail.

NOTE AL: This parallel interface is intended to be supported in a future products to be released in the near future.

In addition to the VCNTL control interface options described above, your DSP also supports SmartReflex Class 0 and Class 3 power management over I2C. The Keystone II family of DSP's now incorporate two power i2c interfaces (one for DSP and one for ARM if an ARM core is included in your DSP selection).

The original design goal was to only support only SmartReflex Class 3 over the respective power I2C interface. TI is currently evaluating support for both Class 0 and Class 3 over the power I2C interface and believes both will be possible with a small amount of software intervention prior to the release of first silicon.

As an alternative backup plan, SmartReflex Class 0 is also possible over the regular I2C interface but requires a small amount of software to pull the Class 0 MMR (memory mapped register) binary value and properly format it on the regular I2C (SDA/SCL) bus to communicate with the respective POL/SMPS power supply.

NOTE:
Various methods of AVS power control are available for the Keystone II family of devices; different modes of control are identified and intended for use but not yet validated.

As with all new silicon devices in a family – customers are requested to take all precautions to minimize the risk of a particular control mechanism not being fully functional or fully validated prior to the release of silicon.

The following top level block diagrams illustrate various other concepts that can be implemented to support power requirements of your Keystone II device. Level translators (where utilized are the TI PCA series (e.g. PCA9306)) are Texas Instruments devices unless otherwise specified.

Figure 2: DSP + ARM Core, Separate POL Supplies

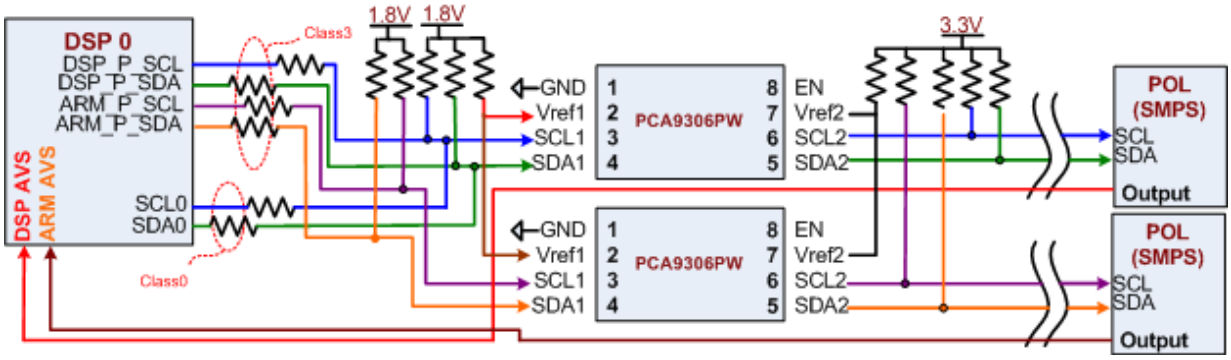


Figure 2 (above) illustrates a Keystone II DSP with both an ARM and DSP AVS control output. In figure 2 each variable core controls a separate POL/SMPS supply over i2c/PMBus. This illustrated method supports Class 3 SmartReflex currently over the power i2c bus and Class 0 over the regular i2c bus. TI intends to also support Class 0 over power i2c by time silicon is released. A small amount of software intervention will be required to allow for SmartReflex Class 0 to operate on the power i2c bus.

Figure 3: DSP + ARM Core, Control Tied Together with 1 POL

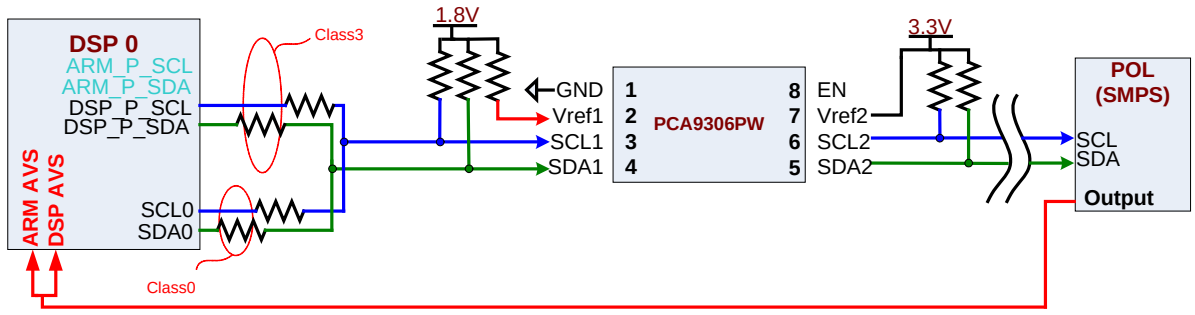


Figure 3 (above) illustrates a Keystone II DSP with both an ARM and DSP AVS control outputs controlled from a single set of i2c control pins (Should always be the DSP i2c pins). In figure 3 the variable core controls a single POL/SMPS supply over the i2c/PMBus. This illustrated method supports Class 3 SmartReflex currently over the power i2c bus and Class 0 over the regular i2c bus. TI intends to also support Class 0 over power i2c by time silicon is released. A small amount of software intervention will be required to allow for SmartReflex Class 0 to operate on the power

i2c bus. Depending on the control mechanism, either the i2c or power i2c components can be removed.

Figure 4: DSP Core Only, Single POL Supply

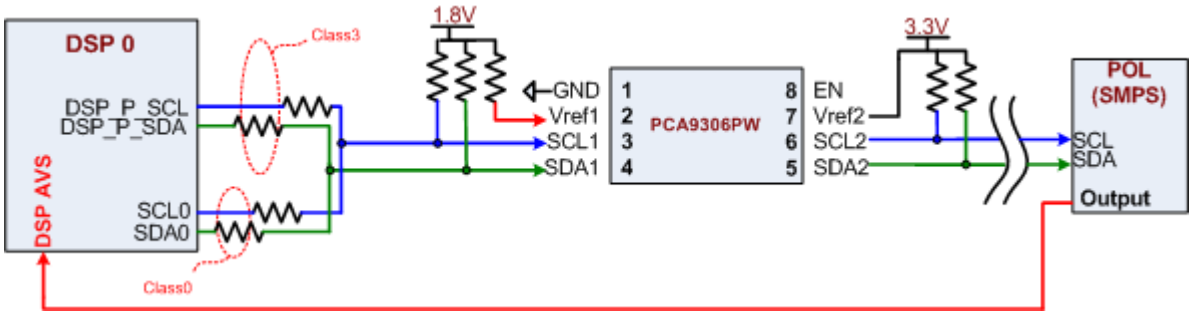


Figure 4 (above) illustrates a Keystone II DSP with only a DSP core and DSP AVS control output. In figure 4 the variable core controls a single POL/SMPS supply over the i2c/PMBus. This illustrated method supports Class 3 SmartReflex currently and is intended to also support Class 0 by time silicon is released. A small amount of software intervention will be required to allow for SmartReflex Class 0 to operate on the power i2c bus.

Figure 5: DSP + ARM Core, Separate Controls using UCD Digital Controller

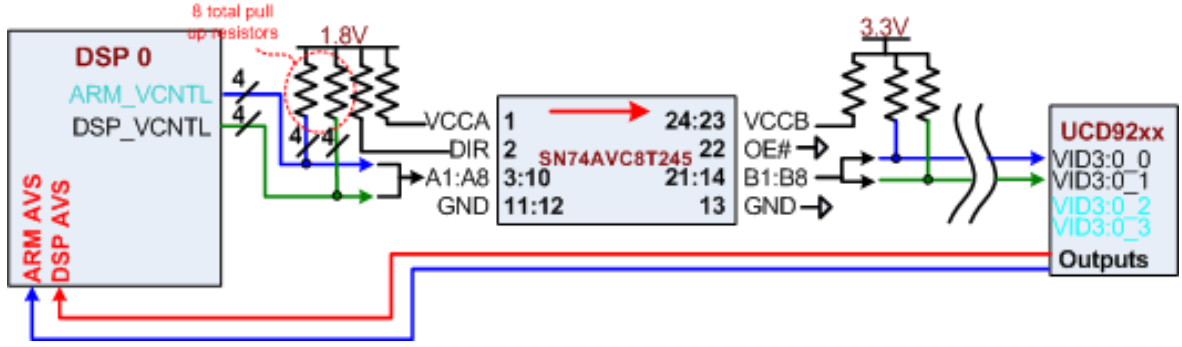


Figure 5 (above) illustrates the potential use of a TI digital controller (in this example it is either a UCD9222 or UCD9244). Using the VCNTL interface to your processor, this combination supports either SmartReflex Class 0 or Class 3 over the parallel interface. It should be noted that the parallel interface illustrated is the 4 pin 6 bit interface similar to the control mechanism implemented in the Keystone I family of processors. In this example the driver and mosfets are not depicted and must be scaled properly to meet the end use application.

Figure 6: DSP + ARM Core, controls tied together using UCD Digital

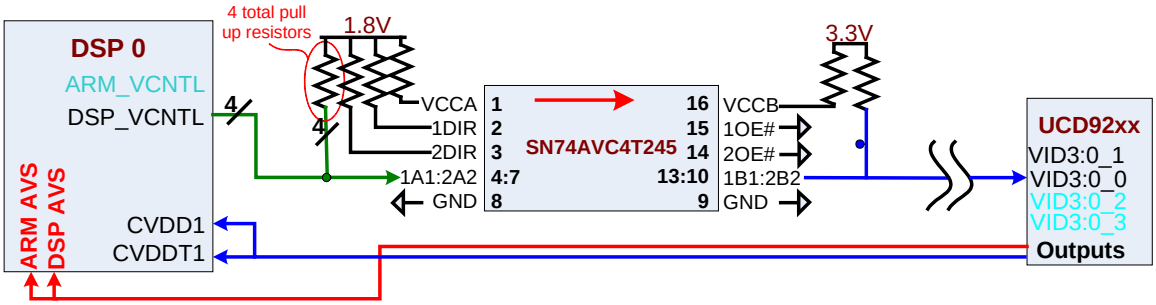


Figure 6 (above) is similar to figure 5 with the exception that the AVS outputs share a common control interface (DSP). In this illustration a single output is level shifted to the correct voltage level and driven into the UCD92xx digital controller on the first rail. Using the VCNTL interface to your processor, this combination also supports SmartReflex Class 0 or Class 3 over the parallel bus. It should be noted that the parallel interface illustrated is the 4 pin 6 bit interface similar to the control mechanism implemented in the Keystone I family of processors. In this example the driver and mosfets are not depicted and must be scaled properly to meet the end use application.

The secondary output of the digital controller (outputs 3 & 4 if using the UCD9244) is used to control a fixed rail supply (in this example the fixed core supplies which are tied together)

Figure 7: DSP + ARM Core, controls tied together using LM10k interface

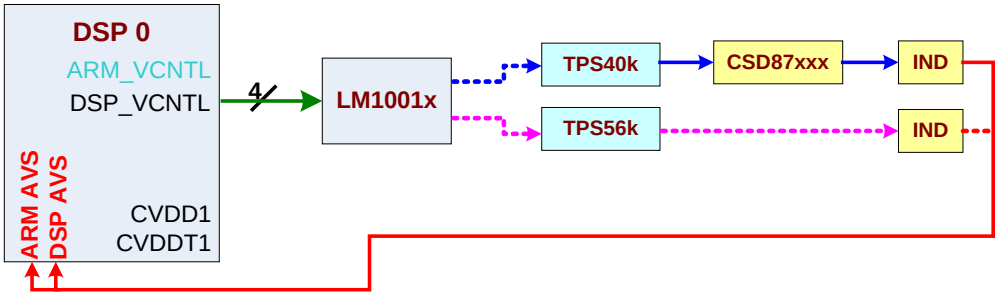


Figure 7 (above) illustrates yet another possible control mechanism using the Keystone II VCNTL interface. The LM1001x (10 or 11) devices interface between the 4 pin 6 bit device and provide a feedback current into the DC-DC controller. This interface device is a low cost alternative that allows for standard DC-DC converters to be used like the TPS40k or TPS56k series of controllers (verify selection prior to completing your specific design). In figure 7, two different designs have been implemented, one using the TPS40k (TPS40100) and the TPS56k (TPS56221) devices. This illustration is intended to illustrate two options – under no circumstances should both be implemented in parallel! Using the TPS40k family of DC-DC controllers along with one of the TI NexTFET's and associated inductor, it is possible to achieve up to 50A output (other parts may be available). Using the TPS56k family of DC-DC controllers along with the associated inductor, it is possible to achieve up to 25A output on a single rail (other parts may be available).

It should be noted that there exists multiple power solutions from Texas Instruments that meet the interconnect and performance criteria. The above referenced figures are only intended to illustrate a few of possibilities.

APPENDIX A

The combination of power rails is made possible in order to simplify designs and reduce the total number of overall components. Although in theory this looks simpler to implement there are additional considerations that must be considered before proceeding.

The following is a listing of concerns to consider before selecting to combine allowable rails:

- Total overall current will increase
- Copper power planes on PCB will most likely have to increase to a minimum of 1oz thick (calculations required)
- Thermal vias and traces will have to be designed for higher current
- Ambient temperature and temperature rises will have to be taken into account
- The IR drop or voltage drop will have to be taken into account
- Configurations with multiple SoC utilizing common rails must still meet all sequencing requirements for clocking, sync currents, and power

----- NOTICE -----

In some instances and device revisions it may be mandatory to combine certain power rails, refer to the respective data manual and device errata's prior to finalizing your design.