SYSTEM ON MODULE

Top-Level Overview

Date: 12.04.2026

Author: Ti2i3

Revision: A1

DDR3

DDR3L Memory

MT41K64M16TW-107:J

1 Gb / 933 MHz / 16-bit

VDD_DDR: 1.35 V

Datei: DDR3.kicad_sch

16-bit

EMIF

PMIC

TPS65218D0

PMIC Reset Buffer

SN74LVC1G07DBVR

AM3354

Sitara™ ARM®

Cortex®-A8

Ports

24 MHz System Clock

OT2JI11124M

32.768 kHz RTC Clock

SX3M32.768KM20F30TNN

Datei: Ports.kicad_sch

Power

POWER RAILS

CORE & MPU

- VDD_CORE 1.1 V
- VDD_MPU 1.325 V (1 GHz OPP)

MEMORY

- VDD_DDR 1.35 V (DDR3L)

I/O

- VDDS 1.8 V
- VDDSHVx 1.8 V / 3.3 V

All voltages are typical values.

Refer to AM3354 Datasheet for details.

Datei: Power.kicad_sch

KEY COMPONENTS (Critical)

AM3354 Processor

Sitara™ ARM®

Cortex®-A8

DDR3L Memory

MT41K64M16TW-107:J

1 Gb / 933 MHz / 16-bit

1.35 V

GENERAL NOTES

- All capacitors are rated at 10 V.
- Use 16 V capacitors on 5 V rails.

Am3354 to DDR3L

IC1A
AM3354BZCZD80

U?C
MT41K64M16TW-107:J

DDR_A0	F3	A0	N3	A0
DDR_A1	H1	A1	P7	A1
DDR_A2	E4	A2	P3	A2
DDR_A3	C2	A3	N2	A3
DDR_A4	C3	A4	P8	A4
DDR_A5	B1	A5	P2	A5
DDR_A6	D5	A6	R8	A6
DDR_A7	E2	A7	R2	A7
DDR_A8	D4	A8	T8	A8
DDR_A9	C1	A9	R3	A9
DDR_A10	F4	A10	L7	A10AP
DDR_A11	F2	A11	R7	A11
DDR_A12	E3	A12	N7	A12BC#
DDR_A13	H3			
DDR_A14	H4			
DDR_A15	D3			
DDR_D0	M3	DQ0	E3	DQ0
DDR_D1	M4	DQ1	F7	DQ1
DDR_D2	N1	DQ2	F2	DQ2
DDR_D3	N2	DQ3	F8	DQ3
DDR_D4	N3	DQ4	H3	DQ4
DDR_D5	N4	DQ5	H8	DQ5
DDR_D6	P3	DQ6	G2	DQ6
DDR_D7	P4	DQ7	H7	DQ7
DDR_D8	J1	DQ8	D7	DQ8
DDR_D9	K1	DQ9	C3	DQ9
DDR_D10	K2	DQ10	C8	DQ10
DDR_D11	K3	DQ11	C2	DQ11
DDR_D12	K4	DQ12	A7	DQ12
DDR_D13	L3	DQ13	A2	DQ13
DDR_D14	L4	DQ14	B8	DQ14
DDR_D15	M1	DQ15	A3	DQ15
DDR_DQS0	P1	LDQS+	F3	LDQS
DDR_DQSN0	P2	LDQS−	G3	LDQS#
DDR_DQS1	L1	UDQS+	C7	UDQS
DDR_DQSN1	L2	UDQS−	B7	UDQS#
DDR_DQM0	M2	LDM	E7	LDM
DDR_DQM1	J2	UDM	D3	UDM
DDR_RESETN	G2	RESET	T2	RESET#
DDR_CSN0	H2	CS	L2	CS#
DDR_RASN	G4	RAS	J3	RAS#
DDR_CASN	F1	CAS	K3	CAS#
DDR_WEN	B2	WE	L3	WE#
DDR_BA0	C4	BA0	M2	BA0
DDR_BA1	E1	BA1	N8	BA1
DDR_BA2	B3	BA2	M3	BA2
DDR_CKE	G3	CKE	K9	CKE
DDR_CK	D2	CK	J7	CK
DDR_CKN	D1	CK−	K7	CK#
DDR_ODT	G1	ODT	K1	ODT
DDR_VTP	J3		L8	ZQ
DDR_VREF	J4			

R? 4.7kΩ +1V35
R? 49.91Ω , (±1%;.20 mW)
R? 240Ω
C? 0.1uF
C? 0.1uF
GND

DDR3L Power

Bulk capacitors

+1V35
C? 10uF
C? 10uF
GND

High−Speed capacitors

+1V35
C2 0.1uF
C? 0.1uF
C11 0.1uF
C? 0.1uF ×6
GND

+1V35
C4 0.1uF
C9 0.1uF
C? 0.1uF ×2
C? 0.1uF ×5
C 0.1uF
GND

U?A
MT41K64M16TW-107:J

B2	VDD	VSSQ	B1
D9	VDD	VSSQ	B9
G7	VDD	VSSQ	D1
K2	VDD	VSSQ	D8
K8	VDD	VSSQ	E2
N1	VDD	VSSQ	E8
N9	VDD	VSSQ	F9
R1	VDD	VSSQ	G1
R9	VDD	VSSQ	G9
A1	VDDQ	VSSQ	A9
A8	VDDQ	VSS	B3
C1	VDDQ	VSS	E1
C9	VDDQ	VSS	G8
D2	VDDQ	VSS	J2
F1	VDDQ	VSS	J8
E9	VDDQ	VSS	M1
H2	VDDQ	VSS	M9
H9	VDDQ	VSS	P1
M8	VREFCA	VSS	P9
H1	VREFDQ	VSS	T1
		VSS	T9

+1V35
GND

U?B
MT41K64M16TW-107:J

J1	NC	NC	M7
J9	NC	NC	T3
L1	NC	NC	T7
L9	NC		

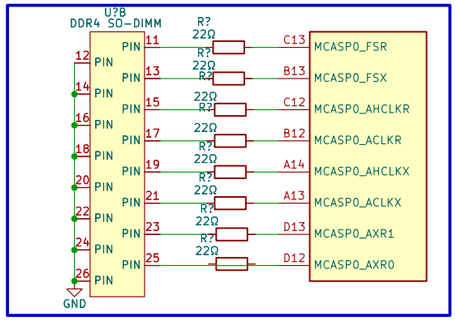
@ Vref, Voltage divider

+1V35
C? 0.1uF
R? 1 kΩ 1%
C? 0.1uF
R? 1 kΩ 1%
GND

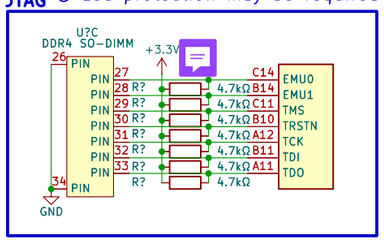
Sheet: /DDR3/	
File: DDR3.kicad_sch	
Title:	
Size: A3	Date:
KiCad E.D.A. 10.0.1	Id: 2/4

Rev:

Audio

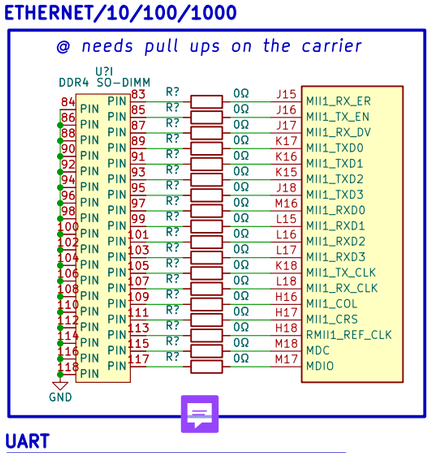


JTAG @ Esd protection may be required

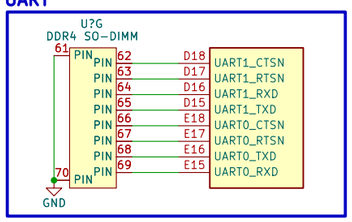


ETHERNET/10/100/1000

@ needs pull ups on the carrier

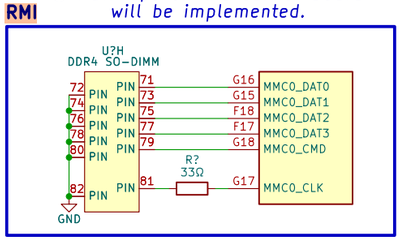


UART

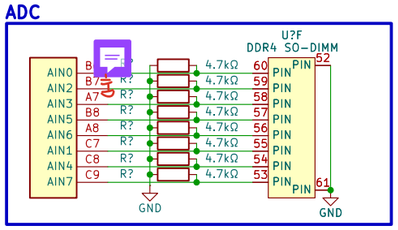


@ Pull-ups on the carrier board will be implemented.

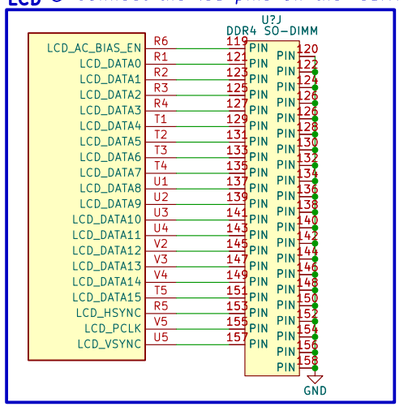
RMI



ADC



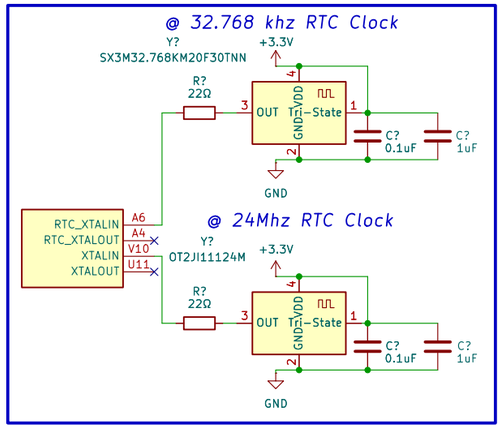
LCD @ Connect the lcd pins on the carrier



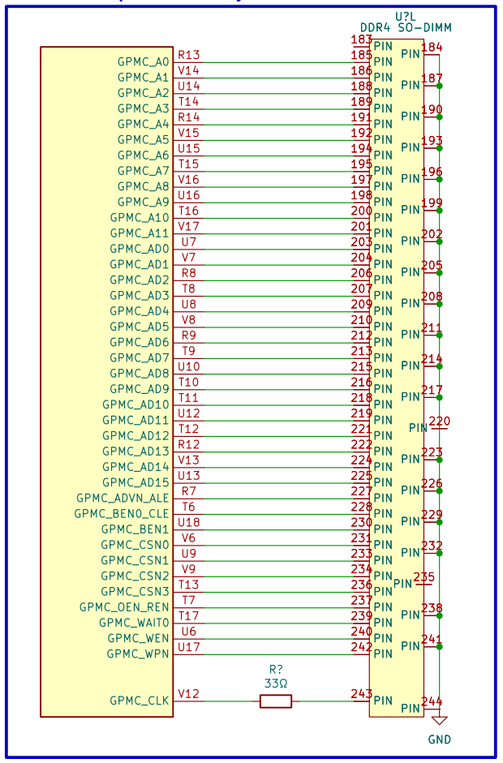
@ High speed signals

USB Minimize addition of series resistor or TP

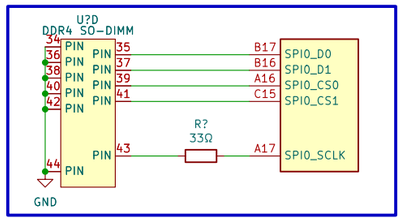
CLOCK



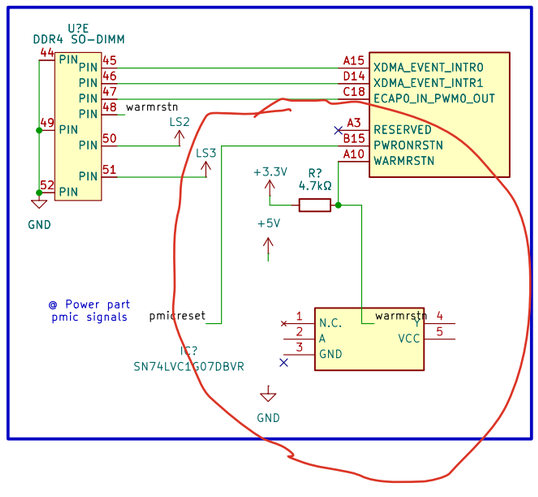
General-Purpose Memory Controller



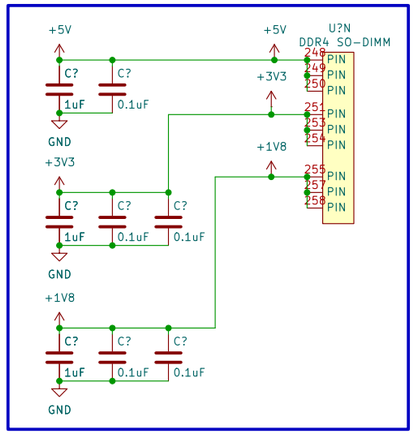
SPI



REST @ Connect the rtc pins on the carrier!



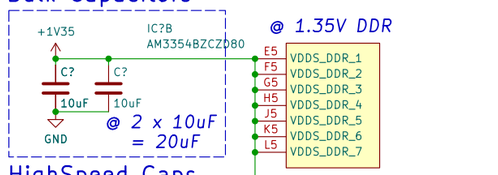
SODIMM Power Pins



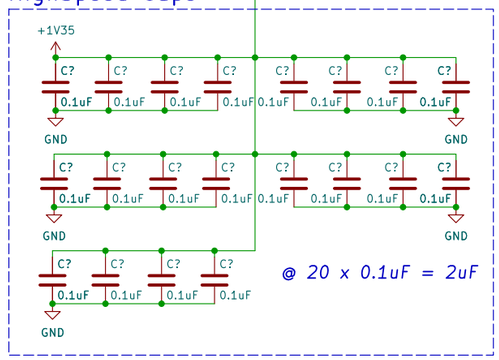
Sheet: /Ports/		
File: Ports.kicad_sch		
Title:		
Size: A3	Date:	**Rev:**
KiCad E.D.A. 10.0.1		Id: 3/4

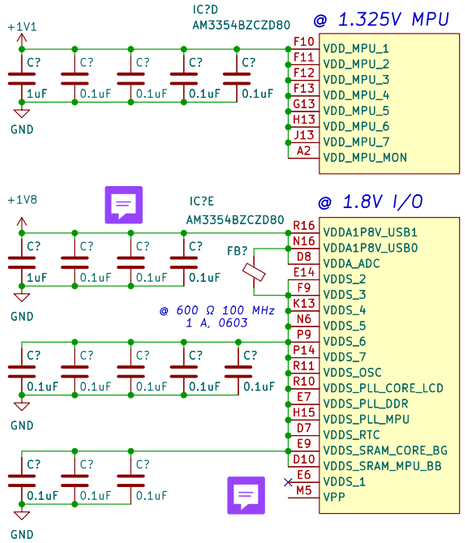
Power AM3354

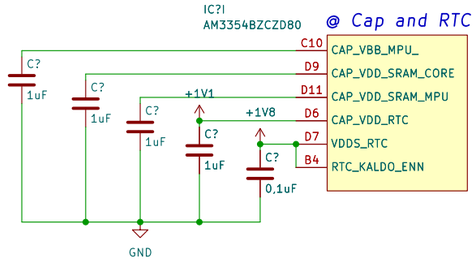
Bulk Capacitors

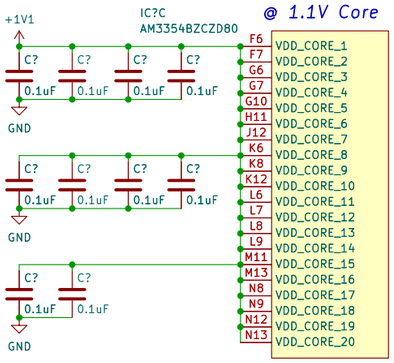


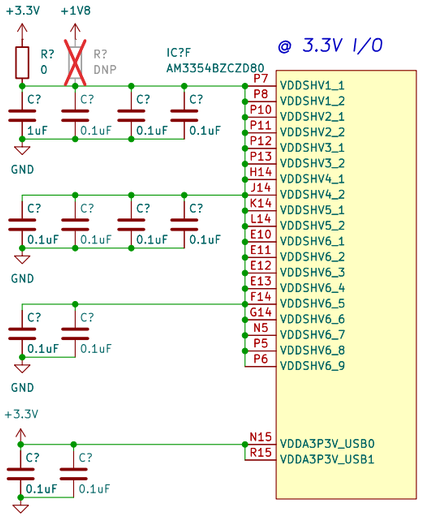
HighSpeed Caps

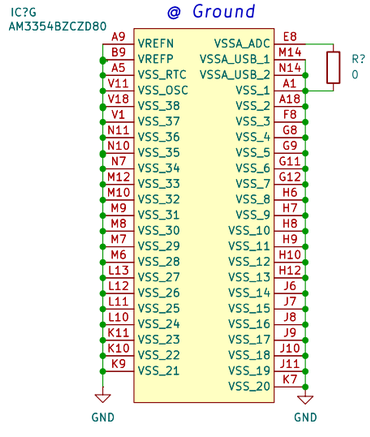




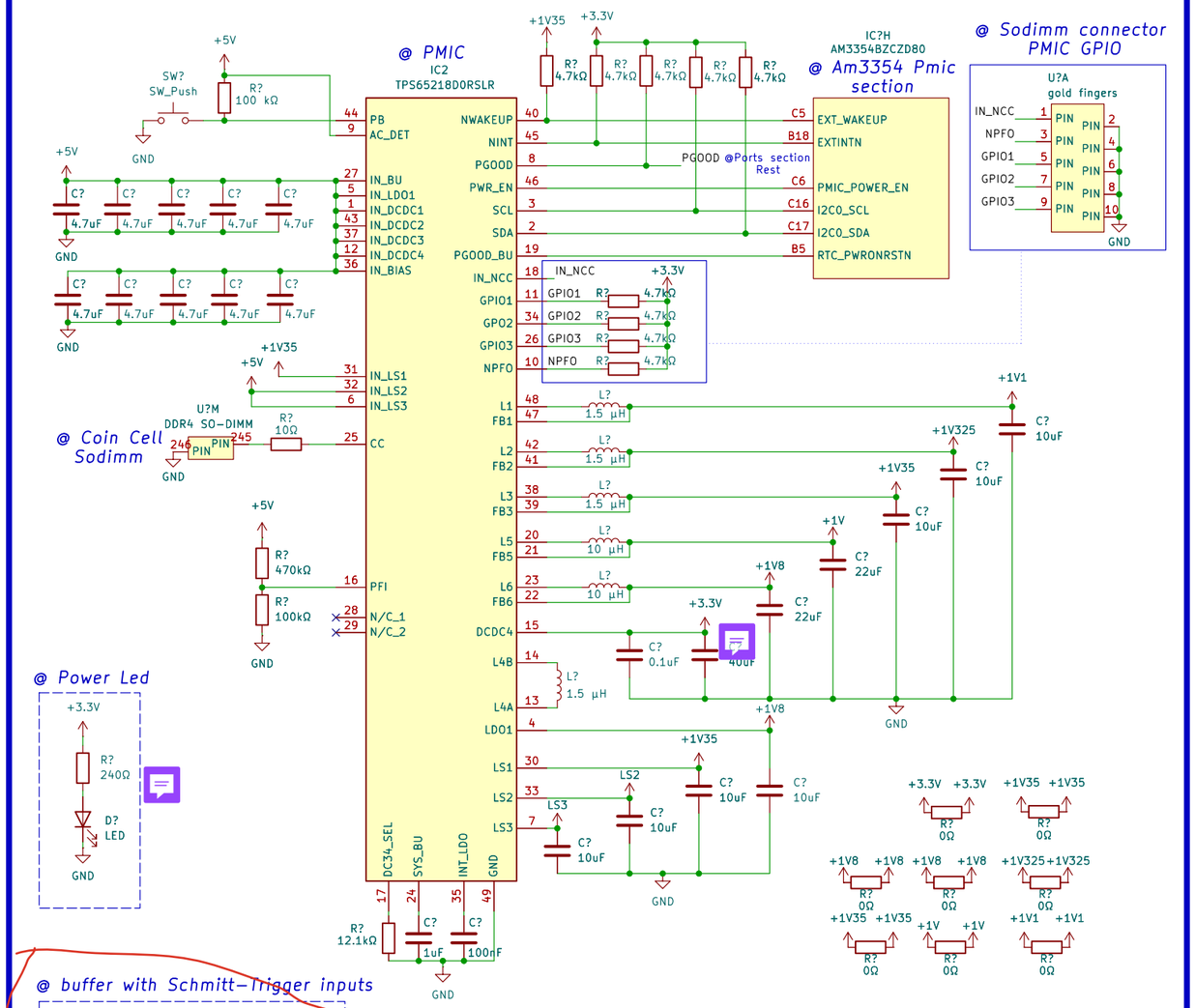


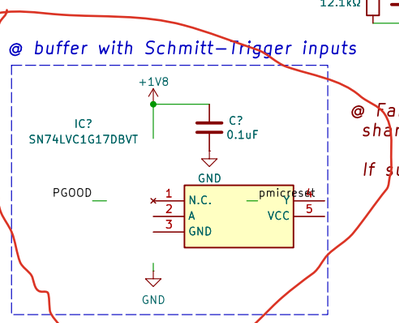






PMIC TPS65218D0RSLR





@ Fail-safe protection is not implemented, as all connected I/O devices share the same supply source as the corresponding VDDSHV domains.
External power injection on I/O pins is not supported.
If such use cases are required, fail-safe protection must be evaluated.

Sheet: /Power/		
File: Power.kicad_sch		
Title:		
Size: A3	Date:	**Rev:**
KiCad E.D.A. 10.0.1		Id: 4/4