pdk_jacinto_07_00_00¥packages¥ti¥board¥diag¥norflash¥src¥ospi_quad_test.c：Test Code Main

(*1) when using QSPI, the DTR (DDR) protocol is disabled. (PDK original)

(*2) In our confirmation, DAC (Direct Access Controller) is enabled. (Added by us)
*Config is changed here only

C:¥TI¥SDK70_TEMP¥pdk_jacinto_07_00_00¥packages¥ti¥board¥diag¥norflash¥src¥ospi_quad_test.c - sakura

ファイル(F) 編集(E) 変換(C) 検索(S) ツール(T) 設定(O) ウィンドウ(W) ヘルプ(H)

ospi_quad_test.c

```
366  *            0  - In case of success
367  *           -1  - In case of failure
368  *
369  */
370 static int8_t BoardDiag_norFlashTest(void)
371 {
372     Board_flashHandle boardHandle;
373     Board_FlashInfo *flashInfo;
374     bool testStatus = true;          /* return value */
375     OSPI_v0_HwAttrs ospi_cfg;
376
377     UART_printf("¥nReading Device ID¥n");
378
379     /* Get the default OSPI init configurations */
380     OSPI_socGetInitCfg(BOARD_SPI_NOR_INSTANCE, &ospi_cfg);
381
382     /* Modify the default OSPI configurations if necessary */
383     ospi_cfg.intrEnable = false;
384
385 #if defined(UDMA_ENABLE)
386     ospi_cfg.dmaEnable  = true;
387     ospiUdmaInit(&ospi_cfg);
388 #else
389     ospi_cfg.dmaEnable  = false;
390 #endif
391 #if defined(j721e_evm)
392     ospi_cfg.phyEnable  = false;
393 #endif
394     ospi_cfg.xferLines = OSPI_XFER_LINES_QUAD;
395     ospi_cfg.dtrEnable = false;
396
397 // [2023/06/07 TEST] ADD Start
398     ospi_cfg.dacEnable = true;      // DAC Enable
399 // [2023/06/07 TEST] ADD End
400
401     /* Set the default OSPI init configurations */
402     OSPI_socSetInitCfg(BOARD_SPI_NOR_INSTANCE, &ospi_cfg);
403
404     /* Open the Board NOR device with port 1
405        and use default NOR configurations */
406
407     boardHandle = Board_flashOpen(BOARD_FLASH_ID_MT25QU512ABB,
408                                   BOARD_SPI_NOR_INSTANCE, NULL);
409     if (!boardHandle)
410     {
411         UART_printf("¥n Board_flashOpen Failed. ¥n");
412         return -1;
413     }
414     else
415     {
416         flashInfo = (Board_FlashInfo *)boardHandle;
417         UART_printf("¥nNOR device ID: 0x%x, manufacturer ID: 0x%x ¥n",
418                 flashInfo->device_id, flashInfo->manufacturer_id);
419     }
420
421 #if defined(DIAC_COMPLIANCE_TEST)
```

(*1)

(*2)

ヘルプ目次 ブックマーク グループを uudecodeし Base64デコ UTF-7→SJ UTF-8→SJ UTF-

365 行 1 桁 LF U+00

pdk_jacinto_07_00_00¥packages¥ti¥drv¥spi¥src¥v0¥OSPI_v0.c：Open Operation

C:¥TI¥SDK70_TEMP¥pdk_jacinto_07_00_00¥packages¥ti¥drv¥spi¥src¥v0¥OSPI_v0.c - sakura 2.4.1.2849

ファイル(F) 編集(E) 変換(C) 検索(S) ツール(T) 設定(O) ウィンドウ(W) ヘルプ(H)

OSPI_v0.c

```
386
387 /*
388  *  ======== OSPI_open_v0 ========
389  */
390 static SPI_Handle OSPI_open_v0(SPI_Handle handle, const SPI_Params *params)
391 {
392     SemaphoreP_Params        semParams;
393     uintptr_t                key;
394     SPI_Handle               retHandle = handle;
395     OSPI_v0_Object          *object = NULL;
396     OSPI_v0_HwAttrs const   *hwAttrs = NULL;
397     OsalRegisterIntrParams_t interruptRegParams;
398     int32_t                  retFlag = 0;
399     uint32_t                 numAddrBytes;
400
401     if (handle != NULL)
402     {
403         /* Get the pointer to the object and hwAttrs */
404         object = (OSPI_v0_Object *)handle->object;
405         hwAttrs = (OSPI_v0_HwAttrs const *)handle->hwAttrs;
406
407         /* Determine if the device index was already opened */
408         key = SPI_osalHardwareIntDisable();
409     }
410
411     if ((handle == NULL) || (object->isOpen == (bool)true))
412     {
413         if (handle != NULL)
414         {
415             SPI_osalHardwareIntRestore(key);
416             retHandle = NULL;
417         }
418     }
419     else
420     {
```

(*3)

In the Open operation, if the DTR (DDR) protocol is disabled, specify 3-byte Addressing. (PDK original)

```
579             /* Set default baud rate divider value */
580             if (hwAttrs->phyEnable)
581             {
582                 CSL_ospiSetPreScaler((const CSL_ospi_flash_cfgRegs *)(hwAttrs->baseAddr),
583                                      CSL_OSPI_BAUD_RATE_DIVISOR(2U));
584             }
585             else
586             {
587                 /* Disable high speed mode when PHY is disabled */
588                 CSL_ospiSetPreScaler((const CSL_ospi_flash_cfgRegs *)(hwAttrs->baseAddr),
589                                      CSL_OSPI_BAUD_RATE_DIVISOR_DEFAULT);
590
591                 /* Disable PHY mode */
592                 CSL_ospiPhyEnable((const CSL_ospi_flash_cfgRegs *)(hwAttrs->baseAddr), FALSE);
593
594                 /* Disable PHY pipeline mode */
595                 CSL_ospiPipelinePhyEnable((const CSL_ospi_flash_cfgRegs *)(hwAttrs->baseAddr), FALSE);
596             }
597
598             if (hwAttrs->dtrEnable)
599             {
600                 numAddrBytes = CSL_OSPI_MEM_MAP_NUM_ADDR_BYTES_4;
601             }
602             else
603             {
604                 numAddrBytes = CSL_OSPI_MEM_MAP_NUM_ADDR_BYTES_3;
605             }
606
607             /* Set device size cofigurations */
608             CSL_ospiSetDevSize((const CSL_ospi_flash_cfgRegs *)(hwAttrs->baseAddr),
609                                numAddrBytes,
610                                hwAttrs->pageSize,
611                                hwAttrs->blkSize);
612
613             /* Set indirect trigger address register */
```

(*3)

ヘルプ目次 ブックマーク グループを開 uudecode(_ Base64デコ UTF-7→SJ UTF-8→SJ UTF-16→S EUC→SJIS E-Mail(JIS- 自動判別→

577 行 53 桁 LF LF UTF-8 REC 挿入

pdk_jacinto_07_00_00¥packages¥ti¥board¥src¥flash¥nor¥ospi¥nor_qspi.c：Erase operation

C:¥TI¥SDK70_TEMP¥pdk_jacinto_07_00_00¥packages¥ti¥board¥src¥flash¥nor¥ospi¥nor_qspi.c - sakura 2.4.1.2

ファイル(F) 編集(E) 変換(C) 検索(S) ツール(T) 設定(O) ウィンドウ(W) ヘルプ(H)

nor_qspi.c

```
563 }
564
565 NOR_STATUS Nor_qspiErase(NOR_HANDLE handle, int32_t erLoc, bool blkErase)
566 {
567     uint8_t         cmd[5];
568     uint32_t        cmdLen;
569     uint32_t        address = 0;
570     uint8_t         cmdWren  = NOR_CMD_WREN;
571     NOR_Info       *norOspiInfo;
572     SPI_Handle      spiHandle;
573     OSPI_v0_HwAttrs const *hwAttrs;
574
575     if (!handle)
576     {
577         return NOR_FAIL;
578     }
579
580     norOspiInfo = (NOR_Info *)handle;
581     if (!norOspiInfo->hwHandle)
582     {
583         return NOR_FAIL;
584     }
585     spiHandle = (SPI_Handle)norOspiInfo->hwHandle;
586     hwAttrs = (OSPI_v0_HwAttrs const *)spiHandle->hwAttrs;
587
588     if (erLoc == NOR_BE_SECTOR_NUM)
589     {
590         cmd[0]  = NOR_CMD_BULK_ERASE;
591         cmdLen = 1;
592     }
593     else
594     {
595         if (blkErase == true)
596         {
597             if (erLoc >= NOR_NUM_BLOCKS)
598             {
```

(*4)
If the DTR (DDR) protocol is disabled, the Erase operation requests 3-byte addressing. (PDK original)

```
599             cmd[0] = NOR_CMD_BLOCK_ERASE;
600         }
601         else
602         {
603             if (erLoc >= NOR_NUM_SECTORS)
604             {
605                 return NOR_FAIL;
606             }
607             address   = erLoc * NOR_SECTOR_SIZE;
608             cmd[0] = NOR_CMD_SECTOR_ERASE;
609         }
610
611         if (hwAttrs->dtrEnable == (bool)true)
612         {
613             cmd[1] = (address >> 24) & 0xff; /* 4 address bytes */
614             cmd[2] = (address >> 16) & 0xff;
615             cmd[3] = (address >>  8) & 0xff;
616             cmd[4] = (address >>  0) & 0xff;
617             cmdLen = 5;
618         }
619         else
620         {
621             cmd[1] = (address >> 16) & 0xff;
622             cmd[2] = (address >>  8) & 0xff;
623             cmd[3] = (address >>  0) & 0xff;
624             cmdLen = 4;
625         }
626     }
627
628     if (Nor_qspiCmdWrite(spiHandle, &cmdWren, 1, 0))
629     {
630         return NOR_FAIL;
631     }
632
633     if (Nor_qspiWaitReady(spiHandle, NOR_WRR_WRITE_TIMEOUT))
634     {
```

(*4)

ヘルプ目次 ブックマーク グループを uudecode Base64デコ UTF-7→SJ UTF-8→SJ

600 行 10 桁 CR