TI Analog Solutions for Keystone2 Family of SOCs (multicore ARM and DSP) 66AK2Hxx and 66AK2Exx

Overview

- Keystone2 family overview and system details
- Power solutions for SOC Core and Aux rails
- Power sequencing solutions
- Hot swap controllers, Current / Power Monitors and Temperature Sensors
- MCUs for system health monitoring
- Clocks
- High speed solutions for PCIe, SAS, SATA, Ethernet
- General purpose analog (ESD protection, Logic, etc)

Keystone2 Family Overview and System Level Details

Keystone2 SOCs Overview

Purpose-built servers

4 ARM A15
8 C66xDSP

4 ARM A15
2 C66xDSP

High performance computing
Media processing
Video analytics
Advanced video (H.265)
Gaming
Virtual Desktop Infrastructure
Radar

And many more…

Embedded enterprise

4 ARM A15
1 C66xDSP

1ARM A15
1 C66xDSP

Enterprise video
Digital video recording
Video analytics
Industrial imaging
Industrial control
Voice gateways
Avionics

And many more…

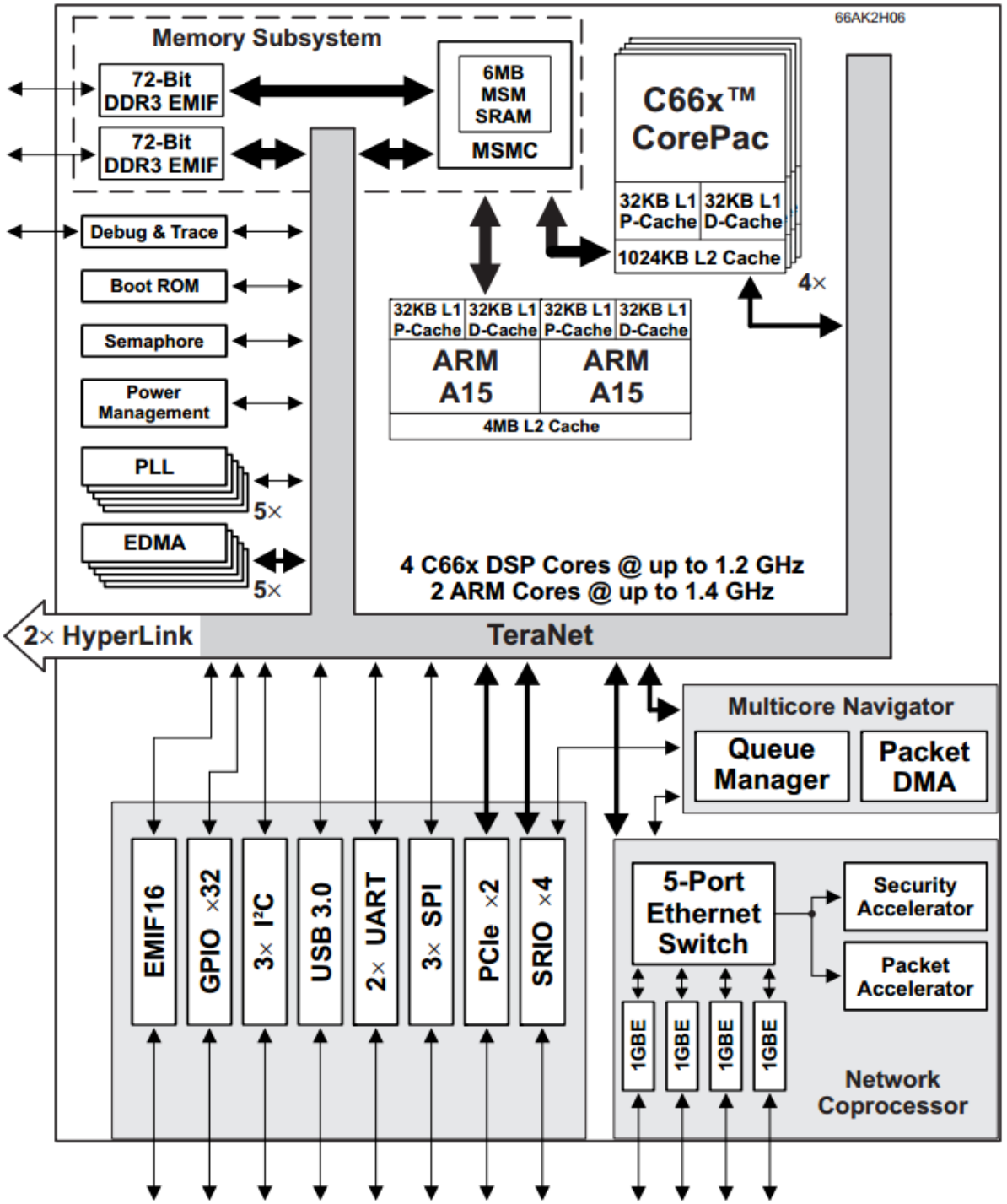
Power networking

4 ARM A15

2 ARM A15

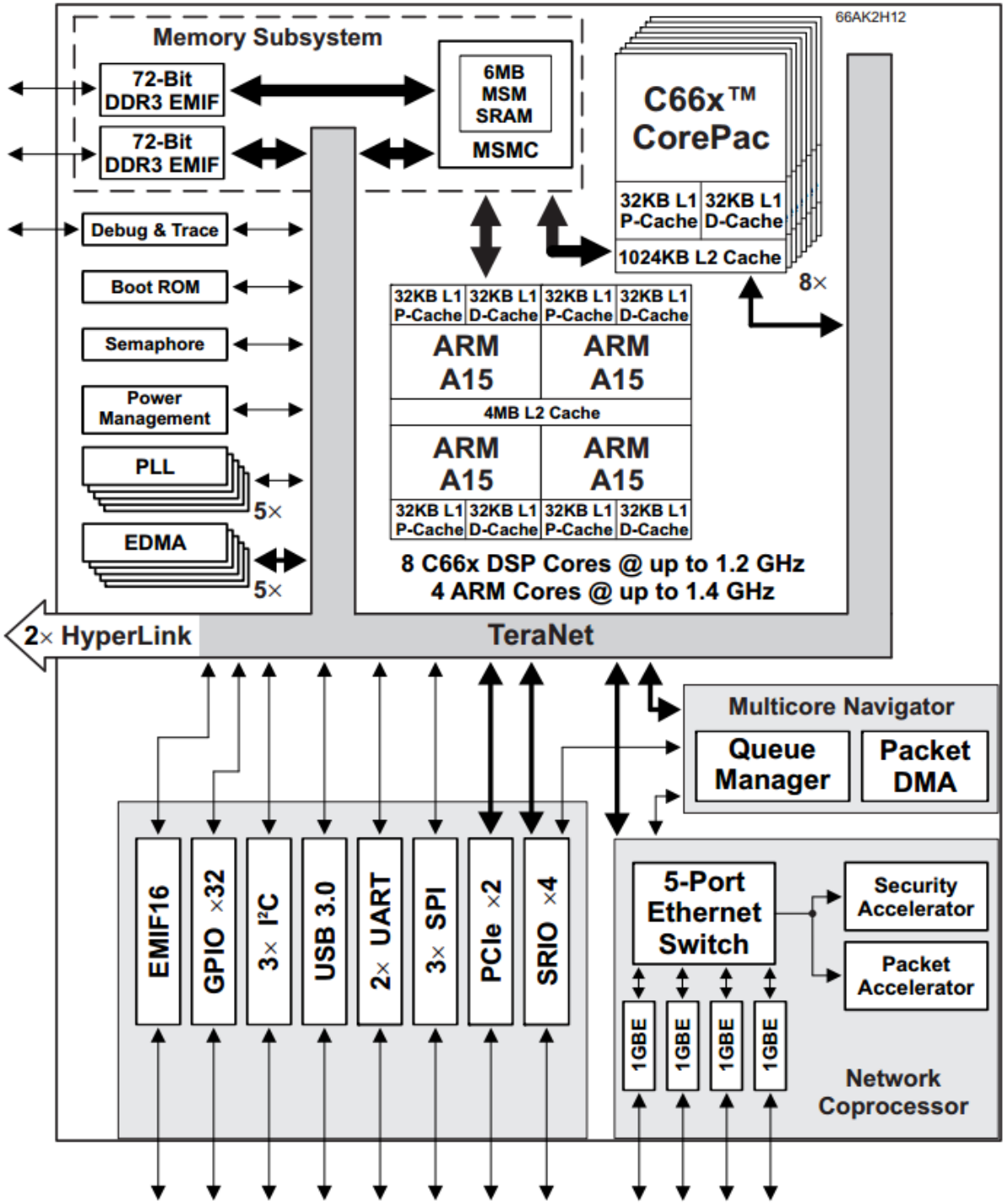
Cloud infrastructure
Networking control plane
Routers
Switches
Wireless transport
Wireless core network
Industrial sensor networks

And many more…



66AK2H06 Functional Block Diagram

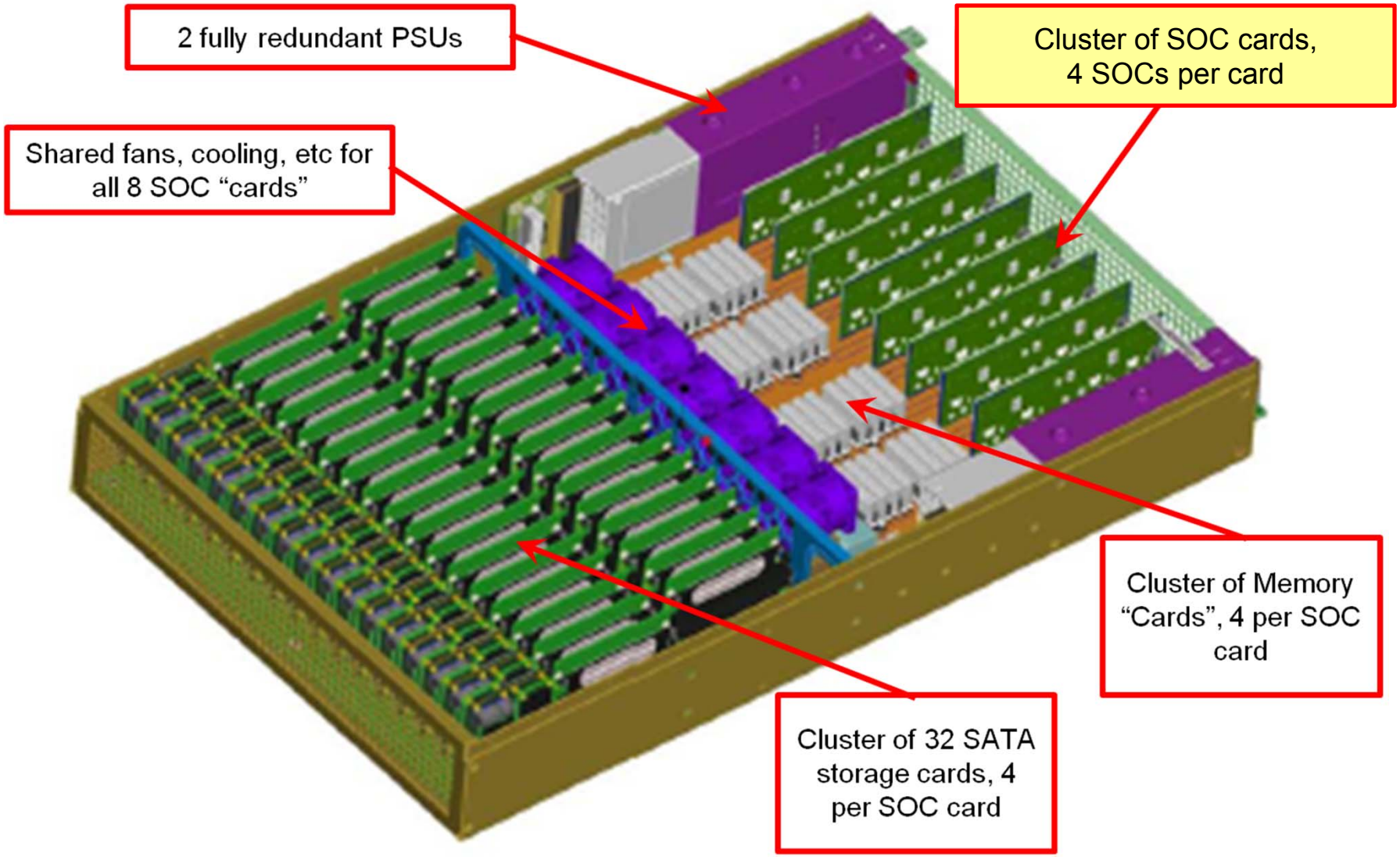
Texas Instruments



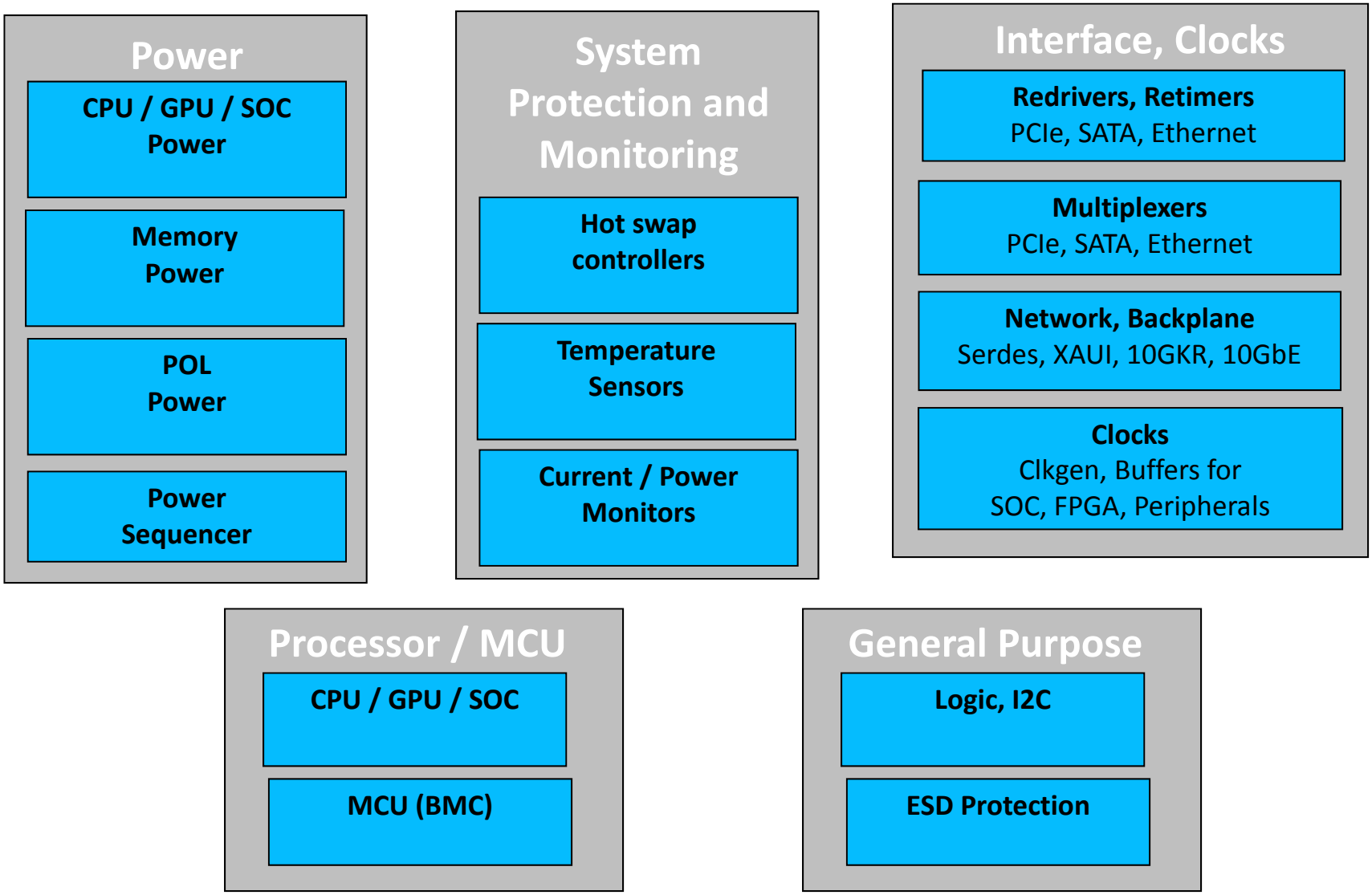
66AK2H12 Functional Block Diagram

Texas Instruments

Microserver Concept Sketch



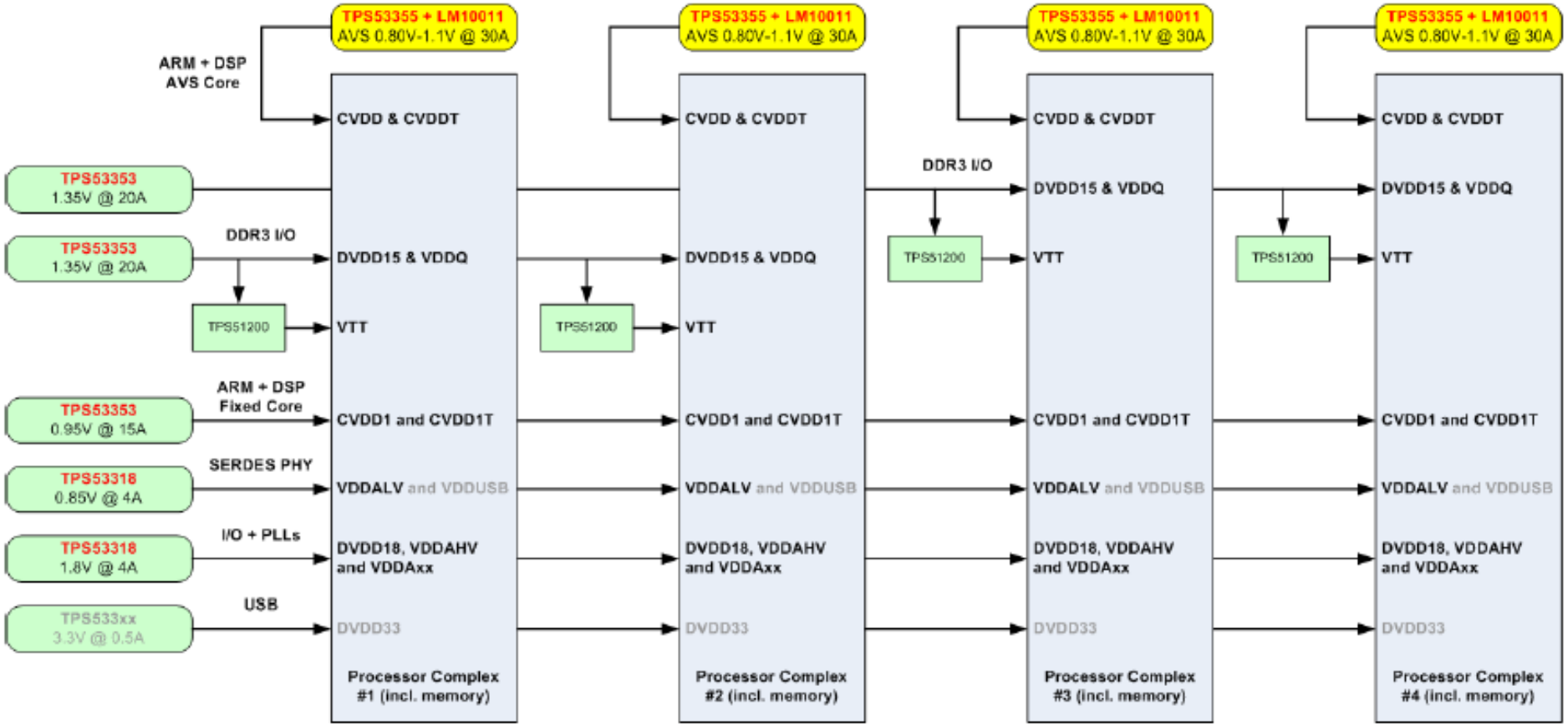
Microserver SOC Card Subsystems



Power Solutions for

SOC Core and Aux Rails

66AK2H12 SOC Power Map



TPS533XX

8A/14A/20A/30A Sync Buck Converter with Eco-Mode

Light Load

Features

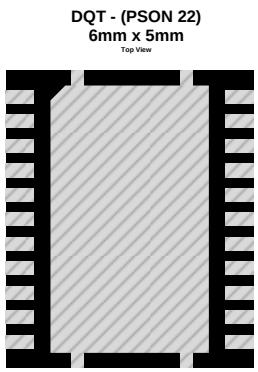
- V_{IN}: 4.5V to 18V
- V_{OUT}: 0.6V to 5.5V
- 0.8% (typ) 0.6V Reference
- D-CAP™ Mode - 100ns Transient Response
- Built-in LDO
- Dedicated EN Input and Power Good Output
- 8 Selectable Frequency Setting
- 1/2/4/8ms Selectable Internal Softstart
- OVP/UVP/OTP with Programmable OCP
- Supports Pre-Biased Start-Up

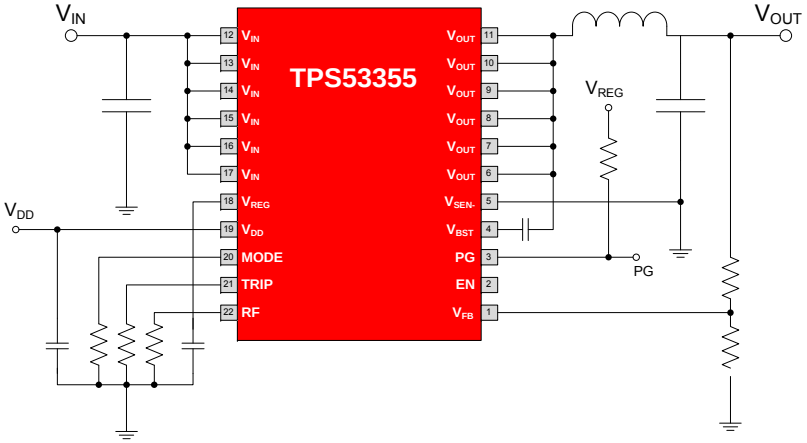
Benefits

- Directly convert from 12V
- Supports the most common rail voltages
- Improves accuracy at point of load
- No loop compensation and save output caps
- No external bias voltage required
- Applications requiring sequencing
- Efficiency and cost optimization
- Sequential start-up to reduce in-rush current
- Load is fully protected
- Soft start-up over pre-biased output

Applications

- Servers
- Storage
- Embedded PCs, POS Terminals
- Switches, Routers





Pin to Pin Compatible!!!

Texas Instruments

Top 10 Reasons To Use TPS53318/19/53/55

- Best in class efficiency
- Save output caps, least BOM cost
- Insensitive to output capacitor type@value
- Easy design, no compensation
- Single rail input
- Small quiescent current and high efficiency
- Support Light Load, seamless DCM/CCM transition
- Upgrade designs from discrete controller TPS53219 with the same external components
- Fully protected: OVP/UVP/OTP and thermal and Rds,on compensated OCP with tight tolerance
- Pin to Pin compatible: 30A@TPS53355, 20A@TPS53353, 14A@ TPS53319 and 8A@TPS53318

DSP Power Requirements and LM10011 Benefits

Requirements

- **VID interface for TI Keystone DSP power solution**
  - *Dynamic control of DSP power consumption and thermals*
- **A cost effective analog solution for DSP power**
  - *Instead of expensive digital controller*
- **Support both 4-pin 6-bit and 4-pin 4-bit VID patterns**
  - *For both Nyquist DSP and Gaia ASIC*
  - *For NSN Flexi 3.5 and Flexi 4 baseband processing*
- **High current accuracy (±1%) within full temperature range**
- **Adjustable IDAC output current during startup**

Benefits

- **LM10011 is recognized as the "Go-To" solution for TI DSP power**
- LM10011 allows customer to select DSP power converter within TI's wide analog product portfolio
- Reduce design risk and time line for DSP board solution
- Higher current accuracy to reduce power dissipation
- **Adjustable IDAC current to improve reliability during power up**
- Can support both DSP and ASIC power requirements

The most flexible DSP power solution in industry!

- **LM10011** is the only VID controller to fully support 6-bit (Nyquist DSP) and 4-bit (Gaia ASIC) VID interfaces and patterns
- The only other solutions are microprocessor VR and full digital control – which either result in higher cost, less flexibility, or both

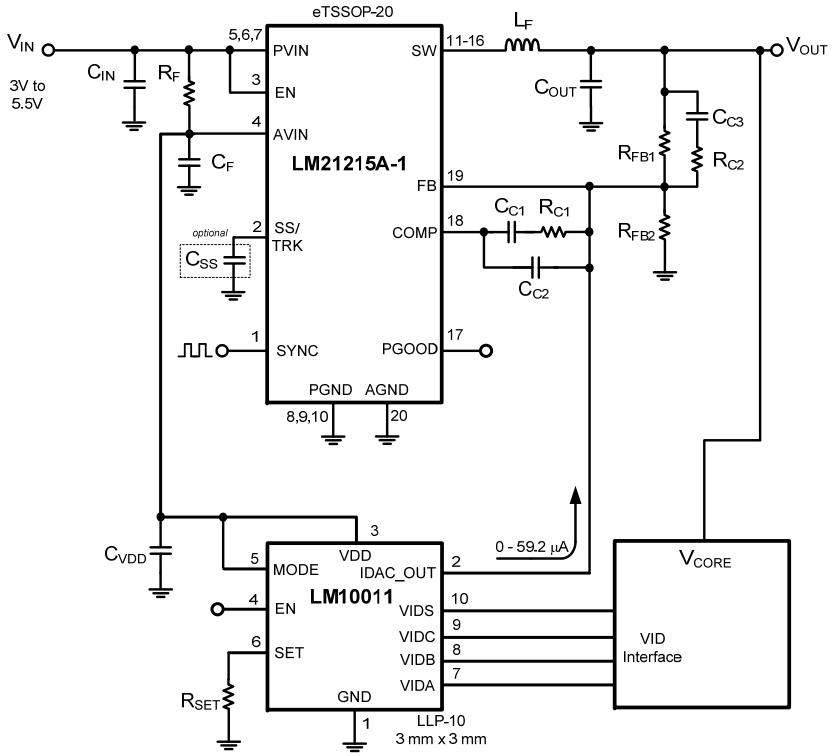
Specifications	LM10011	TPS40197	UCD9244	ISL6314	MAX17409
VID Bits	4-bit or 6-bit	4-bit only	4-bit, 6-bit or 8-bit	6-bit only	6-bit only
Output Voltage Resolution (mV)	I_{DAC_OUT} (0~59.2 μA) x R_{FB1}	20	N/A	12.5	12.5
Function	VID controller	VID + Voltage Controller	VID + Voltage Controller	VID + Voltage Controller	VID + Voltage Controller
Voltage Regulation Scheme	Support any control mode	Voltage mode	Fully digital	APA +APP (Current Mode with nonlinear transient control)	Constant ON-time

- Fit different applications
- Adjustable via ext R value
- Wide application range, flexible to select control mode
- Simple function, low system risk

LM10011 VID Voltage Programmer

Features

- Compatible with Nyquist DSP SmartReflex Power Management
- Works with any POL having Rfb adjust
- **Pin selectable VID interfacing**
  - 4 pin parallel VID inputs
  - 4-pin/6-bit VID inputs
- Input voltage range: 3V to 5.5V
- Precision current DAC connects to the feedback node of an external regulator to provide output voltage control
- **1.0% DAC output current accuracy**
- **Resistor settable default IDAC output**
- Precision enable to support custom UVLO
- DFN-10 Package (3mm x 3mm)
- -40 to 125°C operating temperature



Applications

- Telecom DSP for Baseband Processing
- TI Nyquist DSP Family

Availability

- Samples: May 2012
- Production: Q4 2012

TPS51200

3A Source-Sink DDR Termination Regulator

Features

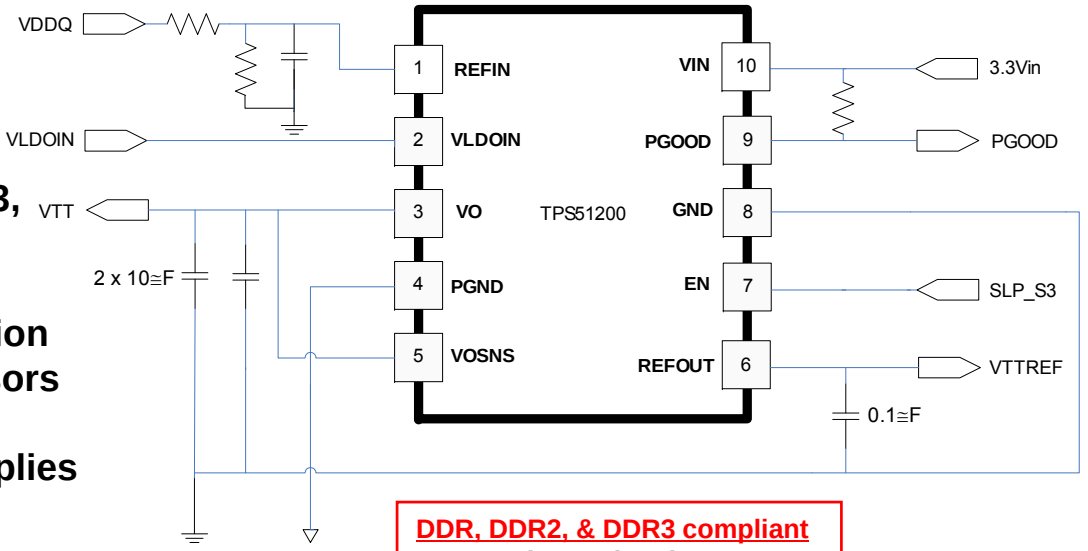
- Requires only 20uF of ceramic output capacitance
- Direct interface to S3 and sensing of S5 control signals
- Supports high-Z in S3 and soft-off in S5
- LDO input can be reduced to 1.2V
- SS, UVLO, OCL and thermal shutdown
- Enable input and Power Good output
- 10-pin SON package

Benefits

- Lower cost and size than competing parts requiring 600uF or more of electrolytic capacitance
- Ease of use
- Fewer external components and lower cost
- Lower power dissipation
- System protection
- Controlled turn-on and monitored output regulation
- Enables small form factor designs

Applications

- DDR, DDR2, DDR3, and low-power DDR3/DDR4 VTT Memory Termination
- Graphics Processors
- Core Supplies
- Chipset/RAM supplies as low as 0.5V



Low VIN Requirement
2.375V to 3.5V

PGOOD Output
Open drain Output to indicate VTT is within regulation

VTTREF sink and source
+/- 10mA

DDR, DDR2, & DDR3 compliant
Post package trimming to meet any DDR3 V_{TT} tolerance spec

Texas Instruments

TPS51216

Complete DDR2, DDR3 and DDR3L Power Solution

Features

Synchronous Buck Controller (VDDQ)

- Conversion Voltage Range: 3 V to 28 V
- D-CAP™ Mode for Fast Transient Response
- Selectable 300 kHz/400 kHz
- Optimized Efficiency at Light loads
- Supports Soft-Off in S4/S5 States
- OCL/OVP/UVP/UVLO Protections

2-A LDO(VTT), Buffered Reference(VTTREF)

- 2-A (Peak) Sink and Source Current
- Thermal Shutdown
- 20-Pin, 3 mm × 3 mm, QFN Package

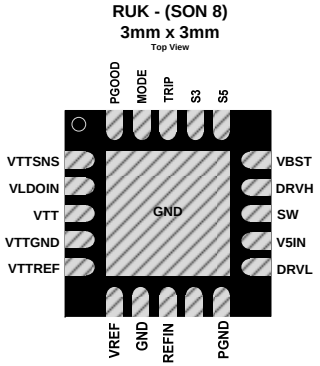
Benefits

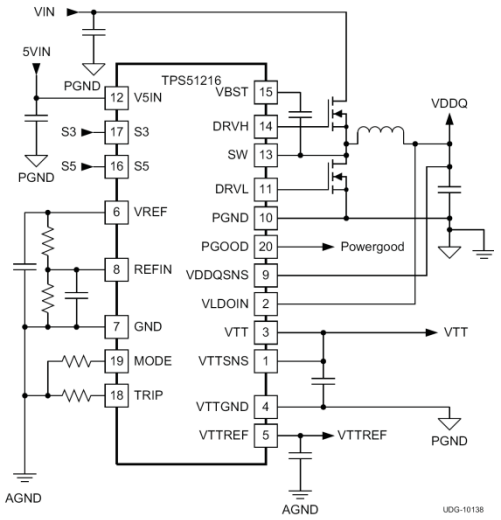
- Wide range of input voltages
- No loop compensation makes easier to use
- Design flexibility
- Designs requiring High Efficiency at light loads
- Eliminates Pre-Bias issues
- Full suite of protection

- Compatible with both DDR2, DDR3 and DDR3L
- Built in protection
- Thermally enhanced packaging

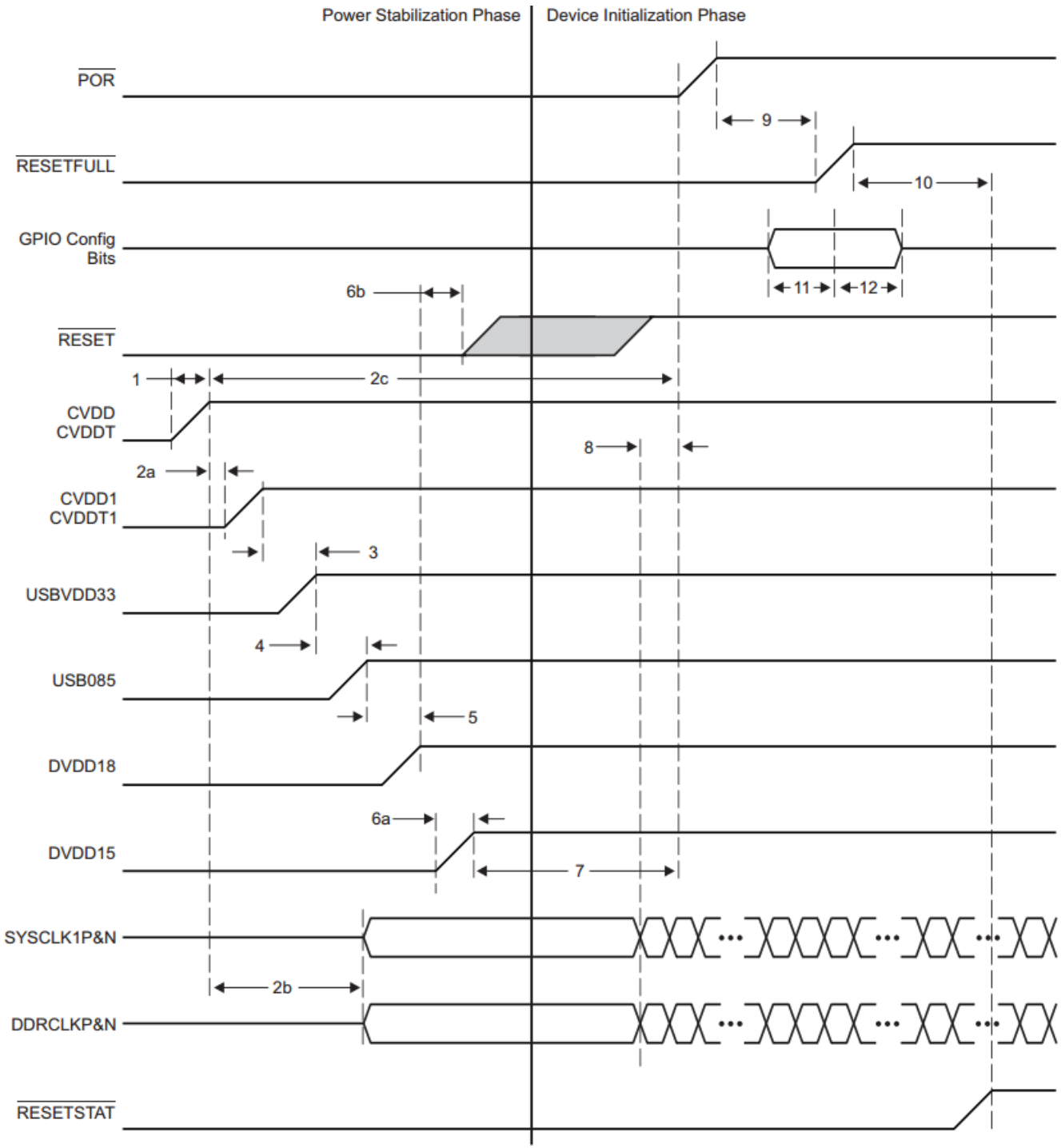
Applications

- DDR2/DDR3/DDR3L Memory Power Supplies
- SSTL_18, SSTL_15, SSTL_135 and HSTL Termination





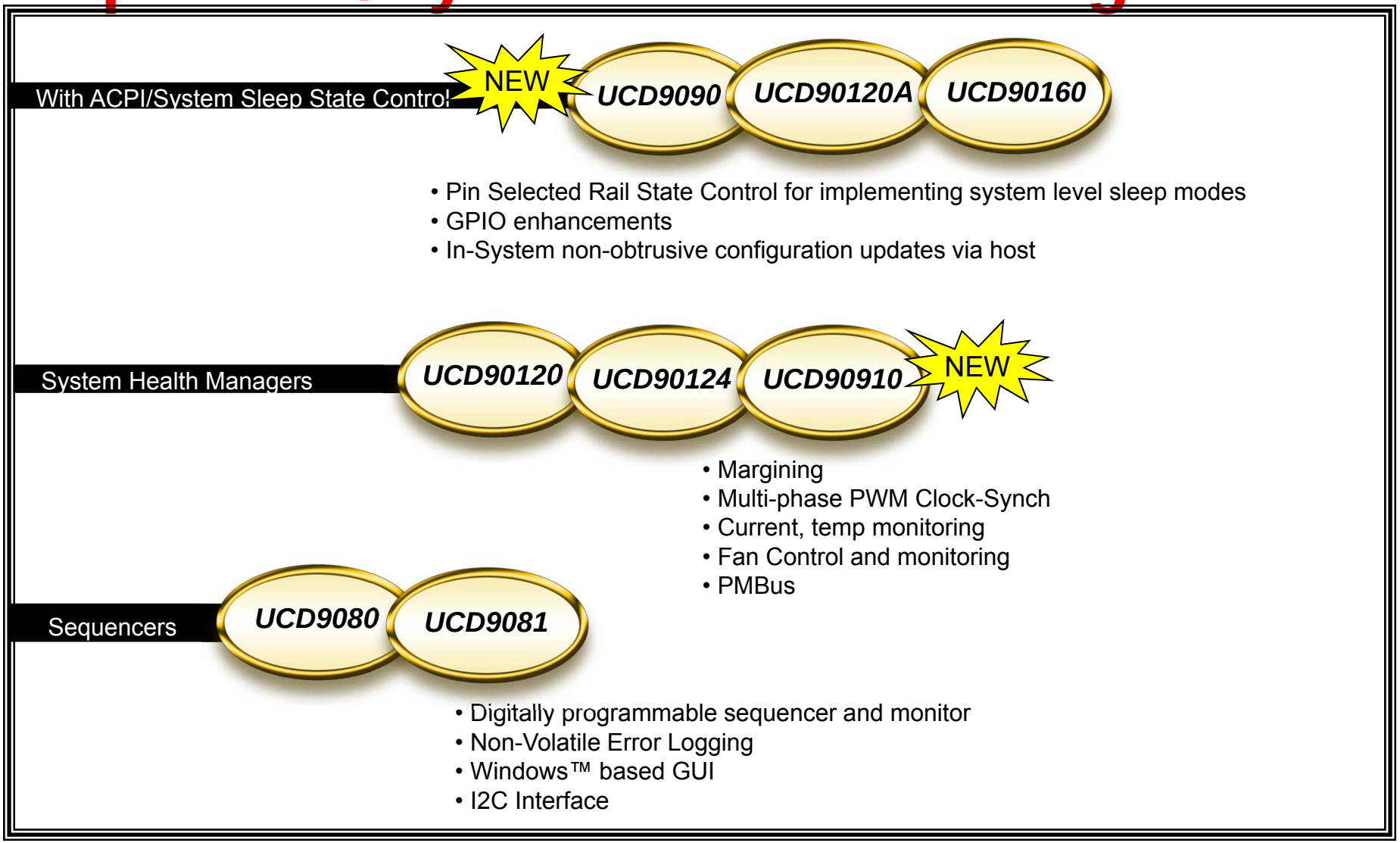
UCD9K Series
Power Sequencing Solutions



Power Sequence for 66AK2H12

Texas Instruments

Sequencer/System Health Managers



UCD9090: 10-Rail Sequencer and System Health Monitor with ACPI System Sleep State Control

Features

- **Sequence, Monitor, and Margin up** to 10 Rails
- Independent Turn and Turn off dependencies
- Dependencies on time, parent rails, GPIs, and I2C commands
- Flexible GPIO configuration with BOOLEAN Logic capability
- 11 ADC Inputs with user settable scale factors for detecting voltage (OV/UV), current(OC/UC), or temp faults
- 6 optional comparators for fault response in < 80 us
- Respond to faults by configuring retries, shutdown delays, re- sequencing and groups of rails to shutdown
- **Non-Volatile fault and peak logging**
- Simultaneously **margin/trim** up to 10 rails using PWM outputs and I2C commands
- Up to 8 multi-phase PWM clock outputs
- Easy-to-use **Fusion Digital Power Designer GUI**
- JTAG and PMBus interfaces provide flexible options for in-system host communication and configuration
- **Pin Selected Sleep State control for use with ACPI or similar system power specifications**

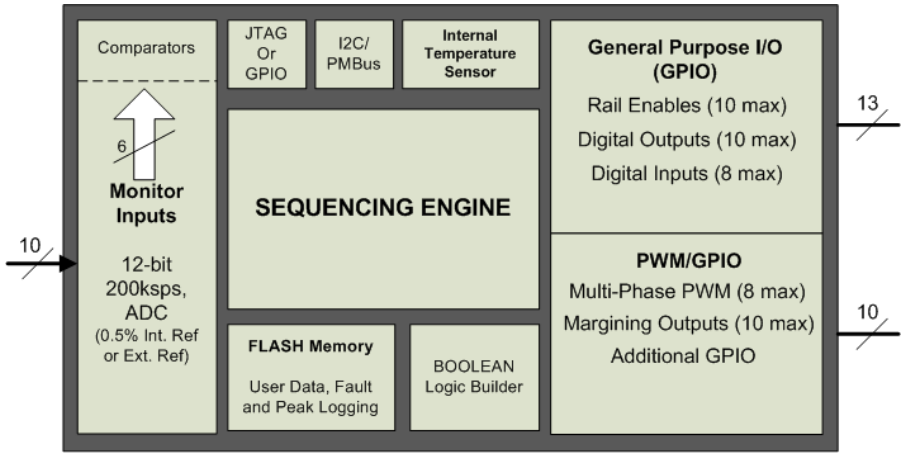
Benefits

- Flexibility sequencing requirements supports most possible sequencing scenarios
- Detect power supply warnings and faults and store to non-volatile memory for failure analysis
- Monitor voltage, current and temp in actual system units to eliminate host software scaling
- Closed-Loop Margining for corner testing of power supplies allows designers to identify possible system reliability issues
- Multi-phase PWM outputs eliminate need for separate chip to synch switch mode power supplies
- ACPI sleep state control allows host to shut down rails that are not in use and conserve system power
- TI's ***Fusion Digital Power GUI*** eliminates need to write code

Applications

- Server/Storage Systems
- Communication Infrastructure
- Industrial/ATE
- Embedded Computing

Samples 1Q11
Production 3Q11



48-pin QFN

Texas Instruments

Sequencer Portfolio Selection Guide

	UCD90160	UCD90120	UCD90120A	UCD90124	UCD9090	UCD90910	UCD9081
# Rails Sequenced	16	12	12	12	10	10	8
# of Monitor Inputs	16	13	13	13	11	13	8
ADC Ref Accuracy	0.5% Internal	0.5% Internal	0.5% Internal	0.5% Internal	0.5% Int ot Ext	0.5% Internal	External
Voltage Margining*	10	10	10	10	10	10	
Fan Control*	N/A	N/A	N/A	4	N/A	10	N/A
Multi-phase PWM clock outputs*	8	N/A	8	8	8	8	N/A
ACPI Sleep State Control	Yes	No	Yes	No	Yes	No	No
Current and Temp Monitor Scaling	No	Yes	Yes	Yes	Yes	Yes	No
NV Fault Logs	8	16	TBD	10	15	20	8
Other NV Logging	Peaks, Resets, Run-time clock	Peaks, Resets, Run-time clock	Peaks, Resets, Run-time clock	Peaks, Resets, Run-time clock	Peaks, Resets, Run-time clock	Peaks, Resets, Run-time clock	N/A
Max GPI/GPO*	8/16	8/12	8/12	8/12	8/10	8/10	0/4
Internal Temp Sensor	Yes	Yes	Yes	Yes	Yes	Yes	No
Communication and Programming I/F	PMBus/I2C, JTAG	PMBus/I2C, JTAG	PMBus/I2C, JTAG	PMBus/I2C, JTAG	PMBus/I2C, JTAG	PMBus/I2C, JTAG	I2C
Watchdog Timer	Yes	Yes	Yes	Yes	Yes	Yes	No
Package Type (size)	64-pin QFN(9x9)	64-pin QFN(9x9)	64-pin QFN(9x9)	64-pin QFN (9x9)	48-pin QFN (7x7)	64-pin QFN (9x9)	32-pin QFN (5x5)
Availability	Production	Production	Production	Production	Production	Production	Production

* Table shows the max number of each feature supported by each device. For example, the UCD90124 has 12 PWM pins used as any combination of margining, PWM, fan control, or GPIO up to the max listed. See data sheets for details.

Hot swap controllers,

Current / Power monitors

And Temperature Sensors

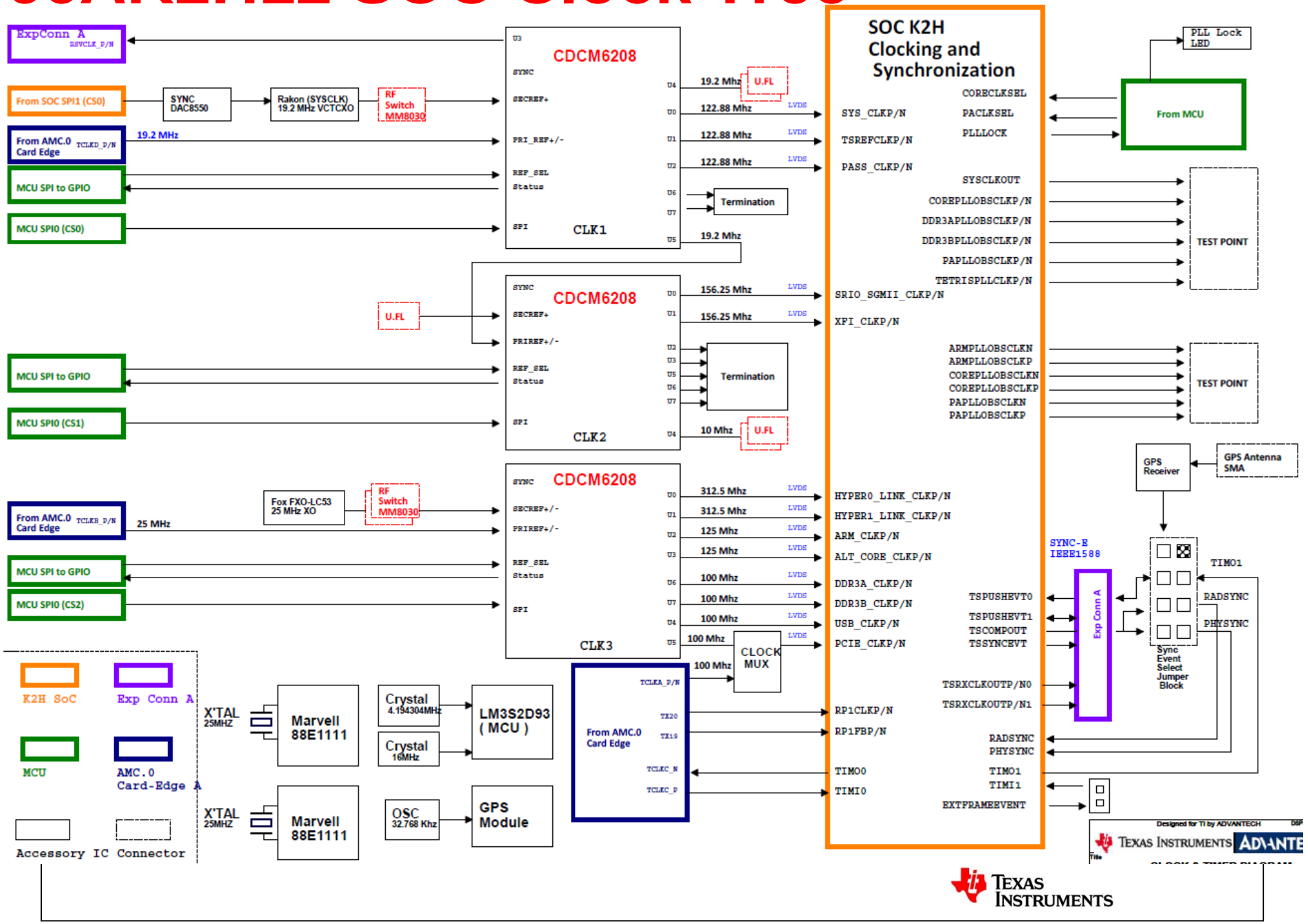
MCUs for

System Health Monitoring

Clocks

www.ti.com/clocks

66AK2H12 SOC Clock Tree



Keystone DSP suggests ....

3.5 Clocking and Clock Trees (Fan out Clock Sources)

For systems with multiple high performance DSP processors, it is not recommended that a single clock source be used (single output only). Excessive loading, reflections, and noise will impact performance. Instead it is recommended that differential clocking be used which include a differential clock tree.

Texas Instruments has developed a specific line of clock sources to meet the challenging requirements of today's high performance DSPs. In most applications the use of these specific clock sources eliminates the need for external buffers, level translators, external jitter cleaners, or multiple oscillators.

A few of the recommended parts include:

- CDCM6208*- Single PLL, 8 Differential Output Clock Tree with 4 Fractional Dividers

TEXAS INSTRUMENTS

Application Report
SPRABI2—November 2010

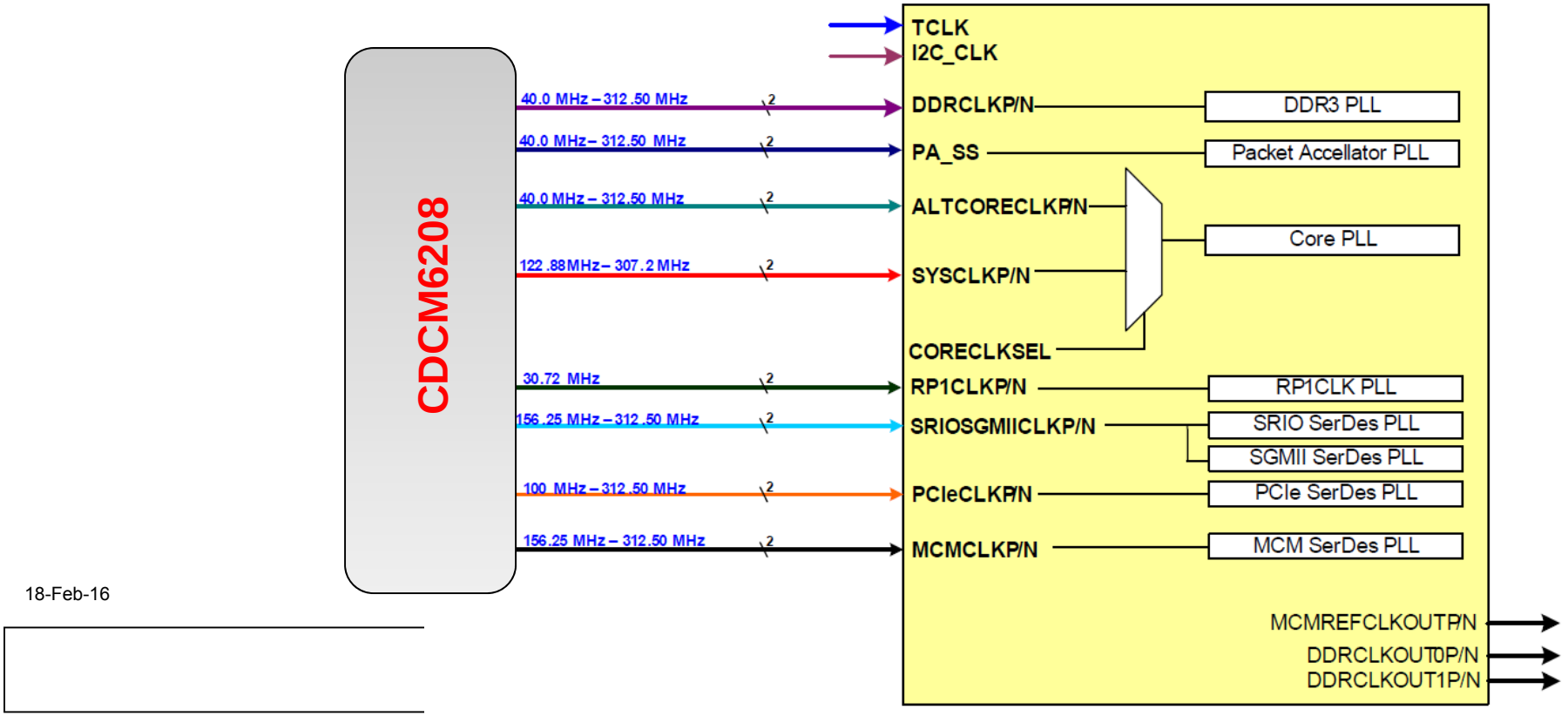
Hardware Design Guide for KeyStone Devices

High-Performance and Multicore Processors

Abstract

This document describes hardware system design considerations for the KeyStone family of digital signal processor. This design guide is intended to be used as an aid during the development of respective application hardware. Other aids including but not limited to device data sheets and explicit collateral should also be used.

Figure 4 KeyStone DSP Reference Clocks

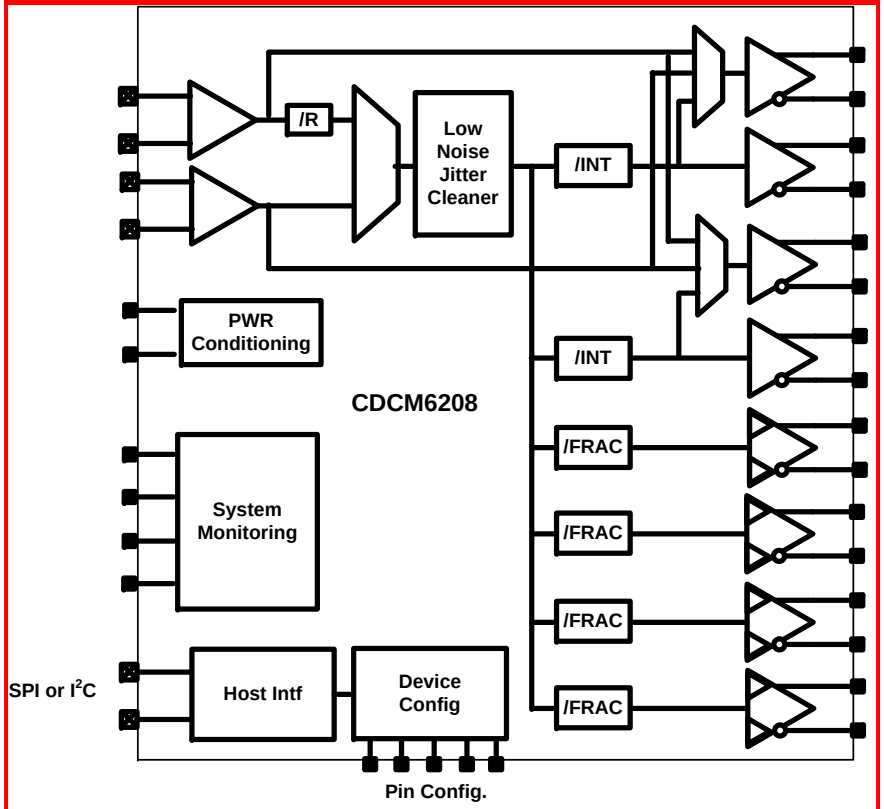


CDCM6208: Low Jitter Clock Generator

Superior Performance with Low Power & Flexible Frequency Planning

Features	
RMS jitter @ 156.25MHz	265 fs (12kHz – 20MHz) 25 MHz Crystal as reference
Max f_{OUT}	800 MHz
Output Format	LVDS, CML, LVPECL, HCSL or LVCMOS
Typical Power Consumption	< 0.5 W (best in the market)
Supply Voltage	1.8 V, 2.5 V and/or 3.3 V Allowing Mixed Supply Voltages
Total Number of Outputs	8 differential outputs. Up to 8 single ended
Input Reference Clocks	Crystal, XO, Single ended or Differential Clock
Multiple Clock Frequencies	4 Fractional dividers 2 Integer dividers
Independent Clock Domains	5

CDCM6208 Block Diagram



Ideal clock for TI-DSPs (Keystone)

In Production

Texas Instruments

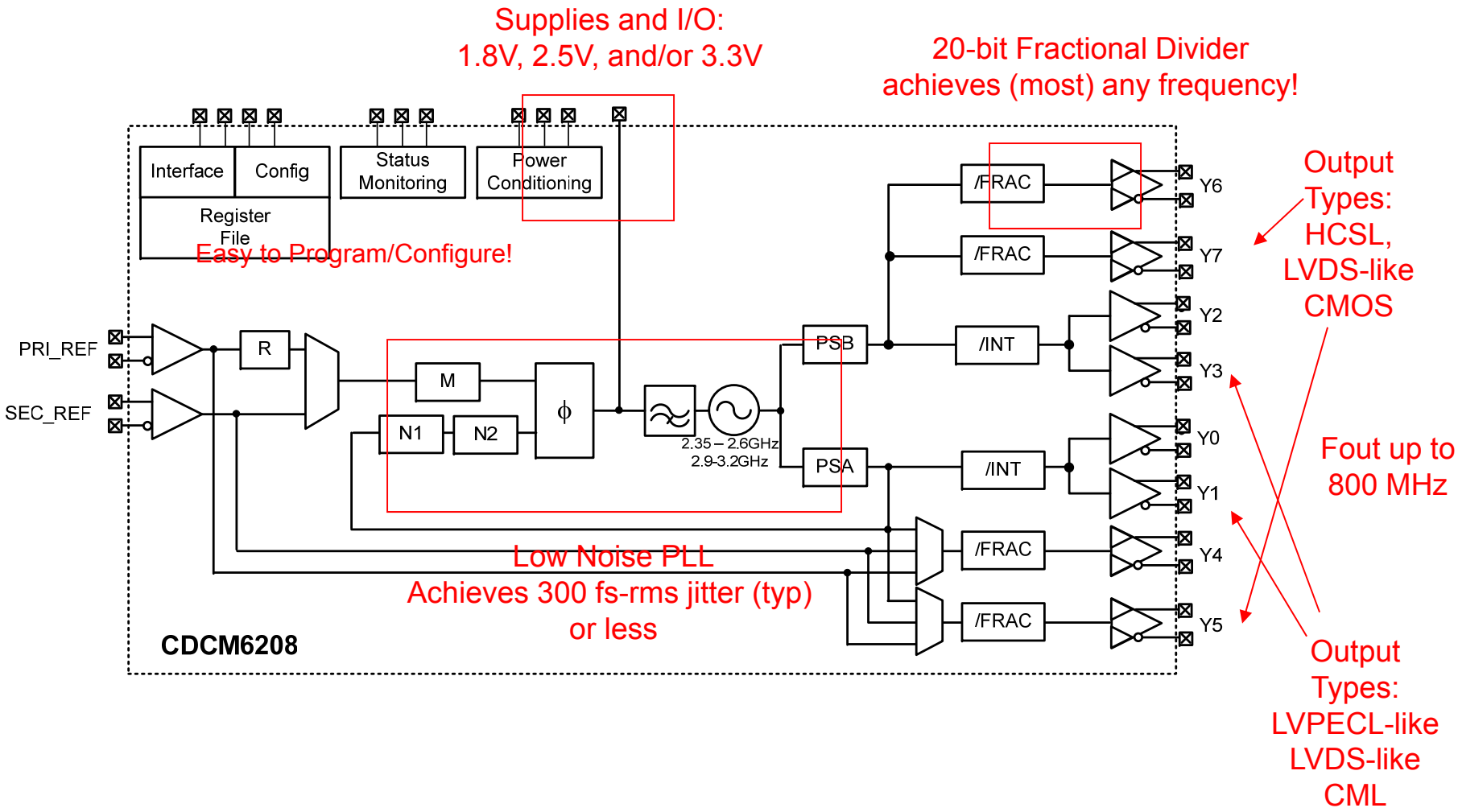
Jitter Budget Keystone DSP and CDM6208 actuals

integer & fractional output compliant to 10GbE

	Logic (NYQ)*	CDCM6208		Input Jitter spec NYQ (9) *	CDCM6208 measured	Trise / Tfall 3 *	Duty Cycle %	Stability *
SRIO_SGMII_CLKp SRIO_SGMII_CLKn (if SRIO is used)	LJCB or LVDS (1)	LVDS	156.25MHz	4ps RMS 56 ps pk-pk @ 1x10^{-12} BERT [1.875MHz to 20MHz single-pole filter bound] IEEE802.3ae spec page 280	**56ps pk-pk with unbound jitter; 44ps-pk-pk with bounded jitter**	50 – 350 ps2	45 / 55	± 100 PPM
SRIO_SGMII_CLKp SRIO_SGMII_CLKn (SRIO not used)	LJCB or LVDS (1)			8ps RMS 112 ps pk-pk @ 1x10E-12 BER7		50 – 350 ps2	45 / 55	± 100 PPM
PCIe_CLKp PCIe_CLKn	LJCB or LVDS (1)			4ps RMS 56 ps pk-pk		50 – 350 ps2	45 / 55	± 100 PPM
RPI_CLKp RP1_CLKn	LVDS	LVDS or PECL	30.72MHz (0-ppm)	4 ps RMS 56 ps pk-pk	**0.1ps RMS (10k-20M) 12ps pk-pk (DJ unbound)**	50 – 350 ps2	45 / 55	± 100 PPM
MCM_CLKp MCM_CLKn	LJCB or LVDS (1)			8ps RMS 112 ps pk-pk @ 1x10E-12 BER7		50 – 350 ps2	45 / 55	± 100 PPM
ALTCORE_CLKp ALTCORE_CLKn	LJCB or LVDS (1)			100 ps pk-pk		50 – 350 ps2	45 / 55	± 100 PPM
PA_SS_CLKp PA_SS_CLKn	LJCB or LVDS (1)			100 ps pk-pk		50 – 350 ps2	45 / 55	± 100 PPM
SYSCLKp SYSCLKn	LJCB or LVDS (1)	LVDS or PECL	122.88MHz (0-ppm)	2 ps RMS (28 ps pk–pk), period5 [10k-20M]	**0.3ps RMS (10k-20M) 13ps-pp (DJ unbound)**	50 – 350 ps2	45 / 55	± 100 PPM
DDR_CLKp DDR_CLKn	LJCB or LVDS (1)	LVDS	66.67MHz (-0.02ppm or +55 ppm)	2.5% of DDRCLK output period (pk-pk)4 (which is 374ps-pp)	**0.98ps-rms (10k-20M) 32ps-pp DJ (10k-20M)**	50 – 350 ps2	45 / 55	± 100 PPM
FGPA 100MHz	CMOS	CMOS (1.8V, 2.5V or 3.3V)	100MHz (-0.1ppm or -33 ppm)		**1.1ps RMS (10k-20M) 6ps pk-pk DJ (10k-20M)**			± 100 PPM ??

CDCM6208

Block Diagram

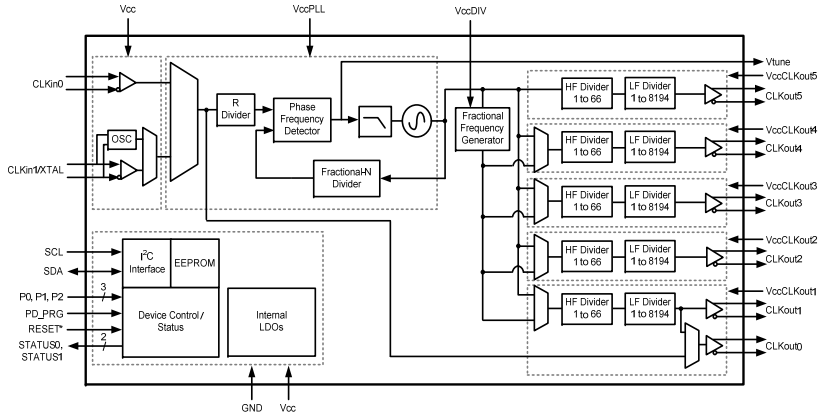


LMK03305: Any Freq Clock Generator

Ultra-Low Jitter Clocks Made Easy

Features	
RMS Jitter	<300 fs @ 156.25 MHz (12 kHz – 20 MHz) <100 fs @ 156.25 MHz (1.875 – 20 MHz)
Output Frequency	Any integer/fractional output from 1 to 850 MHz (250 MHz for HCSL/CMOS)
Output Format	Programmable as LVPECL, CML, LVDS, HCSL, or 2x CMOS
Input Format	Crystal input: 10 to 40 MHz CMOS input: 10 to 250 MHz Differential input: 1 to 300 MHz
Spread Spectrum	Available on each output (max. +/- 15%), with programmable triangular modulation.
Interface	I2C with on-chip EEPROM
PSRR	- 70 dBc
Power Supply	3.3V Core, 2.5V/3.3V Independent Output Supplies

Block Diagram



- Any Frequency, Any Format, 5 Differential or 11 Single Ended Programmable Outputs
- Integrated Level Translator
- High PSRR
- Smaller Size (6x6, 36 pin QFN)

Lowest Jitter & Spurs in Integer & Fractional Divider Mode

Samples in Q1 2013

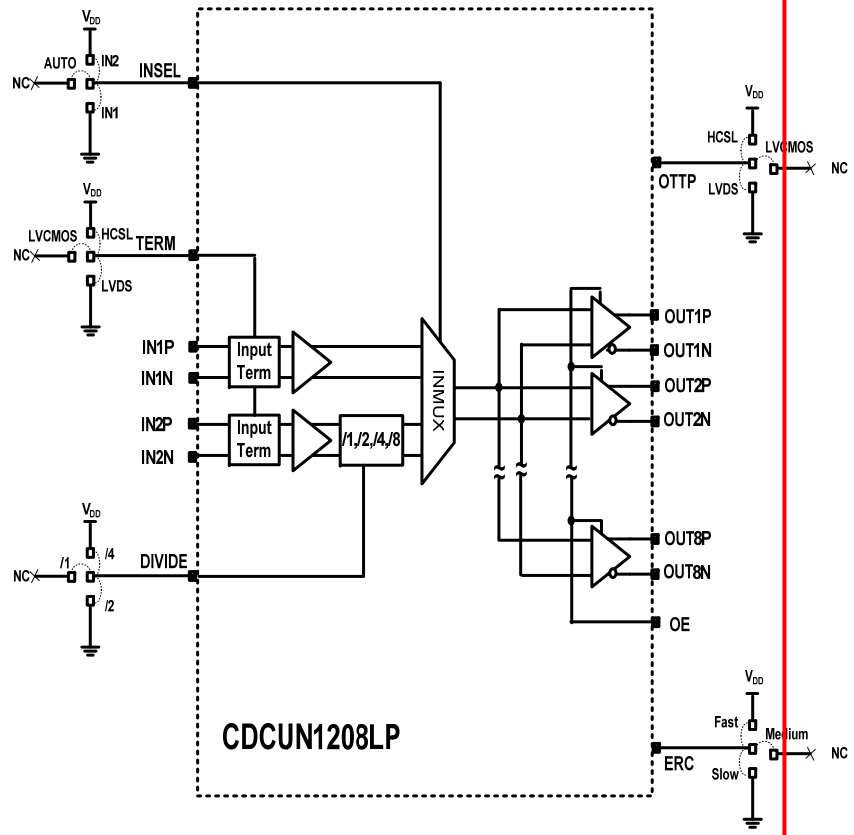
Texas Instruments

CDCUN1208LP

Ultra Low Power Universal Fan-out Buffer PCIE gen2, gen3 clock buffer

Features	
Additive jitter	200 fs (12k to 20M Hz) @ 100 MHz LVDS PCIE gen2, gen3 support
Supply Current	10mA per output @100MHz LVDS
Supply Voltage	1.8V, 2.5V or 3.3 V
Max Frequency	400 MHz
Universal Input Buffers	LVPECL, LVDS, CML, SSTL, HSTL, and LVCMOS input
Universal Output signaling	HCSL, LVDS, LVCMOS pin selectable Internal termination
Slew Rate Control	Slow, Medium and Fast Edge Rate Settings Different edge rates for each I/O
Max Output Skew	50 ps

CDCUN1208LP Block Diagram

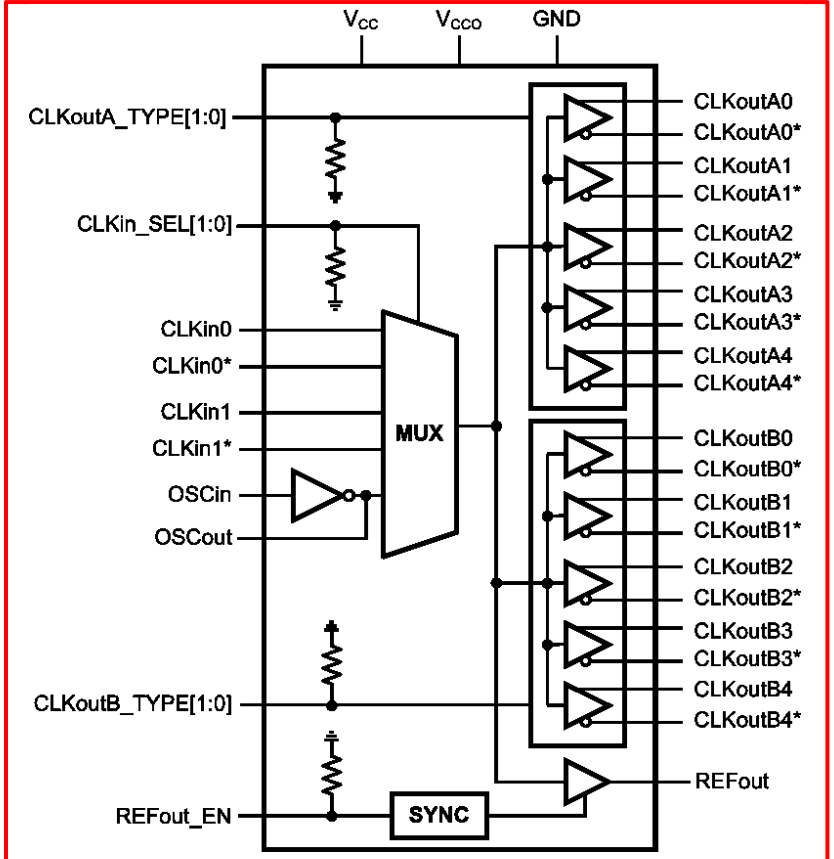


LMK00301

10 Universal Fanout Buffer / Level Translator

Features	
Additive jitter	45 fs (12k to 20M Hz) @ 156.25 MHz LVPECL
Max Frequency	3.1 GHz
Universal Input Buffers	LVPECL, LVDS, CML, SSTL, HSTL, and LVCMOS input
Crystal Input	10 to 40 MHz
Two Output Banks	Each bank can be configured to LVPECL, LVDS, HCSL, Hi-Z
Max Output Skew	50 ps
Core Supply Output Supply	3.3 V 3.3 V or 2.5V

Block Diagram



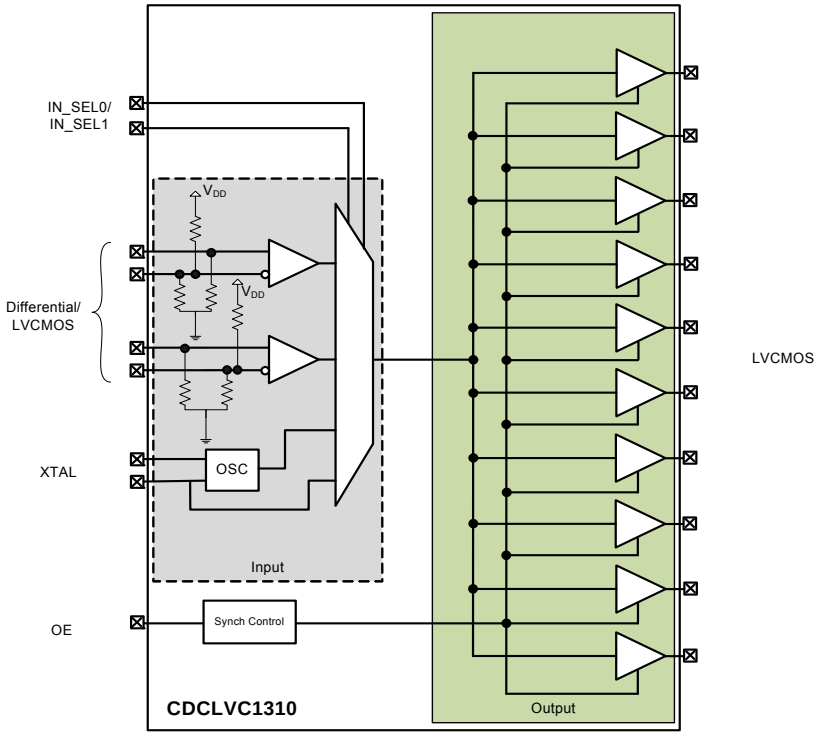
✓ Lowest Additive Jitter, Extreme Flexibility, Integrated LDOs, High PSRR

CDCLVC1310: Low-Noise Clock Buffer

10-Output LVCMOS Buffer / Level Translator

Features	
Additive jitter	25 fs_{RMS} (12k to 20 MHz) @ 156.25 MHz LVPECL
Output Frequency	200MHz
Noise Floor	-169 dBc/Hz (25 MHz Crystal input)
Universal Input Buffers	LVPECL, LVDS, CML, SSTL, HSTL, and LVCMOS input
Crystal Input	8 to 50 MHz
Output Skew	30 ps (typ)
Core Supply Output Supply	3.3 V or 2.5V 3.3 V, 2.5V, 1.8V or 1.5V

CDCLVC1310 Block Diagram



Low Additive Jitter, Low Power & Level Translation

In Production

Texas Instruments

High Speed Interface

(PCIe, USB3, SAS, SATA, Ethernet)

and Serdes Solutions

www.ti.com/sigcon

www.ti.com/usb

www.ti.com/serdes

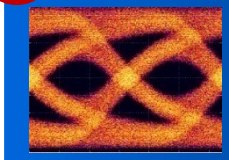
Enterprise, Infrastructure Systems

Interface Challenges

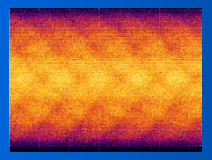
Doubling Data Rate,
Reach Remains Same

Signal / Noise Problem

1



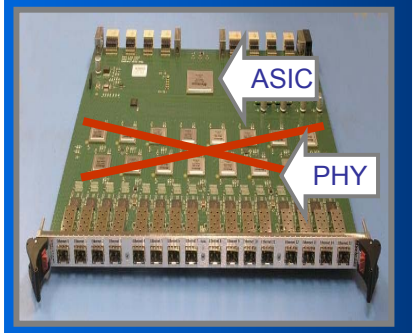
< 2006
(2.5 Gbps)



> 2009
(8 Gbps+)

20" FR-4 Trace

2



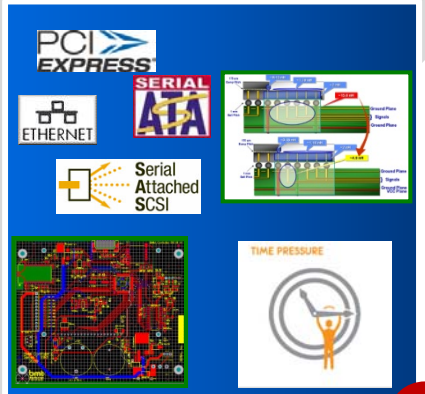
Shrinking CMOS Cells,
PHY Integration,

Jitter Problem

Higher Density,
Chassis Life Extension

Cross Talk Problem

3



4

Plethora of Standards,
Complex Designs

Time-to-Market Problem

Right Tool for The Right Job

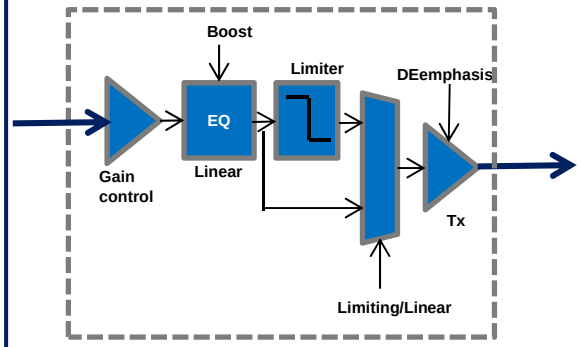
Analog IP Library – Goes up to 28 Gbps

BiCMOS SiGe Process Technology

3-Step Application Specific Products

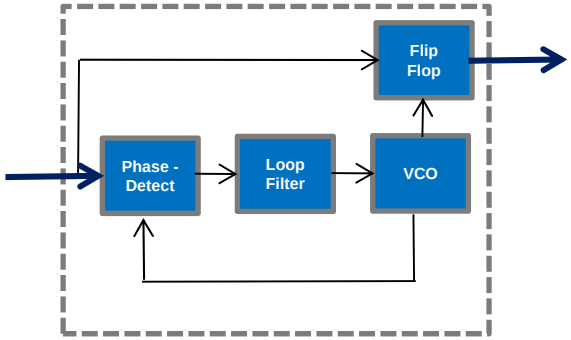
Unique Support Service

Equalization & De-Emphasis Driver



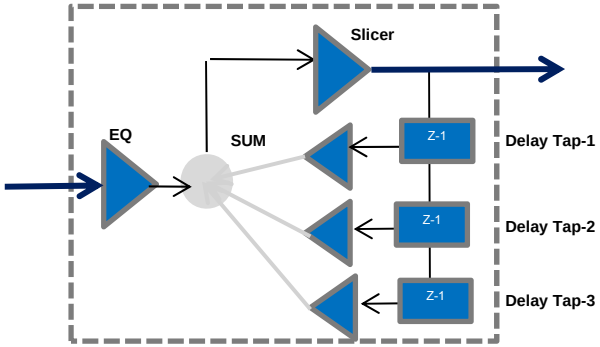
✓ Insertion Loss

Clock Data Recovery (CDR)



✓ Jitter

Decision Feedback EQ (DFE)



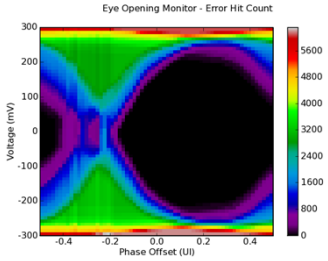
✓ X-Talk, Reflections

High Speed SigCon Portfolio – 3 Vectors

Pin Compatible Upgrade, Application Specific

BiCMOS SiGe Process Technology | **3-Step Application Specific Products** | **Unique Support Service**

Ease of Use Features



- ✓ *On chip diag – EyeMon, BERT*
- ✓ *Flow-thru package*
- ✓ *Single power supply*
- ✓ *No reference clock*

Signal Conditioning Function

Pin Compatible Upgrade

3. Adv Retimer – Retimer with DFE (Decision Feedback EQ)
2. Retimer – Repeater + CDR (Clock-Data-Recovery)
1. Repeater – Equalizer + De-Emphasis Driver

Channel/Port Configuration: 2, 4, 8, NEW! 16

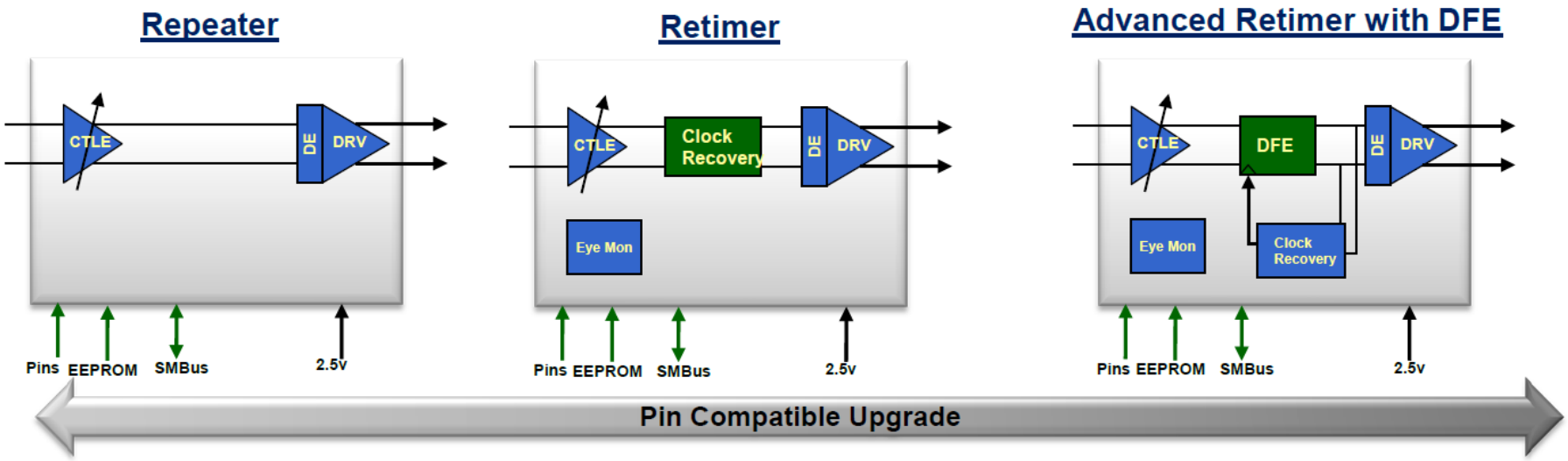
Protocol, Data Rate: 8.5G, 10G, NEW! 15G, 28G

ETHERNET, Serial Attached SCSI, fibre channel, PCI EXPRESS, SERIAL ATA, INFINIBAND, USB

Texas Instruments

3-Step Signal Conditioner Portfolio

Easy Pin Compatible Upgrade



Loss

Repeater

- EQ + De-Emphasis (DE) Driver
- DS100BR410 : Quad, Up to 10.3G
- DS100BR210/111 : Dual, Up to 10.3 G
- 55 mW/Chn power consumption

NEW!

Loss & Jitter

Retimer

- Adaptive EQ + CDR + DE Driver
- DS125RT410 : Quad, 9.8 to 12.5G
- DS110RT410 : Quad, 8.5 to 11.3G
- DS100RT410 : Quad, 10.3G / 1.25G
- 145 mW/Chn power consumption
- No reference clock required

NEW!

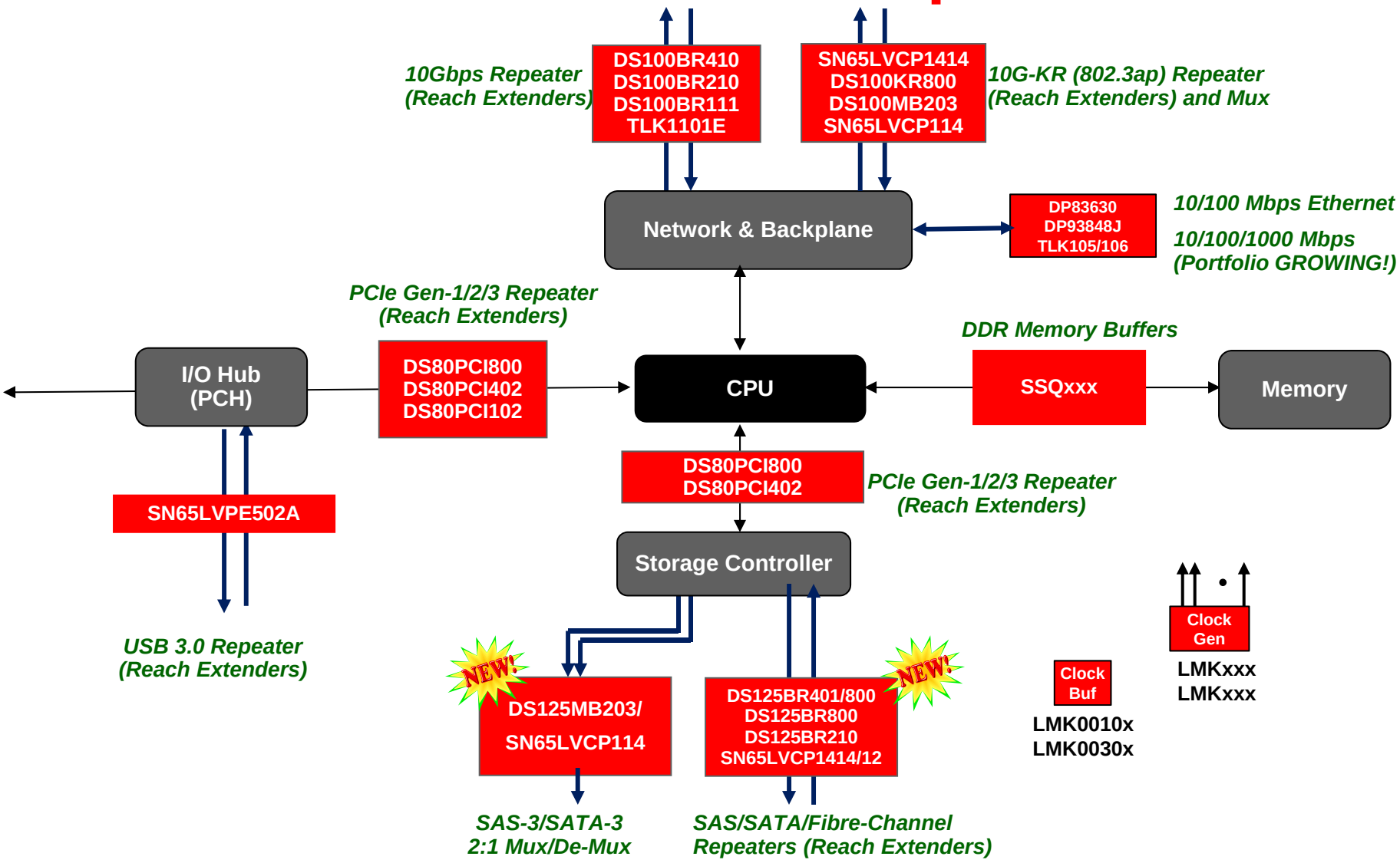
Loss, Jitter & X-Talk

Advanced Retimer

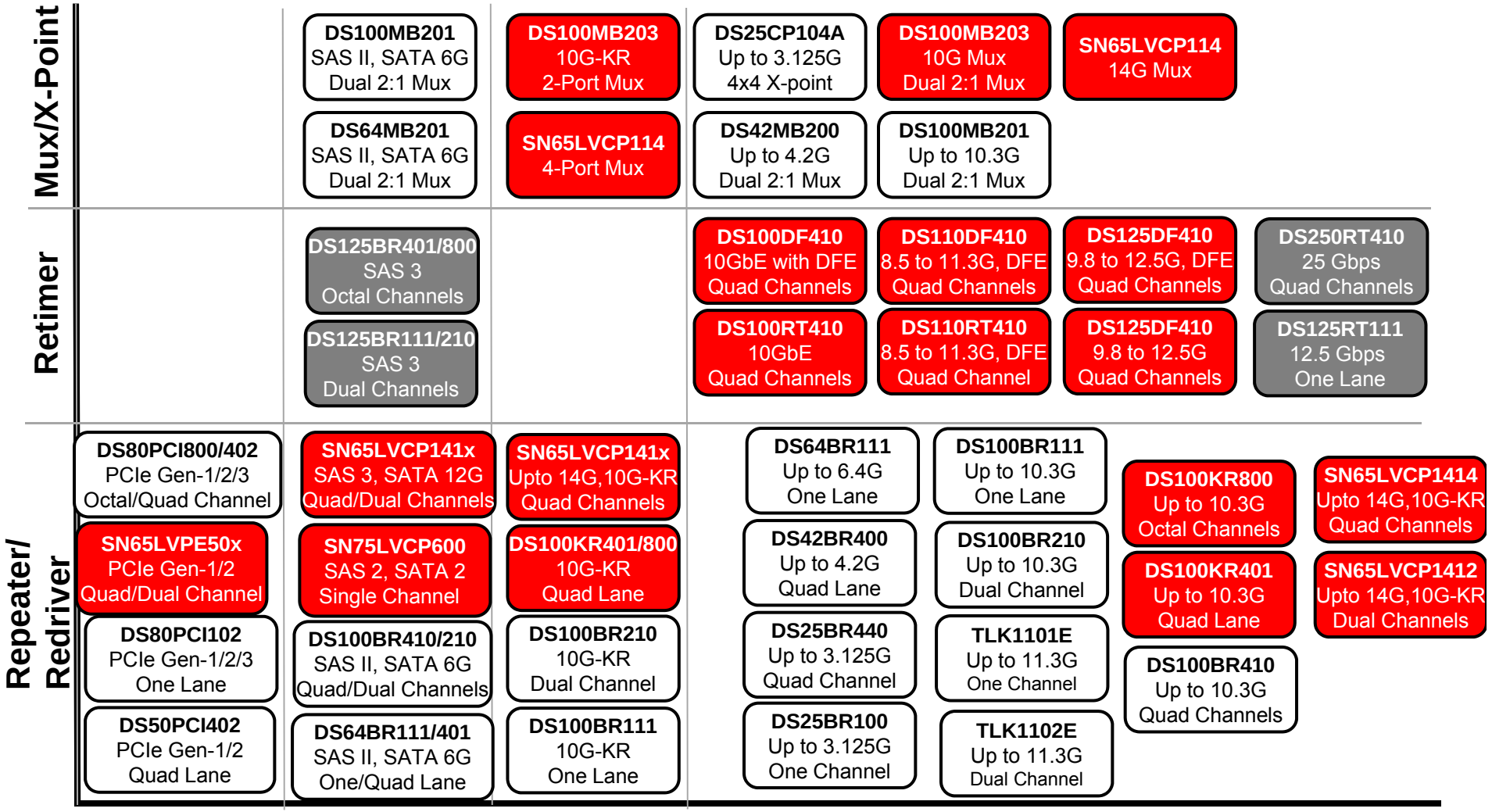
- Adaptive EQ + DFE + CDR + DE
- DS125DF410 : Quad, 9.8 to 12.5G
- DS110DF410 : Quad, 8.5 to 11.3G
- DS100DF410 : Quad, 10.3G / 1.25G
- 175 mW/Chn power consumption
- 5-Tap self-adapting DFE
- No reference clock required

Texas Instruments

Interface Solutions for Server, Storage, Network and Backplane



Signal Conditioning Solutions from TI



Products Highlighted in RED are New Arrivals, Dark Grey are In Development/Sampling

LANE/PORT = Bi-DIRECTIONAL, CHANNEL = Uni-DIRECTIONAL

PCIe - Repeaters

	DS80PCI800 (x16, x8 PCIe) DS80PCI402 (x4 PCIe)	DS80PCI102 (x1 PCIe)	SN65LVPE501/4
Channels	*8-channel (PCI800),* *4-lane (PCI402)*	*4-lane(PCI102)*	*1-port (501)* *4-channel(504)*
Interop Tested	*Interop Tested with Intel's Sandy Bridge CPUs & PCI-SIG*	*Interop Tested with Intel's Sandy Bridge CPUs & PCI-SIG*	-
Max Data Rate	8 Gbps	8 Gbps	5Gbps
Typ power/channel	65 mW, 3.3v or 2.5v supply (selectable)	65 mW 3.3v or 2.5v supply (selectable)	330mW/575mW 3.3v supply (multiple power saving modes)
Input Sig Con (EQ)	+36 dB	+36 dB	+15 dB/+15 dB
Output Sig Con (DE)	-12 dB	-12 dB	-9.5 dB/-11 dB
Output Diff VOD Vp-p	600 to 1200mV	600 to 1200mV	800 to 1200mV
Package	54-QFN, 10 mm x 5.5 mm, 0.5mm pitch	24-QFN, 4mm x 4mm, 0.5mm pitch	24-QFN, 4mm x 4mm, 0.5mm pitch (501) 42-QFN, 9mm x 3.5mm, 0.5mm pitch (504)
Configuration	Pins/SMBus/ Direct EEPROM	Pins/SMBus/ Direct EEPROM	Pins

LANE/PORT = Bi-DIRECTIONAL, CHANNEL = Uni-DIRECTIONAL

SAS2/SATA2 – Buffers/Repeaters

	DS100BR210 DS100BR111/A	DS100BR410	SN75LVCP412 SN75LVCP412A SN75LVCP422	SN75LVCP600/ SN75LVCP601	TLK6201E
Channels	*2-channel* *1-port*	*4-channel*	*1-port*	*1-channel* *1-port*	*1-channel*
Max Data-rate	10.3125 Gbps	10.3 Gbps	3 Gbps	6 Gbps	6.25 Gbps
Typ power/channel (2.5v)	65 mW	55 mW	180mW (3.3v)	100mW (3.3v) (600/S) 215mW (3.3v) (601)	-
Input Sig Con (EQ)	+36 dB	+28.9 dB	7 dB	14 dB/15 dB	+17 dB
Output Sig Con (DE)	-12 dB	-9 dB	2.5 dB	-1.2dB/-1.3dB/-4 dB	-12 dB
Output Diff VOD Vp-p	700 to 1200mV	750 to 1200mV	400 to 800mV	400 to 900mV (600/1) 385 to 1300mV (600S)	600 to 1500 mV
Package	24-QFN, 4mm x 4mm	48-QFN, 7 mm x 7 mm	20-QFN, 4 x 4mm 20-SSOP	8-QFN, 2x2mm 10-QFN, 2.5x2.5mm 20-QFN, 4x4mm	16-QFN, 3mm x 3mm
Configuration	Pins/SMBus/ Direct EEPROM	Pins/SMBus	Pins	Pins	Pins
Protocols Supported	SAS2/SATA2	SAS2/SATA2	SATA1/eSATA	SAS2/SATA2	SAS2/SATA2

LANE/PORT = Bi-DIRECTIONAL, CHANNEL = Uni-DIRECTIONAL

12.5Gbps+/SAS3/SATA3 – Buffer/Repeaters

	DS125BR401	DS125BR800	DS125BR111	DS125BR210	SN65LVCP1412/ SN65LVCP1414
Channels	*4-port*	*8-channel*	*1-port*	*2-channel*	*4-channel (1414)*
Max Data-rate	12.5 Gbps	12.5 Gbps	12.5 Gbps	12.5 Gbps	14.25 Gbps
Typ power/channel (2.5v)	65 mW	65 mW	65 mW	65 mW	75 mW
Input Sig Con (EQ)	+30 dB (12.5 Gbps)	+30 dB (12.5 Gbps)	+30 dB (12.5 Gbps)	+30 dB (12.5 Gbps)	+18 dB
Output Sig Con (DE)	-12 dB	-12 dB	-12 dB	-12 dB	Linear
Output Diff VOD Vp-p	700 to 1300mV	700 to 1300mV	700 to 1300mV	700 to 1300mV	Up to 1200mV
Package	54-QFN, 10mm x 5.5mm	54-QFN, 10mm x 5.5mm	24-QFN, 4mm x 4mm	24-QFN, 4mm x 4mm	24-QFN (1412) 4mm x 5mm, 38-QFN (1414)
Configuration	Pins/SMBus/ Direct EEPROM	Pins/SMBus/ Direct EEPROM	Pins/SMBus/ Direct EEPROM	Pins/SMBus/ Direct EEPROM	Pins/I2C
Protocols Supported	10G-KR, SAS-3 SATA, PCIe 3/2/1, 10GbE, PCIe IB, FC, others	10G-KR, SAS-3 SATA, PCIe 3/2/1, 10GbE, PCIe IB, FC, others	10G-KR, SAS-3 SATA, PCIe 3/2/1, 10GbE, PCIe IB, FC, others	10G-KR, SAS-3 SATA, PCIe 3/2/1, 10GbE, PCIe IB, FC, others	10G-KR, SAS-3 SATA, PCIe 3/2/1, 10GbE, PCIe IB, FC, others

LANE/PORT = Bi-DIRECTIONAL, CHANNEL = Uni-DIRECTIONAL

10G-KR: Equalizers

	SN65LVCP1414	SN65LVCP1412	DS100KR800	Competition
Channels	*4-channel*	*2-channel*	*8-channel*	*4-channel*
Max Data-rate	14.2 Gbps	14.2 Gbps	10.3 Gbps	< 10.3 Gbps
Typ power/channel (2.5v)	80mW	75 mW	65 mW	150 mW+
Input Sig Con (EQ)	+17 dB	+18 dB	+36 dB	10 to 20 dB
Output Sig Con (DE)	Linear	Linear	-12 dB	-3 to -9 dB
Output Diff VOD Vp-p	Up to 1200mV	Up to 1200mV	700 to 1300mV	800 to 1000 mV
Package	38-QFN, 5mm x 7mm	24-QFN, 4mm x 5mm	54-WQFN, 10mm x 5.5mm	Various
Configuration	GPIO/I2C	GPIO/I2C	Pins/SMBus/Direct EEPROM	Pins/I2C
Protocols Supported	10G-KR, SAS/SATA, 10GbE, CPRI, IB, FC, Protocol Agnostic	10G-KR, SAS/SATA, 10GbE, CPRI, IB, FC, Protocol Agnostic	10G-KR, SAS/SATA, 10GbE, CPRI, IB, FC, others	-

LANE/PORT = Bi-DIRECTIONAL, CHANNEL = Uni-DIRECTIONAL

10G: Redrivers

	DS100BR210 DS100BR111	DS100BR111A	DS100BR410	TLK1101E
Channels	*2-channel* *1-lane*	*1-channel*	*4-channel*	*1-channel*
Max Data-rate	10.3125 Gbps	10.3125 Gbps	10.3125 Gbps	11.3 Gbps
Typ power/channel (2.5v)	65 mW	65 mW	55 mW	180 mW
Input Sig Con (EQ)	+36 dB	+36 dB	+36 dB	30 dB
Output Sig Con (DE)	-12 dB	-12 dB	-12 dB	-7 dB
Output Diff VOD Vp-p	700 to 1200mV	600 to 1200mV	600 to 1200mV	300 to 900mV
Package	24-WQFN, 4mm x 4mm	24-WQFN, 4mm x 4mm	48-QFN, 7 mm x 7 mm	20-QFN, 4 x 4mm
Configuration	Pins/SMBus/ Direct EEPROM	Pins/SMBus/ Direct EEPROM	Pins/SMBus	GPIO
Protocols Supported	SAS/SATA, 10GbE, CPRI, IB, FC, others	SAS/SATA, 10GbE, CPRI, IB, FC, others	SAS/SATA, 10GbE, CPRI, IB, FC, others	10GbE, SAS/SATA/8GFC, 10GFC, 10G SONET, others

LANE/PORT = Bi-DIRECTIONAL, CHANNEL = Uni-DIRECTIONAL

10Gbps+ Mux

Feature *Comparison*

	DS100MB201	DS100MB203	SN65LVCP114
Channels	*2 Port (Dual 2:1 Mux, 1:2 Fanout)*	*2 Port (Dual 2:1 Mux, 1:2 Fanout)*	*4 Port (Quad 2:1 Mux, 1:2 Fanout)*
Max Data-rate	10.3125 Gbps	10.3125 Gbps	14.2 Gbps
Typ power/Port (2.5v)	100 mW	195 mW	150 mW
Input Sig Con (EQ)	+10 dB	+36 dB	+14 dB
Output Sig Con (DE)	-12 dB	-12 dB	-
Output Diff VOD Vp-p	500 to 700mV	600 to 1300mV	600 to 1200mV
Package	54-QFN, 10mm x 5.5mm	54-QFN, 10mm x 5.5mm	167-BGA, 12mm x 12mm
Configuration	Pins/SMBus	Pins/SMBus/Direct EEPROM	Pins/I2C
Protocols Supported	SAS/SATA, 10GbE, CPRI, IB, FC, others	10G-KR, 10GbE, CPRI, IB, FC, PCIe, others	10G-KR, 10G EPON, 16GFC, CPRI, 4x10GbE others

SN65LVPE502A: SuperSpeed USB Redriver

Features

- Corrects issues identified in using a redriver with integrated xHCI controllers
- Selectable Equalization, De-emphasis and Output Swing Control
- U2/U3 Mode Detection will selectively turn-off internal circuitry to save on power
- Low active power consumption
- Supports USB 3.0 LFPS Protocol Compliance test

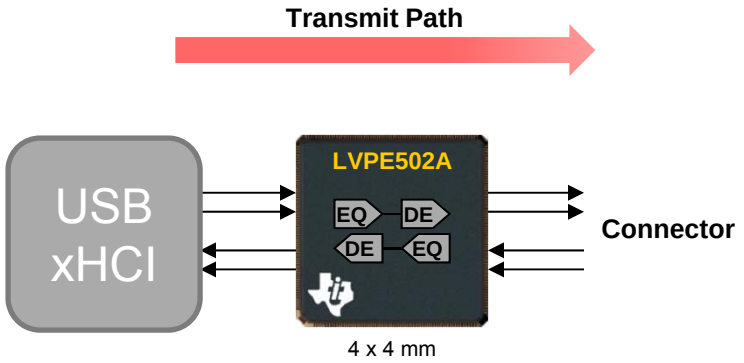
Benefits

- Enables the broadest interoperability with various host implementations
- Provides customer with optimized power vs. performance settings for their system implementation
- Typical power saving is about 75% lower than normal operating mode
- Expected to save approximately 40% active power versus the competition
- Allows customers to pass all certification testing and utilize SuperSpeed USB logo

Applications

Low Power, Small Footprint

- PC Motherboards
- PC Docking Stations
- PC Add–in Cards
- Backplane & Cabled applications



HD3SS3412/3415: 8GHz Differential Switch

Features

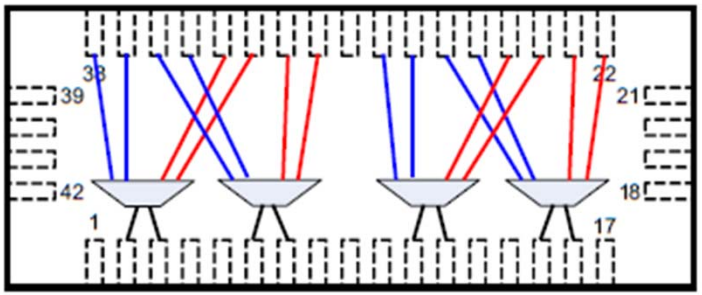
- 4 Channel Differential Switch
- High Performance
  - –3dB Bandwidth: >7.5 GHz
  - Data rates over 12 Gbps
    - Silicon tested in lab at rates up to 13 Gbps
  - Crosstalk: –35dB
  - Insertion Loss: –1.5 dB
  - Return Loss: -9 dB
  - Off Isolation: -19dB
- VDD : 3.3 V ± 10%
- ESD over 2KV HBM
- 42 pad TQFN, 9 x3.5 with flow-through pinout for optimal layout
  - 2 pinout options available via ‘3412 and ‘3415

Applications

- PC Motherboards
- PC Docking Stations
- PC Add–in Cards
- Backplane applications
- PCIe Bus Multiplexing and expansion

Benefits

- Supports latest Gen PCIe/SATA/SAS/USB interface common in today’s computing applications
- Low I/O capacitance minimizes loading & signal distortion
- Adds flexibility in rerouting high speed signals



High Speed SerDes Solutions

- Ethernet and Fiber Channel key Interfaces for Networking
  - 1GbE and 10GbE key building block I/O
  - New 10G Ethernet SerDes enables 10GbE compliant links
    - TLK10034
    - TLK10232
- Gigabit serial links proliferating within Networking applications
  - Driving up cost, Increased power consumption, Increased system complexity, Impact to time to market
  - **Cable, Link Consolidation** -> 10 Gbps Serial link aggregation provides potential solution
    - TLK10022
    - TLK10081

TLK10002

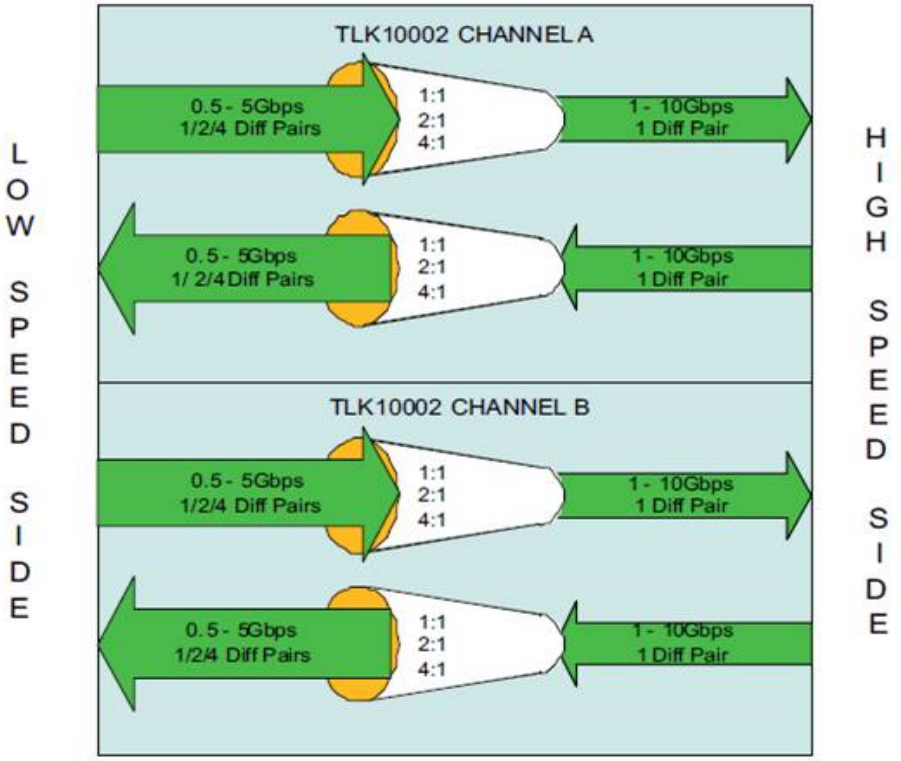
Dual-Channel 10Gbps Multi-Rate Transceiver

Features

- Supports all CPRI and OBSAI Data Rates
- Supports SerDes Operation upto:
  - 10Gbps Data Rate on the High Speed Side
  - 5Gbps on the Low Speed Side
- Supports transmit De-emphasis and receive Adaptive Equalization improve signal integrity
- 65nm Advanced CMOS Technology
- Interface to Backplanes, Passive and Active Copper Cables or SFP/SFP+ Optical Modules
- Industrial Ambient Operating Temperature (–40°C to 85°C)
- Device Package: 13mm x 13mm, 144-pin PBGA, 1-mm Ball Pitch

Benefits

- Simplified Serial interface to ASIC/FPGA
- Simplified signal chain clocking
- Lower cost of implementation
- Flexible parallel interfaces
- Low power consumption



Applications

- Wireless Infrastructure CPRI and OBSAI Links
- High-Speed Video Applications
- Proprietary Cable/Backplane Links
- High-Speed Point- to-Point Transmission Systems

TLK10034

4 Channel XAUI to 10GBASE-KR SerDes

Features

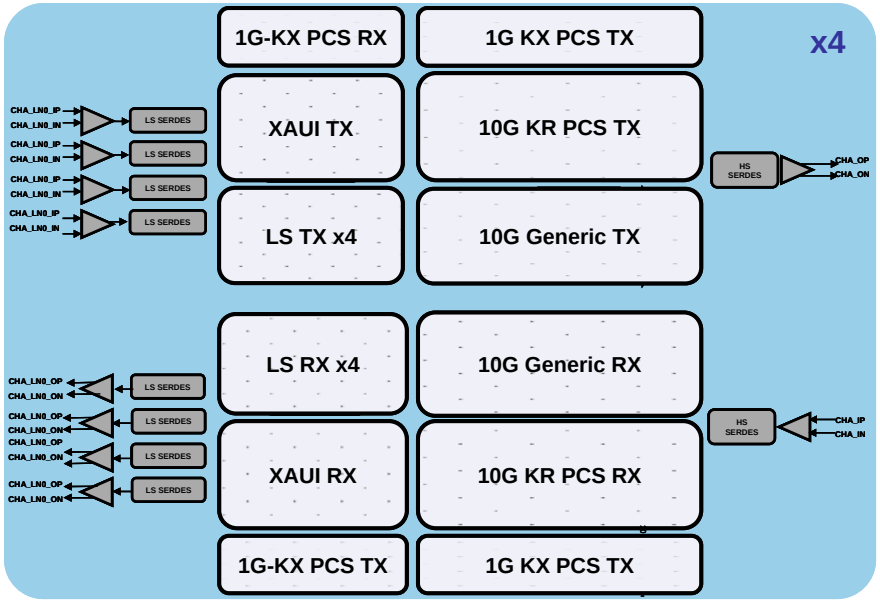
•4 Channel XAUI to 10GBASE-KR SerDes
• Compliant to IEEE802.3ap standard
• Support to XFI interface
• Super Jumbo Packet Size support to 800KB
• Programmable CTC Depth Support
• Link Training Support
• Auto-negotiate Support
• Industry standard XAUI interface
• Decision Feedback equalization (DFE) with Feed-Forward Equalization (FFE)
• Support for 10/1GbE rate with Auto-negotiation
• Core supply 1V; I/O: 1.5V/1.8V
• Single reference clock input at 156.25MHz
• 8B/10B and 64B/66B coding support
• MDIO Clause 45 (All datapaths) and 22 support (8b/10b only)
• Multiple Test Pattern Support

Applications

• 10G Ethernet backplane links
• 40G Ethernet Switch Routers
• High Density Blade Servers
• High Performance Network Switches
• Driving SFP+ Optical Modules

Benefits

• Industry standard 10GbE interface support
• Wide data rate range
• Superior signal integrity performance
• Low Power Operation: < 900mW/channel
• Flexible clocking
• Support for existing MDIO control architecture



One Channel Shown Only

General Purpose Analog

(ESD Protection, Logic, Multiplexers)

www.ti.com/esd

www.ti.com/switches

www.ti.com/logic

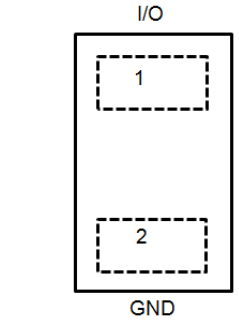
TPDxE05U06

Samples NOW

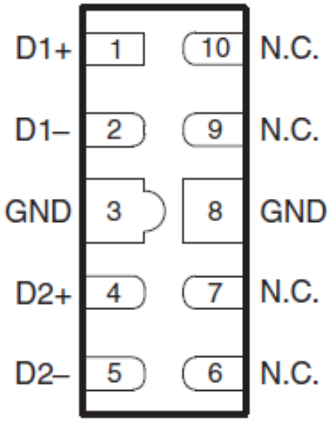
One/Four/ Six Channel ESD for Ultra High-Speed Differential Signal

Features

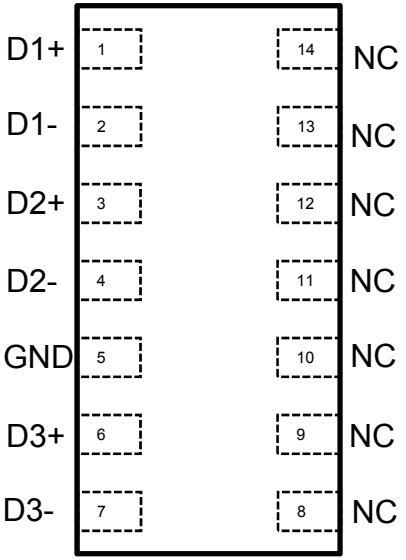
- Supports differential data rate up to 5GBps
- Optimized package, pin-mapping for high-speed differential lines
- ±15KV contact ESD ratings
- 5-A Peak Pulse Current (8/20 µS Pulse)
- $C_{IO\ to\ GND\ MAX}$ <0.5pF
- R_{dyn} < 0.5Ω



DPY
1 mm x 0.6 mm x 0.35mm
(0.65-mm pitch)



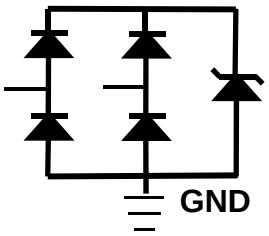
2.5 mm x 1 mm x 0.5mm
(0.5-mm pitch)

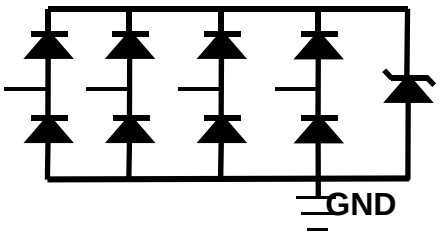


3.5 mm x 1.35 mm x 0.5mm
(0.5-mm pitch)

Applications

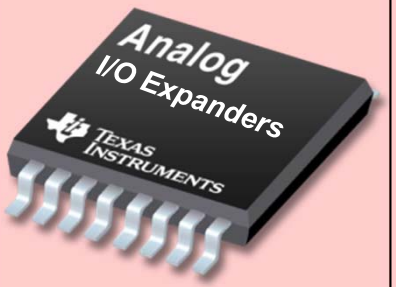
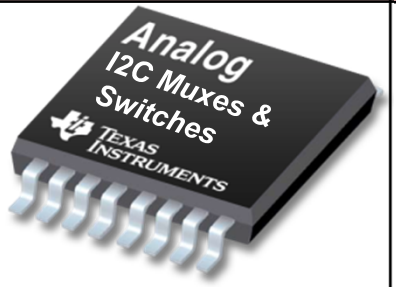
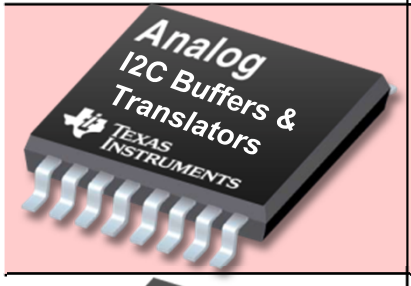
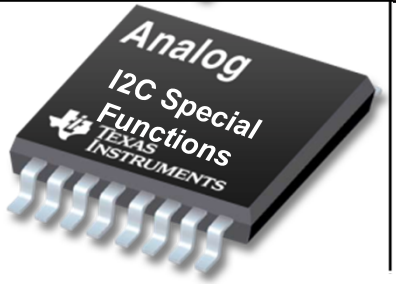
- USB3.0
- MHL, HDMI, Thunderbolt
- PCIe Gen3, SAS, SATA





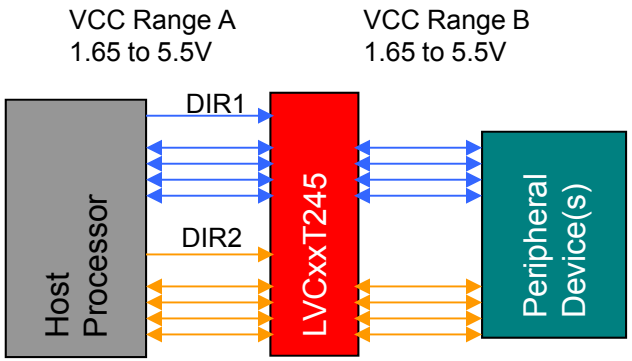
Texas Instruments

I2C Products by Category and Application Type

	• General purpose I2C I/O expanders to be used with system chips running out of I/O's • Reduces PCB complexity by routing simplification • Can provide voltage level translation • General purpose LED controls • Variations: HW/SW Interrupts, Hardware reset, integrated pull-up pull downs, number of address pins. Dual supply rails.	Example: TCA6408A TCA9535 TCA7408 TCA6416A TCA6424A
	• Allows expansion, muxing and/or isolation of I2C bus. • Can provide voltage level translation • Variations: HW/SW Interrupts, Hardware reset, integrated pull-up pull downs, number of address pins	Example: PCA9543A PCA9544A PCA9545A
	• Increases the number of I^2C devices that can be connected to a I^2C master. • Enables the IC signal to be used over longer trace lengths or over a cable • Level translation to mixed voltage I^2C systems	Example: TCA4311A TCA9509 PCA9306 PCA9515 PCA9517
	• Keypad scan ICs manage 80 to 104 keys through I^2C • LED Blinking devices • Single wire interface output expander	Example: TCA8418/E LM8330 TCA6507 TCA5405

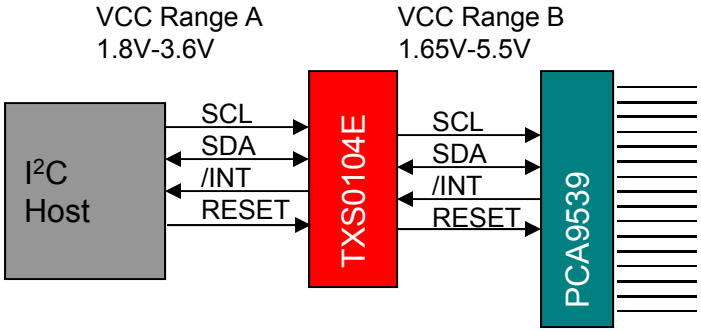
Most Common Voltage Translation Use Cases

Typical Bus/GPIO Interface



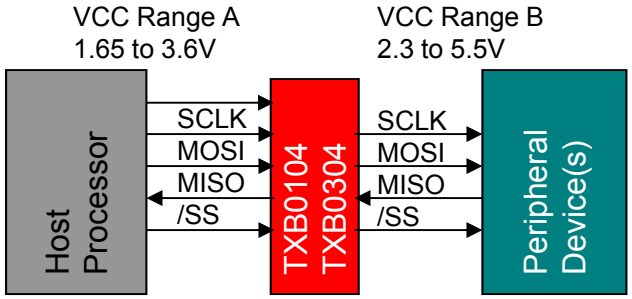
Translation for wide bit width buses require either the LVC or AVC family of devices. These translators have a pin to control the output direction of data. Each direction control is separated into banks of two (DIR1/DIR2).

Typical I²C Interface



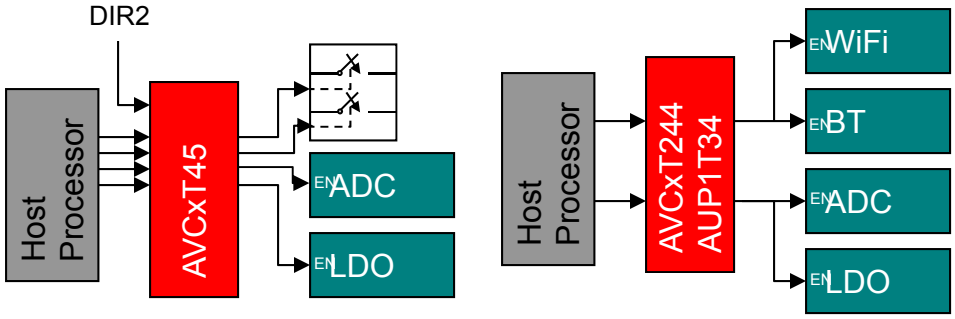
TI provides several options for translating open drain outputs. The TXS102/TXS0104E is ideal for I²C lines. The TXS0104E has two extra bits for either an interrupt or RESET.

Typical SPI Interface



TXB is an autodirection sensing translator for push pull applications. If you have an application (like SPI) which has a mixture of bits going to different directions, the TXB product can handle it effortlessly.

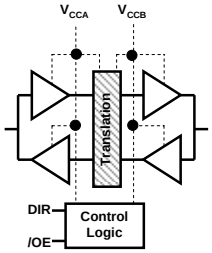
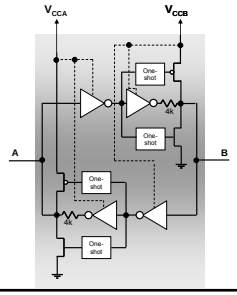
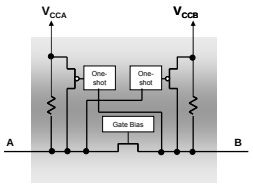
Typical Control Input Interface



Lower bit width devices only require one DIR pin. It is for multiple control bits

Our AVC2T244 and AUP1T34 are single direction translators good for general purpose buffer/translating and fanout to multiple loads

General Purpose Voltage Translators (Level Shifters)

Type	Advantages	Limitations	Bit Options
SN74xxx245 	▪ Fast data rate (~300Mbps) ▪ Fully configurable: $V_{CCA} < V_{CCB}$ or $V_{CCB} < V_{CCA}$ ▪ Low Power Consumption ▪ Hi-Z if V_{CCA} or V_{CCB} = 0V ▪ Good DC Current Drive (12mA)	▪ DIR (direction control) required	1, 2, 4, 8, 16, 20, 24, and 32
TXB010x/TXB030x 	▪ Auto-Sensing (no DIR control needed) ▪ Medium data rate (up to 140Mbps) ▪ Low Power Consumption ▪ Hi-Z if V_{CCA} or V_{CCB} = 0V ▪ 15kV HBM ESD protection (B port)	▪ Weak DC drive (few 100uA) ▪ Not good for open drain buses	1, 2, 4, 8
TXS010x/TXB030x 	▪ Auto-Sensing (no DIR control needed) ▪ Good for open-drain buses (I2C) ▪ Low data rate (up to 40Mbps) ▪ Hi-Z if V_{CCA} or V_{CCB} = 0V ▪ 15kV IEC ESD protection (B port)	▪ Higher power consumption compared to ‘245 or weak buffer translators	1, 2, 4, 8

Switches and Multiplexers by Interface Type

	Data-Rate	Signal Swing	# of Data Lines	Signal Switch Device
USB 2.0	480Mhz	Data swing 0mV to 400mV VBUS = 5V	3 Data lines +1 VBUS	TS3USB221/A/E TS3USB3x/E TS5USBA224 
USB3.0	5Gbps	Data swing 0V to 400mV VBUS = 5V	6 Data lines +1 VBUS line/ 7 Data lines +1 VBUS line	***HD3SS3412*** ***HD3SS3415*** 
VGA	<50Mbps	Data line 0.7V Control line 5V	5 Line (9-pin connector)/ 9 line (15 pin connector)	TS3V712E TS3V713EL 
DVI/ HDMI/ DisplayPort	3.4Gbps	Data Swing 2.7V to 3.3V Control Lines up to 5V	12 Data Lines	TS3DV20812 TS3DV421 
Ethernet	1Gbps	3.3V	8 Lines	TS3L500AE TS3L501E 
RS-485/ 422/ 232/ CAN	>200Mbps	±5V to ±15V	2 Line or multiples	TS12A12511 
Audio	<20KHz	-5V to 5V	2 Lines, 5 Lines	TS5A22364 
eSATA	6Gbps	1V	4 Line	***HD3SS3412*** ***HD3SS3415*** 
DDR2/DDR3 Memory	1066MHz	1.8V/1.5V	12 lines total	TS3DDR3812 TS2DDR2811 

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Standard Linear

- Amplifiers and Comparators
- Interface ICs
- Power ICs

Functions

Comparators	Amplifiers
Buffers	Flip-Flop/Latches
Interface	Logic Gates
Linear Regulators	I^2C Logic
LDO Regulators	Signal Switches
Buses	JTAG Logic
Voltage Supervisors	Drivers
Timers	Translators

& many more…

Standard Logic

- I^2C
- Little Logic
- Voltage Level Translation
- Analog Switch
- Specialty Logic

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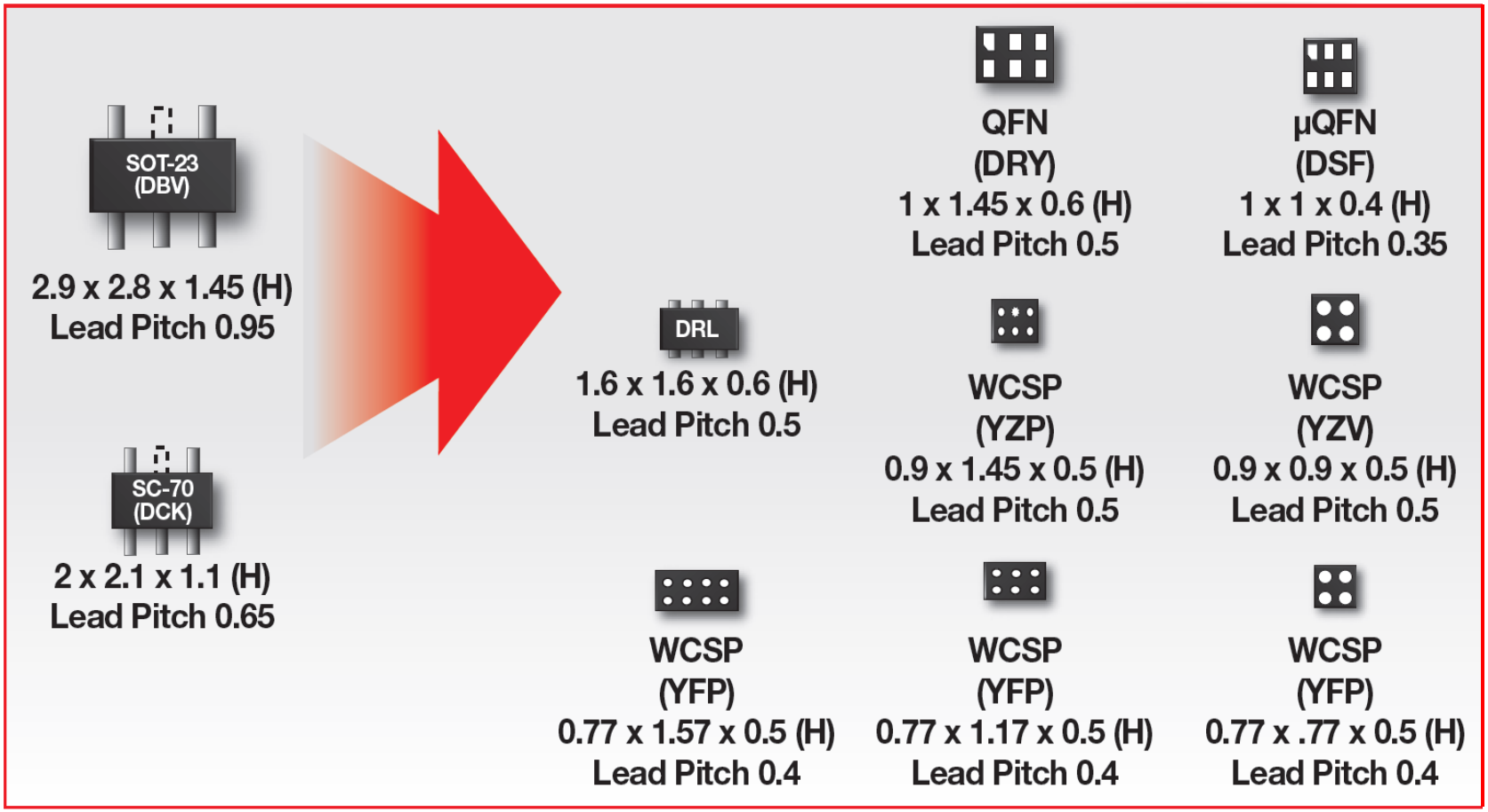
Core, Safety, Surge

Broadest Portfolio

Little Logic Packaging Trend



Standard Linear Packaging Trend

Voltage Regulators

Sot-89/Sot-223 | TO-92 | SOT | DPAK/D2PAK | QFN

Op Amps

PDIP | SOIC | TSSOP | MSOP | SOT | Nano

Data Transmission Line Drivers

PDIP | SSOP | SOIC | TSSOP | QFN | SON

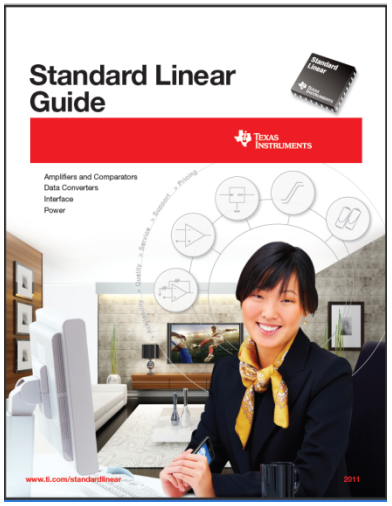
Peripheral Drivers

PDIP | SSOP | SOIC | TSSOP | SON

SLL Tools

www.ti.com/littlelogicguide

www.ti.com/5mg



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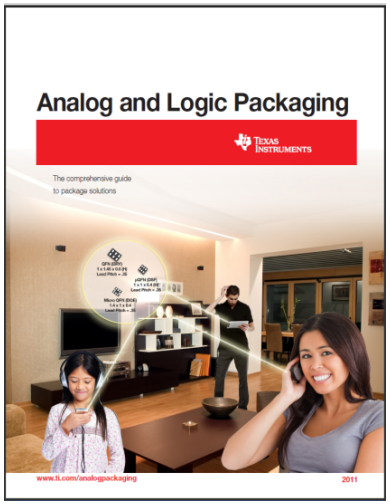

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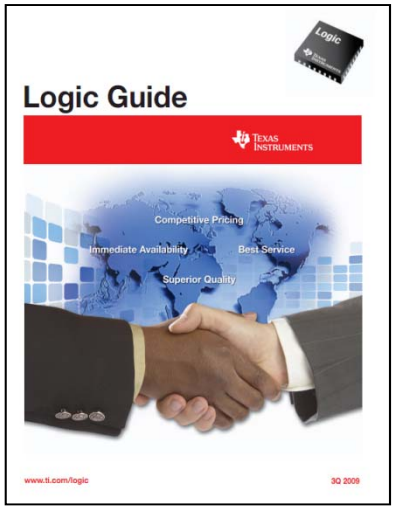

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TI Logic Manufacturing Strategy

'*Core, Safety, Surge*'

- For more than two years now the new SLL Manufacturing Strategy offers a flexible support of SLL products across the globe
- We implemented a 3 Step supply strategy which allows us to react on customer requests and market forces like no other
- 74% of our volume is now covered with *Core, Safety* and *Surge* Suppliers

Package	*Core*		*Safety*		*Surge*	
	Location	Int/Ext	Location	Int/Ext	Location	Int/Ext
SOIC	Mexico	Int	China	Ext	Malaysia	Int
TSSOP	Malaysia	Int	China	Ext	Malaysia	Ext
SOT-23	China	Ext	China	Ext	Thailand	Ext
SC-70	China	Ext	China	Ext	China	Ext
WCSP	China	Ext	Philippines	Int	Taiwan	Ext
uQFN (DSF/DRY)	China	Ext	Thailand	Ext		

Thank you!