

REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	29 AUG 2022	Drafted from PROC142E1 Schematics. R651 value changed to 1K. DNI'd R618 and R676.Changed the I2C buffer parts to TCA9517DR. Changed the part SN74AVC4T245RSVR to SN74AVC4T245DGVR	Mistral Design Team		
0.02	08 SEP 2022	Added the second GPIO Expander U110 Part# TCA6408ARGTR	Mistral Design Team		
0.03	21 SEP 2022	Changed the Current monitors Res Filter values from 10E to 0E to the Sense pins.	Mistral Design Team		
0.04	19 OCT 2022	Added Testpoint to TEMP_DIODE_P pin of SoC. Changed the GPIO_OLDI_RSTn net name to GPIO_TS_RSTn.	Mistral Design Team		
0.05	24 OCT 2022	Changed the Fulton PMIC part from TPS6521903RHBR to TPS6521904RHBR. Mounted R699 and DNI'd R123. DNI'd the current monitor section of U36	Mistral Design Team		
0.06	3 Nov 2022	Changed the DDR4 part from MT40A1G16KD-062E IT:E to MT40A1G16TB-062E IT:F. Changed the eMMC part from MTFC16GAPALBH-IT to MTFC32GAZAQHD-IT.	Mistral Design Team		
0.07	15 Nov 2022	Removed the PMIC_STBY connection from SOC to PMIC.	Mistral Design Team		
0.08	22 Nov 2022	Added 2x 47uF on VCC_5V0. DNI'd C432, C433(10uF) and changed C415 to 4.7uF. Added 22pF CAP across R108	Mistral Design Team		
0.09	1 Dec 2022	Removed MMC2 connector section (J18) and associated resistors	Mistral Design Team		
0.10	11 APR 2023	Changed the HDMI external swing resistance to 7.5K. Added Standoff,Screw & Washer for M.2 connector. DNI'd R650 on SoC_USB1_DRVVBUS	Mistral Design Team		
0.11	16 MAY 2023	Depopulated Pull up of SOC_WLAN_IRQ_1V8 (R6)	Mistral Design Team		

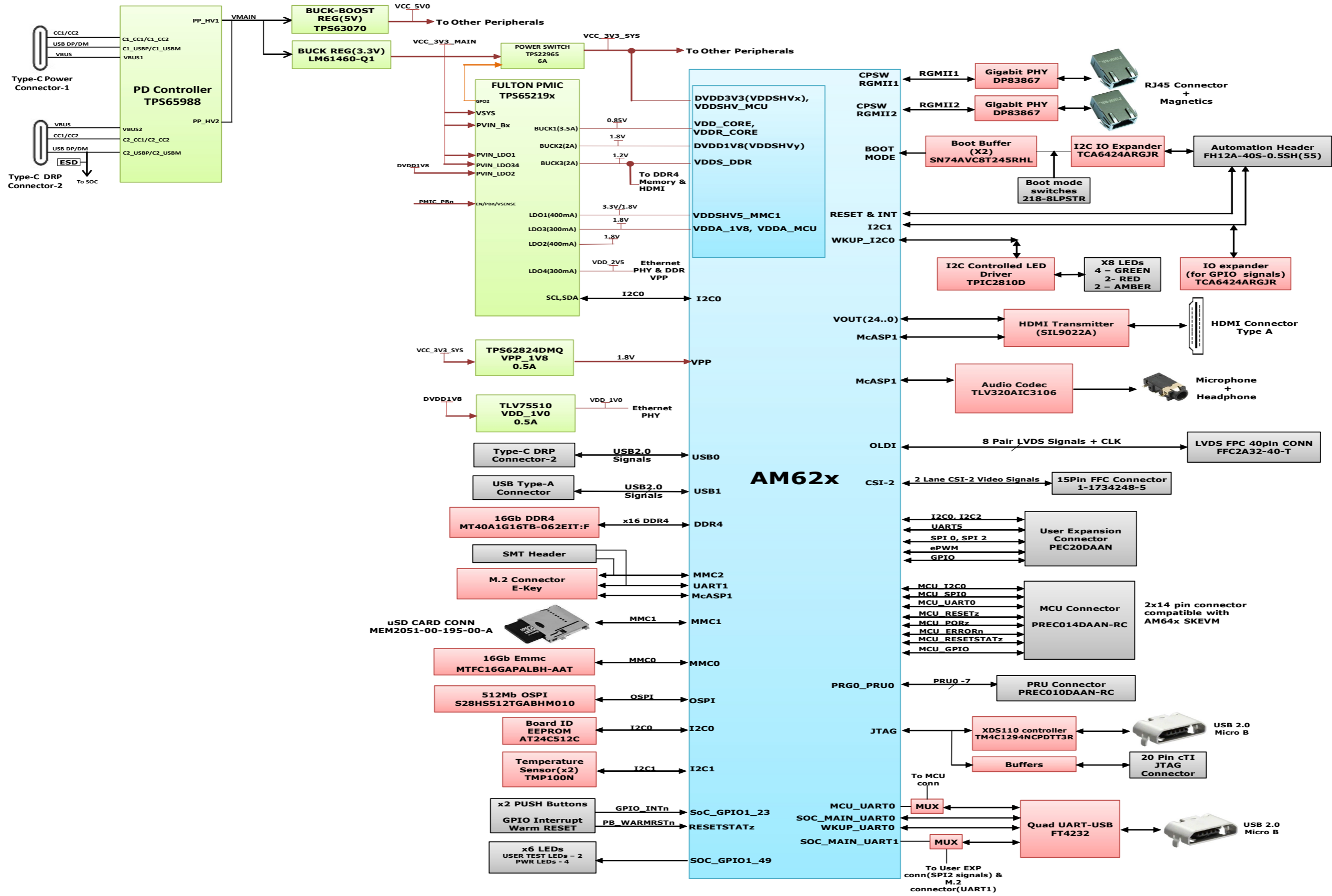
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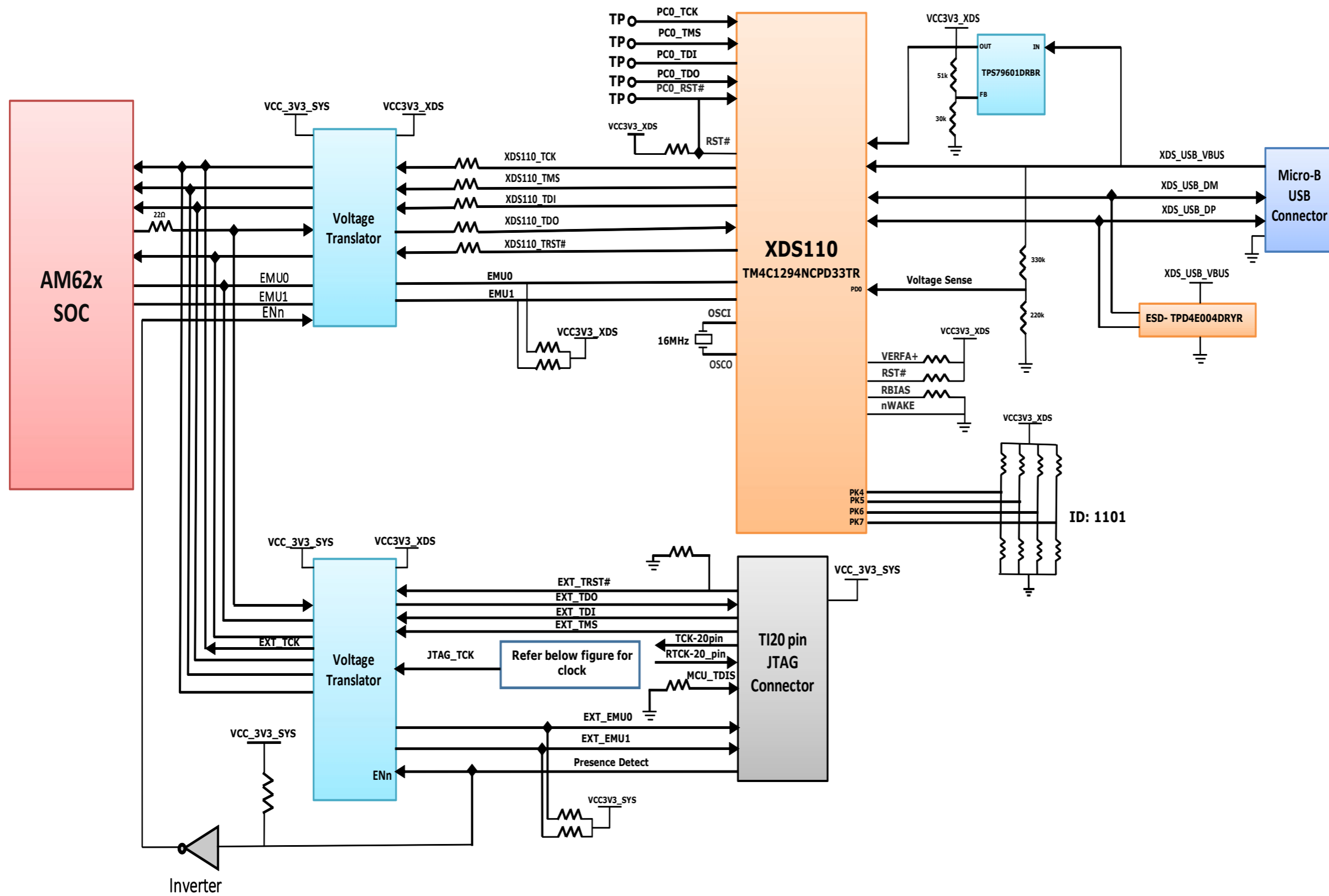
Title REVISION HISTORY

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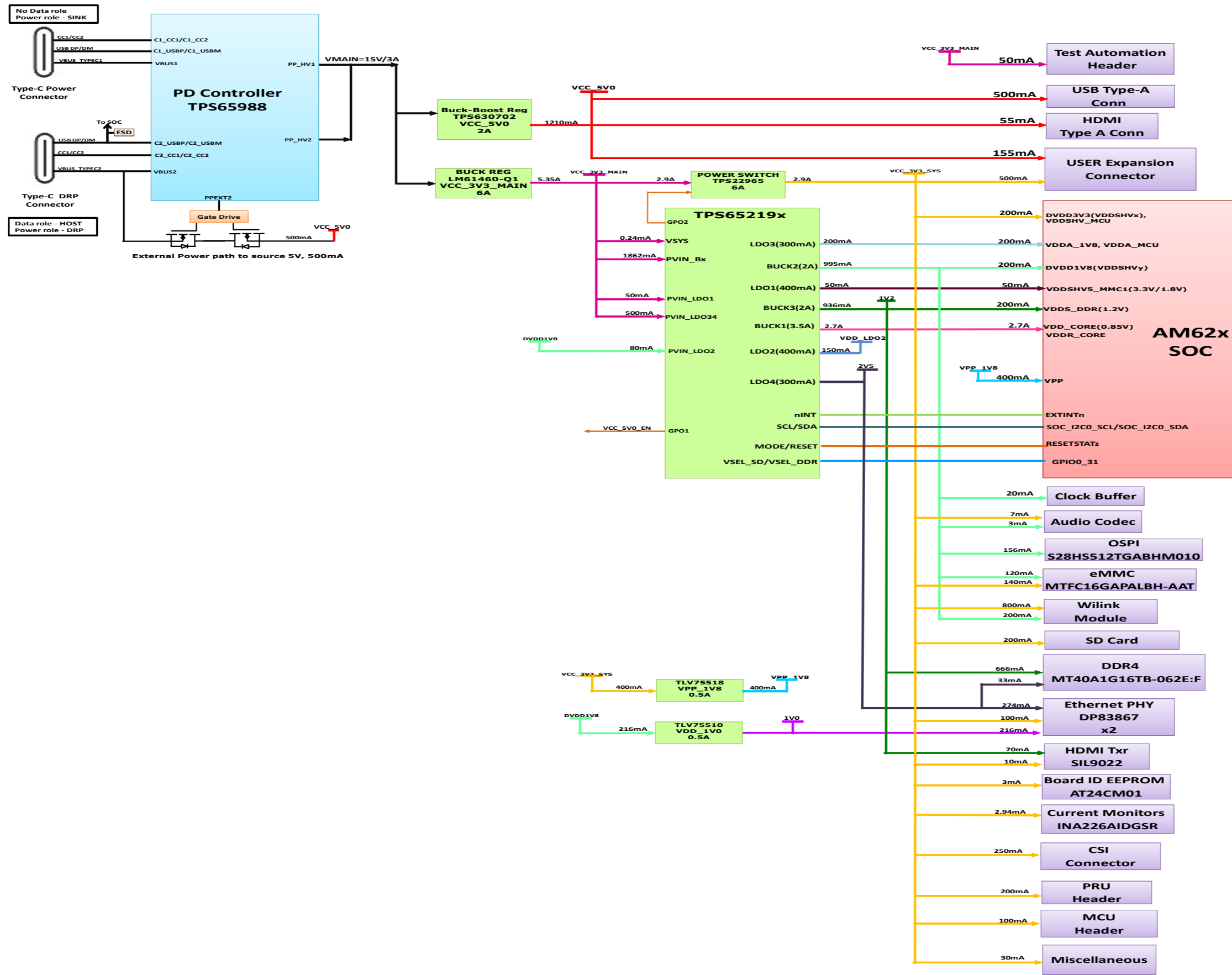
BLOCK DIAGRAM



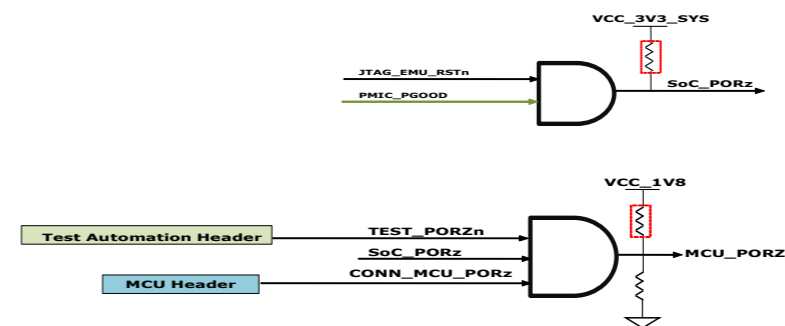
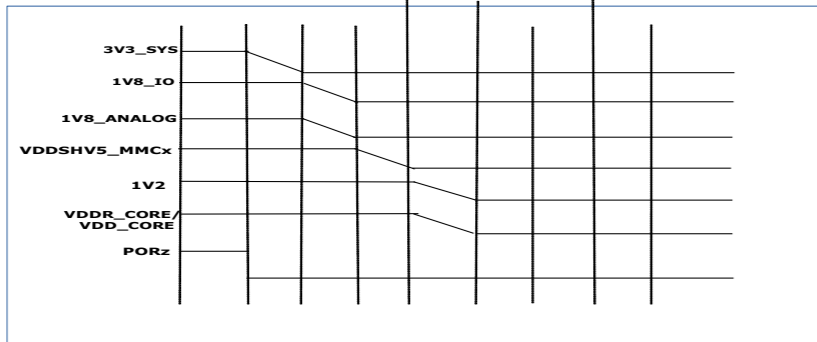
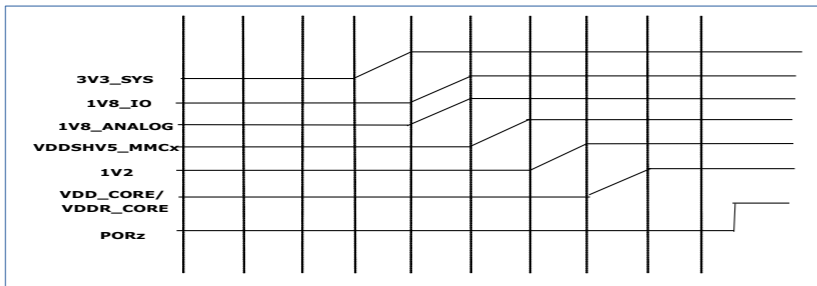
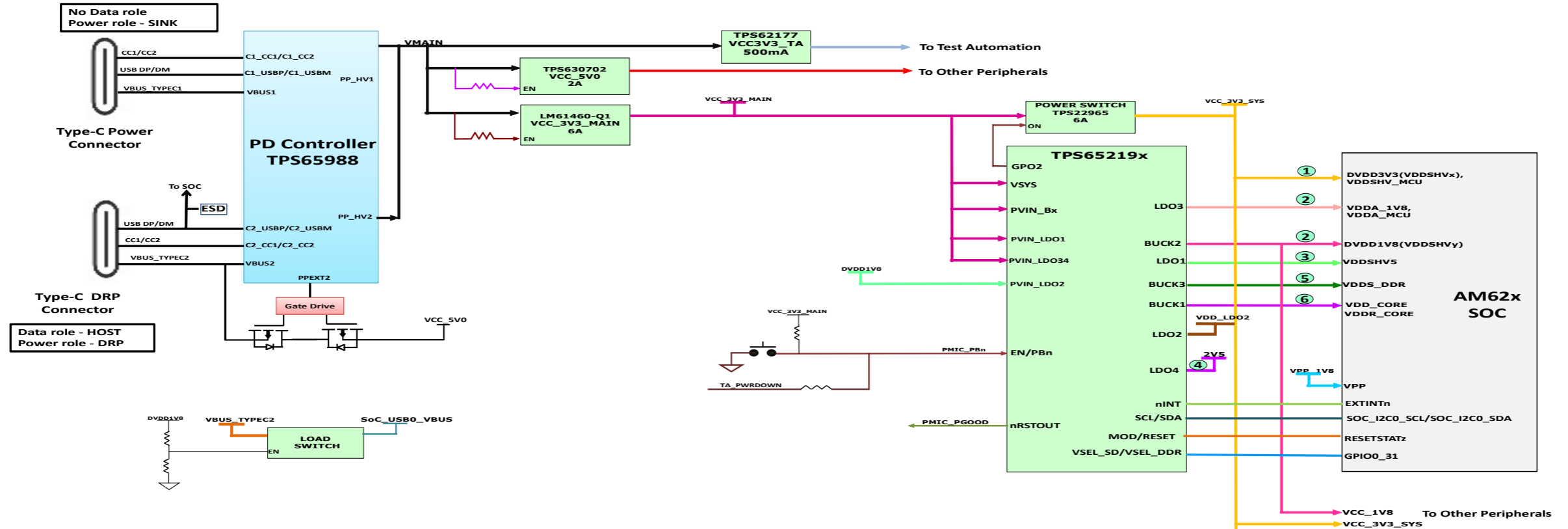
BLOCK DIAGRAM_XDS110



POWER BLOCK DIAGRAM



POWER SEQUENCE



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Title POWER SEQUENCE

Size PROC142A1

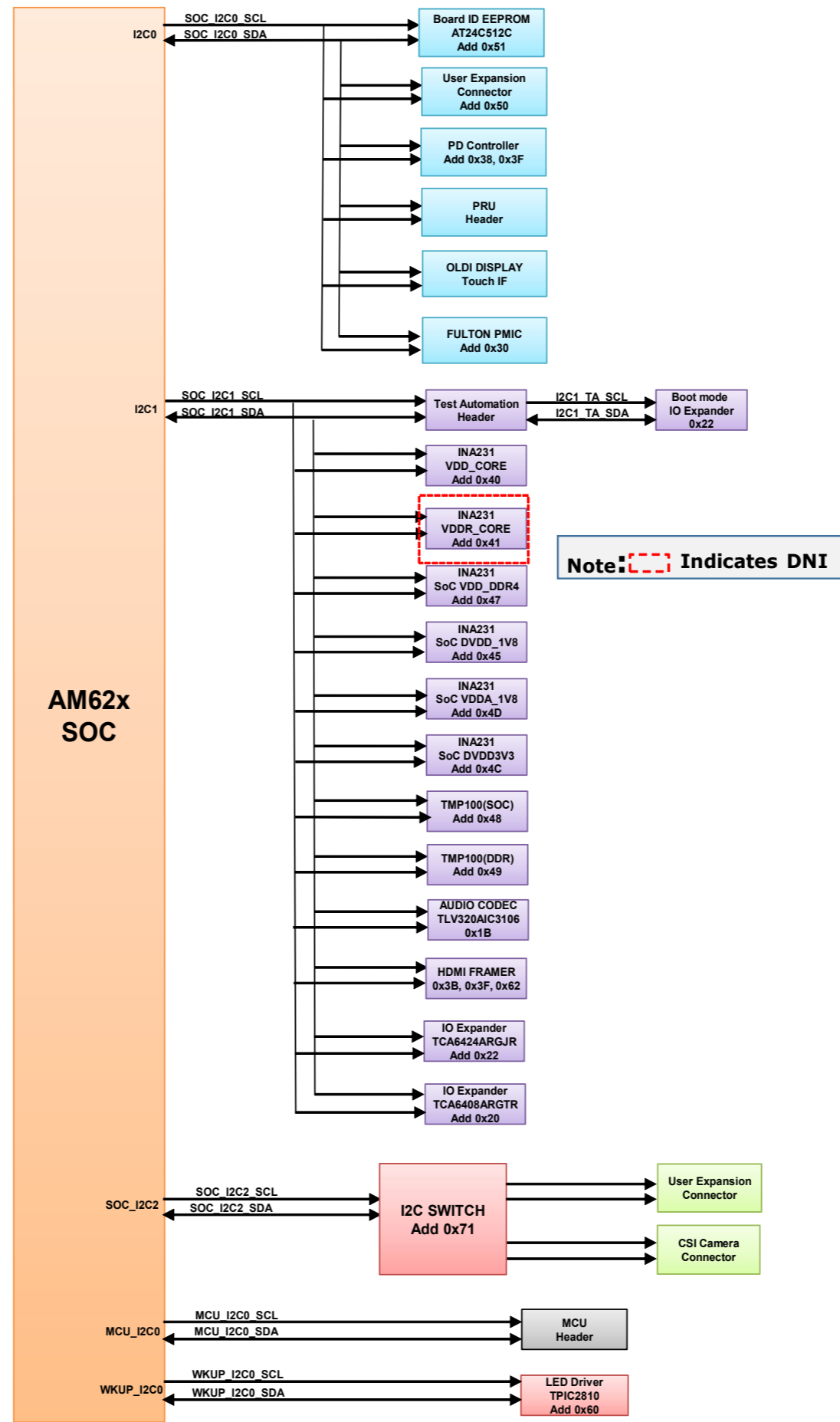
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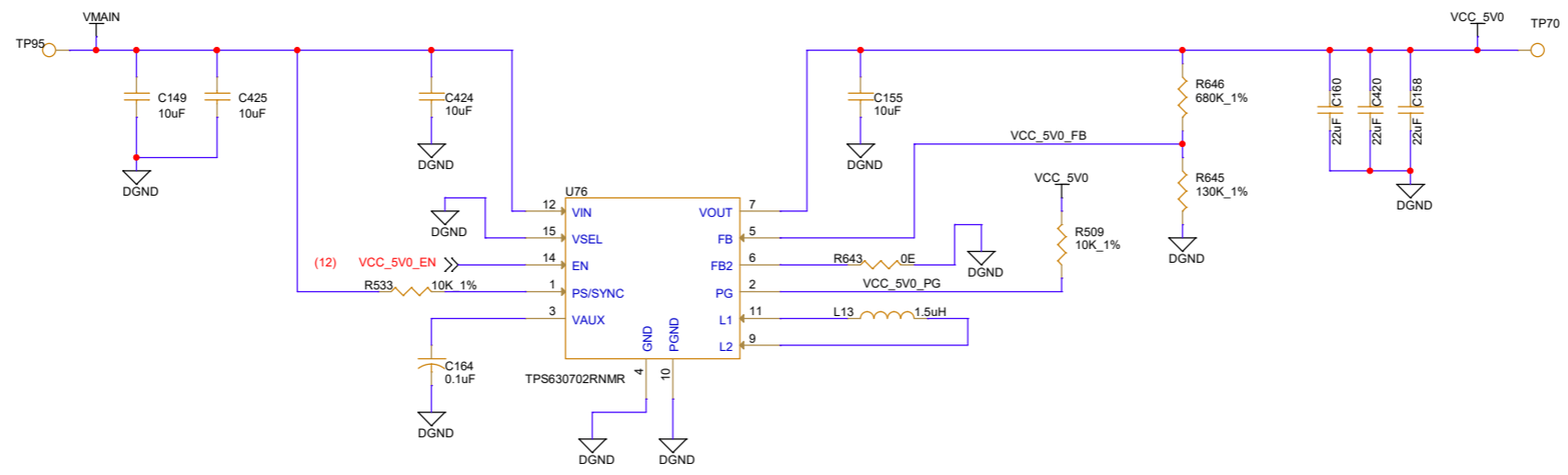
I2C TREE



GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	Functionality	GPIO USED	SOC MUXED SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE CONNECTED ON SKEVM
1	Enable for WLAN Interface	SoC_WLAN_EN_1V8	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	SoC_WLAN_IRQ_1V8	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC_3V3	ENABLE	MCU_GPIO0_1	MCU_SPIO_CS0	OUTPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn/PRU_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
	PRU Connector Interrupt									
	PMIC_INTn									
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	SD Card IO Voltage Select	VSEL_SD	ENABLE	GPIO0_31	GPMCO_CLK	OUTPUT	LOW	HIGH	VDDSHV3	SoC_DVDD3V3
8	IO Expander Interrupt	MCU_GPIO0_15	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	SoC_DVDD3V3
9	TEST GPIO1 from Test Automation Connector/ User Interrupt Push Button									
10	User Test LED 1	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 01										
1	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	PRU Board Detection	PRU_DETECT	DETECTION	IO EXPANDER - P02		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER - P03		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER - P04		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER - P05		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER - P06		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
8	EXP CONN HAT Board Detection	RPI_HAT_DETECT	DETECTION	IO EXPANDER - P07		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
9	M.2 Connector Alert	WLAN_ALERT_3V3	ALERT	IO EXPANDER - P10		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	M.2 Connector WAKEUP	BT_UART_WAKE_SOC_3V3	WAKEUP	IO EXPANDER - P11		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
11	SOC UART1 Mux Select	UART1_MUX_SEL	SELECT	IO EXPANDER - P12		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
12	Enable for Wilink Level Translators	WL_LT_EN	ENABLE	IO EXPANDER - P13		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER - P14		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	Raspberry Pi Camera CSIO GPIO1	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER - P15		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
15	Raspberry Pi Camera CSIO GPIO2	CSI_GPIO2	INPUT/OUTPUT	IO EXPANDER - P16		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	PRU Power Switch Enable	PRU_3V3_EN	ENABLE	IO EXPANDER - P17		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER - P20		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO for communications with AM62x	IO EXPANDER - P21		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
19	MCASP2 Enable and Direction Control	AUD_BUF_EN	ENABLE	IO EXPANDER - P22		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
20		WL_BUF_EN	ENABLE	IO EXPANDER - P23		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
21		AUD_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P24		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
22		WL_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P25		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
23	OLDI Display Touch Interrupt	TS_INT#	INTERRUPT	IO EXPANDER - P26		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER - P27		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 02										
1	M.2 Connector SDIO Reset Control GPIO	WLAN_SDIO_RST_3V3	RESET	IO EXPANDER - P0		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	OLDI Display Reset control	GPIO_TS_RSTn	RESET	IO EXPANDER - P1		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	DETECTION	IO EXPANDER - P2		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	eMMC Reset control GPIO	GPIO_eMMC_RSTn	RESET	IO EXPANDER - P3		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3

PERIPHERAL POWER SUPPLY-1



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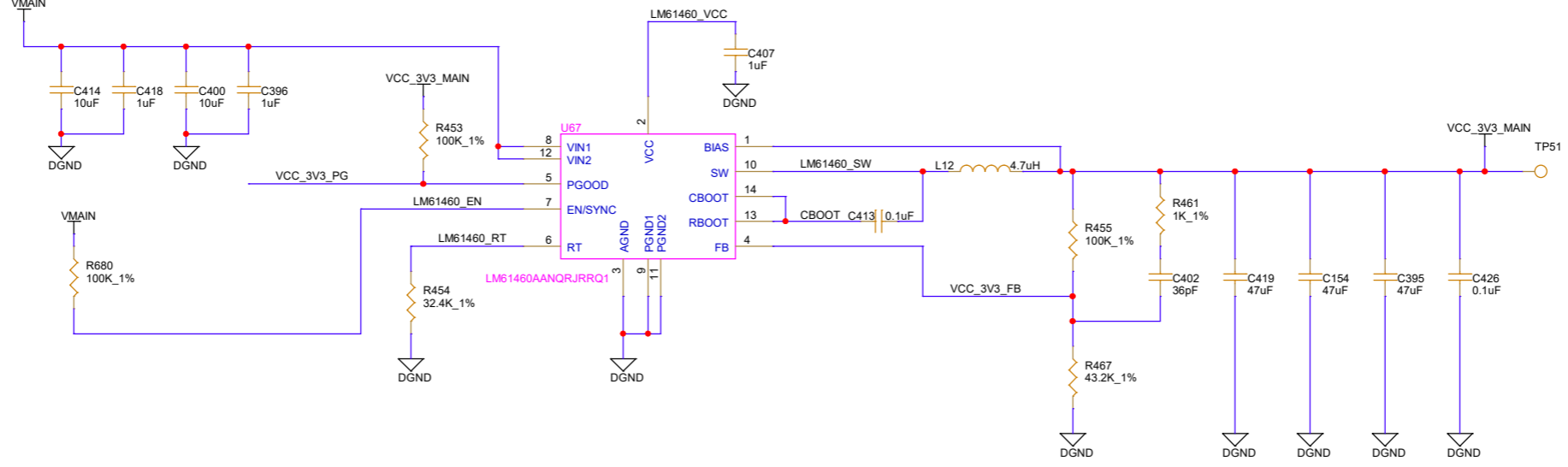
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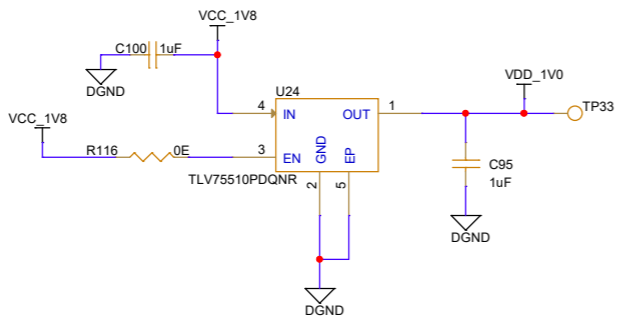
PERIPHERAL POWER SUPPLY-2

VinMin = 4.5V
 VinMax = 24V
 Vout = 3.3V @ 6A

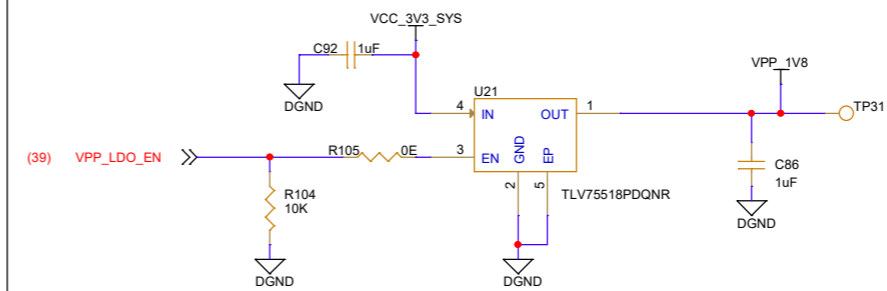
3.3V, 6.0AMPS SUPPLY



1.0V, 0.5AMPS SUPPLY (ETHERNET)



1.8V VPP, 0.5AMPS SUPPLY



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Title PERIPHERAL POWER SUPPLY-2

Size C PROC142A1

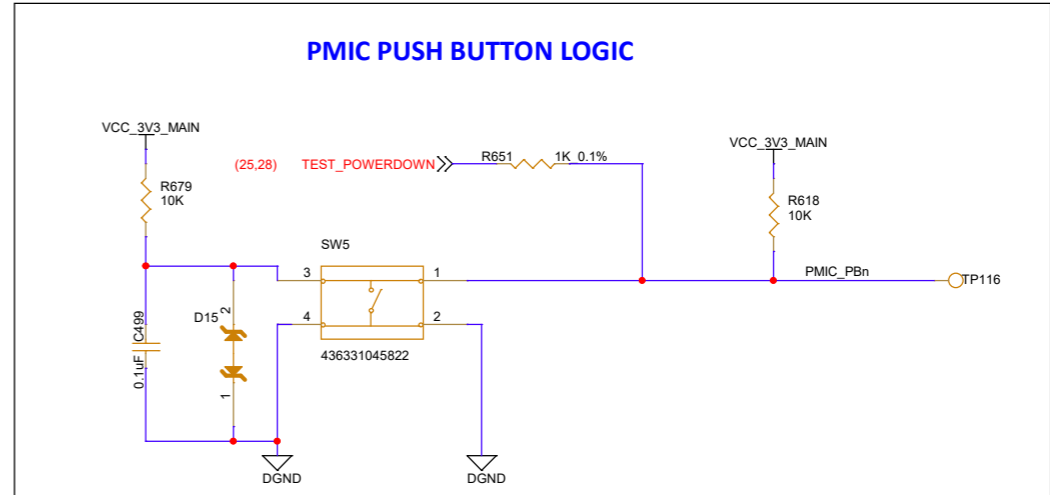
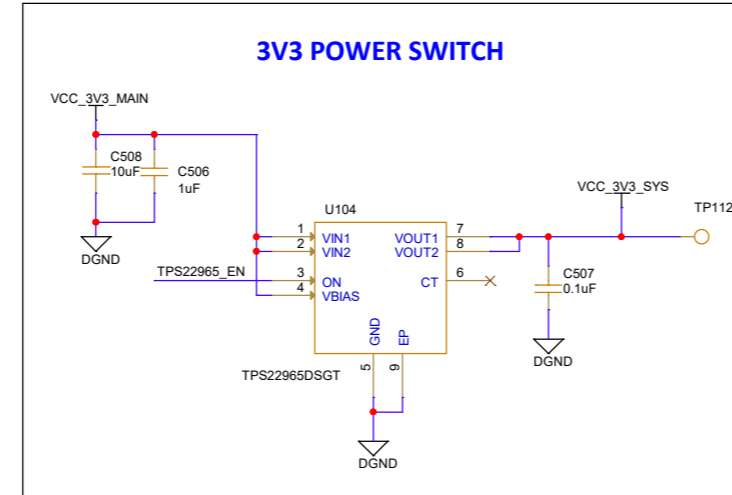
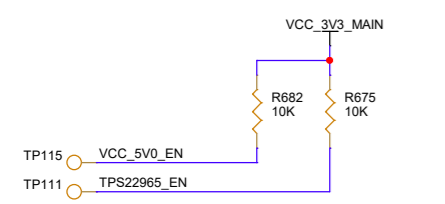
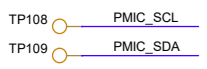
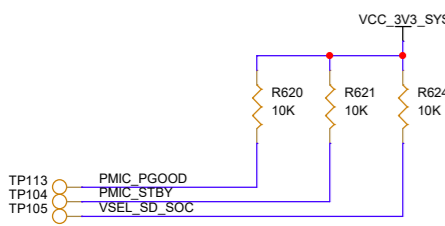
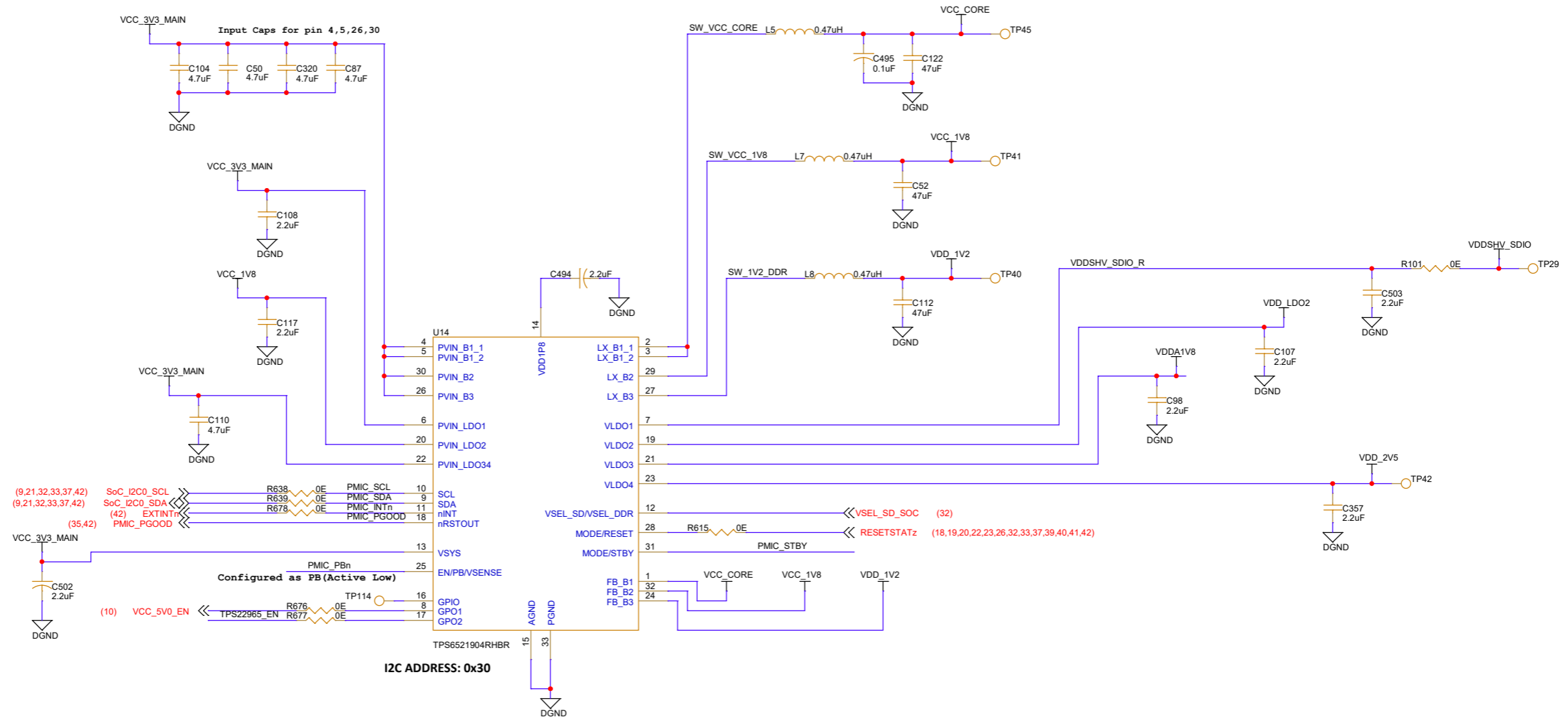
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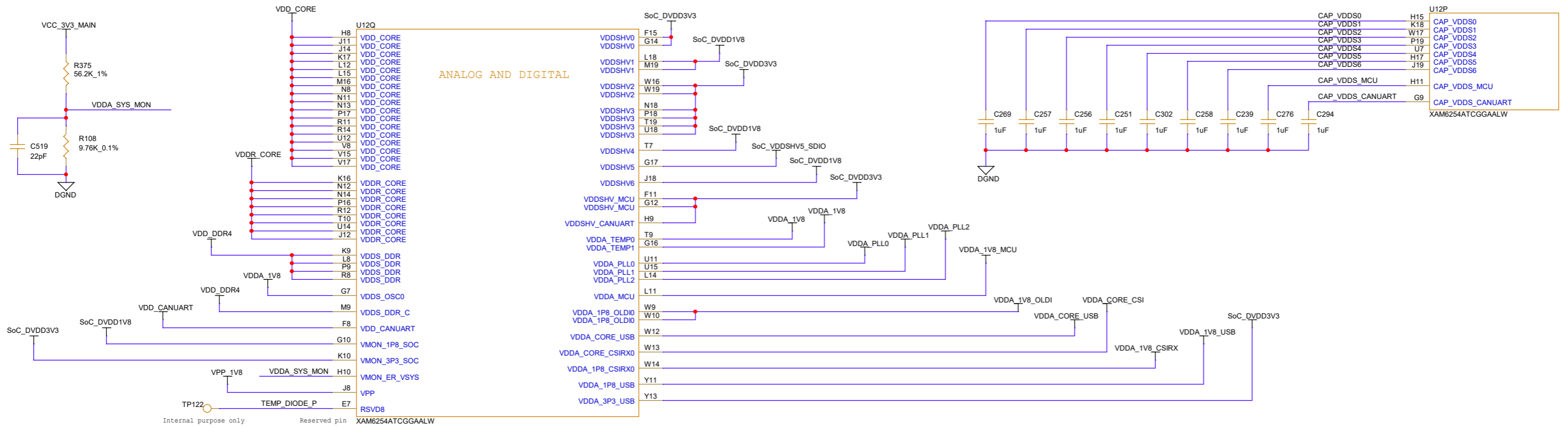
Rev A1

FULTON PMIC

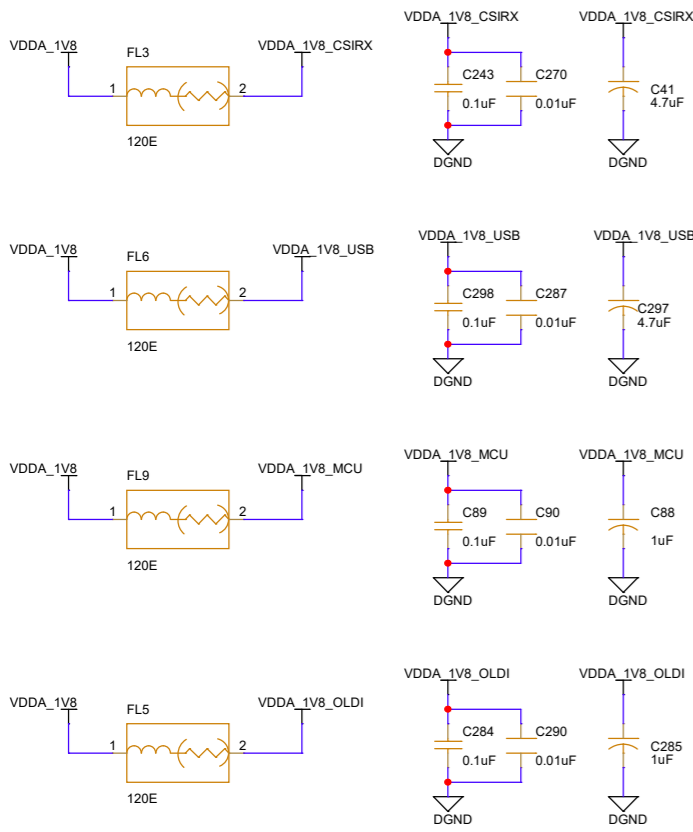
PMIC REGULATORS	VOLTAGE RAIL	CURRENT (mA)
BUCK 1	VCC_CORE (0.85V)	2700
BUCK 2	VCC_1V8	995
BUCK 3	VDD_1V2	936
LDO 1	VDDSHV_SDIO	50
LDO 2	VDD_LDO2	150
LDO 3	VDDA1V8	200
LDO 4	VDD_2V5	300



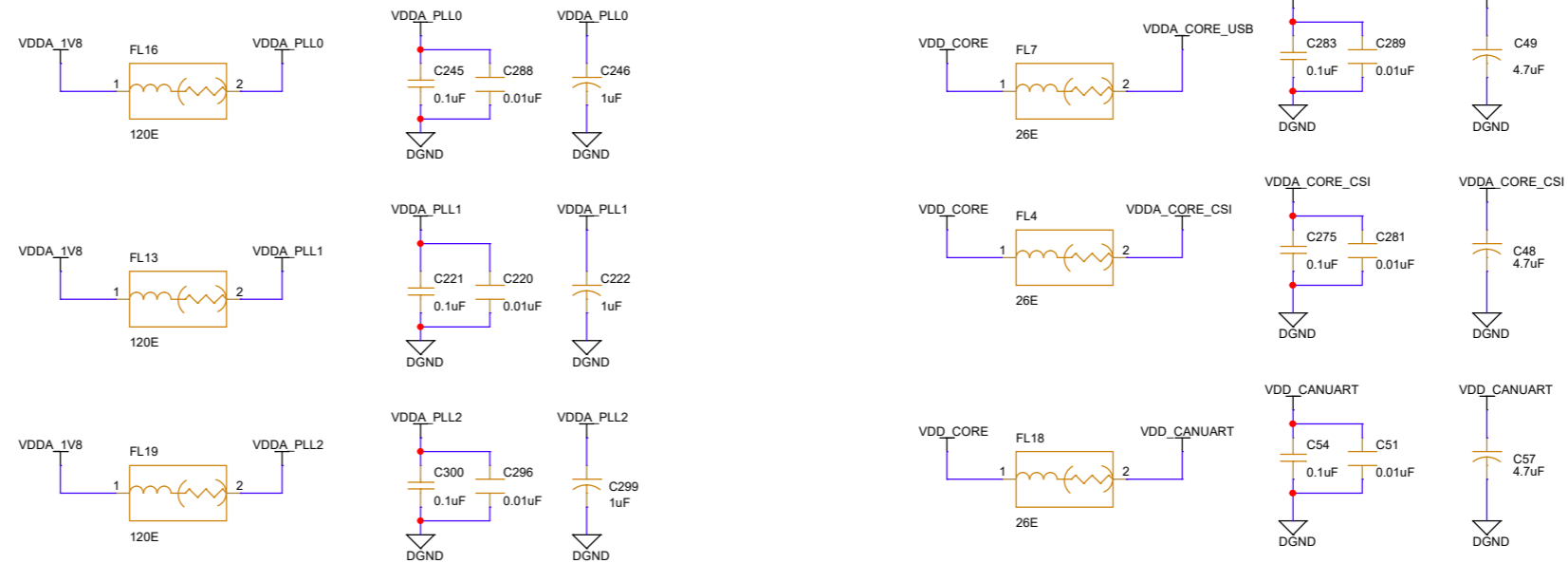
SOC POWER



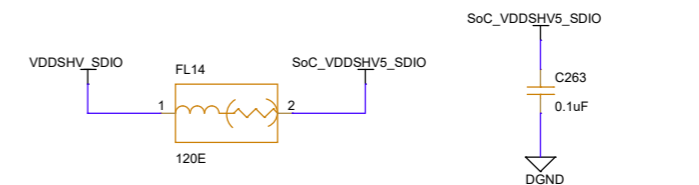
1.8V Analog SUPPLY



CORE SUPPLY



3.3V/1.8V MMC1 SUPPLY



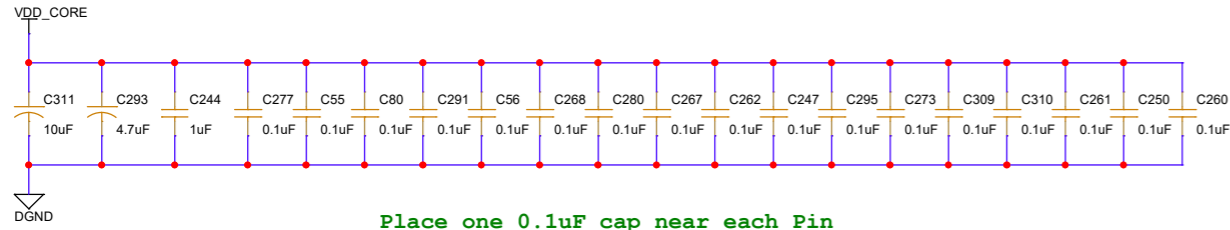
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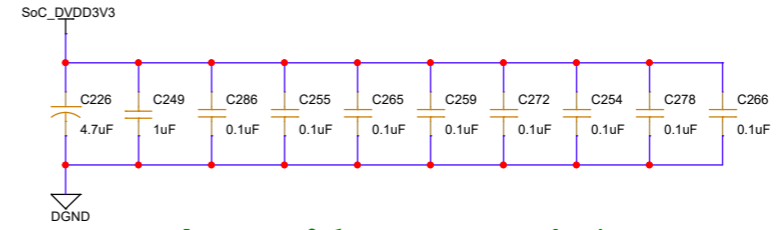
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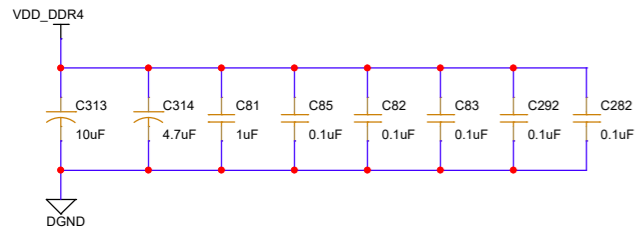
SOC POWER DECAPS



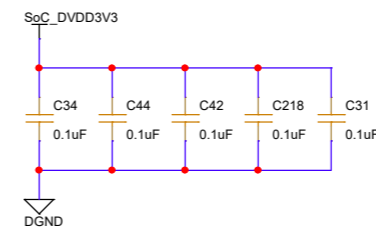
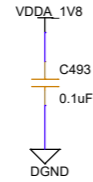
Place one 0.1uF cap near each Pin



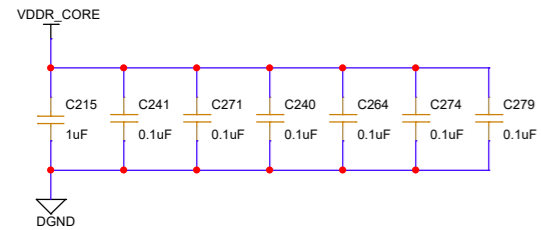
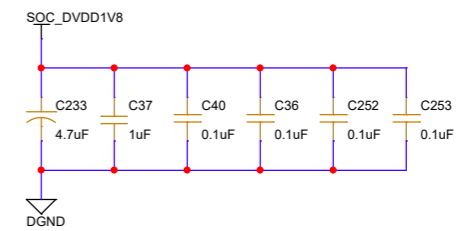
Place one 0.1uF cap near each Pin



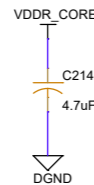
Place one 0.1uF cap near each Pin



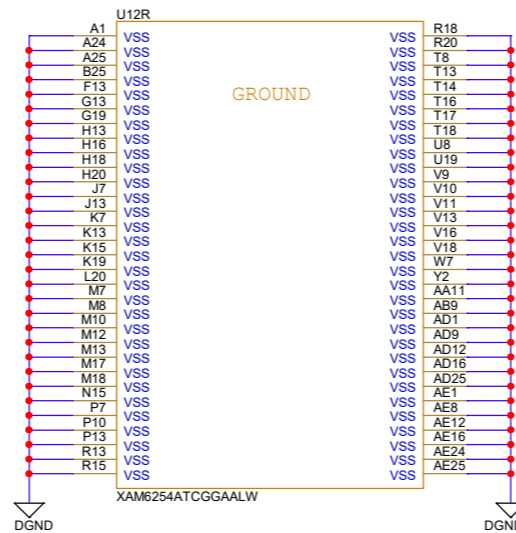
Place one 0.1uF cap near each Pin



Place one 0.1uF cap near each Pin



SOC VSS



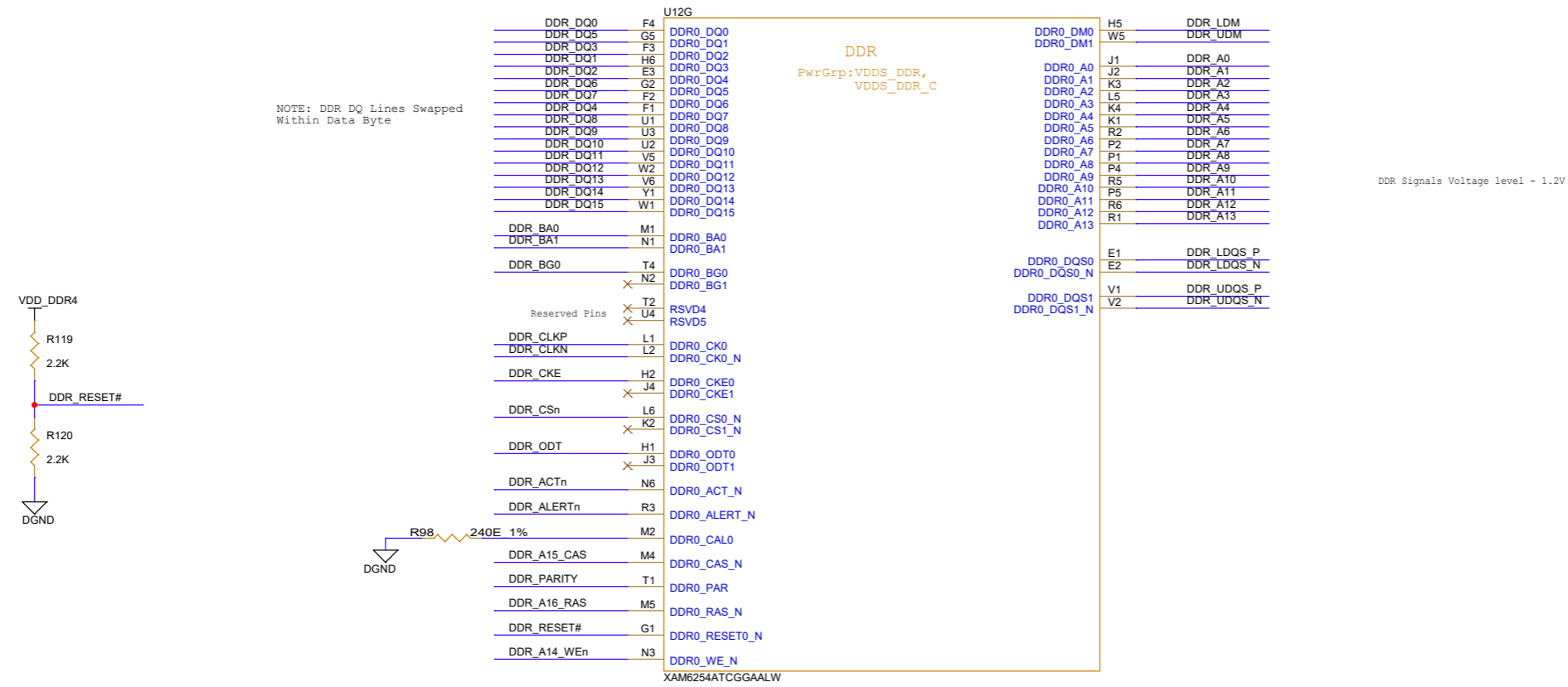
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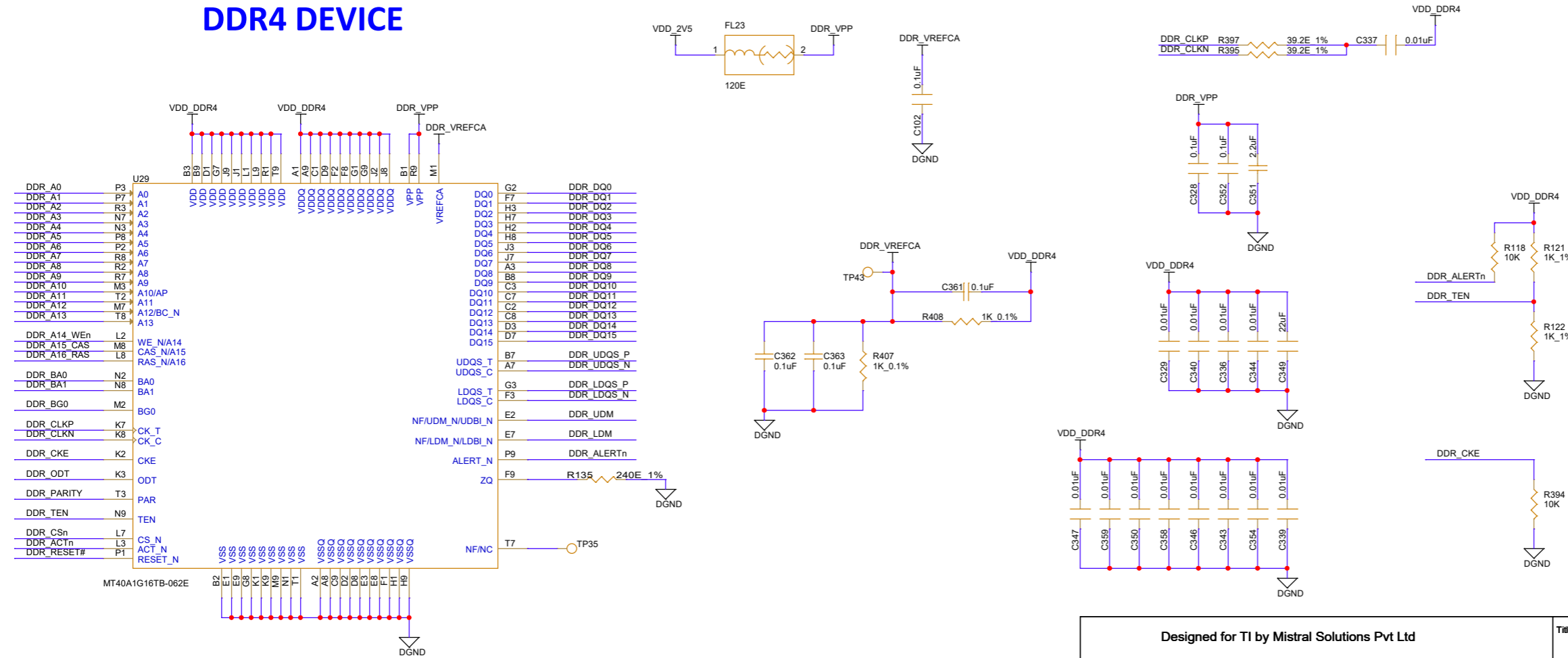
Title: SOC POWER CAPS & SOC VSS

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SOC DDR INTERFACE



DDR4 DEVICE

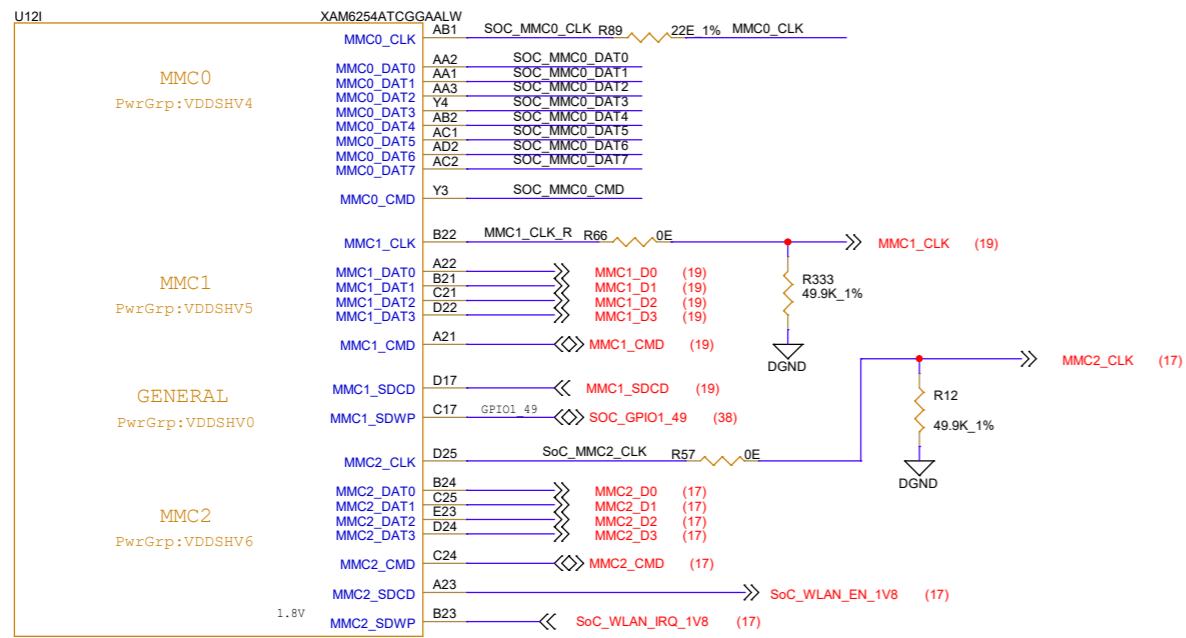


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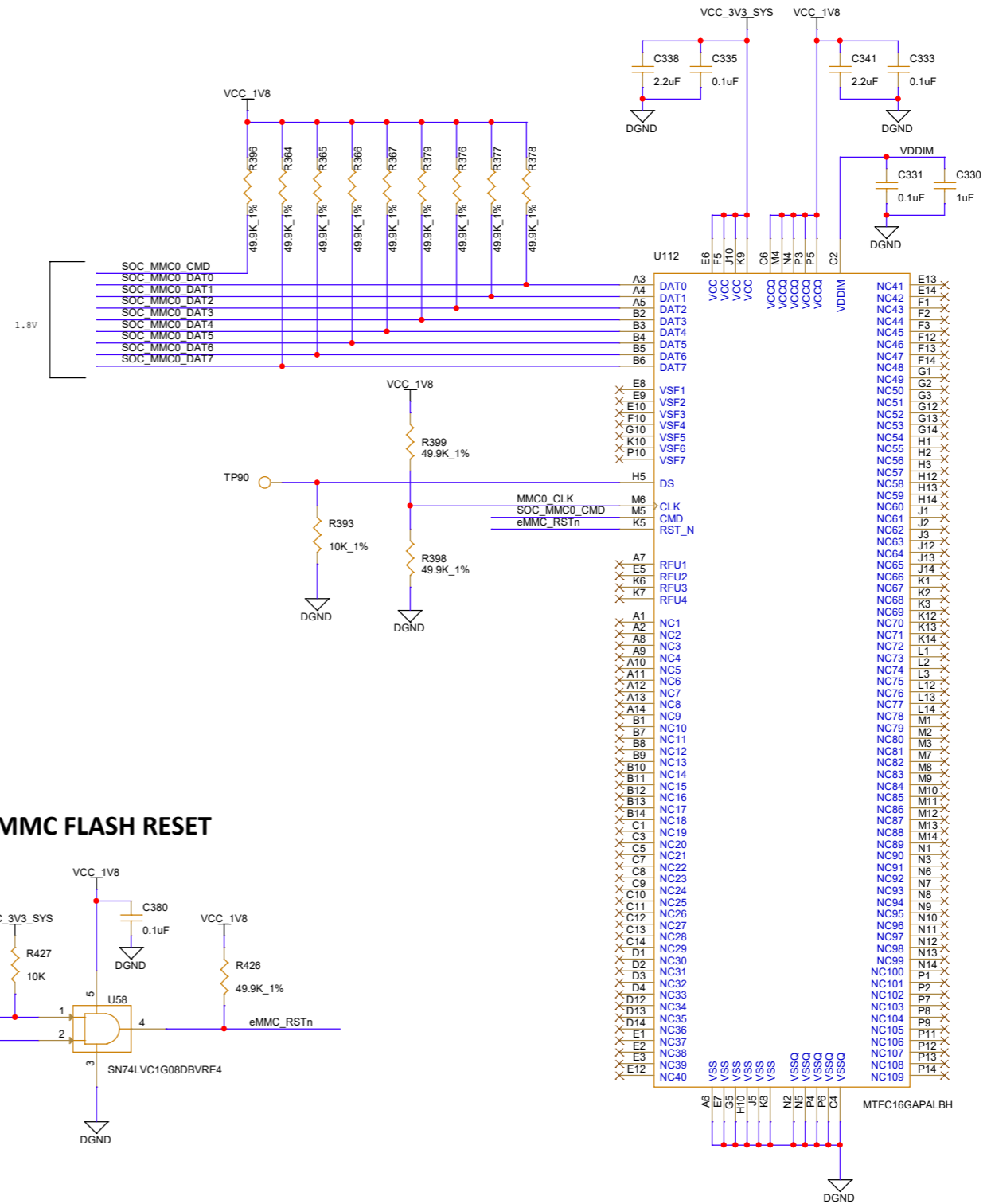
TEXAS INSTRUMENTS **MISTRAL**

Title: DDR4 Interface		Rev: A1
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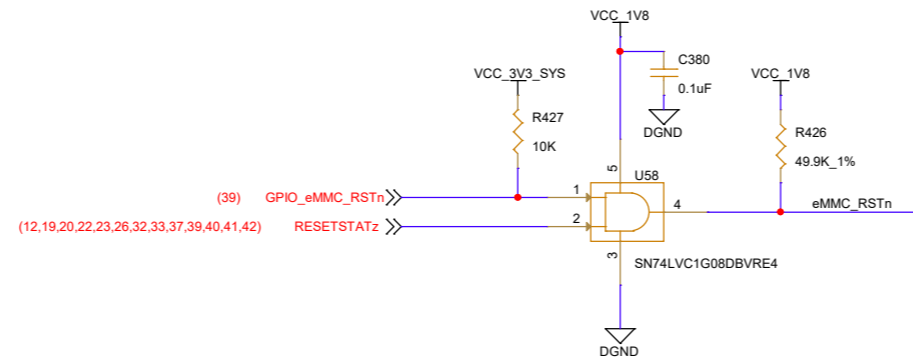
SOC - MMC Interface



eMMC FLASH



eMMC FLASH RESET



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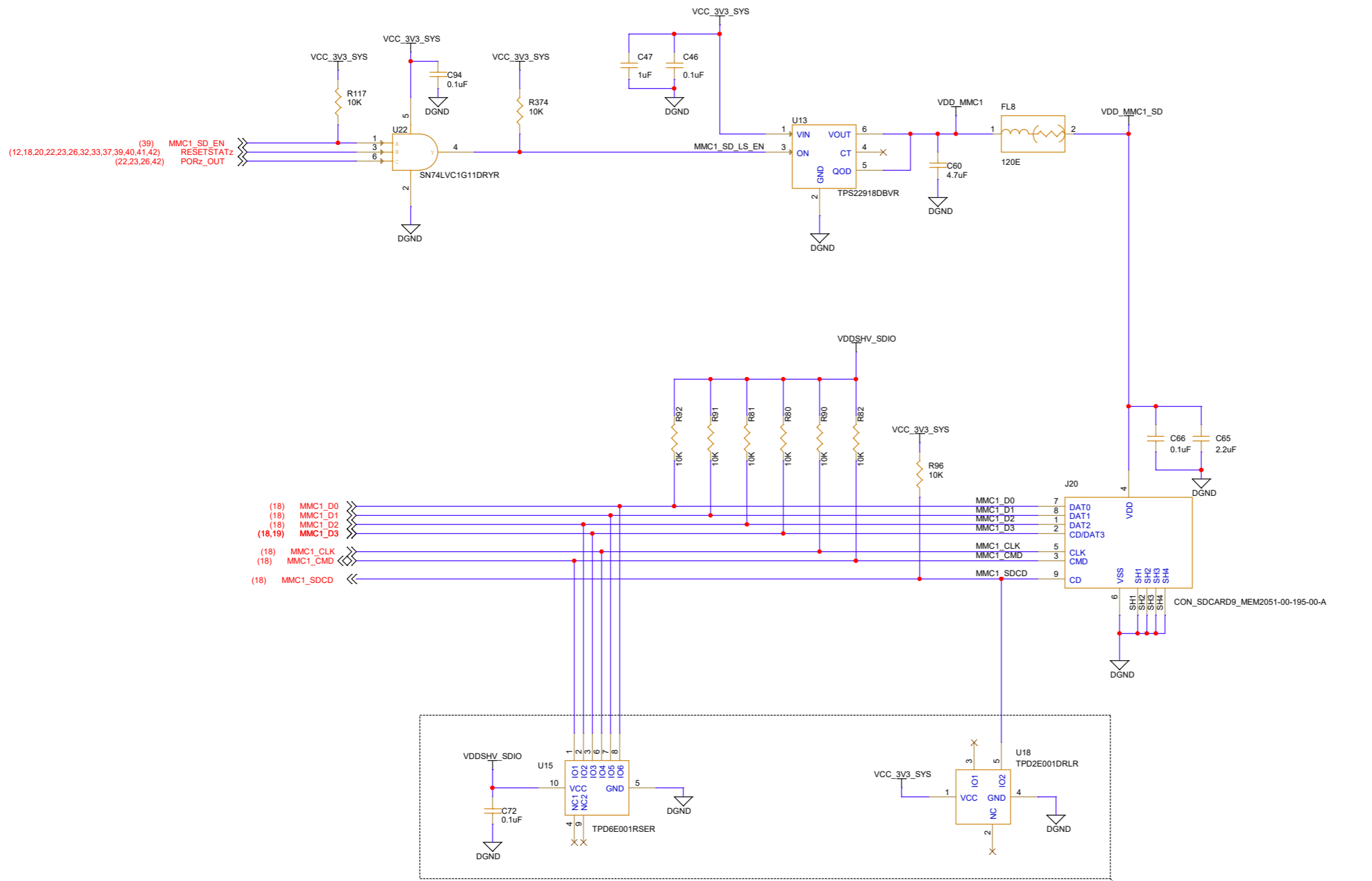
Title eMMC FLASH INTERFACE

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SD CARD INTERFACE

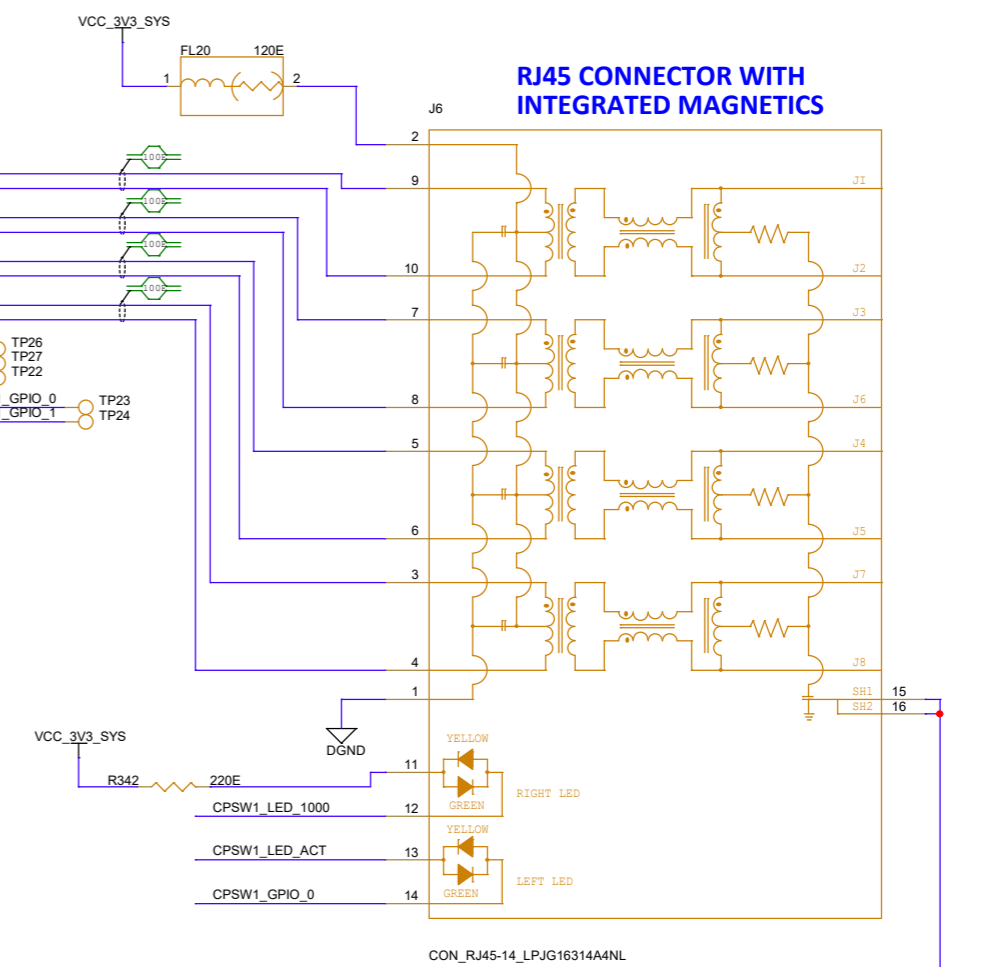
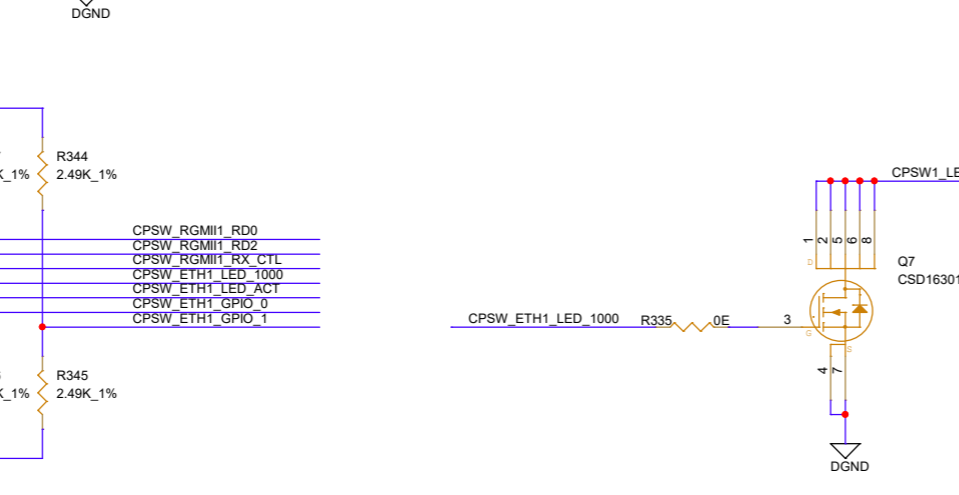
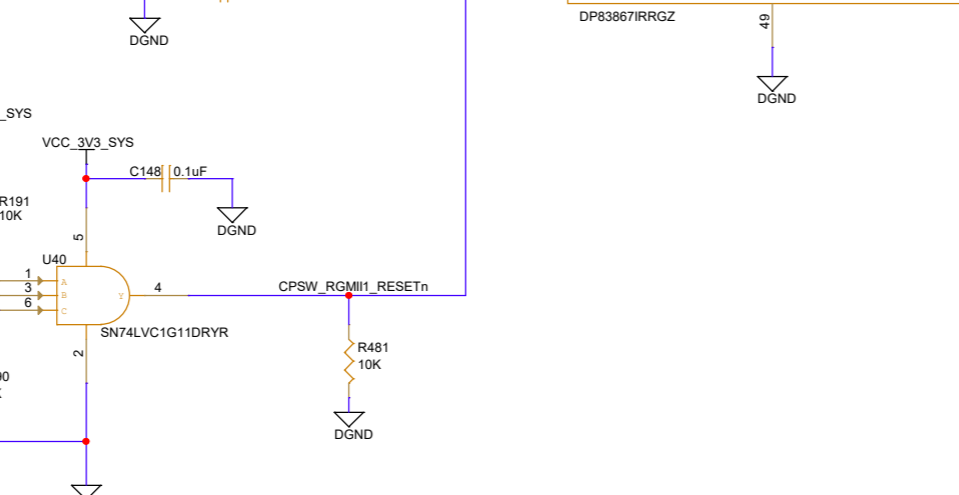
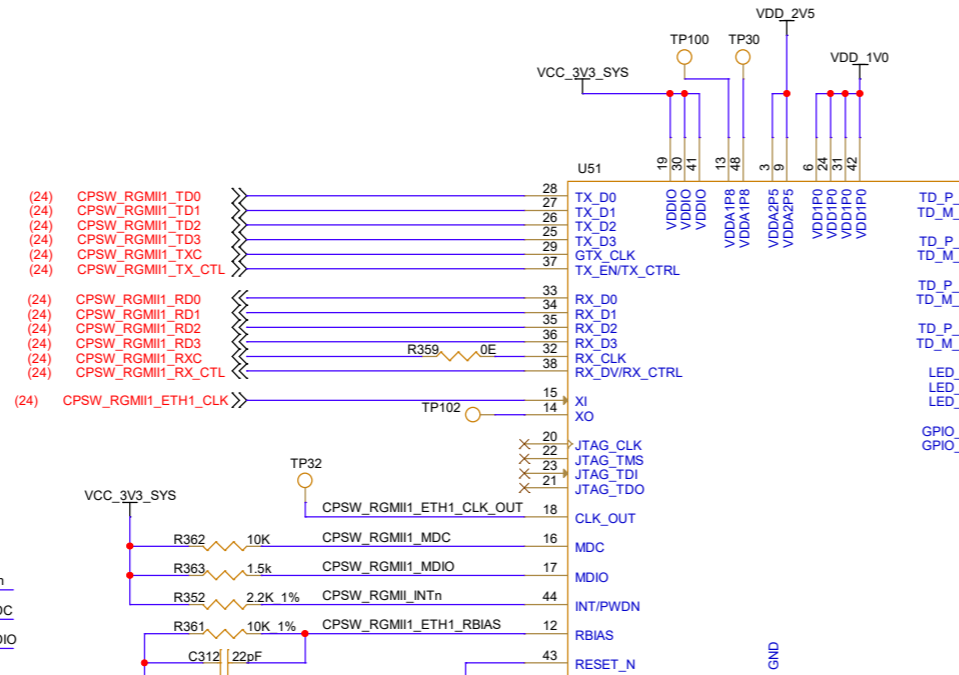
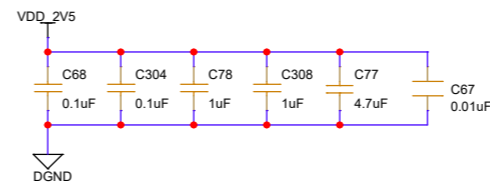
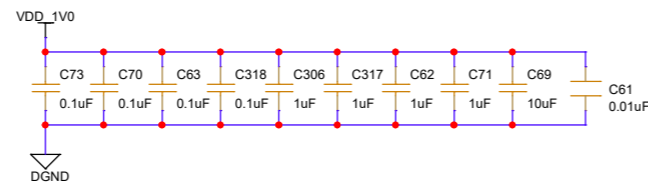
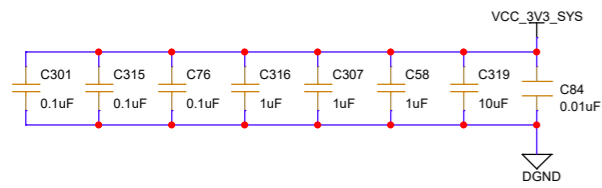
SD CARD RESET

LOAD SWITCH



Place near SD Card Connector

CPSW RGMII 1 - PHY

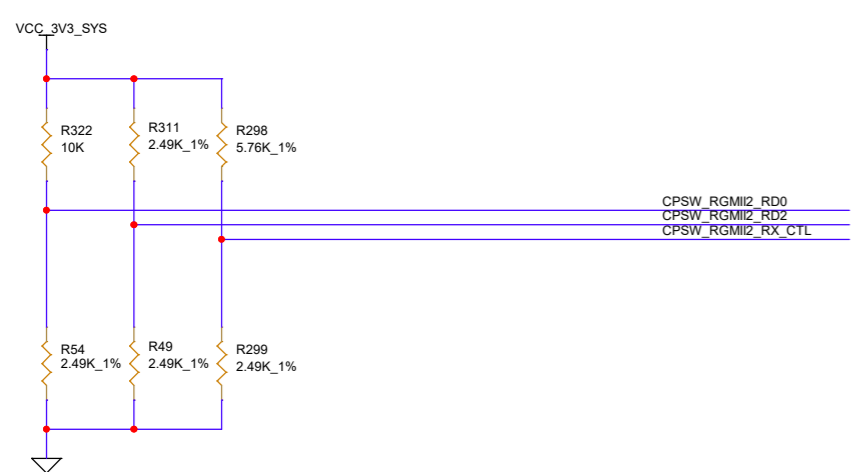
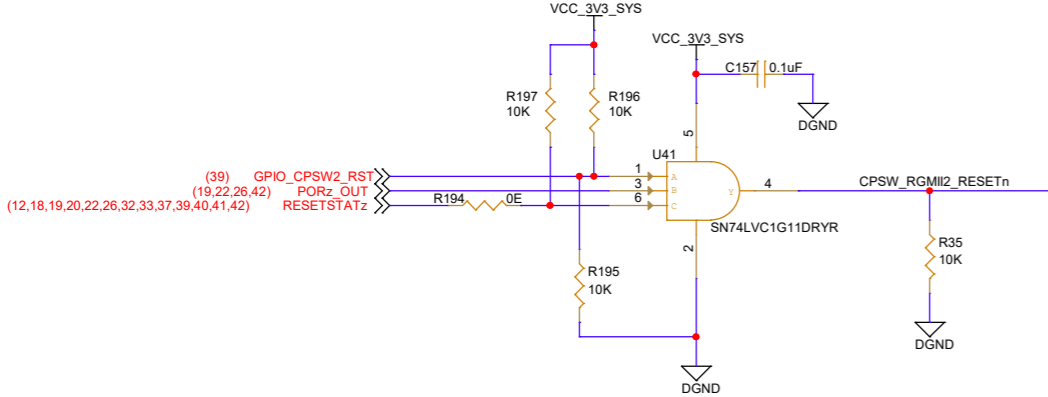
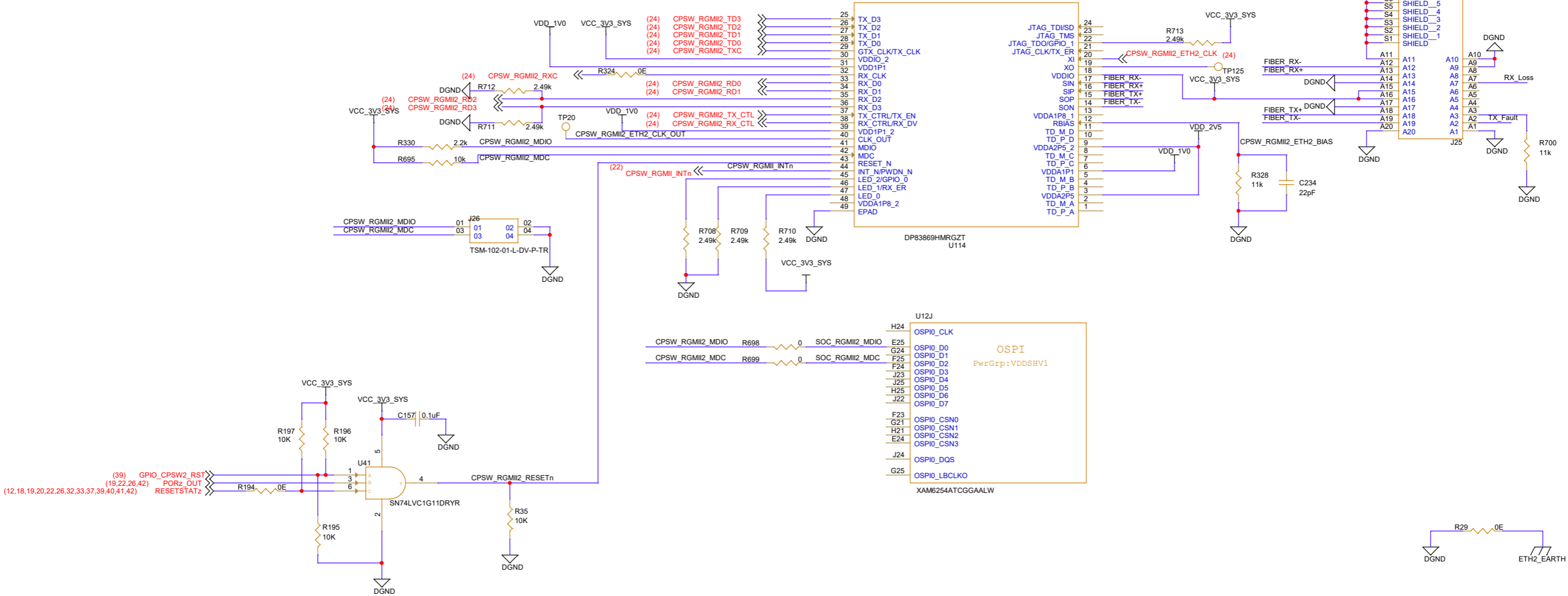
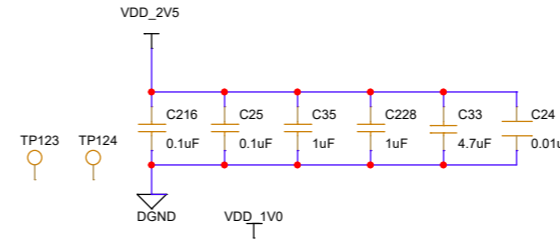
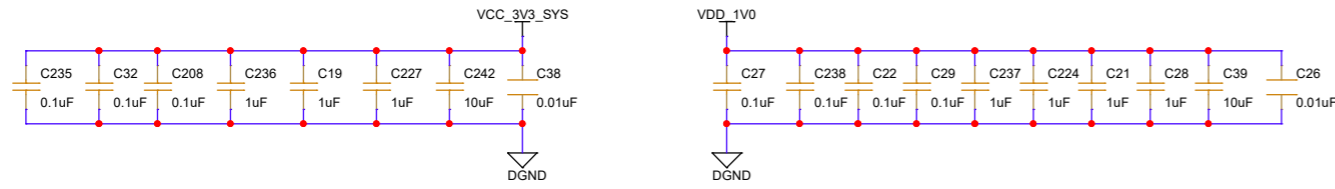


Silk: CPSW PHY-1

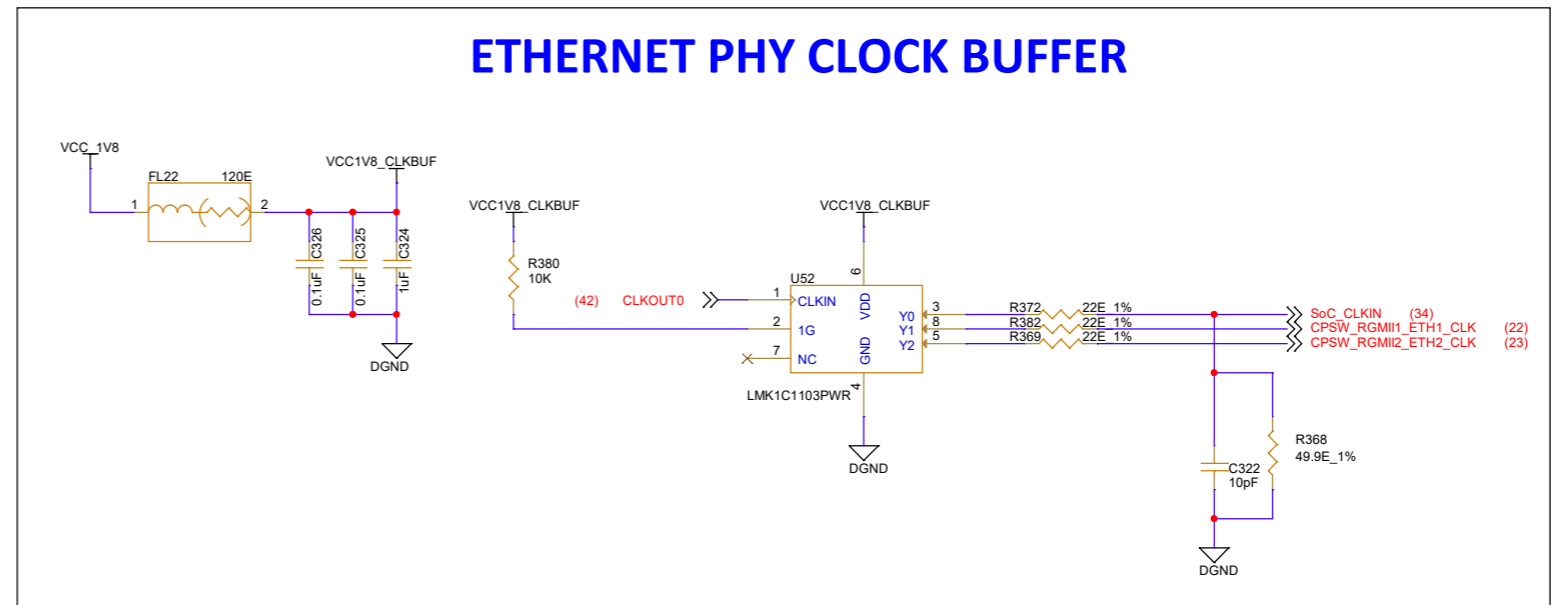
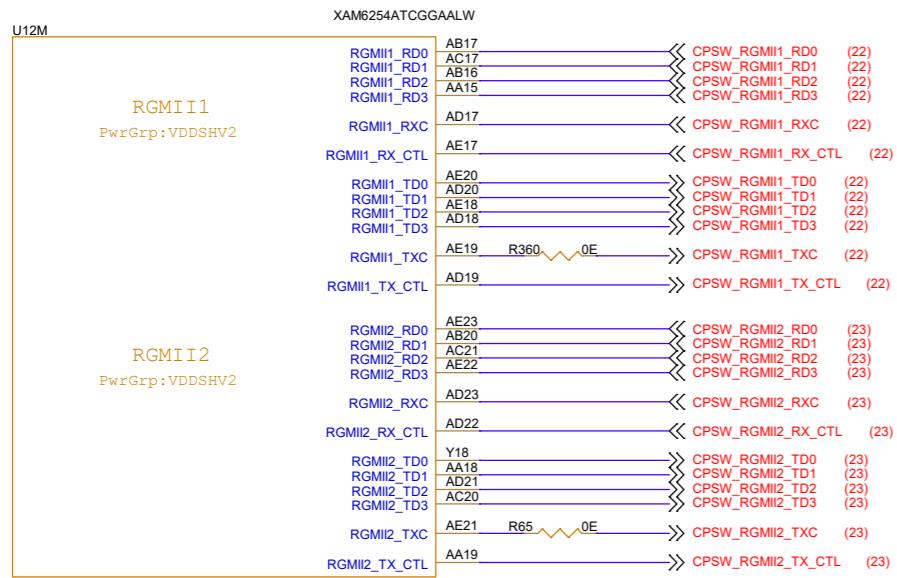
PHY ADDRESS = 00000
 Auto-negotiation Enabled
 10/100/1000 advertised, Auto-MDI-X
 Tx Clock Skew = 0ns
 Rx Clock Skew = 2ns

CPSW RGMII 2 - PHY

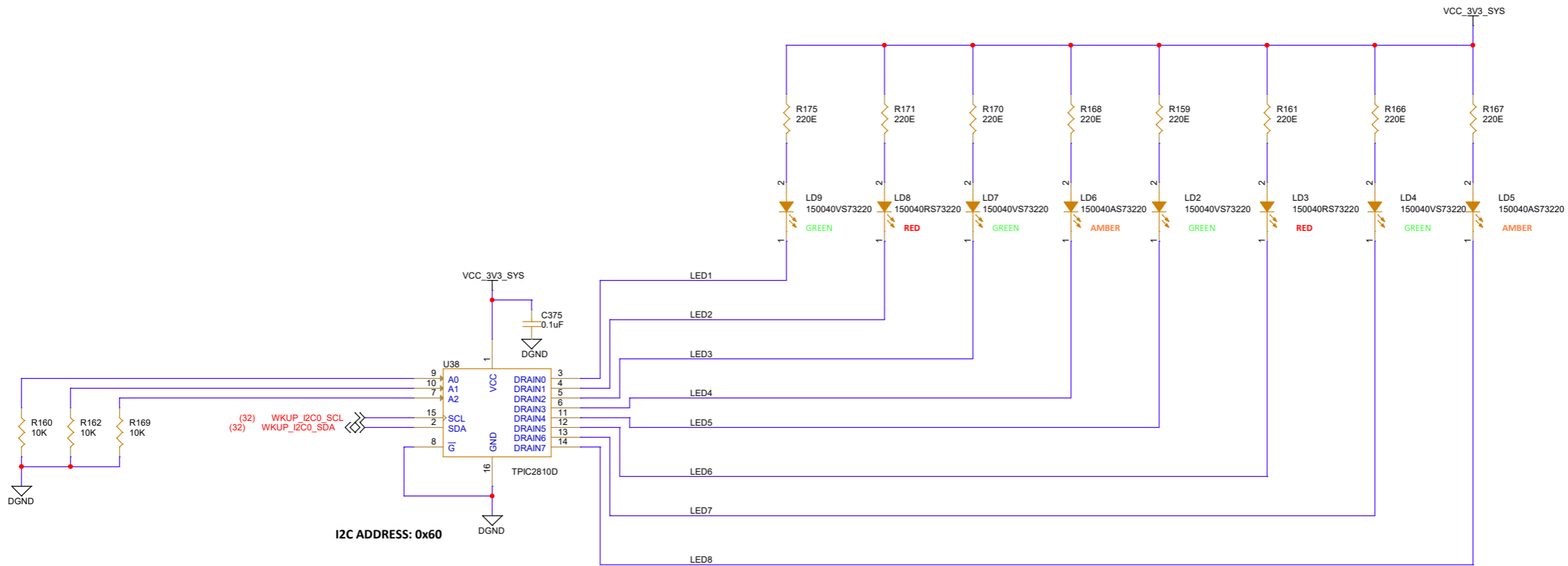
RJ45 CONNECTOR WITH INTEGRATED MAGNETICS



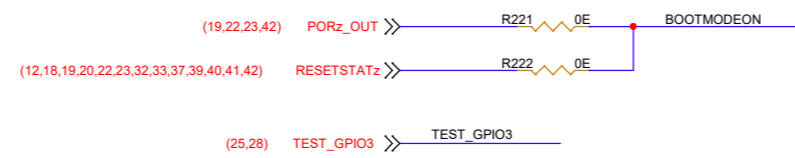
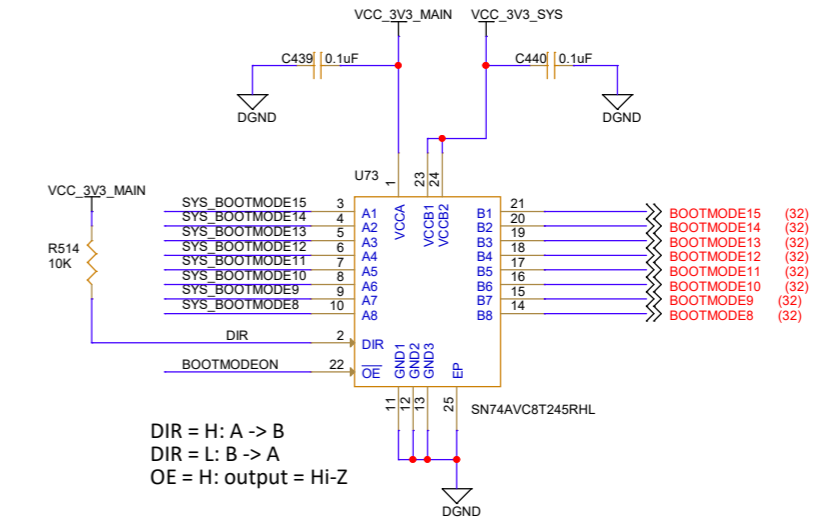
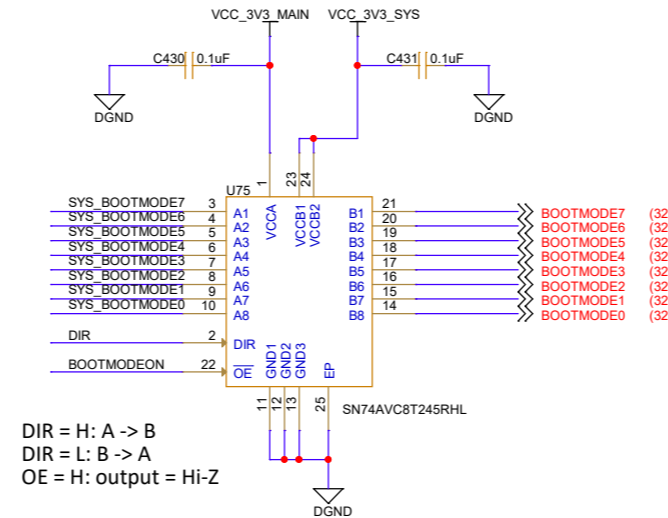
PHY ADDRESS = 00001
 Auto-negotiation Enabled
 10/100/1000 advertised, Auto-MDI-X
 Tx Clock Skew = 0ns
 Rx Clock Skew = 2ns



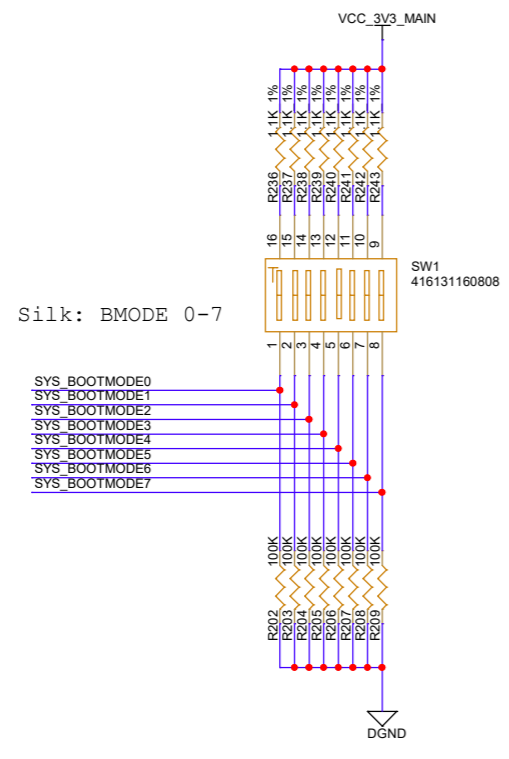
LED DRIVER



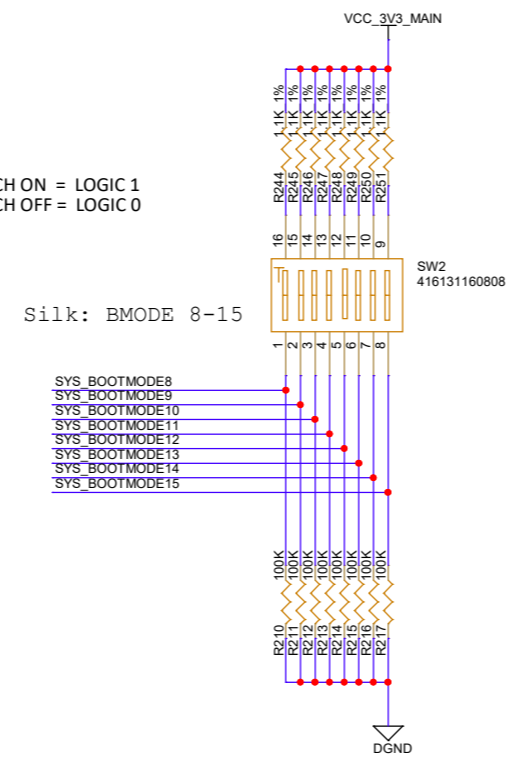
BOOT MODE BUFFERS



BOOT MODE SWITCHES

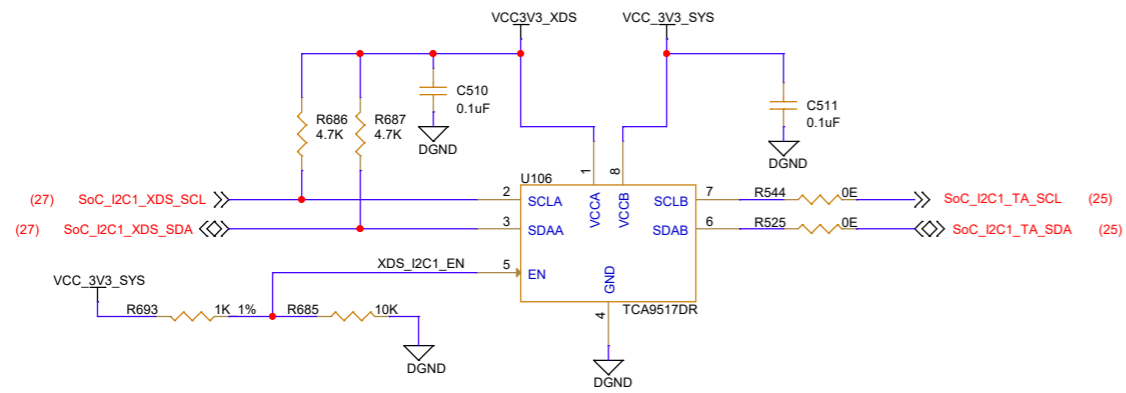


SWITCH ON = LOGIC 1
 SWITCH OFF = LOGIC 0

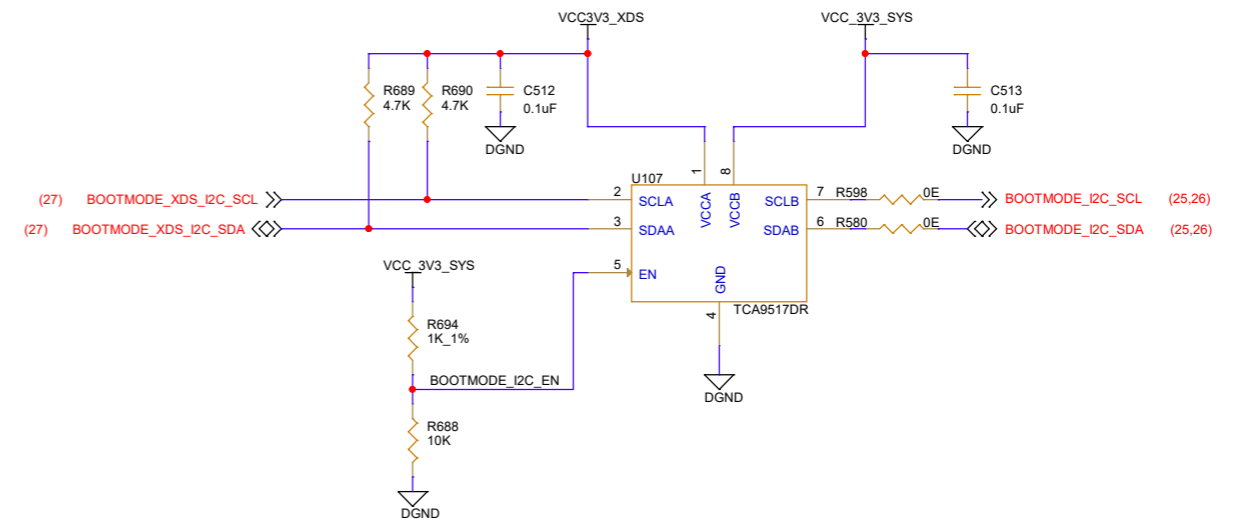


BOOT MODES SUPPORTED	
1.	OSPI
2.	MMC1 - SD CARD
3.	UART
4.	eMMC
5.	BACKUP BOOT OPTION

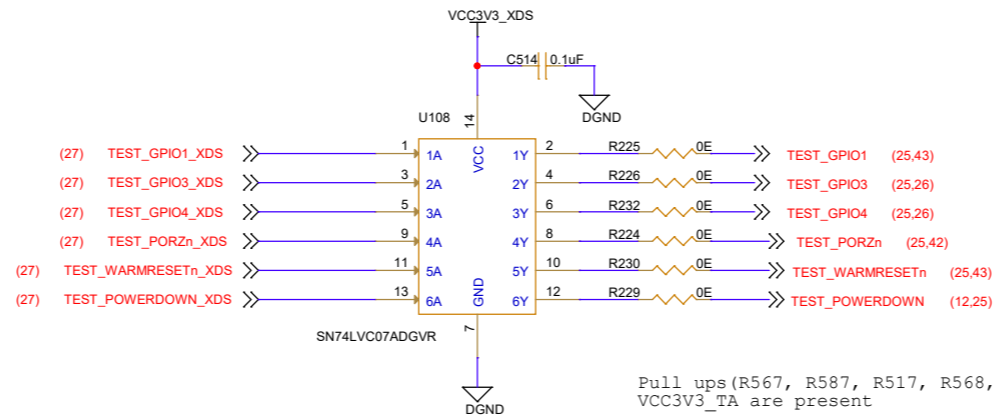
I2C_TA BUS BUFFER



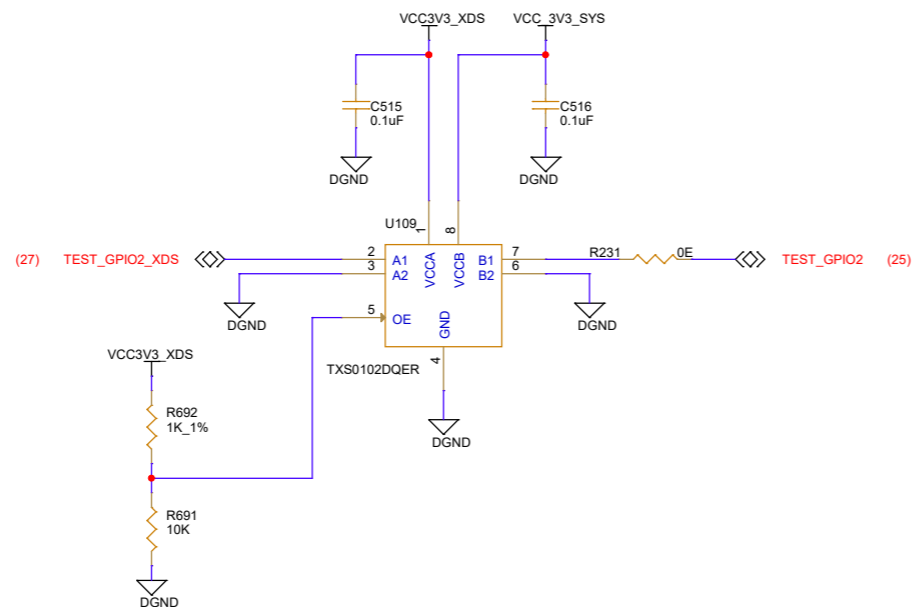
BOOTMODE_I2C_TA BUFFER



ISOLATION BUFFERS FOR TA SIGNALS



Pull ups (R567, R587, R517, R568, R585, R586 & R566) to VCC3V3_TA are present



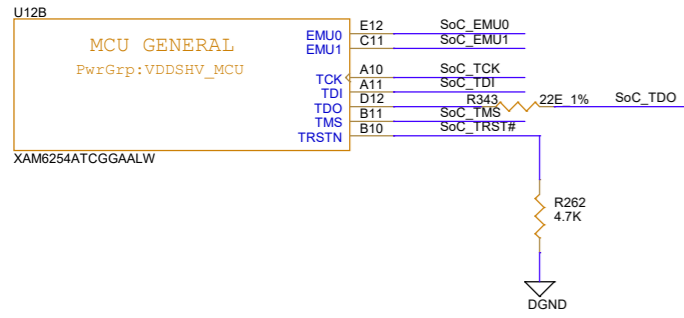
Designed for TI by Mistral Solutions Pvt Ltd



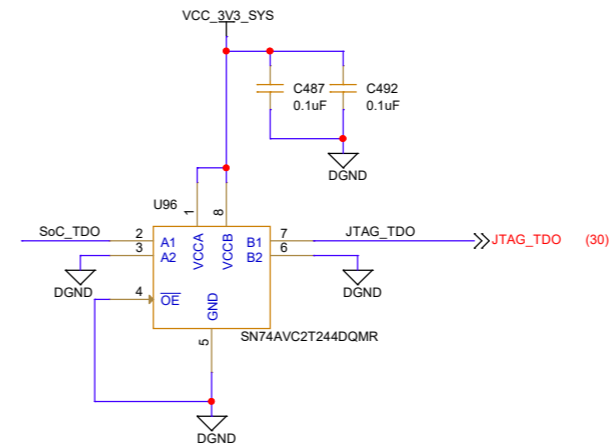
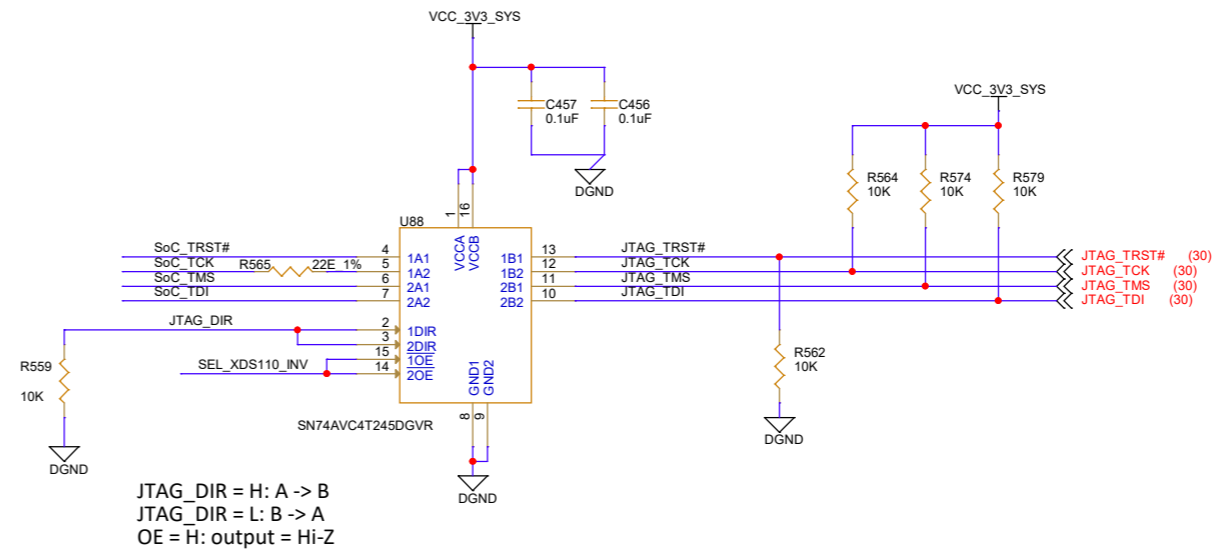
Title AUTOMATION SIGNALS BUFFER

Size	PROC142A1	Rev	A1
Date:	Friday, April 04, 2025	Sheet	28 of 44

JTAG SOC SECTION



cTI20 JTAG BUFFERS



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Title JTAG BUFFER

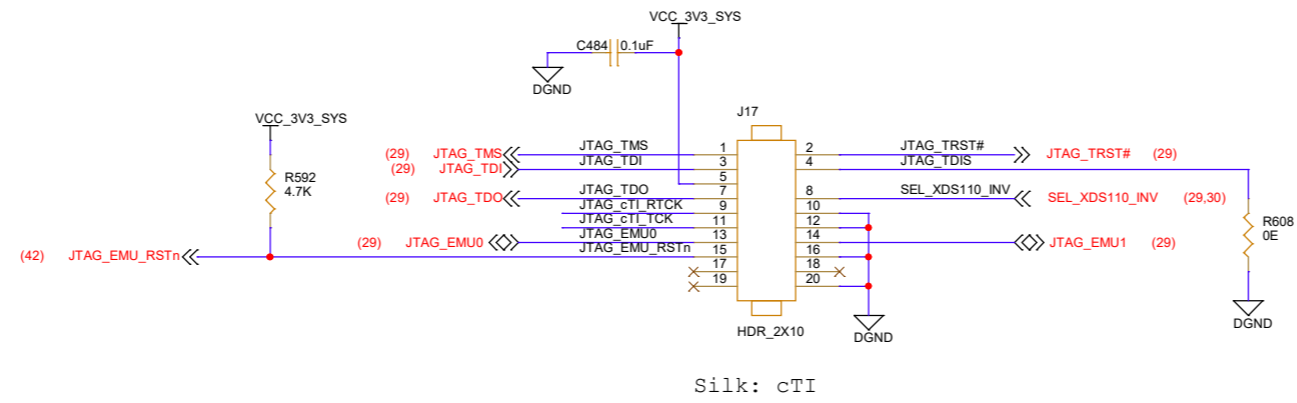
Size PROC142A1

Date: Wednesday, March 19, 2025

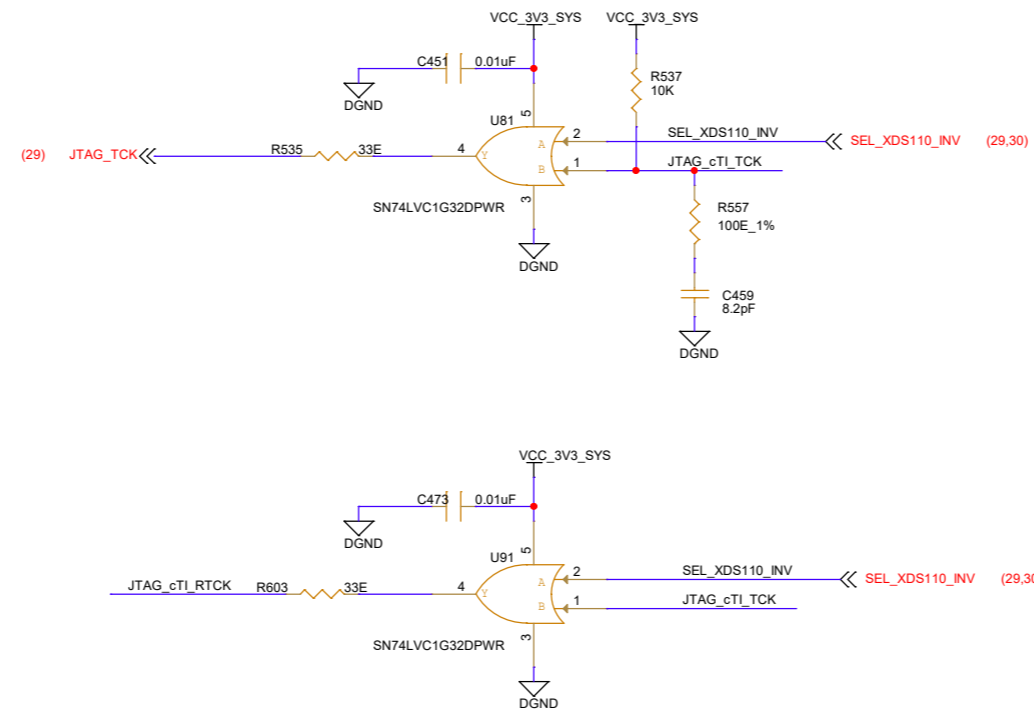
Sheet 29 of 44

Rev A1

JTAG 20 PIN cTI CONNECTOR



JTAG CLOCK BUFFER



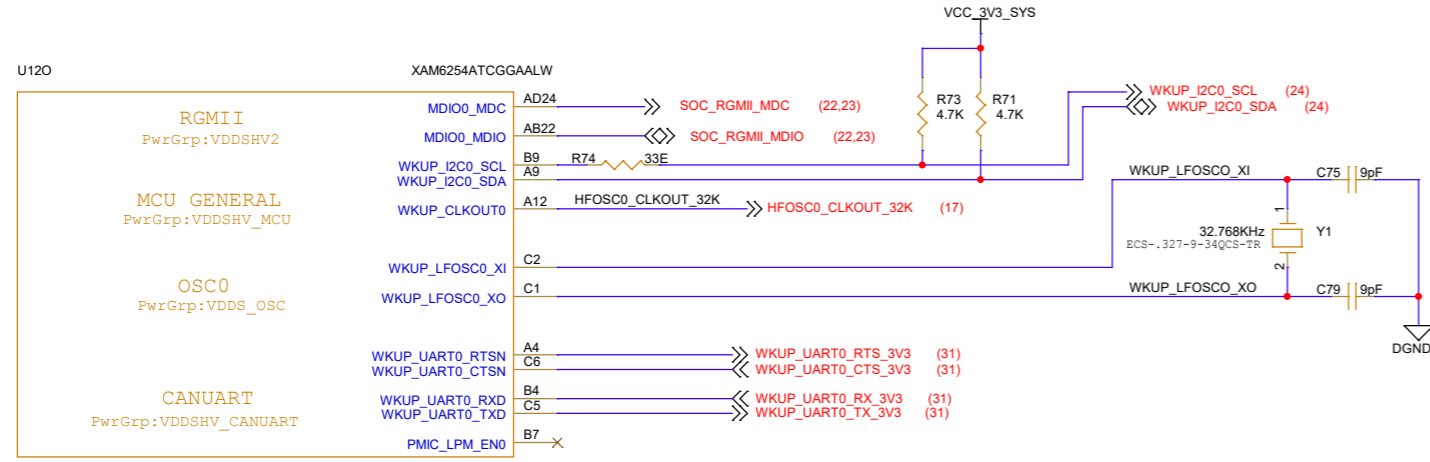
Designed for TI by Mistral Solutions Pvt Ltd



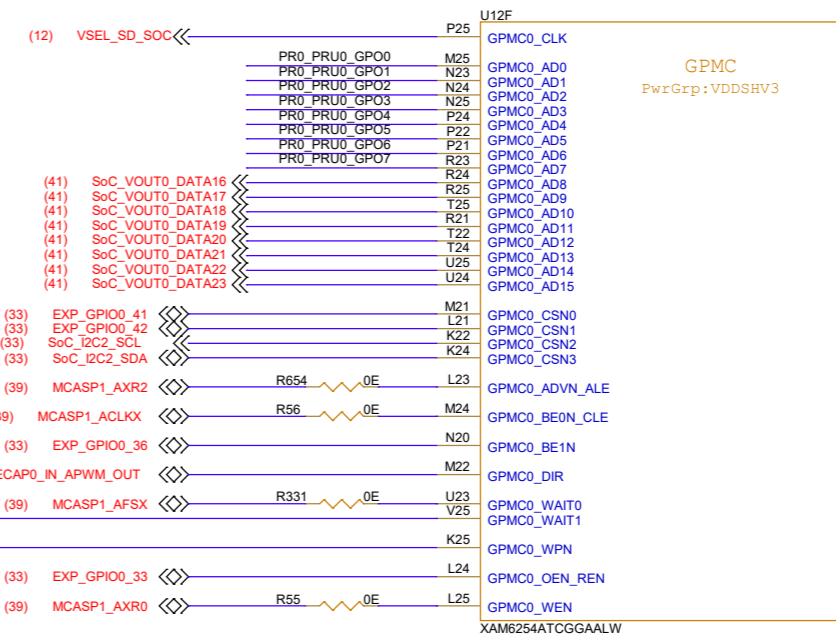
Title: JTAG 20 PIN cTI CONNECTOR

Size	PROC142A1	Rev	A1
C			
Date:	Sunday, April 13, 2025	Sheet	30 of 44

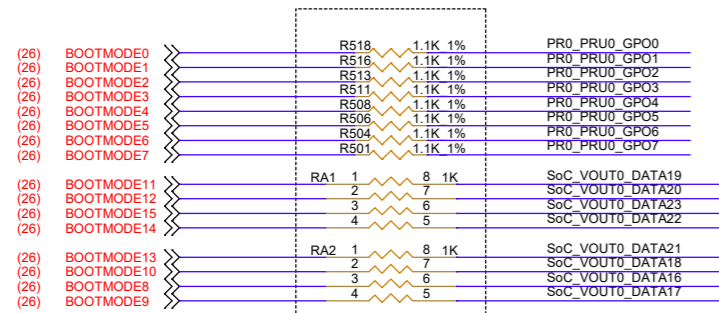
SOC WKUP DOMAIN



SOC GPMC

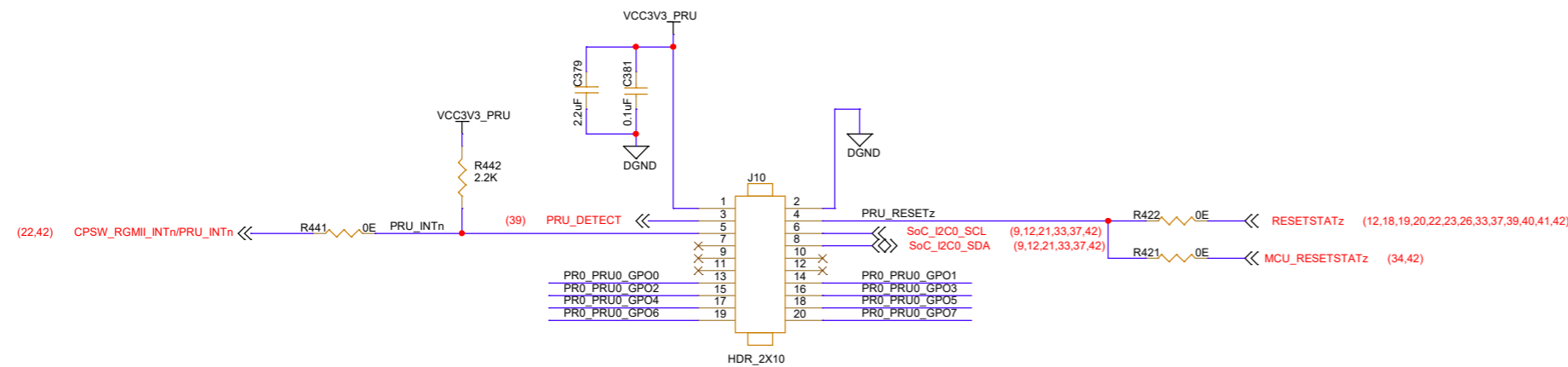


BOOTMODE PINS



NOTE: Resistors are used to isolate the BOOTMODE control logic after the value is latched

PRU HEADER



Silk: PRU HDR

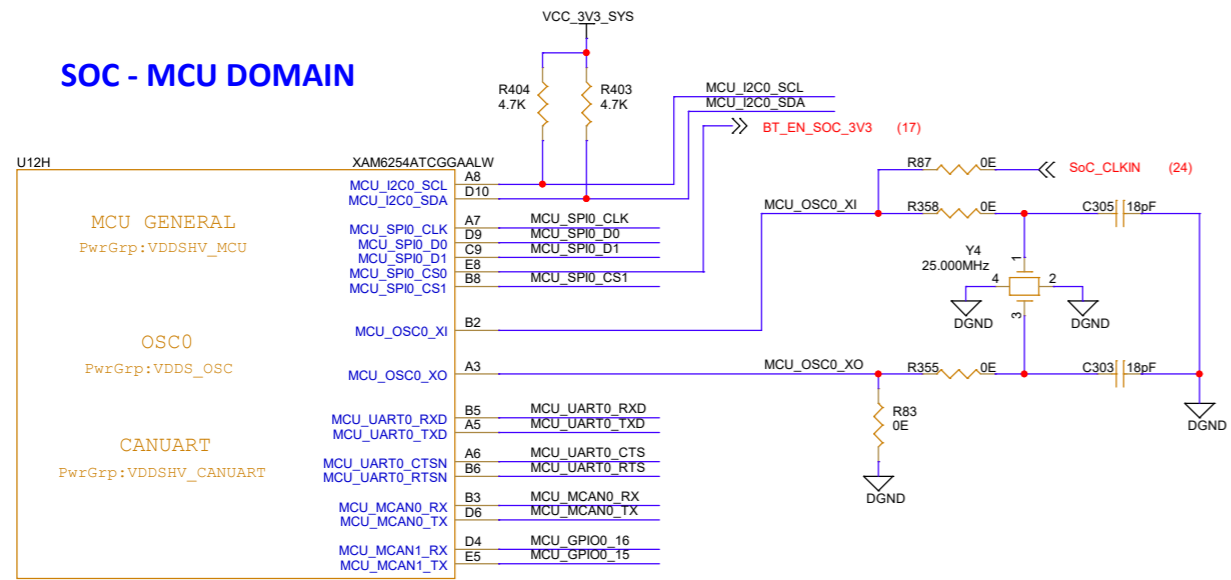
NOTE: PRU Header I/O are not fail-safe and shall not be driven when AM62x Starter Kit is not powered.

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Title		PRU HEADER	
Size	PROC142A1	Rev	A1
Date:	Sunday, April 13, 2025	Sheet	32 of 44

SOC - MCU DOMAIN



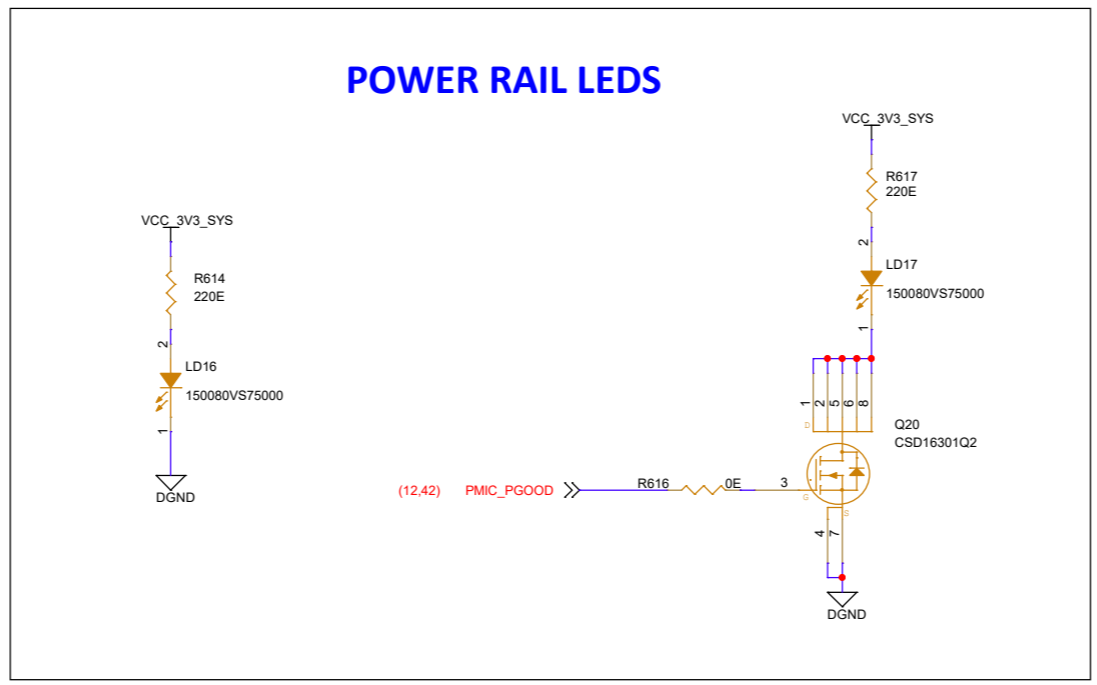
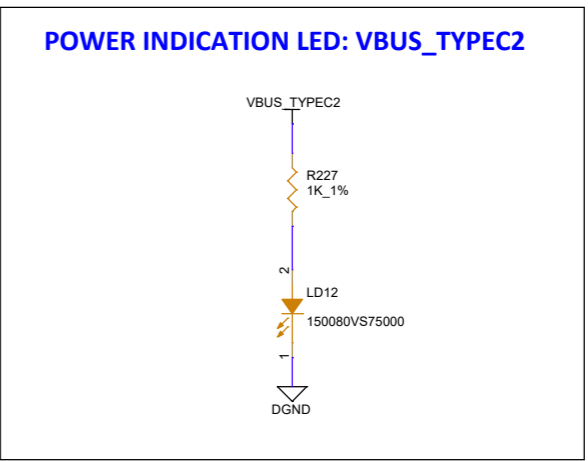
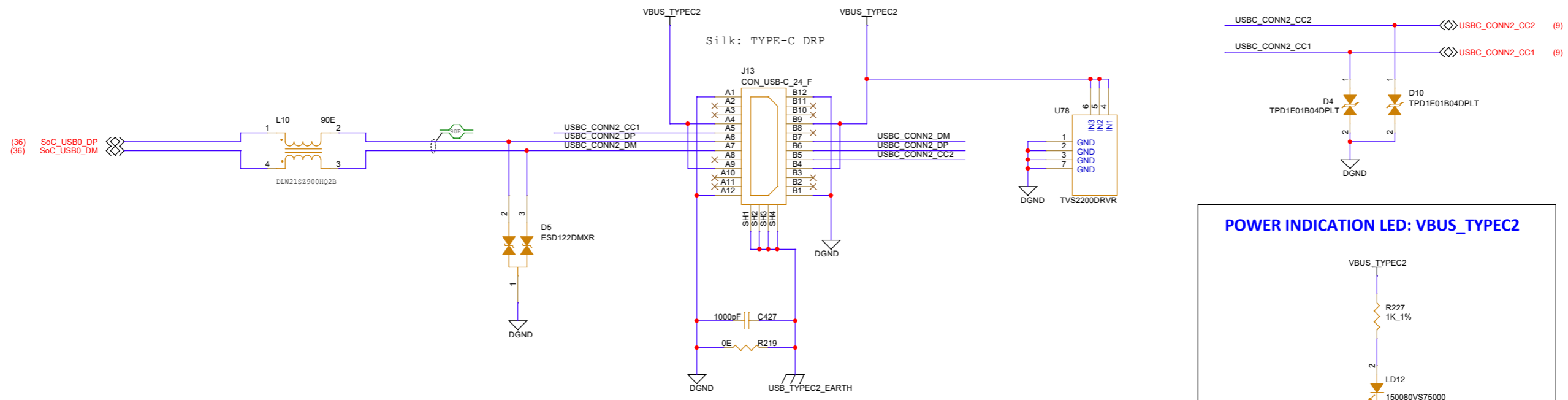
Designed for TI by Mistral Solutions Pvt Ltd



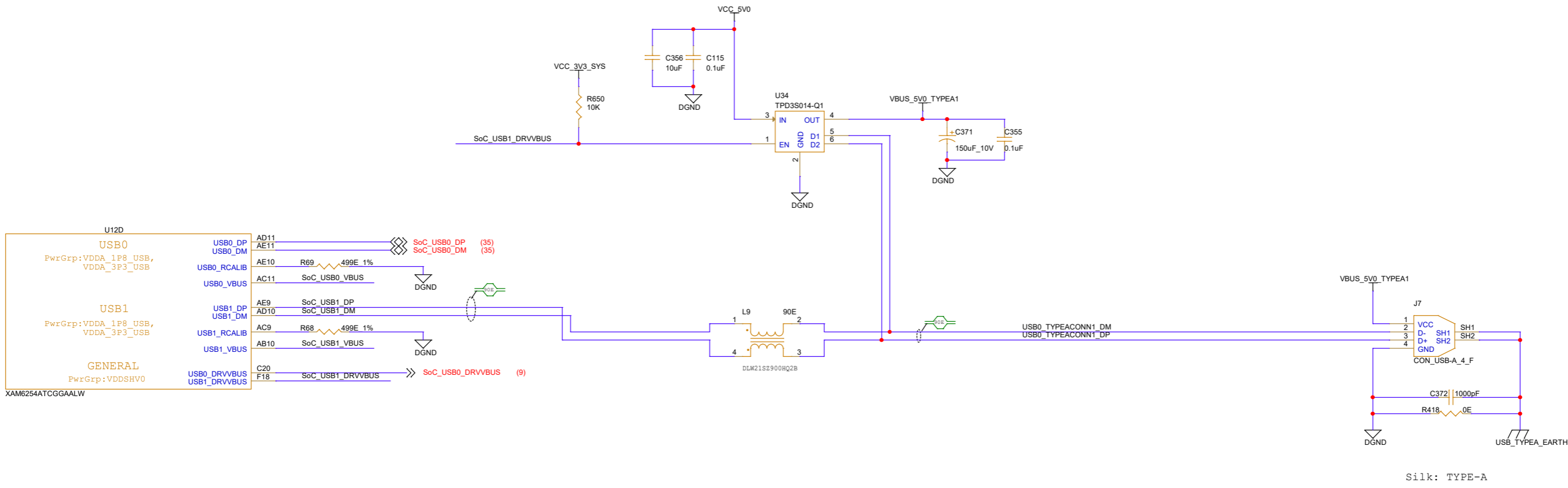
Title: MCU HEADER

Size	PROC142A1	Rev	A1
Date:	Sunday, April 13, 2025	Sheet	34 of 44

USB0 TYPE-C DRP



USB1 TYPE-A



U12D

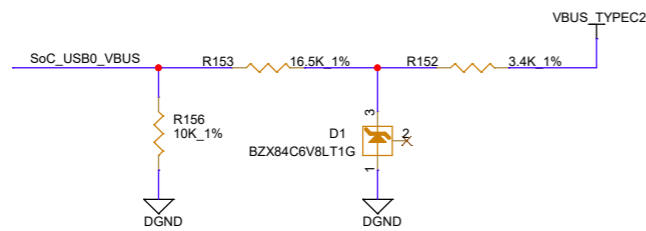
USB0	AD11	SoC_USB0_DP (35)
USB0_DM	AE11	SoC_USB0_DM (35)
USB0_RCALIB	AE10	R69 499E 1%
USB0_VBUS	AC11	SoC_USB0_VBUS
USB1	AE9	SoC_USB1_DP
USB1_DM	AD10	SoC_USB1_DM
USB1_RCALIB	AC9	R68 499E 1%
USB1_VBUS	AB10	SoC_USB1_VBUS
GENERAL	C20	SoC_USB1_DRVVBUS (9)
USB0_DRVVBUS	F18	SoC_USB1_DRVVBUS
USB1_DRVVBUS		

PwrGrp: VDDA_1P8_USB, VDDA_3P3_USB

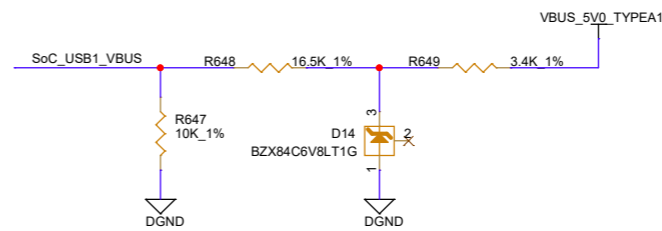
PwrGrp: VDDSHV0

XAM6254ATCGGAALW

Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS



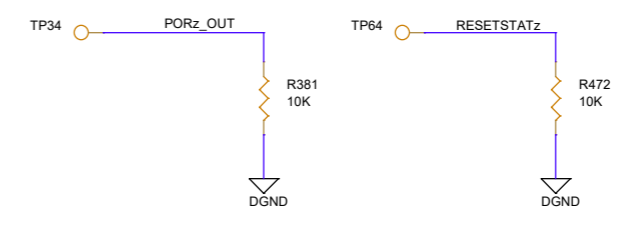
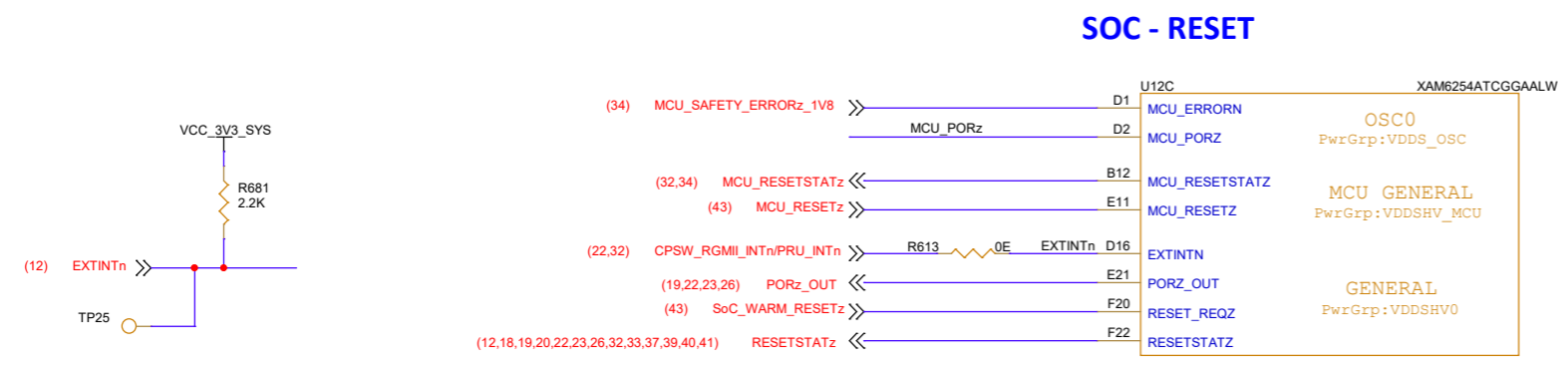
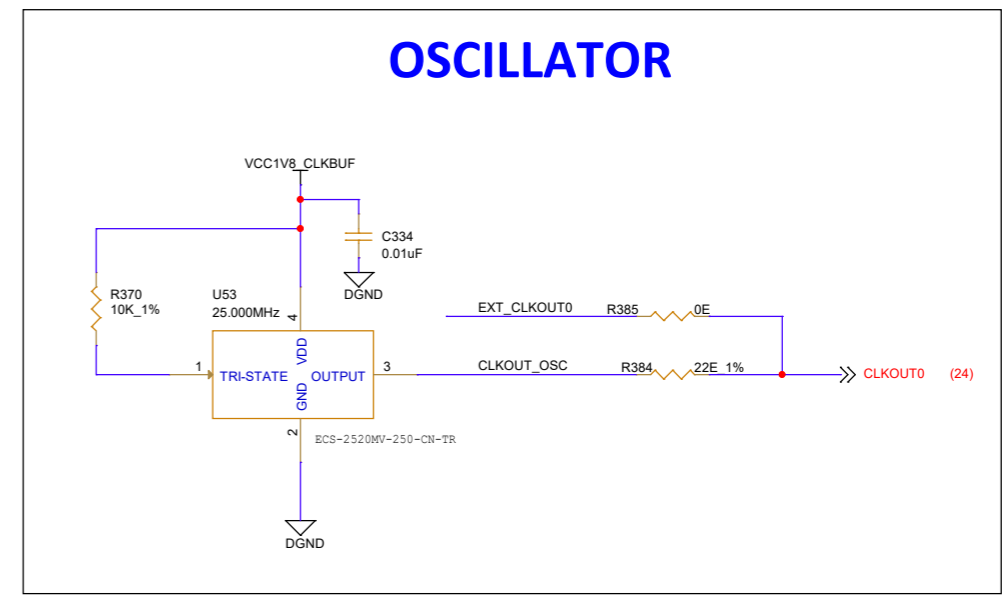
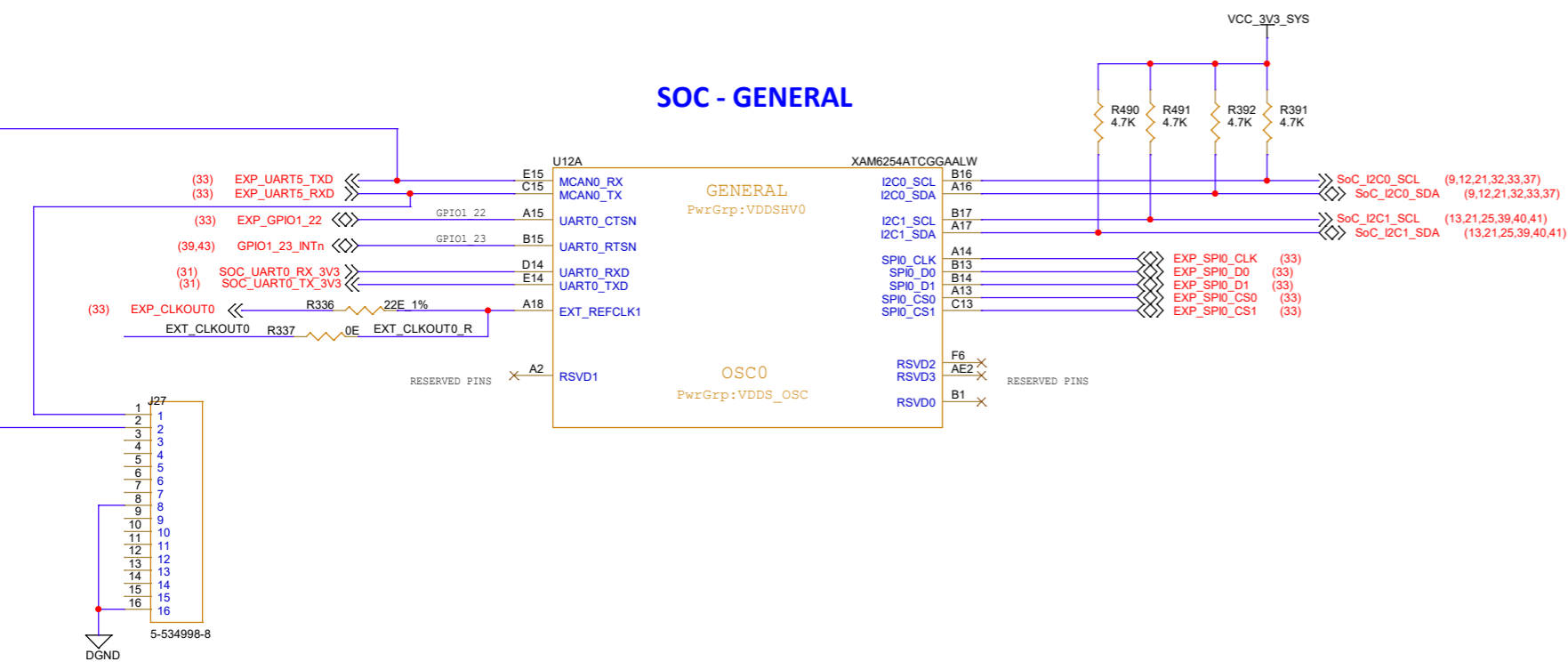
Note: Recommended VBUS circuit for SoC_USB1_VBUS



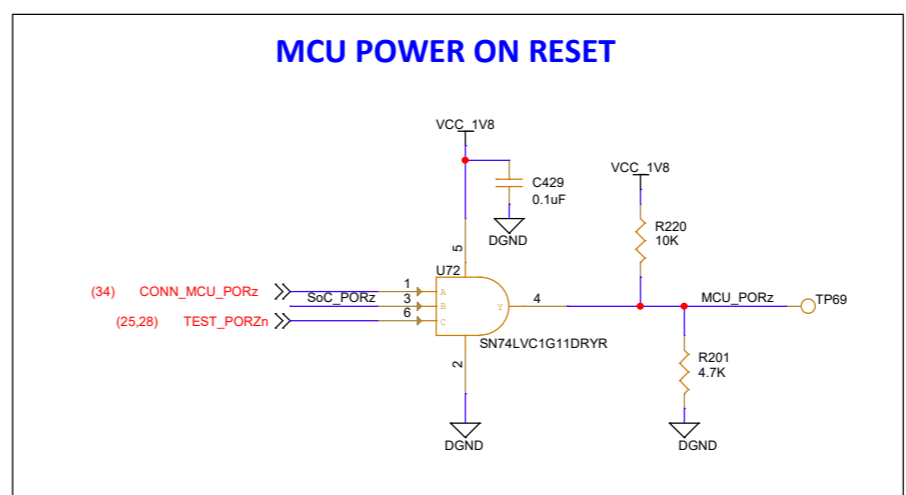
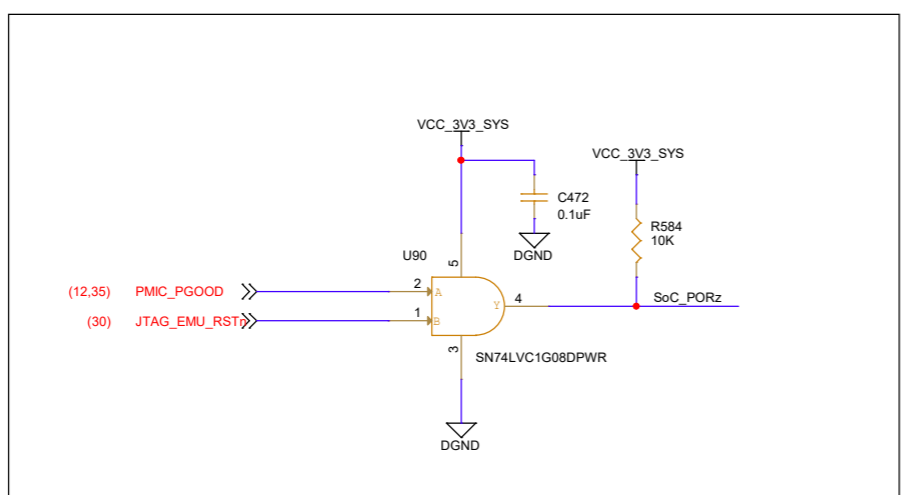
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Title		USB1 TYPE-A	
Size	PROC142A1	Rev	A1
C			
Date:	Sunday, April 13, 2025	Sheet	36 of 44

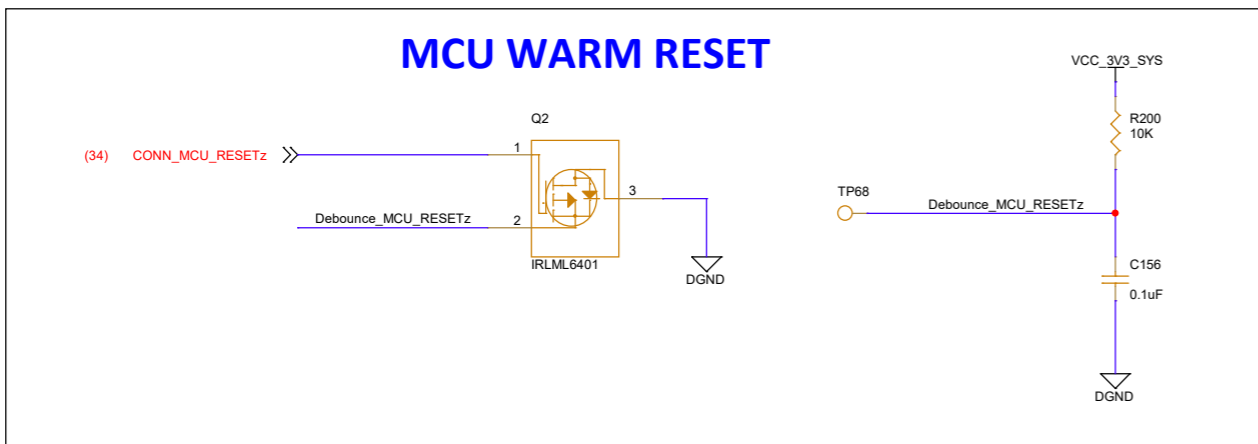


Full-down resistor on PORz_OUT is provided to keep the signal low until the processor is released from reset during the power-up sequence

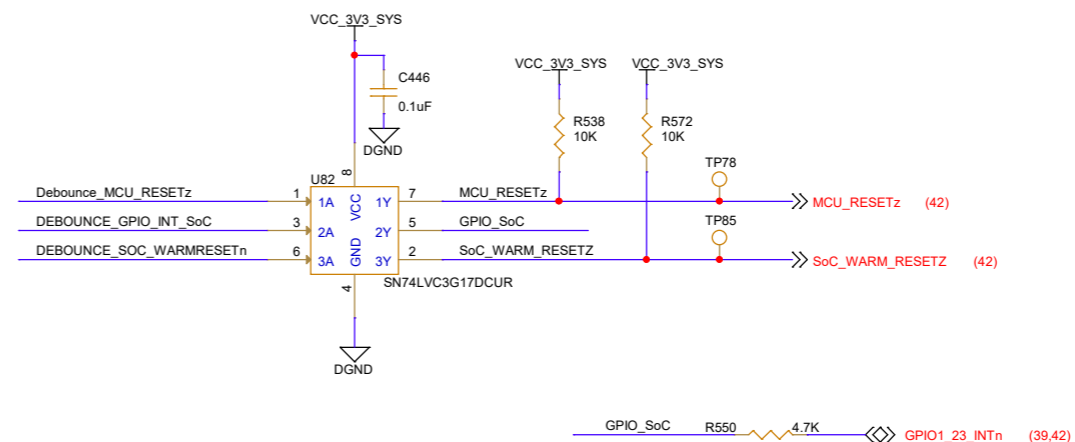


RESET

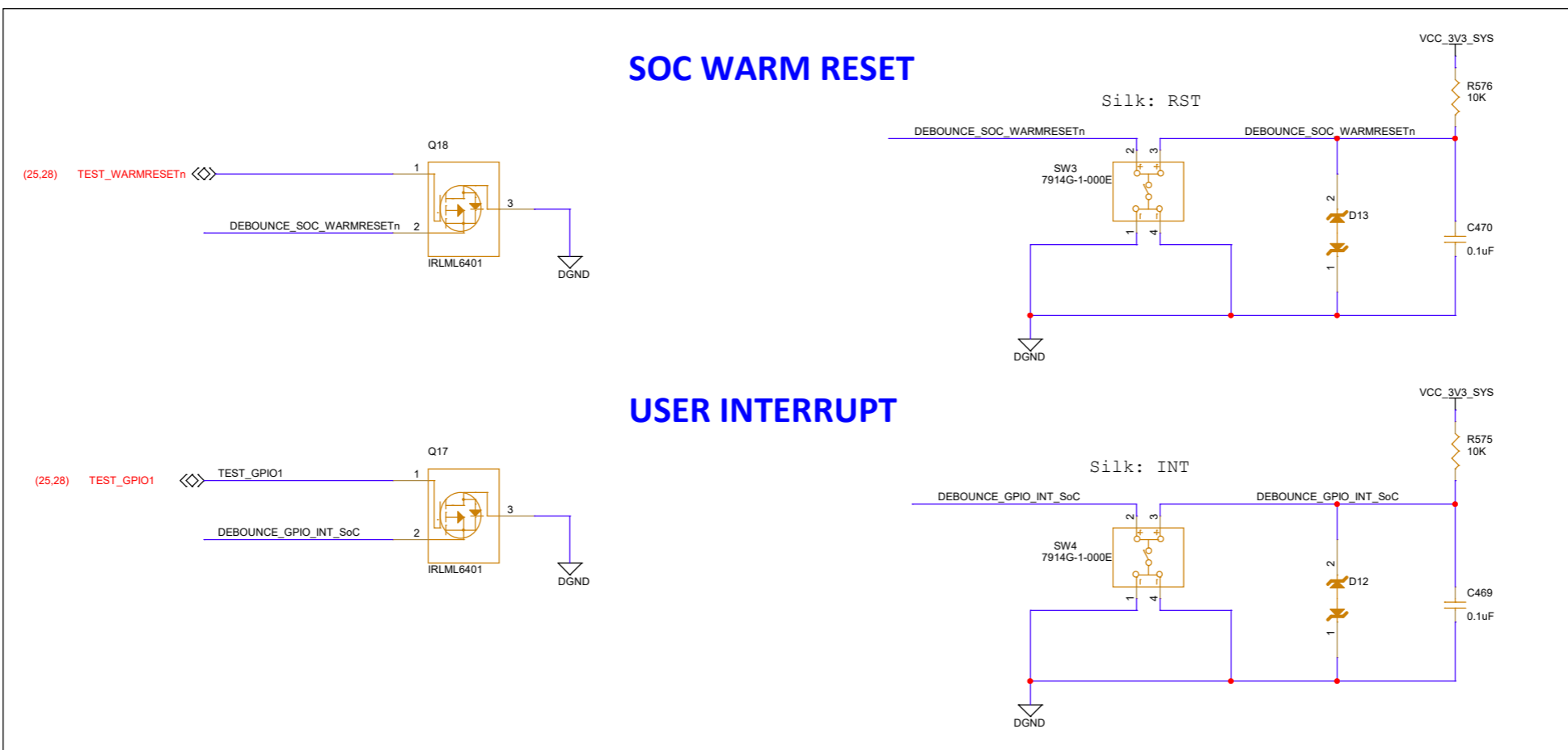
MCU WARM RESET



DEBOUNCE CIRCUIT



SOC WARM RESET



Designed for TI by Mistral Solutions Pvt Ltd



Title		RESET
Size	PROC142A1	Rev
C		A1
Date:	Sunday, April 13, 2025	Sheet 43 of 44

HARDWARE SCHEMATICS

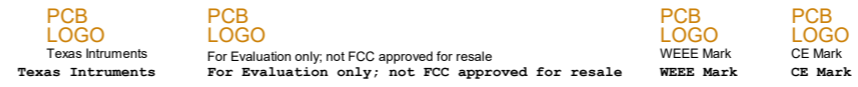
ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

BARE PCB

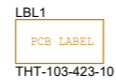


LOGOs

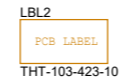


LABELS

Board Serial No.



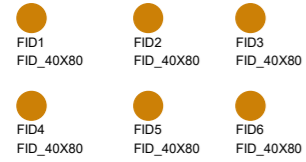
Assembly Revision



STANDOFF, SCREW & WASHER FOR PCIe M.2



FIDUCIALS



ORDERABLE PART NO



Orderable Part Number	
Variant	Label Text
001	SK-AM62-P1
002	SK-AM62B-P1

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Title: HARDWARE SCHEMATICS

Size	PROC142A1	Rev	A1
C			
Date:	Wednesday, February 19, 2025	Sheet	44 of 44