TI Designs

Acoustic Echo Canceller Reference Design Guide

TI Designs

Acoustic echo canceller (AEC) reference design provides a robust, wideband AEC algorithm software module that runs on the TMS320C674X or OMAP-L13X suite of processors. The design lets developers insert the AEC, running on the digital signal processor (DSP) on the TMS320C6748 DSP low-cost development kit (LCDK), into the audio path of hands-free equipment. The developer can then tune the audio path and the AEC, and test the performance of the AEC in a realistic environment. When the developer has proven that the AEC brings superior voice quality to the product, they can confidently choose the appropriate TMS320C674X or OMAP-L13X device on which to run the AEC and can leverage the AEC reference design software and adapt it to meet the specific hardware requirements of the product.

Design Resources

TIDEP0071	TI Design Files
DSP Soundware AEC-LCDK-REF	Software Kit
TMS320C6748	Product Folder
OMAPL138	Product Folder
TMDSLCDK6748	Tools Folder
TMDSLCDK138	Tools Folder
Starterware-C6748	Tools Folder

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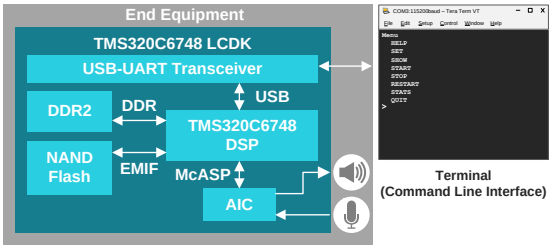
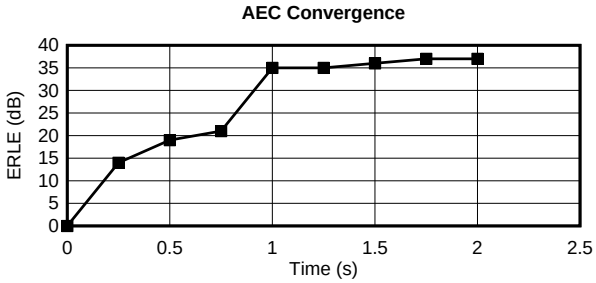
Design Features

- Wideband AEC
- Powerful Noise Reduction (NR)
- Dereverberation
- Simple Command Line User Interface
- Out-of-the Box Testing With Target Hardware

Featured Applications

- Speakerphone
- Voice-Enabled Internet of Things (IoT) Equipment
- Automatic Speech Recognition (ASR) Preprocessing





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1 Key System Specifications

- Full-duplex operation: Type 1
- Initial convergence: Less than 0.6 seconds
- Reconvergence: Less than 0.7 seconds
- Echo return loss enhancement (ERLE): 38 dB (without NLP)
- Programmable sampling rate: 8 to 48 kHz
- Nonlinear processor (NLP)
- Spectrally representative comfort noise generator (CNG)
- Noise reduction (NR): 18-dB signal-to-noise ratio (SNR) improvement typical
- Dereverberation: 6-dB improvement typical

2 System Description

Figure 1 shows a block diagram of a typical product that employs the AEC.

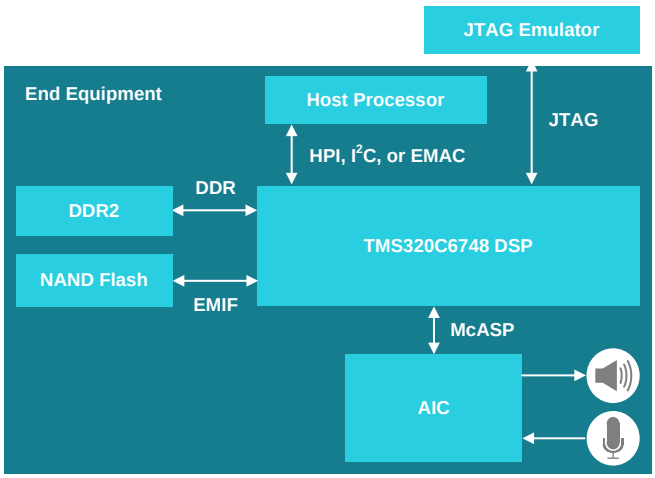

Figure 1. Hands-Free Equipment With AEC

Because the AEC is designed for use in hands-free equipment such as speakerphones and intercoms, a typical design includes a speaker and microphone. The speaker and microphone are connected to one of the many TI analog interface chips (AICs). The AIC includes a microphone interface and a speaker amplifier, which eliminates additional circuitry. The AIC has integrated anti-aliasing filters.

The AIC is connected to the TMS320C6748 DSP through the multichannel audio serial port (McASP). The McASP can support the commonly used I2S interface. The typical design includes the TMS320C6748 DSP and a host processor. In the TMS320C6748 LCDK-based demonstration, a PC emulates a host processor. The PC is connected to the DSP through a USB-serial interface. When the AEC is used in an embedded system, a typical host processor can be connected to the DSP through a number of TMS320C6748 peripherals such as the host port interface (HPI), inter-integrated circuit bus (I^2C), or Ethernet media access controller (EMAC). If an ARM® ARM9™ core is an appropriate host processor, the designer can choose the OMAP-L138 or OMAP-L132, which include an ARM9 core and a TMS320C674X core. This additional integration saves cost and board space, and allows for sharing external memory between the DSP and ARM-9 core.

In this example, a DDR2 is connected to the DDR interface of the DSP, providing external RAM. A NAND flash memory is connected to the external memory interface (EMIF). The JTAG interface is crucial for bringing up hardware, developing software, and debugging.

3 Block Diagram

Figure 2 shows the block diagram of the TMS320C6748 DSP processor.

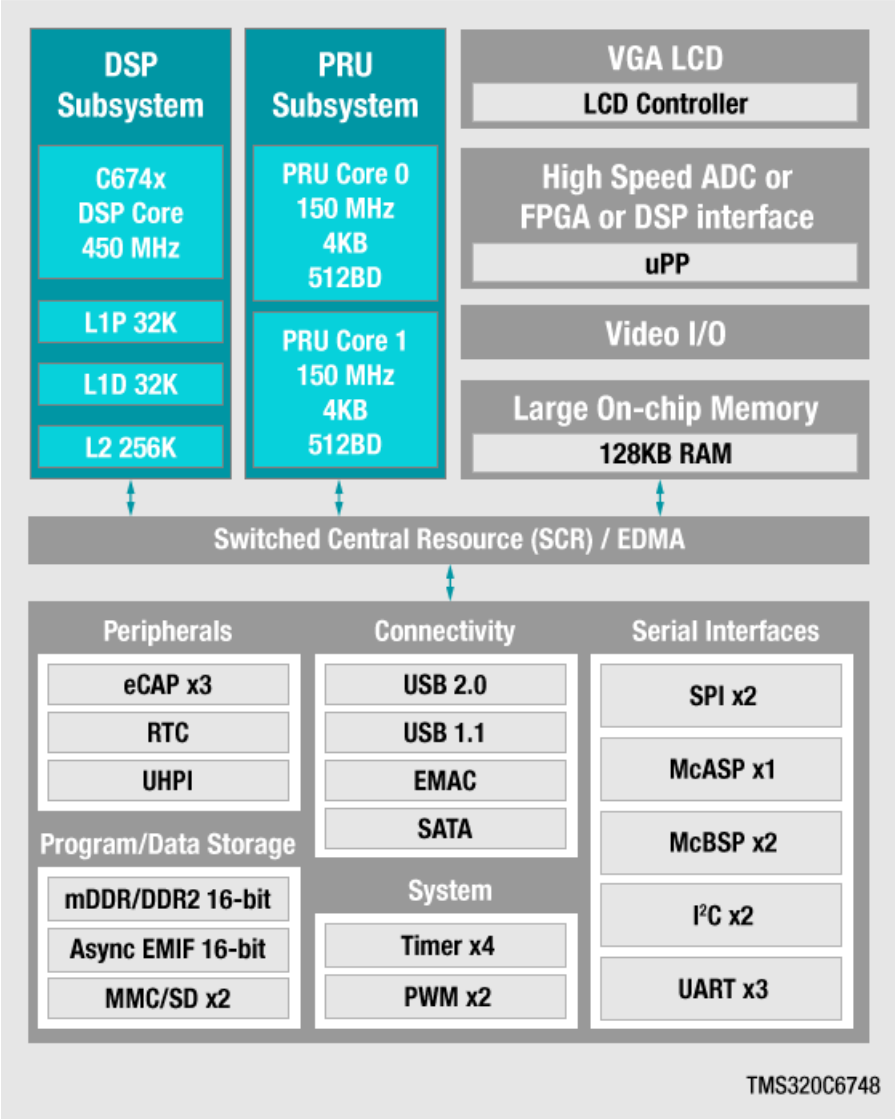

Figure 2. TMS320C6748 DSP Processor Block Diagram

4 Highlighted Products

The C6748 LCDK design is based on the TI TMS320C6748 DSP processor and its associated peripherals and is the engine of the design. The TMS320C6748 C6000™ DSP processor is a low-power applications processor based on a C674x DSP core. This processor provides significantly lower power than other members of the TMS320C6000 platform of DSPs.

The TMS320C6748 processor includes the following features:

- 375- and 456-MHz C674x fixed- and floating-point VLIW DSP
- C674x instruction set features:
  - Superset of the C67x+ and C64x+ ISAs
  - Up to 3648 MIPS and 2746 MFLOPS
  - Byte-addressable capability (8-, 16-, 32-, and 64-bit data)
  - 8-bit overflow protection
  - Bit field extract, set, clear
  - Normalization, saturation, and bit-counting
  - Compact 16-bit instructions
- C674x 2-level cache memory architecture:
  - 32KB of L1P program RAM/cache
  - 32KB of L1D data RAM/cache
  - 256KB of L2 unified Mapped RAM/cache
  - Flexible RAM/cache partition (L1 and L2)
- Enhanced direct memory access controller 3 (EDMA3):
  - 2 channel controllers
  - 3 transfer controllers
  - 64 independent DMA channels
  - 16 quick DMA channels
  - Programmable transfer burst size
- TMS320C674x floating-point VLIW DSP core
  - Load-store architecture with nonaligned support
  - 64 general-purpose registers (32-bit)
  - Six ALU (32- and 40-bit) functional units
    - 32-bit integer, SP (IEEE single precision/32-bit) and DP (IEEE double precision/64-bit) floating point
    - Up to four SP additions per clock and four DP additions every two clocks
    - Up to two floating-point (SP or DP), reciprocal approximation (RCPxP), and square-root reciprocal approximation (RSQRxP) operations per cycle
  - Two multiply functional units:
    - Mixed-precision IEEE floating-point multiply supported up to the following:
      - 2 SP × SP → SP per clock
      - 2 SP × SP → DP every two clocks
      - 2 SP × DP → DP every three clocks
      - 2 DP × DP → DP every four clocks
    - Fixed-point multiply that supports two 32 × 32-bit multiplies, four 16 x 16-bit multiplies, or eight 8 x 8-bit multiplies per clock cycle, and complex multiples
  - Instruction packing that reduces code size
  - All instructions as conditional
  - Hardware support for modulo loop operation

  - Protected mode operation
  - Exceptions support for error detection and program redirection
- Software Support
  - StarterWare™
  - Chip support library
  - DSP library
- 128KB of RAM shared memory
- 1.8- or 3.3-V LVCMOS I/Os (except for USB and DDR2 interfaces)
- Two external memory interfaces:
  - EMIFA
    - NOR (8- or 16-bit-wide data)
    - NAND (8- or 16-bit-wide data)
    - 16-bit SDRAM with 128-MB address space
  - DDR2/Mobile DDR memory controller with one of the following:
    - 16-bit DDR2 SDRAM with 256-MB address space
    - 16-bit mDDR SDRAM with 256-MB address space
- Three configurable 16550-Type UART modules:
  - Modem control signals
  - 16-byte FIFO
  - 16x or 13x oversampling option
- LCD controller
- Two serial peripheral interfaces (SPIs) each with multiple chip selects
- Two multimedia card (MMC)/secure digital (SD) card interfaces with secure data I/O (SDIO) interfaces
- Two master and slave inter-integrated circuits (I^2C bus)
- One host-port interface (HPI) with 16-bit-wide muxed address and data bus for high bandwidth
- Programmable real-time unit subsystem (PRUSS)
  - Two independent programmable real-time unit (PRU) cores
    - 32-bit load-store RISC architecture
    - 4KB of instruction RAM per core
    - 512 bytes of data RAM per core
    - Capability to disable PRUSS through software to save power
    - Capability to export register 30 of each PRU from the subsystem in addition to the normal R31 output of the PRU cores
  - Standard power-management mechanism
    - Clock gating
    - Entire subsystem under one PSC clock gating domain
  - Dedicated interrupt controller
  - Dedicated switched central resource
- USB 1.1 OHCI (host) with integrated PHY (USB1)
- USB 2.0 OTG port with integrated PHY (USB0)
  - USB 2.0 high- and full-speed client
  - USB 2.0 high-, full-, and low-speed host
  - Endpoint 0 (control)
  - Endpoints 1, 2, 3, 4 (control, bulk, interrupt, or ISOC) RX and TX
- One McASP:
  - Two clock zones and 16 serial data pins

  - TDM, I2S, and similar formats
  - DIT capable
  - FIFO buffers for transmit and receive
- Two multichannel buffered serial ports (McBSPs):
  - TDM, I2S, and similar formats
  - AC97 audio codec interface
  - Telecom interfaces (ST-Bus, H100)
  - 128-channel TDM
  - FIFO buffers for transmit and receive
- 10/100 Mbps EMAC:
  - IEEE 802.3 compliant
  - MII media-independent interface
  - RMII reduced media-independent interface
  - Management data I/O (MDIO) module
- Video port interface (VPIF):
  - Two 8-bit SD (BT.656), single 16-bit or single raw (8-, 10-, and 12-bit) video capture channels
  - Two 8-bit SD (BT.656), single 16-bit video display channels
- Universal parallel port (uPP):
  - High-speed parallel interface to FPGAs and data converters
  - Data width on both channels is 8- to 16-bit inclusive
  - Single-data rate (SDR) or dual-data rate (DDR) transfers
  - Multiple interfaces with START, ENABLE, and WAIT controls
- Serial ATA (SATA) controller:
  - SATA I (1.5 Gbps) and SATA II (3.0 Gbps)
  - All SATA power-management features
  - Hardware-assisted native command queueing (NCQ) for up to 32 entries
  - Port multiplier and command-based switching
- Real-time clock (RTC) with 32-kHz oscillator and separate power rail
- Three 64-bit general-purpose timers (configurable as two 32-bit timers)
- One 64-bit general-purpose or watchdog timer (configurable as two 32-bit general-purpose timers)
- Two enhanced high-resolution pulse width modulators (eHRPWMs):
  - Dedicated 16-bit time-base counter with period and frequency control
  - Six single-edge outputs, six dual-edge symmetric outputs, or three dual-edge asymmetric outputs
  - Dead-band generation
  - PWM chopping by high-frequency carrier
  - Trip zone input
- Three 32-bid enhanced capture (eCAP) modules:
  - Configurable as three capture inputs or three auxiliary pulse width modulator (APWM) outputs
  - Single-shot capture of up to four event time stamps
- Packages:
  - 361-ball Pb-Free plastic ball grid array (PBGA) [ZCE suffix], 0.65-mm ball pitch
  - 361-ball Pb-Free PBGA [ZWT suffix], 0.80-mmb ball pitch
- Commercial, extended, or industrial temperature

For more information on the TMMS320C6748 (including data sheets, silicon errata, and technical reference manuals), see http://www.ti.com/product/TMS320C6748.

5 System Theory

Whenever using a hands-free device, there are acoustic impairments. The following sections discuss the impairments and the methods used to combat them.

5.1 Acoustic Impairments

This design solves three types of acoustic impairments:

- Echo
- Reverberation
- Background noise

Acoustic echo is caused by coupling the speaker of a hands-free device (speakerphone, intercom, and so forth) and a microphone. Figure 3 shows acoustic echo as a light green signal coming from the person at the bottom of the diagram, through the telecommunications network, to the speakerphone on the conference room table. From the speaker, the signal couples directly to the microphone of the speakerphone and indirectly through reflections of the walls ceiling, floor, and objects in the room.

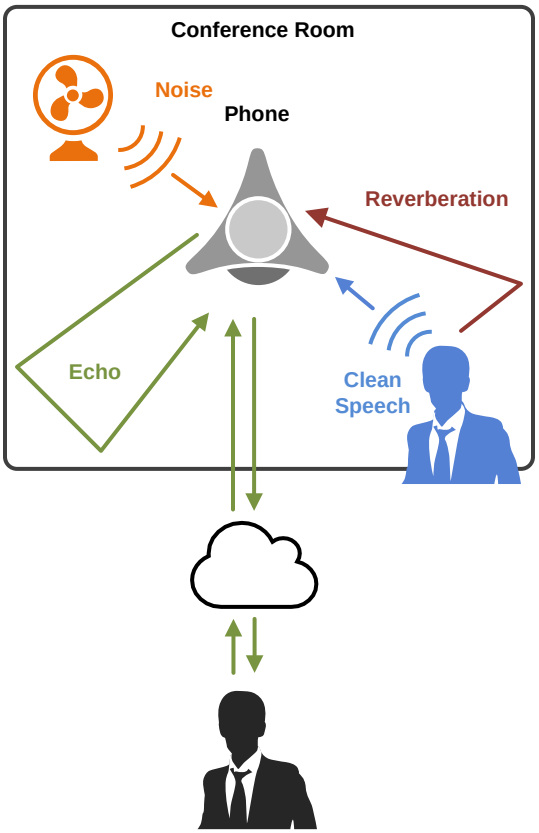

Figure 3. Acoustic Impairments

Figure 3 shows reverberation in red and blue. A direct path (blue) between the presenter and the speakerphone and indirect path (red) reflects before reaching the speakerphone. The fan on the right wall with its signal moving toward the speakerphone shows background noise.

Without acoustic echo cancellation to cancel the echo, dereverberation to mitigate the reverberation, and noise reduction to reduce the noise, the person at the other end of the phone connection can experience severely degraded voice quality and intelligibility.

Even a moderate amount of echo can be a serious impairment to voice quality. The degree of the impairment depends on the loudness of the echo and the delay between the original speech and the incidence of the echo.

When you speak in an enclosed space, your speech travels directly from your mouth to your ears with almost no delay. Your speech also reflects off of walls and so forth and you hear a slightly delayed signal. Multiple reflections occur at different delays. The delay is typically so small that you cannot perceive the reflections as an echo.

In the case of a voice communication system, the sources of delay follow:

- Network: A network can be the traditional public-switched telephone network (PSTN), the internet (in the case of voice over IP [VoIP]), or some other type. There is always a finite amount of time for a speech signal to pass through a network. Longer delays are attributable to propagation delay when using satellites and packet transmission delay in packet networks.
- Buffering: In a digital system, speech samples may be buffered into frames— each frame is usually the same duration. Buffering can occur in a software operating system or some other layer of an embedded software system. Buffering occurs in both directions of transmission.
- Packetization: In the case of a packet-switched network, speech data is sent in bursts that comprise many frames worth of speech. Each frame contains a segment of speech—each segment is usually of the same duration. Before sending a packet, all the frames of speech must be collected and sometimes processed. This process causes a delay.
- Acoustic: Acoustic delay is caused by the finite speed of sound. This delay is typically short for the direct paths (mouth to microphone and speaker to ears), but the indirect paths through reflections can be longer.

If the total round-trip delay is short, the echo is imperceptible. If the delay becomes longer, the echo becomes perceptible. This effect is known as *the precedence effect*. When a sound and a delayed copy is heard, the two copies are perceptually linked if the delay is short enough. As the delay increases, a person becomes more aware of the echo; the echo (and reverberation) must be removed more effectively to achieve acceptable voice quality.

5.2 Eliminating the Impairments

Suppressing an echo is the simplest way to remove it in a 2-way voice communication system. An echo suppressor determines which party is dominant by monitoring the speech signal level of both parties. Echo suppression turns what should be full-duplex (2-way) conversation into a half-duplex one. When both parties speak at the same time, only one party can hear the other one. This effect causes the parties to talk in intermittent periods, often asking the other person to repeat themself often. Conversely, an echo canceller estimates the echo and subtracts it rather than suppressing it. This effect results in full-duplex conversation.

Noise can be suppressed easily when speech is not present. When suppression is used, the noise is present when the speech is present. Noise reduction must be employed that can remove noise when speech is present and when it is not.

Reverberation is more complex. Reverberation cannot be suppressed like noise because reverberation is present only when near-end speech is present. Also, blindly suppressing reverberation has the unwanted effect of suppressing desired speech. Dereverberation, AEC, and noise reduction must achieve a balance between removing the undesired signals while preserving the desired signals.

5.3 High-Level Description

Figure 4 shows some of the primary aspects of an AEC operating in a hands-free product.

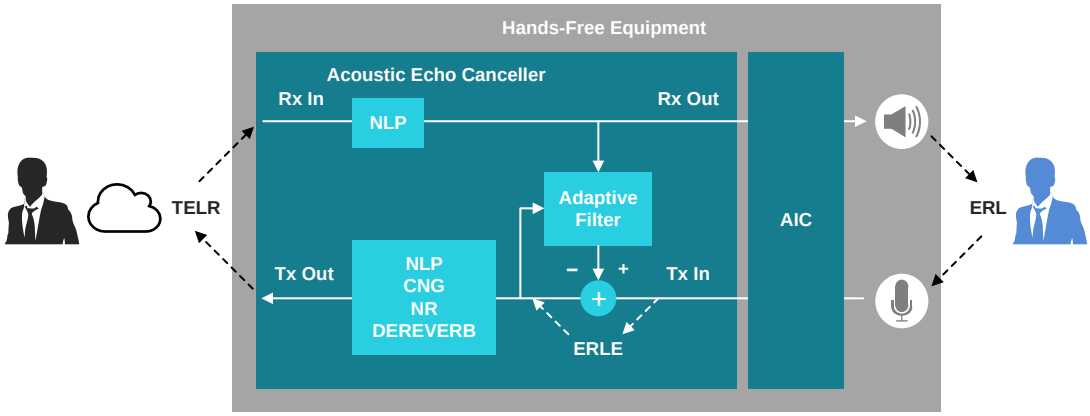

Figure 4. AEC Block Diagram

Transmit (Tx) and receive (Rx) are defined with respect to the person (blue) using the hands-free device that contains the echo canceller. He is speaking into the microphone of the device and listening to the speaker of the device. His speech is being transmitted to the other party (red) and he is listening to the signal that is received from the other party. Specifically, the inputs and outputs are defined as follows:

- Tx In (transmit input) is the signal coming from the local microphone.
- Tx Out (transmit output) is the signal transmitted to the person at the other end of the link.
- Rx In (receive input) is the signal that is received from the person at the other end of the link.
- Rx Out (receive output) is the signal that is sent to the local speaker.

Follow the path of the signal path. The signal of the far-end talker is sent through the network (shown as a cloud in Figure 4) and enters the AEC through the Rx In port. The signal passes through a nonlinear processor (NLP) that can attenuate the signal somewhat when both parties are speaking (double-talk). The output of the NLP is sent to the Rx Out port, which is connected to the local speaker and is also sent to an adaptive filter described later.

An acoustic path exists between the speaker and microphone. The speech of the far-end talker passes from the Rx Out port (speaker) to the Tx In port (microphone). The loss (gain) between the speaker and microphone is echo return loss (ERL), which is usually expressed in dB. If the local talker is quiet and there is no background noise in the room, the Tx In port consists only of echo. This condition is far-end single talk.

The Tx In port is connected to the adaptive filter. The filter estimates the acoustic echo characteristics and formulates a filter that estimates the echo, when excited by the Rx Out signal. The echo estimate is subtracted from the Tx In port to form the residual signal, sometimes called the residual echo signal. During far-end single-talk, the goal of the adaptive filter is for the residual echo to be zero. Adaptive filtering techniques are imperfect for the following reasons:

- Near-end speech or background noise interferes with adaptation.
- Approximations are made by the algorithm.
- Computational Precision can result in small numerical errors.

Echo return loss enhancement (ERLE) is the echo attenuation achieved by the adaptive filter. An important figure of merit for an AEC, ERLE is usually expressed in dB. A higher ERLE translates to a lower-level echo, which results in less-perceptible echo.

The sum of the ERLE of the adaptive filter and the ERL of the acoustic loss cannot sufficiently remove the echo. Some NLP must be incorporated to further suppress the echo. Avoid engaging the NLP during double-talk to avoid making the conversation half-duplex.

A higher ERLE leads to less reliance on NLP. The International Telecommunications Union (ITU) categorizes hands-free equipment in terms of how much it relies NLP or according to the degree of full-duplex operation that it can achieve.

There are NLP blocks in both the receive and transmit paths of the block diagram. The transmit NLP does the majority of the work. Because the perceived echo at the far end is the sum of all losses (receive NLP, ERL, ERLE, and transmit NLP), some benefit can be gained by applying an NLP in the receive direction.

Noise reduction (NR), comfort noise generation (CNG), and dereverberation are included in the same block as the NLP. When the NLP activates, it suppresses not only the residual echo but the background noise returns. When the NLP disengages, the attenuation is removed and the background noise returns. As a result, the far-end talker hears no background noise each time they speak but the background noise returns each time they pause. This effect is *noise pumping* and can be annoying. The CNG replaces the suppressed noise with artificially generated noise that matches the background noise in level and spectral characteristics.

Talker echo loudness rating (TELR) is the echo loudness as perceived by the far-end talker. The loudness is a function of the all the signal processing components of the AEC and by the ERL of the speaker-to-microphone loss.

6 Performance

Table 1 lists characterization data measured using the TMS320C6748 LCDK with L2 configured as all (256KB) cache, 300-MHz CPU clock, and 150-MHz DDR2. The AEC was configured at a sampling rate of 16 kHz.

Table 1. CPU and Memory Use

Tail Length (msec)	Program (KB)	Data (KB)	Per Channel Data	MIPS (MHz)
64	31.2	6.5	229	93
128	31.2	6.5	257	99
256	31.2	6.5	315	114

7 Getting Started

7.1 Equipment

To run the demonstration, the following is required:

- The DSP Soundware Algorithm Demonstration Kit
- The TMS320C6748 LCDK
- The Flashburn utility
- An audio source
- An audio listening device (speaker or headphones)
- A PC with USB serial port and terminal program (such as Tera Term)

7.2 Getting Started

See the quick start guide that accompanies the DSP Soundware Algorithm Demonstration Kit to learn about the following:

- Setting up the hardware
- Installing the software
- Running tests
- Tuning the algorithms

To request the DSP Soundware Algorithm Demonstration Kit, see http://www.dspsoundware.com/demo-software/aec-lcdk-ref or e-mail sales@dspsoundware.com.

8 Design Files

This TI Design highlights the audio subsystem on the TMS320C6748 LCDK. Download the design files including schematics, schematic source, and bill-of-materials for the audio subsystem at http://www.ti.com/tool/TIDEP0071.

8.1 Bill of Materials

To download the bill of materials for the audio subsystem, see the design files at http://www.ti.com/tool/TIDEP0071.

Table 2. Bill of Materials

Item	Qty	Reference	Value	Part Description	Manufacturer	Manufacturer Part Number	PCB Footprint
1	11	C172, C176, C180, C182, C183, C185, C186, C187, C188, C189, C190	0.1 µF/16-V X7R	CAP .10 µF 16 V CERAMIC X7R	Murata	GRM155R71C104KA88D	402
2	2	C173, C175	0.47 µF/16-V X5R	CAP CER .47 µF 16 V X5R 0402	TDK	C1005X5R1C474M050BC	402
3	2	C174, C177	220 pF/50-V X7R	CAP 220 pF 50 V CERAMIC X7R 0402	Yageo	CC0402KRX7R9BB221	402
4	4	C178, C179, C184, C191	10 µF/10-V X5R	CAP 10 µF 10 V CERAMIC X5R 0805	TDK	C2012X5R1A106M125AB	805
5	1	C181	1 µF/10-V X5R	CAP CER 1 µF 10 V X5R 0402	Murata	GRM155R61A105KE15D	402
6	3	FB14, FB15, FB16	MMZ2012S121A	FERRITE CHIP 120 Ω 800 MA 0805	TDK	MMZ2012S121A	805
7	1	J10	CK3.5-1230-08	CONN STEREO JACK 3.5-MM 3/3P PCB	Fosen Electronics Technology Co. Ltd. / Zai Kuai Sales, Ltd. Co.	CK3.5-1230-08	CX3_5-1230-08
8	1	J11	STX-3500-4NTR	Phone Connectors 3.5-mm SMT STEREO JACK 4P NON THREADED T/R	Kycon	STX-3500-4NTR	STX3500
9	3	R94, R95, R164	33E /5% 1/16 W	RES 33-Ω 1/16 W 5% 0402 SMD	Yageo	RC0402FR-0733RL	402
10	5	R150, R151, R158, R159, R162	2 K/1% 1/16 W	RES 2-kΩ 1/16 W 1% 0402 SMD	Vishay Dale	CRCW04022K00FKED	402
11	2	R152, R154	0E/5% 1/10 W	RES zero-Ω 1/10 W 5% 0402	Panasonic	ERJ-2GE0R00X	402
12	2	R153, R155	5.6 K, DNI	RES 5.60-kΩ 1/16 W 1% 0402	Yageo	AC0402FR-075K6L	402
13	2	R156, R157	20 K/1% 1/16 W	RES 20-kΩ 1/16 W 1% 0402 SMD	Yageo	RC0402FR-0720KL	402
14	1	R160	2 K/1% 1/16 W, DNI	RES 2-kΩ 1/16 W 1% 0402 SMD	Vishay Dale	CRCW04022K00FKED	402
15	1	R161	20 K, DNI	RES 20-kΩ 1/16 W 1% 0402 SMD	Yageo	RC0402FR-0720KL	402
16	1	R163	4.7 K/5% 1/16 W	RES 4.7-kΩ 1/16 W 5% 0402 SMD	Yageo	RC0402JR-074K7L	402
17	2	TP16, TP17	TEST POINT, DNI	CONN HEADER 1 POS .100" SGL GOLD	SAMTEC	TSW-101-07-G-S	tp
18	1	U7	OMAP-L138	LOW-POWER ARM+DSP CONTROLLER	TI	OMAPL138ZWT	bga361_w19_p8_16x16
19	1	U22	TLV320AIC3106IRGZ	LOW-POWER STEREO AUDIO CODEC	TI	TLV320AIC3106IRGZ	QFN48_25V
20	1	Y5	CB3LV-3I-24M5760	OSCILLATOR 24.5760-MHz 3.3-V SMD	ABRACON	ASFL1-24.576MHZ-EC-T	OSC4_90-100SMD_130X200

8.2 Software Files

To request the DSP Soundware Algorithm Demonstration Kit on DSP Soundware's website, see http://www.dspsoundware.com/demo-software/aec-lcdk-ref or e-mail sales@dspsoundware.com.

9 References

Texas Instruments E2E Community, http://e2e.ti.com/

10 About the Author

SCOTT KURTZ, the founder and president of DSP Soundware, has been working in the DSP software field since 1983. Since 1984 when the first commercially available TI DSP (the TMS32010) was introduced, Scott has been using TI DSPs in various products at a number of different companies. Scott began his career at RCA developing HF modems for defense communication systems. He continued his career at InterDigital Communications Corporation where he was instrumental in developing voice and modem technology for a digital wireless local loop telephone system. InterDigital's equipment was the predecessor to the technology that makes our cell phones work today. Before founding DSP Soundware, Scott was a cofounder of Adaptive Digital Technologies and served as VP of Engineering there for 17 years. At Adaptive Digital, Scott built an engineering team and DSP software product line that is licensed for use in many of today's VoIP and voice-enabled products. Currently, as founder and president of DSP Soundware, Scott pursues a mission to improve voice quality in hands-free equipment through the use of Digital Signal Processing algorithms and technology – hence the mantra – "Better Living Through DSP." Scott has a Master's degree in Electrical Engineering from Drexel University and a Bachelor's degree in Electrical Engineering from Lehigh University. Scott has authored 12 patents.

RAHUL PRABHU is a senior software applications engineer in TI's Embedded Processing organization who supports ARM-based and the DSP-based SoCs such as AM57xx., 66AK2EXX, OMAPL138, and C667x devices. Rahul brings to this role his extensive experience and knowledge in signal processing, optimizing algorithms, system integration, and application development. Rahul earned MS in Electrical and Computer Engineering from University of Houston.

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