Date	Rev	By	History
V0.29	2/7/2025	BMc	**PDN-3G & -3M Diags only** 1. Fixed power rail connections to OSPI memories by correctly changing name from VDD_MCUIO_1V8 to VDD_IO_1V8 for Grouped PDN scheme. **PDN-3F Diag only** 2. Added Note 14 to clarify removal of SVS-B & MCU_PWRGRP_IRQn board level net due to removing GPIO Retention low power mode. **SoC Pwr Seqs:** 1. Corrected power up seq timing diagram to correctly show time btw pwr up seq Time Step #2 vs #3 as only 0.5ms (instead of 1.0ms) per PMIC 133A's v4 update & as captured in v0.23 changes above.
v0.30	2/19/2025	BMc	**SoC Pwr Seqs:** 1. Corrected diag to show SOC_PWR_EN (PMIC_ENABLE input) signal asserting low 0.1ms (PMIC's internal delay T_{DLY0}) before PMIC's state machine begins executing power down seq by 1st setting MCU_PORz & SOC_PORz low.
v0.31	3/21/2025	BMc	**SoC Pwr Seqs:** 1. Corrected diag to show both VDD_GPIORET_IO_3V3 & VDD_IO_3V3 min enable time could be ~0.1ms after enabling signals (VDD_MCUIO_3V3 & EN_3V3_IO respectfully). 2. An "Immediate Shutdown/Power Down Seq" has recently been approved and will be add to an upcoming data manual version. This simplifies SoC power down to only require both PORz signals to be set low for 1-2us before disabling SoC input supplies in any order.
V0.32	5/15/2025 5/22/2025	BMc	**PDN-3AFGM Diags** 1. Added "Red Dashed Box" to high-light PMIC resources that are no longer needed and could be reassigned by system SW after boot-up. 2. Updated SVS-A & B to capture OV/UV threshold values per PN "004" default settings. Customers can adjust thresholds via I2C after boot as desired.

J784S4 EVM Leo + 2x High-Current Pwr Stages(HCPS) PDN-3A

(All SoC PN variants: TDA4AP/VP/AH/VH)

(Power Rail & GPIO Mapping Overview)

Leo PMIC-A, PN TPS6594133ARWERQ1 (TI PN ID = 1, MP Buck Rails = 3, PG2.0 NVM ID = 3A Rev 5)
HCPS-A & B, Tulip PN TPS62873Y1QWRXSRQ1 (15A PN ID = 3, Jacinto7 Family ID = Y1)
Safety Voltage Supervisor, PN TPS389006004RTERQ1 (OTP ID = 004 = new common PN for use with Jacinto7 J784S4 PDN-3A scheme)

V0.24	5/20/2024	1. Removed in-line ferrite bead filters from VDA_DLL_0V8 connections to SoC's VDDA_0P8_xxx analog supply inputs since filtering of the LDO power resource is not needed. Aligns PDN diag to match latest EVM SCH & board (PROC141E5). 2. Update VPP_EFUSE_1V8 LDO PN from 300mA TLV73318-Q12 to 500mA TPS7A2118P-Q1 to support robust J7xxx Efuse programming. Aligns PDN diag to match latest EVM SCH & board (PROC141E5)
V0.25	6/25/2024	1. Updated PMIC 133A NVM rev to v5 per RTM planned revision.
V0.27	10/31/2024	1. Updated discrete buck's ENABLE input connections to more accurately show the 20k resistor located in-line to voltage translator output. 2. Updated Note 9, example #2 text & diag to show 20k resistor in-line with buck's ENABLE inputs.
V0.32	5/22/2025	1. Updated SVS-A & B to capture OV/UV threshold values per PN "004" default settings. Customers can adjust thresholds via I2C after boot as desired.

Legend:

Power Rails <Pwr Rail Name>
PDN base
MCU Only/Safety Island
GPIO Retention
DDR_Retention (aka S2R)
End Product option
Peripheral loads (SW config'd after boot)

Control Signals: < Signals >
General cntrl & logic
(Italic = SW config'd after boot)
PDN base cntrl
Func Safety
MCU Only/Island
GPIO Retention
DDR_Retention (aka S2R)
End Product option
Peripheral comps
Debug/Development option

Note items
POK On-Chip "Pwr OK" Monitors (OV & UV)
POK-UV On-Chip "Pwr OK" Monitors (UV only)
Provisioned In-Line Supply Filter
High-lighted diagram changes

Features Supported (EVM Max Features):

1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
2. Functional Safety: ASIL-D capable sys w/ isolated Main & MCU power rails (supply FFI)
3. 4x SDRAMs: 32Gb, 4-Die, 32b, 4266MTs, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or Hyperflash & eMMC, UFS
5. Signaling Levels: MCU & Main Dual VIO
6. Low power modes:
   a. MCU Island/Only with Dual VIO (needs 4 indep pwr rails & 1 cntrl signal min)
   b. MCU GPIO Retention (needs 2 indep pwr rails & 1 cntrl signals min)
   c. DDR Retention/S2R (needs 1 add'l indep pwr rail & 1 cntrl signal min)
7. End Product Options:
   a. Compliant high-speed SD Card (needs 1 indep pwr rail & 1 VIO cntrl signal & discrete LDO needs Vin = 5V)
   b. Compliant USB 2.0 data eye (needs 5V, 1 indep pwr rail & discrete LDO needs Vin = 5V)
   c. HS SoC Efuse programming on-board (needs 1 indep pwr rail & 1 cntrl signal)

Notes:

1) Functional Safety requires monitoring all "safety critical" power rails (i.e. VSYS_3V3 input, key SoC supplies) that could cause severe system failures. ASIL classification depends on the end product use case & what SoC resources a customer is using that are considered to be safety-related. SoC has internal OV & UV monitoring for key SoC MCU & Main voltage domains. The status is reported by SoC's Power OK (POK) status bits. Optional SoC voltage monitoring inputs (i.e. VMONx_IR_VEXTxxx) can be used to extend SoC's OV/UV monitoring to a few board level power rails if desired (i.e. load switch Vo = VDD_IO_3V3). The following SoC Main & SDRAM domains are classified as non-critical & do not require direct monitoring: VDDSHV5 (SD Card), VPP_CORE, VPP_MCU, VDDA_3P3_USB & VDD1_LPDDR4_1V8.

2) Load Switches (LdSw) have been used to create VDD_MCUIO_3V3, VDD_GPIORET_3V3 & VDD_IO_3V3 power rails from VCCA_3V3 to provide the following benefits:
   A) Correct SoC power supply sequencing by using PMIC resources (GPIO signals & power resource outputs) with desired start-up & shut-down timing delays per NVM settings.
   B) PMIC monitoring of "VCCA Over Voltage" (+5 to +10%) allows PMIC to disconnect 3.3V power rails from SoC if OV condition is detected.
   C) Enables low power modes (MCU Only, GPIO_RET & DDR_RET) since the different 3.3V power rails must be disabled independently for different low power modes.
   D) Connecting VCCA_3V3 directly to SoC 3.3V input supplies is ONLY recommended if low power modes are used and a full SoC power up seq is executed any time the VCCA_3V3/VSYS_3V3 is energized since partial powering of the SoC for extended time could negatively impact POH reliability.

3.1) PMIC NVM Rev 1 assigned multiple interface signals to GPIO8 with default NVM setting of GPIO_8 = DISABLE _WDOG function and required interface buffer circuitry, see PROC141E4_SCH for details.
   A) DISABLE_WDOG (NVM setting): PMIC latches logic level at GPIO8 pin on rising edge of PMIC's nRSTOUT = H_MCU_PORz_1V8 at end of power-up seq.
      a) High level at GPIO8 pin (SW-1/Jmpr-1 = closed) directs PMIC to disable Watch-Dog Timer (by setting WD_PWRHOLD bit to disable timer's long-window time-out) for development/debug.
      b) Low level at GPIO8 pin (SW-1/Jmpr-1 = open due to PMIC default internal pull-down R) enables Watch-Dog Timer (default setting enables timer's long-window time-out).
   B) After system SW boots, SW needs to reassign GPIO_8 = GPI function to operate with PDN's MAIN_PWRGRP_IRQ/_IRQn (asserted high or low) signal to allow PMIC to take action if a fault occurs.

3.2) PMIC NVM Rev2 & 3 changes are listed below. There are EVM board SCH/BOM impacts, see J784S4_EVM_..._PDN-3A v0.19 for details.
   1. PMIC VCCA input voltage level auto-detection that enables 1x PMIC PN to support PDNs using either 5V or 3.3V.
   2. PMIC internal Watchdog Timer is disabled at start-up. This allows GPIO8 function to be used as a PMIC internal configuration control. MCU SW will need to start watchdog timer as part of enabling full FuSa features.
   3. GPIO8 logic level selects the PDN type/scheme by latching level before the 3ms time step during power up sequence & directs PMIC to configure internal resources as follows:
      Low = Isolated PDN type directs PMIC to create MCU & SOC power groups; Enables BUCK5 per power up seq (Removes MCU SW write requirement needed in NVM Rev1 above.)
      High = Grouped PDN type directs PMIC create only MCU power group; Removes BUCK5 from pwr up seq (Allow SW to reassign Buck5 for peripheral devices that can be enabled after boot)

3.3) PMIC NVM Rev 4 has been optimized for end product production flow by enabling Watch Dog Timer to support FuSa by default, see J784S4_EVM_..._PDN-3A v0.20 & up & PROC141E5_SCH for details. GPIO9 has been used to support multiple interface signals as listed below.
   A) DISABLE_WDOG (optional): PMIC latches logic level at GPIO9 pin at transition from standby to active start-up sequence.
      a) High level at GPIO9 pin (SW-1/Jmpr-1 = closed) directs PMIC to disable Watch-Dog Timer (by setting WD_PWRHOLD bit to disable timer's long-window time-out).
      b) Low level at GPIO9 pin (SW-1/Jmpr-1 = open due to PMIC default internal pull-down R) enables Watch-Dog Timer (default setting enables timer's long-window time-out).
   B) EN_3V3_VIO (required): After PMIC NVM initialization, GPIO9 = GPO function to provide enable & disable control of load switch supplying VDD_IO_3V3 power rail.
      a) Disabling the WDOG timer is for development & debug tasks. Applying a pull-up R to disable WDOG timer will result in early enabling of discrete LDSW-A (VDD_IO_3V3), LD0-E (VDD_SD_DV) & LDO-F (VDA_USB_3V3). All of these supplies are 3.3V level and are part of the 1st group of supplies to be energized at the start of a power up seq. SoC will not be negatively impacted if these 3.3V supplies are enabled ahead of remaining 3.3V supplies sourced from PMIC and before the rest of SoC supplies begin a normal power up seq during temporary development & debugging activities.

4) GPIO Retention (aka GPIO_RET, IO_RET, IO Wake) low power mode requires:
   A) SoC SW executes command sequence that sets key PMIC register bits in order to enter GPIO_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
   B) After entering GPIO_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
      1. VDD_GPIORET_WK_0V8 supplying MCU's VDD_MCU_WAKE1 for MCU's 0.8V wake-up logic
      2. VDD_GPIORET_IO_3V3 supplying MCU's VDDSHV0_MCU for MCU's 3.3V IO toggle activity
   C) PDN system exits GPIO_RET state upon receiving logic toggles on SoC's MCU monitored IO signals ref to VDDSHV0_MCU supply. Then H_MCU_WAKE1n (= SoC's Open-Drain PMIC_WAKE1n, active low) signal connected to PMIC, GPIO_4 (= WKUP1 default function for Full Active or = WKUP2 for MCU Only destination state) is asserted and PMIC state machine transitions PDN system to desired targeted wake up state.
   D) The Open-Drain Buffer SN74LVC1G07DRLI (tri-states IO when power is OFF) connects PMIC_WAKE1n to SOC_PWR_WKn net at discrete open-drain FET node. It is needed to isolate the SoC output buffer from the always on VCCA_3V3 used as pull-up supply to prevent current bleeding into SoC during low power modes (MCU Only, DDR_RET) when VDD_GPIORET_3V3 is typically disabled.

5) DDR Retention (aka DDR_RET, Suspend-to-RAM, S2R) low power mode requires:
   A) PMIC PN to assign GPIO_6 = Regulator Enable (REGEN) function with an open-drain output buffer type per NVM default settings. The board level net H_DDR_RET_1V1 signal is pulled up to VDD_DDR_1V1 & connected to SoC's DDR_RET input. When this input is set high, SoC's EMIF IO buffers are set to high-Z state as part of entering DDR_RET mode.
   B) SoC SW executes command sequence that sets key PMIC register bits in order to enter DDR_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
   C) After entering DDR_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
      1. VDD_DDR_1V1 supplying both SoC EMIF & SDRAM IO voltages
      2. VDD1_DDR_1V8 supplying SDRAM only
   D) PDN system exits DDR_RET upon detecting a CAN_WAKE signal edge toggle on PMIC's GPIO_4 = LP_WKUP1 function per NVM settings that initiates exiting DDR_RET mode & restores Full Active processor operations.

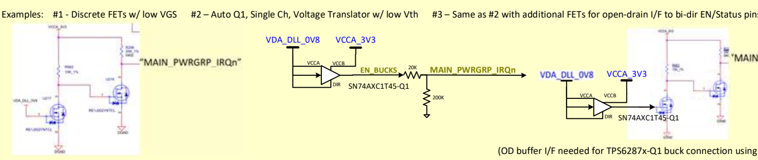
6) SoC devices come in two types: General Purpose (GP) & High Security (HS). All GP devices can leave the VPP domains unconnected per DM. Pre-programmed HS devices can also leave VPP domains unconnected if no additional EFUSE programming is needed. If customer desires capability for in-the-field updates, then on-board EFUSE programming will require an additional 1.8V, 150mA LDO. When disabled, this LDO's Vo will need a high impedance output. Recommended PNs: TPS73101-EP, fixed 1.8V TPS73118-Q1 or TLV70018-Q1. The EN_EFUSE_VPP control signal must be sourced from an SoC GPIO for this PDN (due to limited number of PMIC GPIOs). This allows SoC SW to control Efuse VPP voltage level by enabling & disabling dedicated LDO as needed to program High Security SoC Efuses (see SoC DM for details).

7) PDN shows SoC's VDA_3P3_USB domain supplied from a low noise LDO with a VSYS_5V input as preferred for optimal USB 2.0 data eye mask performance. If USB 2.0 I/F is not used or is only needed for development tasks, then the digital VDD_IO_3V3 rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_3V3 rail to support USB 2.0 I/F removes a discrete LDO & VSYS_5V input but could negatively impact data eye performance due to higher supply noise causing data eye mask violations.

8) PDN shows SoC's Main domain's VDDSHV5 supply being sourced from a dual voltage LDO with a VSYS_5V input as preferred for compliant high-speed SD card operation. If SD card is not used or only standard data rate operation is sufficient, then the digital VDD_IO_3V3 rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_3V3 rail to support SD Card operation removes dual voltage, discrete LDO & VSYS_5V input but will restrict data rates to standard 12Mb/s with VIO = 3.3V.

9) A low voltage translator with a VGS or VIH max spec less than 0.76V (-5% supply tol on 0.8V) is needed to ensure a 3.3V logic high level output. 3x different examples are shown below:
   #1 A discrete FET voltage translator with low VGS threshold below an input min 0.76V. EVM PROC141E2/E3_SCHs use discrete FET PN w/ low VGS but only industrial temp grade.
   #2 A single channel, voltage translator (SN74AXC1T45-Q1) that is automotive AEC-Q100 qualified, grade1 for -40 to +125C operation could be used as an alternative. Ensure valid logic levels are provided at both GPIO8 (as desc above) & discrete Buck's EN input pin (snap-shot shows Buck's internal bi-dir EN/STATUS circuitry).
      A.) The PMIC's GPIO8 has NVM default setting that enables a 400k internal pull-down. This should be sufficient to keep GPIO8 net from "floating" above GPIO's VIH min level when VDA_DLL_0V8 is disabled which causes the SN74AXC1T45-Q1 output to be tri-stated.
      B.) Customer may want to add a pull-down R on the board (showing a 200k below) just in case the PMIC's internal pull-down is not strong enough to ensure a low logic level.
   #3 A non-inverting FET stage (Ex 3, shown below) could be added to shunt the "MAIN_PWRGRP_IRQn" net to Gnd if items 2A or 2B are not sufficient.

Examples: #1 - Discrete FETs w/ low VGS #2 – Auto Q1, Single Ch, Voltage Translator w/ low Vth #3 – Same as #2 with additional FETs for open-drain I/F to bi-dir EN/Status pins



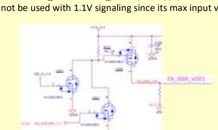
(OD buffer I/F needed for TPS6287x-Q1 buck connection using AEC-100 Translator)

10) Worst case analysis for very high thermal use cases could result in VCCA_3V3 load current in 15-18A range. This large load current range could lead to a 60 – 72mV voltage drop across Safety FET (Recm'd PN: NVMFS4C05N) for a max RDSon = 4mohm. The TPS22965-Q1 load switches have max RDSon = 27mohm with 4A max rating resulting in additional max drop of 108mV. SoC's 3.3V supply tolerance is +/-5% or 165mV. Total RDSon drops across Safety FET & Load Switches range from 168 – 180mV which exceed SoC's min voltage limit. For this reason, the Tulip buck input voltage will be moved from VCCA_3V3 to VSYS_3V3 since VDD_CPU_AVS & VDD_CORE_0V8 rails account for more than 70% of VCCA_3V3 worst case load currents.

11) If GPIO Retention low power mode is desired, then connect all SVS-B VMON inputs to existing MCU supplies (as shown) sourced from PMIC to enable 1x common PN for SVS-A & -B while avoiding false positives on "unconnected" VMONs. If an end product does not need GPIO Retention low power mode, then the 3x following components can be removed from the PDN: LDO-C, LDSW-B & SVS-B. Group the SoC input supplies according to he "PDN Features for Isolated Power Rails" table shown below using the "Standard Operation & MCU Only" assignments row.

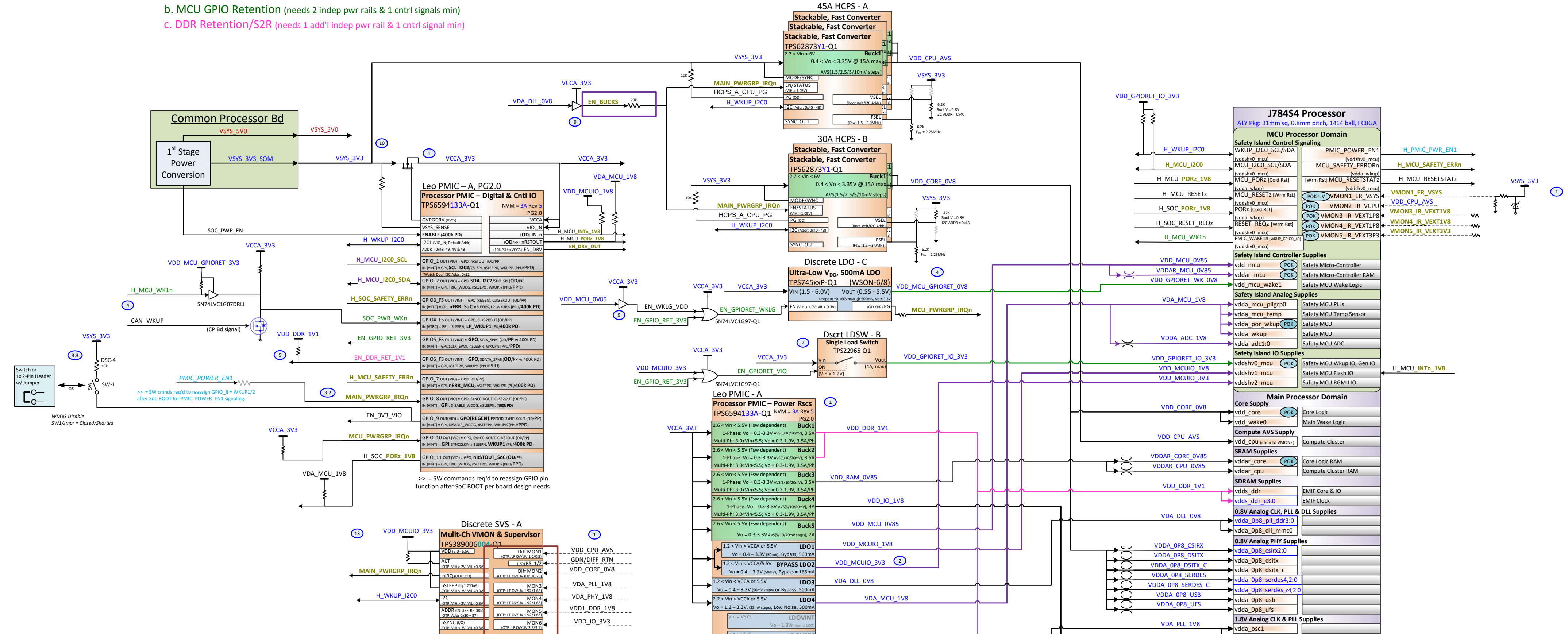
12) The OR gate function enabling the discrete LDO supplying 1.8V to LPDDR4 VDD1 (Internal bias voltage) needs to revert back to original discrete FET OR gate circuitry (see PROC141E2_SCH or snap-shot below). Reason for reverting is due to the OR gate needing a max input voltage threshold less than 1.05V (-5% of 1.1V) since the EN_DDR_RET_1V1 signal is sourced from an open-drain PMIC GPIO with PU resistor to VDD_DDR_1V1 supply with +/-5% supply tolerance. In addition, the OR gate needs to remain energized during DDR Retention low power mode when only VDD_DDR_1V1 & VDD1_DDR_1V8 rails remain energized. Therefore, the OR gate supply must use VSYS_3V3 or VCCA_3V3 input supply that remains on in DDR Ret mode. The single logic gate IC (SN74LVC1G97-Q1) used for enabling other power resources interfaced to 3.3V signaling levels can not be used with 1.1V signaling since its max input voltage threshold for 3.3V supply is ~2.2V.

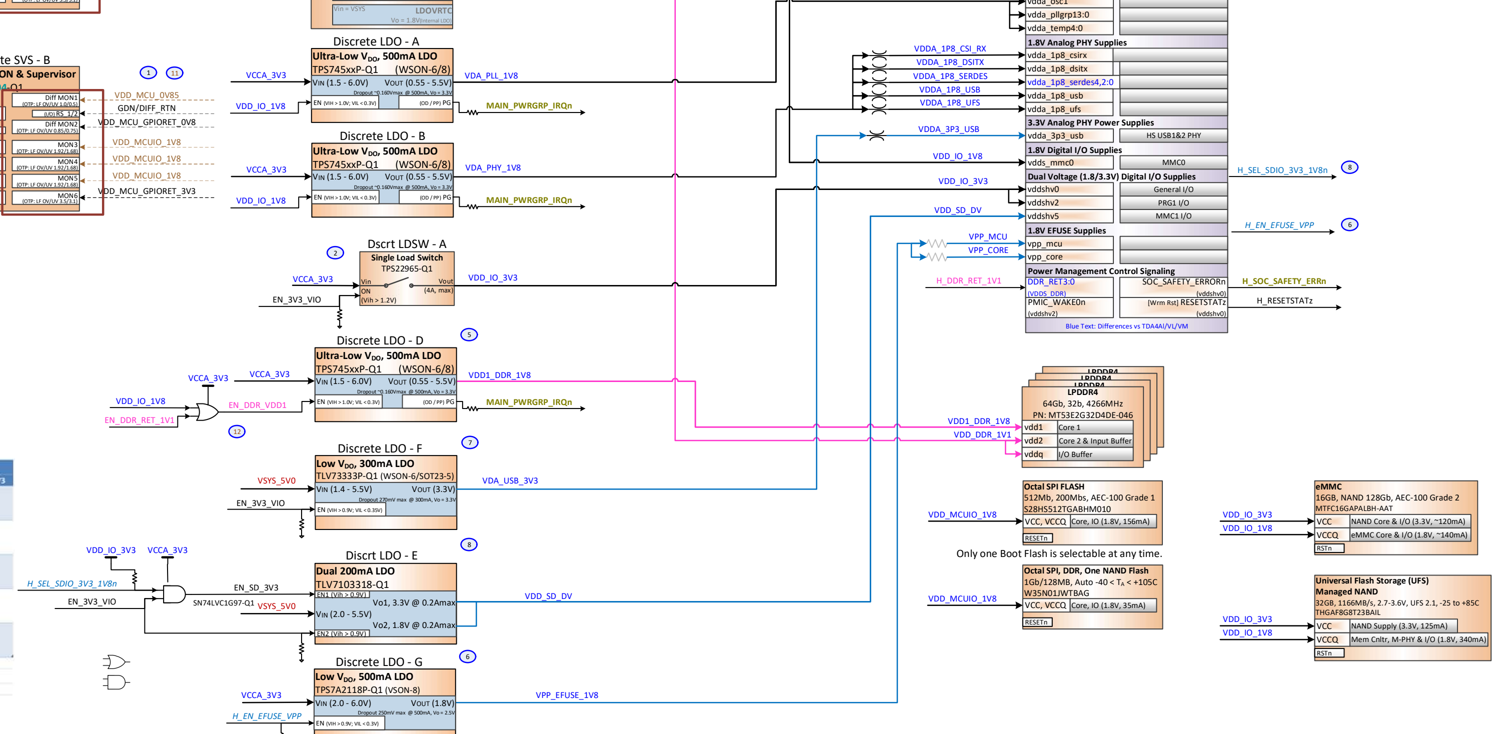
Original discrete FET OR gate circuit used in PROC141E2_SCH:



13) The Safety Voltage Supervisor (SVS-A & SVS-B) supply connections need to be changed from "Always ON" VCCA_3V3 (=VSYS_3V3) to a "PMIC controlled" power rail to enable resetting of an asserted IRQn signal by power cycling SVS devices. During functional testing, it was discovered that an SVS's asserted IRQn could not be reset if MCU processor I2C comm with SVS devices is lost. This will happen if a MCU Power Error occurs (i.e. fault on a MCU supply) since this will cause the PMIC PFSM to transition the system to the desired Safe Recovery state (powers down all SoC supplies). However, if the SoC PDN's input voltage (VSYS_3V3) remains energized, then the energized SVS devices will maintain an asserted IRQn and the system will not be able to execute a SoC cold boot attempt due a previously asserted IRQn will cause the PMIC to abort an SoC power up sequence attempt. A SVS device power cycle will reset an asserted IRQn signal, enabling the desired SoC cold boot attempt. By replacing "Always ON" VCCA_3V3 supply connections with a PMIC controlled power rail (VDD_MCUIO_3V3), the SVS devices will have a power cycle event upon entering the Safe Recovery state (per table below). If a fault occurs on a Main domain supply, the PMIC will transition the system to MCU Only state which allows I2C comm to evaluate & potentially log the fault source. The MCU can use I2C comm to clear an asserted IRQn if a system cold boot attempt is desired to try restarting into the Full Active state since a fault might clear if it's due to a random noise event or temperature dependent. The SVS device's "ACTive" input connection will need to be connected to VDD since the new VDD_MCUIO_3V3 supply connection is enabled as part of the SoC power up seq.. This avoids driving a high logic signal into an unenergized device.

PDN State:	Active	MCU Only	Safe Recovery
	Main supplies = ON	Main supplies = OFF	Main supplies = OFF
	MCU supplies = ON	MCU supplies = ON	MCU supplies = OFF
	SVS-A = ON	SVS-A = ON	SVS-A = OFF
	SVS-B = ON	SVS-B = ON	SVS-B = OFF





Modular PDNs support Flexible Feature Set Reductions

Feature Removals	Power Resource & Power Rail Removals	New Supply Mappings
HS SoC EFUSE Programming	Discrete LDO VPP_EFUSE_1V8	SoC: VPPs => No connects
Compliant, USB 2.0 data eye	Discrete LDO VDA_USB_3V3	SoC: VDDA_3P3_USB => filtered VDD_IO_3V3
Compliant, High-Speed SD Card	Discrete LDO VDD_SD_DV	SoC: VDDSHV5 => VDD_IO_3V3 or VDD_IO_1V8
DDR Retention low power mode	Discrete LDO VDD1_DDR_1V8	LPDDR4: VDD1 => VDD_IO_1V8
MCU GPIO Retention low power mode	Discrete LDO VDD_MCU_GPIORET_0V8	Isolated MCU & Main PDN Schemes: SoC: VDD_MCU_WAKE1 => VDD_MCU_0V85 Grouped MCU & Main PDN Schemes: SoC: VDD_MCU_WAKE1 => VDD_CORE_0V8
	Discrete LDSW VDD_MCU_GPIORET_3V3	Isolated MCU & Main PDN Schemes: SoC: VDDSHV0_MCU => VDD_MCUIO_3V3 or VDD_MCUIO_1V8 Grouped MCU & Main PDN Schemes: SoC: VDDSHV0_MCU => VDD_IO_3V3 or VDD_IO_1V8
	Discrete SVS	PMIC: GPIO_10 pulled-up to VCCA_3V3
Main GPIO Retention low power mode	Discrete LDO VDD_GPIORET_0V8	SoC: VDD_WAKE0 => VDD_CORE_0V8
	Discrete LDSW VDD_GPIORET_3V3	SoC: VDDSHV2 => VDD_IO_3V3 or VDD_IO_1V8
	Discrete SVS	PMIC: GPIO_10 pulled-up to VCCA_3V3

SoC Input Supply to Power Rail Groupings vs PDN Low Power Mode Features

PDN Features	Isolated MCU & Main PDN Power Rails							
	VDD_MCU_0V85	VDD_CORE_0V8	VDD_MCUIO_3V3	VDD_IO_1V8	VDD_IO_3V3	VDD1_DDR_1V8	VDD_GPIORET_0v8	VDD_GPIORET_3V3
Standard Operation & MCU Only	vdd_mcu vddar_mcu vdd_mcu_wake1	vdd_core vdd_wake0	vddshv0_mcu vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0 vddshv2			
DDR Retention	vdd_mcu vddar_mcu vdd_mcu_wake1	vdd_core vdd_wake0	vddshv0_mcu vddshv2_mcu	vdds_mmc0	vddshv0 vddshv2	DDR: vdd1		
GPIO Retention-MCU & Main	vdd_mcu vddar_mcu	vdd_core	vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0		vdd_mcu_wake1 vdd_wake0	vddshv0_mcu vddshv2
GPIO Retention-MCU	vdd_mcu vddar_mcu	vdd_core vdd_wake0	vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0 vddshv2		vdd_mcu_wake1	vddshv0_mcu
GPIO Retention-Main	vdd_mcu vddar_mcu vdd_mcu_wake1	vdd_core	vddshv0_mcu vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0		vdd_wake0	vddshv2

Notes:
1) Power rail names shown in "ALL CAPITAL LETTERS"
2) SoC input supplies shown in "all lower case letters"

J784S4 EVM Leo + 2x High-Current Pwr Stages(HCPS) PDN-3F

(All SoC PN variants: TDA4AP/VP/AH/VH)
(Power Rail & GPIO Mapping Overview)

Leo PMIC-A, PN TPS6594133ARWERQ1 (TI PN ID = 1, MP Buck Rails = 3, PG2.0 NVM ID = 3A Rev 5)
HCPS-A & B, Tulip PN TPS62873Y1QWXRSRQ1 (15A PN ID = 3, Jacinto7 Family ID = Y1)
Safety Voltage Supervisor, PN TPS389006004RTERQ1 (OTP ID = 004 = new common PN for use with Jacinto7 J784S4 PDN-3A scheme)

Version	Date	Changes
V0.27	10/31/2024	1. Updated discrete buck's ENABLE input connections to more accurately show the 20k resistor located in-line to voltage translator output. 2. Updated Note 9, example #2 text & diag to show 20k resistor in-line with buck's ENABLE inputs.
V0.28	12/11/2024	1. Corrected a copy & paste error by changing net name "DSRT_PWRGRP_IRQn" connected to SVS-A's IRQ pin to "MAIN_PWRGRP_IRQn".
V0.29	1/27/2025	1. Added Note 14 to clarify removal of SVS-B & MCU_PWRGRP_IRQn board level net due to removing GPIO Retention low power mode.
V0.32	5/15/2025	1. Added "Red Dashed Box" to high-light PMIC resources that are no longer needed and could be reassigned by system SW after boot-up.
	5/22/2025	2. Updated SVS-A & B to capture OV/UV threshold values per PN "004" default settings. Customers can adjust thresholds via I2C after boot as desired.

Legend:

Power Rails ‹Pwr Rail Name›
- PDN base
- MCU Only/Safety Island
- GPIO Retention
- DDR_Retention (aka S2R)
- End Product option
- *Peripheral loads (SW config'd after boot)*

Control Signals: ‹ Signals ›
- General cntrl & logic
- *(Italic = SW config'd after boot)*
- PDN base cntrl
- Func Safety
- MCU Only/Island
- GPIO Retention
- DDR_Retention (aka S2R)
- End Product option
- Peripheral comps
- Debug/Development option

- Note items
- POK: On-Chip "Pwr OK" Monitors (OV & UV)
- POK-UV: On-Chip "Pwr OK" Monitors (UV only)
- Provisioned In-Line Supply Filter
- High-lighted diagram changes

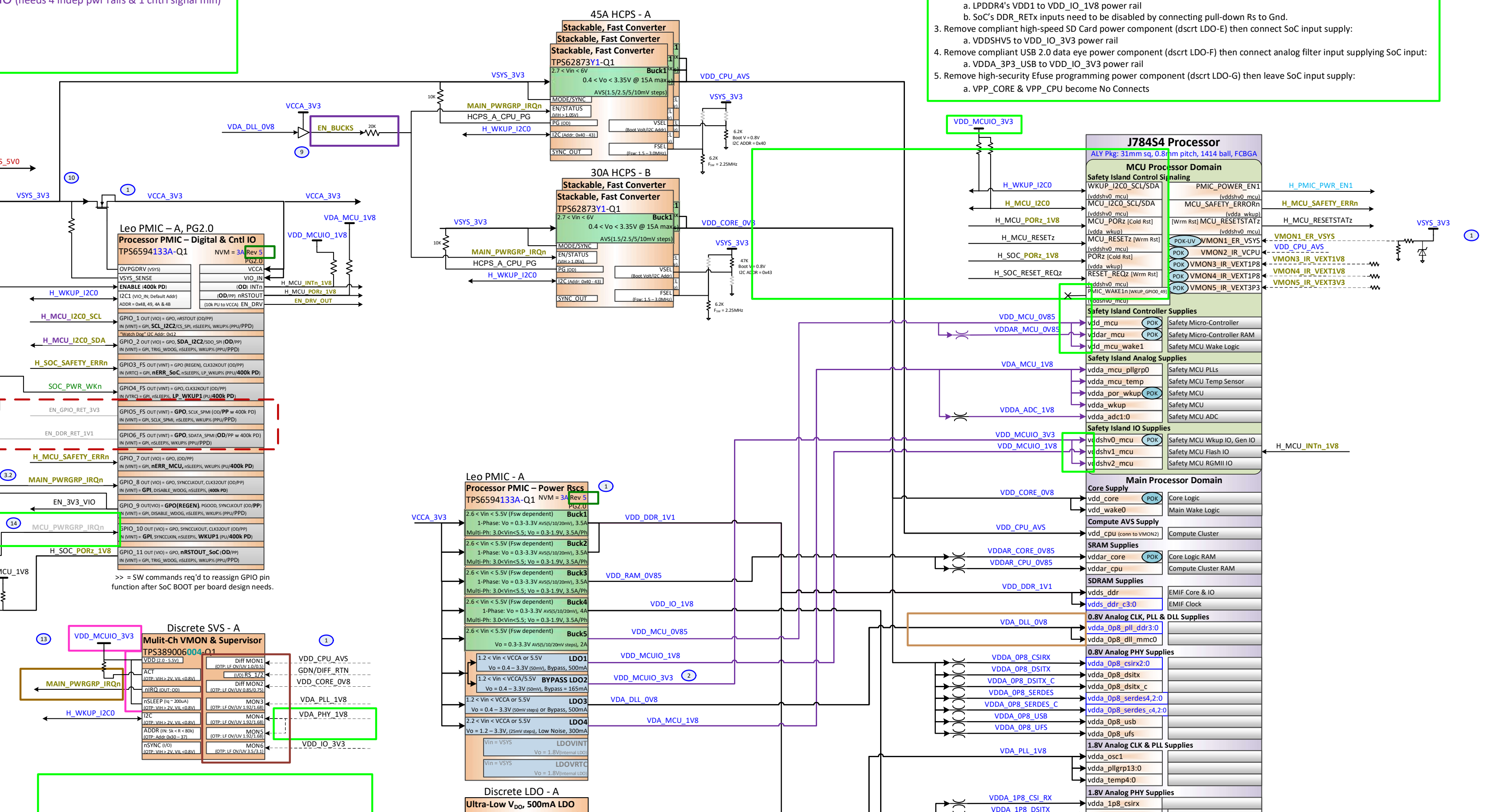
SW option to reassign PMIC resource after boot

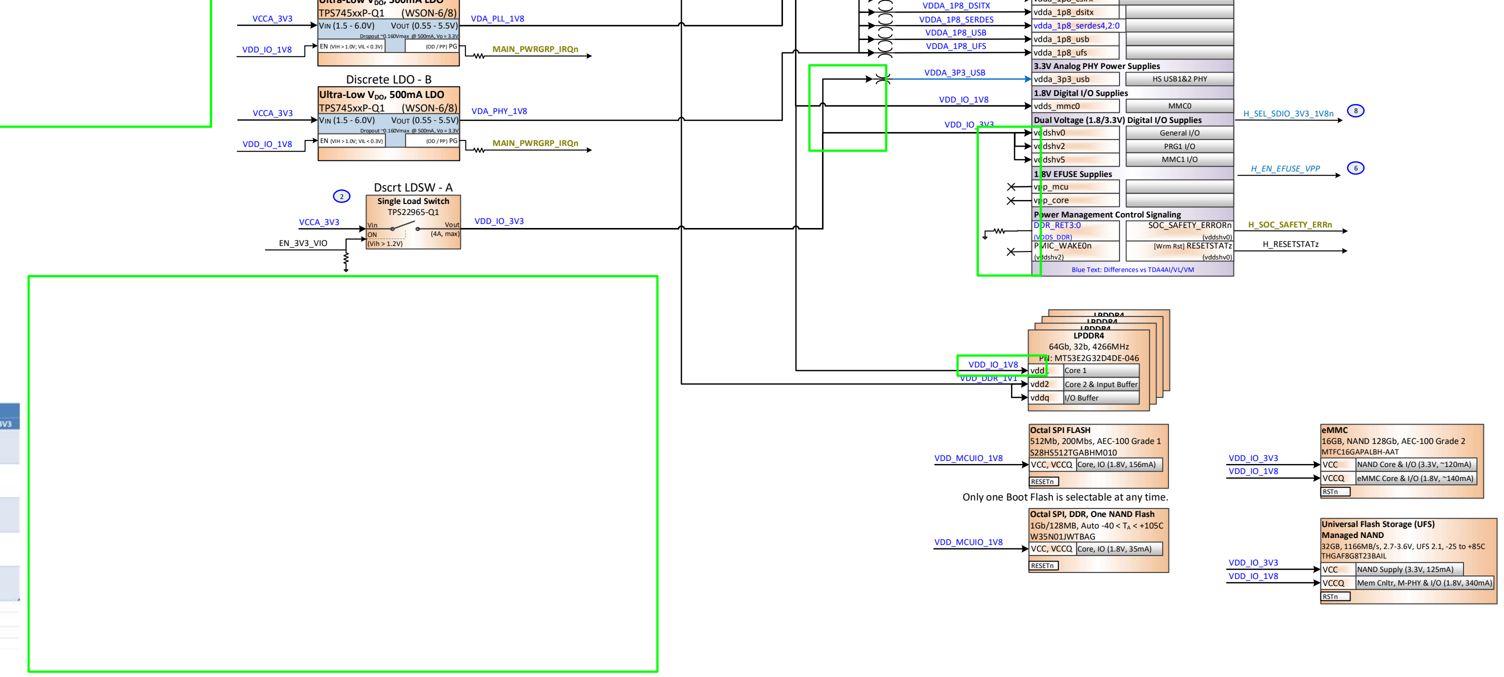
Features Supported (EVM Max Features):

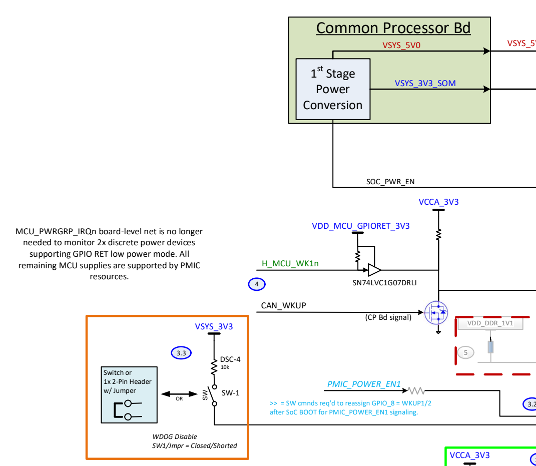
1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
2. Functional Safety: ASIL-D capable sys w/ isolated Main & MCU power rails (supply FFI)
3. 4x SDRAMs: 32Gb, 4-Die, 32b, 4266MTs, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or Hyperflash & eMMC, UFS
5. Signaling Levels: MCU & Main Dual VIO
6. Low power modes:
    a. MCU Island/Only with Dual VIO (needs 4 indep pwr rails & 1 cntrl signal min)

PDN-3F vs -3A Change List Summary:

1. Remove GPIO Ret power & VMON components (dscrt LDO-C, LDSW-B, SVS-B) then connect SoC input supply:
    a. SOC's VDD_MCU_WAKE1 to VDD_MCU_0V85 power rail
    b. SOC's VDDSHV0_MCU to VDD_MCUIO_3V3 power rail
    c. SOC's PMIC_WAKE1n & PMIC_WAKEn0 become No connects
    d. PMIC GPIO5 = EN_GPIO_RET is no needed & can be reassigned by SW after boot.
    e. PMIC GPIO10 = MCU_PWRGRP_IRQn is not needed & must be pulled up to VCCA_3V3.
2. Remove DDR Ret power component (dscrt LDO-D) then connect LPDDR input supply:
    a. LPDDR4's VDD1 to VDD_IO_1V8 power rail
    b. SoC's DDR_RETx inputs need to be disabled by connecting pull-down Rs to Gnd.
3. Remove compliant high-speed SD Card power component (dscrt LDO-E) then connect SoC input supply:
    a. VDDSHV5 to VDD_IO_3V3 power rail
4. Remove compliant USB 2.0 data eye power component (dscrt LDO-F) then connect analog filter input supplying SoC input:
    a. VDDA_3P3_USB to VDD_IO_3V3 power rail
5. Remove high-security Efuse programming power component (dscrt LDO-G) then leave SoC input supply:
    a. VPP_CORE & VPP_CPU become No Connects







MCU_PWRGRP_IRQn board-level net is no longer needed to monitor 2x discrete power devices supporting GPIO RET low power mode. All remaining MCU supplies are supported by PMIC resources.

14) SVS-B device & MCU_PWRGRP_IRQn board-level net are no longer needed to monitor 2x discrete power devices due to removing GPIO Retention low power mode. All remaining MCU supplies are supported by PMIC resources which have OV/UV monitoring & will report faults directly to PMIC PFSM for action. A pull-up resistor must remain connected to GPIO_10 to avoid false positive MCU power group interrupts.

>> = SW commands req'd to reassign GPIO pin function after SoC BOOT per board design needs.

Only one Boot Flash is selectable at any time.

Notes:

1) Functional Safety requires monitoring all "safety critical" power rails (i.e. VSYS_3V3 input, key SoC supplies) that could cause severe system failures. ASIL classification depends on the end product use case & what SoC resources a customer is using that are considered to be safety-related. SoC has internal OV & UV monitoring for key SoC MCU & Main voltage domains. The status is reported by SoC's Power OK (POK) status bits. Optional SoC voltage monitoring inputs (i.e. VMONx_IR_VEXTxxx) can be used to extend SoC's OV/UV monitoring to a few board level power rails if desired (i.e. load switch Vo = VDD_IO_3V3). The following SoC Main & SDRAM domains are classified as non-critical & do not require direct monitoring: VDDSHV5 (SD Card), VPP_CORE, VPP_MCU, VDDA_3P3_USB & VDD1_LPDDR4_1V8.

2) Load Switches (LdSw) have been used to create VDD_MCUIO_3V3, VDD_GPIORET_3V3 & VDD_IO_3V3 power rails from VCCA_3V3 to provide the following benefits:
   A) Correct SoC power supply sequencing by using PMIC resources (GPIO signals & power resource outputs) with desired start-up & shut-down timing delays per NVM settings.
   B) PMIC monitoring of "VCCA Over Voltage" (+5 to +10%) allows PMIC to disconnect 3.3V power rails from SoC if OV condition is detected.
   C) Enables low power modes (MCU Only, GPIO_RET & DDR_RET) since the different 3.3V power rails must be disabled independently for different low power modes.
   D) Connecting VCCA_3V3 directly to SoC 3.3V input supplies is ONLY recommended if low power modes are used and a full SoC power up seq is executed any time the VCCA_3V3/VSYS_3V3 is energized since partial powering of the SoC for extended time could negatively impact POH reliability.

3.1) PMIC NVM Rev 1 assigned multiple interface signals to GPIO8 with default NVM setting of GPIO_8 = DISABLE _WDOG function and required interface buffer circuitry, see PROC141E4_SCH for details.
   A) DISABLE_WDOG (NVM setting): PMIC latches logic level at GPIO8 pin on rising edge of PMIC's nRSTOUT = H_MCU_PORz_1V8 at end of power-up seq.
      a) High level at GPIO8 pin (SW-1/Jmpr-1 = closed) directs PMIC to disable Watch-Dog Timer (by setting WD_PWRHOLD bit to disable timer's long-window time-out) for development/debug.
      b) Low level at GPIO8 pin (SW-1/Jmpr-1 = open due to PMIC default internal pull-down R) enables Watch-Dog Timer (default setting enables timer's long-window time-out).
   B) After system SW boots, SW needs to reassign GPIO_8 = GPI function to operate with PDN's MAIN_PWRGRP_IRQ/_IRQn (asserted high or low) signal to allow PMIC to take action if a fault occurs.

3.2) PMIC NVM Rev2 & 3 changes are listed below. There are EVM board SCH/BOM impacts, see J784S4_EVM_..._PDN-3A v0.19 for details.
   1. PMIC VCCA input voltage level auto-detection that enables 1x PMIC PN to support PDNs using either 5V or 3.3V.
   2. PMIC internal Watchdog Timer is disabled at start-up. This allows GPIO8 function to be used as a PMIC internal configuration control. MCU SW will need to start watchdog timer as part of enabling full FuSa features.
   3. GPIO8 logic level selects the PDN type/scheme by latching level before the 3ms time step during power up sequence & directs PMIC to configure internal resources as follows:
      Low = Isolated PDN type directs PMIC to create MCU & SOC power groups; Enables BUCK5 per power up seq (Removes MCU SW write requirement needed in NVM Rev1 above.)
      High = Grouped PDN type directs PMIC create only MCU power group; Removes BUCK5 from pwr up seq (Allow SW to reassign Buck5 for peripheral devices that can be enabled after boot)

3.3) PMIC NVM Rev 4 has been optimized for end product production flow by enabling Watch Dog Timer to support FuSa by default, see J784S4_EVM_..._PDN-3A v0.20 & up & PROC141E5_SCH for details. GPIO9 has been used to support multiple interface signals as listed below.
   A) DISABLE_WDOG (optional): PMIC latches logic level at GPIO9 pin at transition from standby to active start-up sequence.
      a) High level at GPIO9 pin (SW-1/Jmpr-1 = closed) directs PMIC to disable Watch-Dog Timer (by setting WD_PWRHOLD bit to disable timer's long-window time-out).
      b) Low level at GPIO9 pin (SW-1/Jmpr-1 = open due to PMIC default internal pull-down R) enables Watch-Dog Timer (default setting enables timer's long-window time-out).
   B) EN_3V3_VIO (required): After PMIC NVM initialization, GPIO9 = GPO function to provide enable & disable control of load switch supplying VDD_IO_3V3 power rail.
      a) Disabling the WDOG timer is for development & debug tasks. Applying a pull-up R to disable WDOG timer will result in early enabling of discrete LDSW-A (VDD_IO_3V3), LD0-E (VDD_SD_DV) & LDO-F (VDA_USB_3V3). All of these supplies are 3.3V level and are part of the 1st group of supplies to be energized at the start of a power up seq. SoC will not be negatively impacted if these 3.3V supplies are enabled ahead of remaining 3.3V supplies sourced from PMIC and before the rest of SoC supplies begin a normal power up seq during temporary development & debugging activities.

4) GPIO Retention (aka GPIO_RET, IO_RET, IO Wake) low power mode requires:
   A) SoC SW executes command sequence that sets key PMIC register bits in order to enter GPIO_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
   B) After entering GPIO_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
      1. VDD_GPIORET_WK_0V8 supplying MCU's VDD_MCU_WAKE1 for MCU's 0.8V wake-up logic
      2. VDD_GPIORET_IO_3V3 supplying MCU's VDDSHV0_MCU for MCU's 3.3V IO toggle activity
   C) PDN system exits GPIO_RET state upon receiving logic toggles on SoC's MCU monitored IO signals ref to VDDSHV0_MCU supply. Then H_MCU_WAKE1n (= SoC's Open-Drain PMIC_WAKE1n, active low) signal connected to PMIC, GPIO_4 (= WKUP1 default function for Full Active or = WKUP2 for MCU Only destination state) is asserted and PMIC state machine transitions PDN system to desired targeted wake up state.
   D) The Open-Drain Buffer SN74LVC1G07DRLI (tri-states IO when power is OFF) connects PMIC_WAKE1n to SOC_PWR_WKn net at discrete open-drain FET node. It is needed to isolate the SoC output buffer from the always on VCCA_3V3 used as pull-up supply to prevent current bleeding into SoC during low power modes (MCU Only, DDR_RET) when VDD_GPIORET_3V3 is typically disabled.

5) DDR Retention (aka DDR_RET, Suspend-to-RAM, S2R) low power mode requires:
   A) PMIC PN to assign GPIO_6 = Regulator Enable (REGEN) function with an open-drain output buffer type per NVM default settings. The board level net H_DDR_RET_1V1 signal is pulled up to VDD_DDR_1V1 & connected to SoC's DDR_RET input. When this input is set high, SoC's EMIF IO buffers are set to high-Z state as part of entering DDR_RET mode.
   B) SoC SW executes command sequence that sets key PMIC register bits in order to enter DDR_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
   C) After entering DDR_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
      1. VDD_DDR_1V1 supplying both SoC EMIF & SDRAM IO voltages
      2. VDD1_DDR_1V8 supplying SDRAM only
   D) PDN system exits DDR_RET upon detecting a CAN_WAKE signal edge toggle on PMIC's GPIO_4 = LP_WKUP1 function per NVM settings that initiates exiting DDR_RET mode & restores Full Active processor operations.

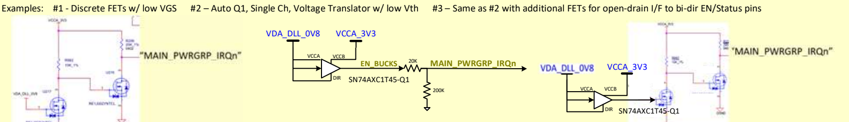
6) SoC devices come in two types: General Purpose (GP) & High Security (HS). All GP devices can leave the VPP domains unconnected per DM. Pre-programmed HS devices can also leave VPP domains unconnected if no additional EFUSE programming is needed. If customer desires capability for in-the-field updates, then on-board EFUSE programming will require an additional 1.8V, 150mA LDO. When disabled, this LDO's Vo will need a high impedance output. Recommended PNs: TPS73101-EP, fixed 1.8V TPS73118-Q1 or TLV70018-Q1. The EN_EFUSE_VPP control signal must be sourced from an SoC GPIO for this PDN (due to limited number of PMIC GPIOs). This allows SoC SW to control Efuse VPP voltage level by enabling & disabling dedicated LDO as needed to program High Security SoC Efuses (see SoC DM for details).

7) PDN shows SoC's VDA_3P3_USB domain supplied from a low noise LDO with a VSYS_5V input as preferred for optimal USB 2.0 data eye mask performance. If USB 2.0 I/F is not used or is only needed for development tasks, then the digital VDD_IO_3V3 rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_3V3 rail to support USB 2.0 I/F removes a discrete LDO & VSYS_5V input but could negatively impact data eye performance due to higher supply noise causing data eye mask violations.

8) PDN shows SoC's Main domain's VDDSHV5 supply being sourced from a dual voltage LDO with a VSYS_5V input as preferred for compliant high-speed SD card operation. If SD card is not used or only standard data rate operation is sufficient, then the digital VDD_IO_3V3 rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_3V3 rail to support SD Card operation removes dual voltage, discrete LDO & VSYS_5V input but will restrict data rates to standard 12Mb/s with VIO = 3.3V.

9) A low voltage translator with a VGS or VIH max spec less than 0.76V (-5% supply tol on 0.8V) is needed to ensure a 3.3V logic high level output. 3x different examples are shown below:
   #1 A discrete FET voltage translator with low VGS threshold below an input min 0.76V. EVM PROC141E2/E3_SCHs use discrete FET PN w/ low VGS but only industrial temp grade.
   #2 A single channel, voltage translator (SN74AXC1T45-Q1) that is automotive AEC-Q100 qualified, grade1 for -40 to +125C operation could be used as an alternative. Ensure valid logic levels are provided at both GPIO8 (as desc above) & discrete Buck's EN input pin (snap-shot shows Buck's internal bi-dir EN/STATUS circuitry).
      A.) The PMIC's GPIO8 has NVM default setting that enables a 400k internal pull-down. This should be sufficient to keep GPIO8 net from "floating" above GPIO's VIH min level when VDA_DLL_0V8 is disabled which causes the SN74AXC1T45-Q1 output to be tri-stated.
      B.) Customer may want to add a pull-down R on the board (showing a 200k below) just in case the PMIC's internal pull-down is not strong enough to ensure a low logic level.
   #3 A non-inverting FET stage (Ex 3, shown below) could be added to shunt the "MAIN_PWRGRP_IRQn" net to Gnd if items 2A or 2B are not sufficient.

Examples: #1 - Discrete FETs w/ low VGS #2 – Auto Q1, Single Ch, Voltage Translator w/ low Vth #3 – Same as #2 with additional FETs for open-drain I/F to bi-dir EN/Status pins



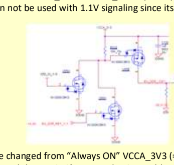
(OD buffer I/F needed for TPS6287x-Q1 buck connection using AEC-100 Translator)

10) Worst case analysis for very high thermal use cases could result in VCCA_3V3 load current in 15-18A range. This large load current range could lead to a 60 – 72mV voltage drop across Safety FET (Recm'd PN: NVMFS4C05N) for a max RDSon = 4mohm. The TPS22965-Q1 load switches have max RDSon = 27mohm with 4A max rating resulting in additional max drop of 108mV. SoC's 3.3V supply tolerance is +/-5% or 165mV. Total RDSon drops across Safety FET & Load Switches range from 168 – 180mV which exceed SoC's min voltage limit. For this reason, the Tulip buck input voltage will be moved from VCCA_3V3 to VSYS_3V3 since VDD_CPU_AVS & VDD_CORE_0V8 rails account for more than 70% of VCCA_3V3 worst case load currents.

11) If GPIO Retention low power mode is desired, then connect all SVS-B VMON inputs to existing MCU supplies (as shown) sourced from PMIC to enable 1x common PN for SVS-A & -B while avoiding false positives on "unconnected" VMONs. If an end product does not need GPIO Retention low power mode, then the 3x following components can be removed from the PDN: LDO-C, LDSW-B & SVS-B. Group the SoC input supplies according to he "PDN Features for Isolated Power Rails" table shown below using the "Standard Operation & MCU Only" assignments row.

12) The OR gate function enabling the discrete LDO supplying 1.8V to LPDDR4 VDD1 (Internal bias voltage) needs to revert back to original discrete FET OR gate circuitry (see PROC141E2_SCH or snap-shot below). Reason for reverting is due to the OR gate needing a max input voltage threshold less than 1.05V (-5% of 1.1V) since the EN_DDR_RET_1V1 signal is sourced from an open-drain PMIC GPIO with PU resistor to VDD_DDR_1V1 supply with +/-5% supply tolerance. In addition, the OR gate needs to remain energized during DDR Retention low power mode when only VDD_DDR_1V1 & VDD1_DDR_1V8 rails remain energized. Therefore, the OR gate supply must use VSYS_3V3 or VCCA_3V3 input supply that remains on in DDR Ret mode. The single logic gate IC (SN74LVC1G97-Q1) used for enabling other power resources interfaced to 3.3V signaling levels can not be used with 1.1V signaling since its max input voltage threshold for 3.3V supply is ~2.2V.

Original discrete FET OR gate circuit used in PROC141E2_SCH:



13) The Safety Voltage Supervisor (SVS-A & SVS-B) supply connections need to be changed from "Always ON" VCCA_3V3 (=VSYS_3V3) to a "PMIC controlled" power rail to enable resetting of an asserted IRQn signal by power cycling SVS devices. During functional testing, it was discovered that an SVS's asserted IRQn could not be reset if MCU processor I2C comm with SVS devices is lost. This will happen if a MCU Power Error occurs (i.e. fault on a MCU supply) since this will cause the PMIC PFSM to transition the system to the desired Safe Recovery state (powers down all SoC supplies). However, if the SoC PDN's input voltage (VSYS_3V3) remains energized, then the energized SVS devices will maintain an asserted IRQn and the system will not be able to execute a SoC cold boot attempt due a previously asserted IRQn will cause the PMIC to abort an SoC power up sequence attempt. A SVS device power cycle will reset an asserted IRQn signal, enabling the desired SoC cold boot attempt. By replacing "Always ON" VCCA_3V3 supply connections with a PMIC controlled power rail (VDD_MCUIO_3V3), the SVS devices will have a power cycle event upon entering the Safe Recovery state (per table below). If a fault occurs on a Main domain supply, the PMIC will transition the system to MCU Only state which allows I2C comm to evaluate & potentially log the fault source. The MCU can use I2C comm to clear an asserted IRQn if a system cold boot attempt is desired to try restarting into the Full Active state since a fault might clear if it's due to a random noise event or temperature dependent. The SVS device's "ACTive" input connection will need to be connected to VDD since the new VDD_MCUIO_3V3 supply connection is enabled as part of the SoC power up seq.. This avoids driving a high logic signal into an unenergized device.

PDN State:	Active	MCU Only	Safe Recovery
	Main supplies = ON	Main supplies = OFF	Main supplies = OFF
	MCU supplies = ON	MCU supplies = ON	MCU supplies = OFF
	SVS-A = ON	SVS-A = ON	SVS-A = OFF
	SVS-B = ON	SVS-B = ON	SVS-B = OFF

Modular PDNs support Flexible Feature Set Reductions

Feature Removals	Power Resource & Power Rail Removals	New Supply Mappings
HS SoC EFUSE Programming	Discrete LDO VPP_EFUSE_1V8	SoC: VPPs => No connects
Compliant, USB 2.0 data eye	Discrete LDO VDA_USB_3V3	SoC: VDDA_3P3_USB => filtered VDD_IO_3V3
Compliant, High-Speed SD Card	Discrete LDO VDD_SD_DV	SoC: VDDSHV5 => VDD_IO_3V3 or VDD_IO_1V8
DDR Retention low power mode	Discrete LDO VDD1_DDR_1V8	LPDDR4: VDD1 => VDD_IO_1V8
MCU GPIO Retention low power mode	Discrete LDO VDD_MCU_GPIORET_0V8	Isolated MCU & Main PDN Schemes: SoC: VDD_MCU_WAKE1 => VDD_MCU_0V85 Grouped MCU & Main PDN Schemes: SoC: VDD_MCU_WAKE1 => VDD_CORE_0V8
	Discrete LDSW VDD_MCU_GPIORET_3V3	Isolated MCU & Main PDN Schemes: SoC: VDDSHV0_MCU => VDD_MCUIO_3V3 or VDD_MCUIO_1V8 Grouped MCU & Main PDN Schemes: SoC: VDDSHV0_MCU => VDD_IO_3V3 or VDD_IO_1V8
	Discrete SVS	PMIC: GPIO_10 pulled-up to VCCA_3V3
Main GPIO Retention low power mode	Discrete LDO VDD_GPIORET_0V8	SoC: VDD_WAKE0 => VDD_CORE_0V8
	Discrete LDSW VDD_GPIORET_3V3	SoC: VDDSHV2 => VDD_IO_3V3 or VDD_IO_1V8
	Discrete SVS	PMIC: GPIO_10 pulled-up to VCCA_3V3

SoC Input Supply to Power Rail Groupings vs PDN Low Power Mode Features

PDN Features	Isolated MCU & Main PDN Power Rails							
	VDD_MCU_0V85	VDD_CORE_0V8	VDD_MCUIO_3V3	VDD_IO_1V8	VDD_IO_3V3	VDD1_DDR_1V8	VDD_GPIORET_0v8	VDD_GPIORET_3V3
Standard Operation & MCU Only	vdd_mcu vddar_mcu vdd_mcu_wake1	vdd_core vdd_wake0	vddshv0_mcu vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0 vddshv2			
DDR Retention	vdd_mcu vddar_mcu vdd_mcu_wake1	vdd_core vdd_wake0	vddshv0_mcu vddshv2_mcu	vdds_mmc0	vddshv0 vddshv2	DDR: vdd1		
GPIO Retention-MCU & Main	vdd_mcu vddar_mcu	vdd_core	vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0		vdd_mcu_wake1 vdd_wake0	vddshv0_mcu vddshv2
GPIO Retention-MCU	vdd_mcu vddar_mcu	vdd_core vdd_wake0	vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0 vddshv2		vdd_mcu_wake1	vddshv0_mcu
GPIO Retention-Main	vdd_mcu vddar_mcu vdd_mcu_wake1	vdd_core	vddshv0_mcu vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0		vdd_wake0	vddshv2

Notes:
1) Power rail names shown in "ALL CAPITAL LETTERS"
2) SoC input supplies shown in "all lower case letters"

J784S4 EVM Leo + 2x High-Current Pwr Stages(HCPS) PDN-3G

(All SoC PN variants: TDA4AP/VP/AH/VH)

(Power Rail & GPIO Mapping Overview)

V0.27 10/31/2024	1. Updated discrete buck's ENABLE input connections to more accurately show the 20k resistor located in-line to voltage translator output. 2. Updated Note 9, example #2 text & diag to show 20k resistor in-line with buck's ENABLE inputs.
V0.29 1/27/2025	1. Fixed power rail connections to OSPI memories by correctly changing name from VDD_MCUIO_1V8 to VDD_IO_1V8 for Grouped PDN scheme.
V0.32 5/22/2025	1. Updated SVS-A & B to capture OV/UV threshold values per PN "004" default settings. Customers can adjust thresholds via I2C after boot as desired.

Legend:

Power Rails <Pwr Rail Name>
PDN base
MCU Only/Safety Island
GPIO Retention
DDR_Retention (aka S2R)
End Product option
Peripheral loads (SW config'd after boot)

Control Signals: < Signals >
General cntrl & logic
(Italic = SW config'd after boot)
PDN base cntrl
Func Safety
MCU Only/Island
GPIO Retention
DDR_Retention (aka S2R)
End Product option
Peripheral comps
Debug/Development option

Note items
On-Chip "Pwr OK" Monitors (OV & UV)
On-Chip "Pwr OK" Monitors (UV only)
Provisioned In-Line Supply Filter
High-lighted diagram changes

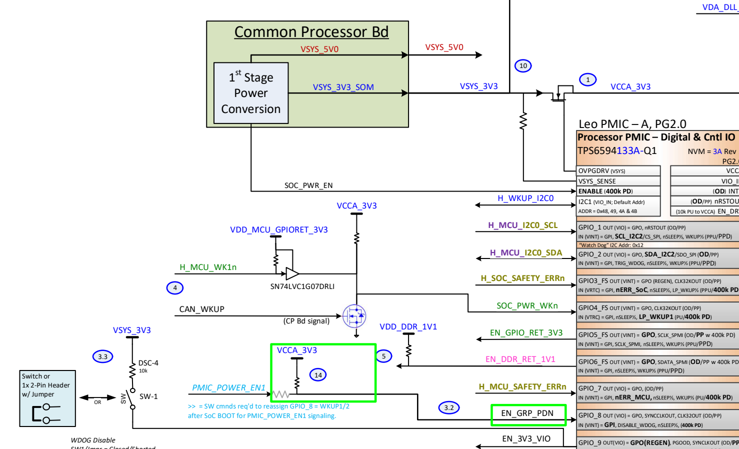
Leo PMIC-A, PN TPS6594133ARWERQ1 (TI PN ID = 1, MP Buck Rails = 3, PG2.0 NVM ID = 3A Rev 5)
HCPS-A & B, Tulip PN TPS62873Y1QWRXSRQ1 (15A PN ID = 3, Jacinto7 Family ID = Y1)
Safety Voltage Supervisor, PN TPS389006004RTERQ1 (OTP ID = 004 = new common PN for use with Jacinto7 J784S4 PDN-3A scheme)

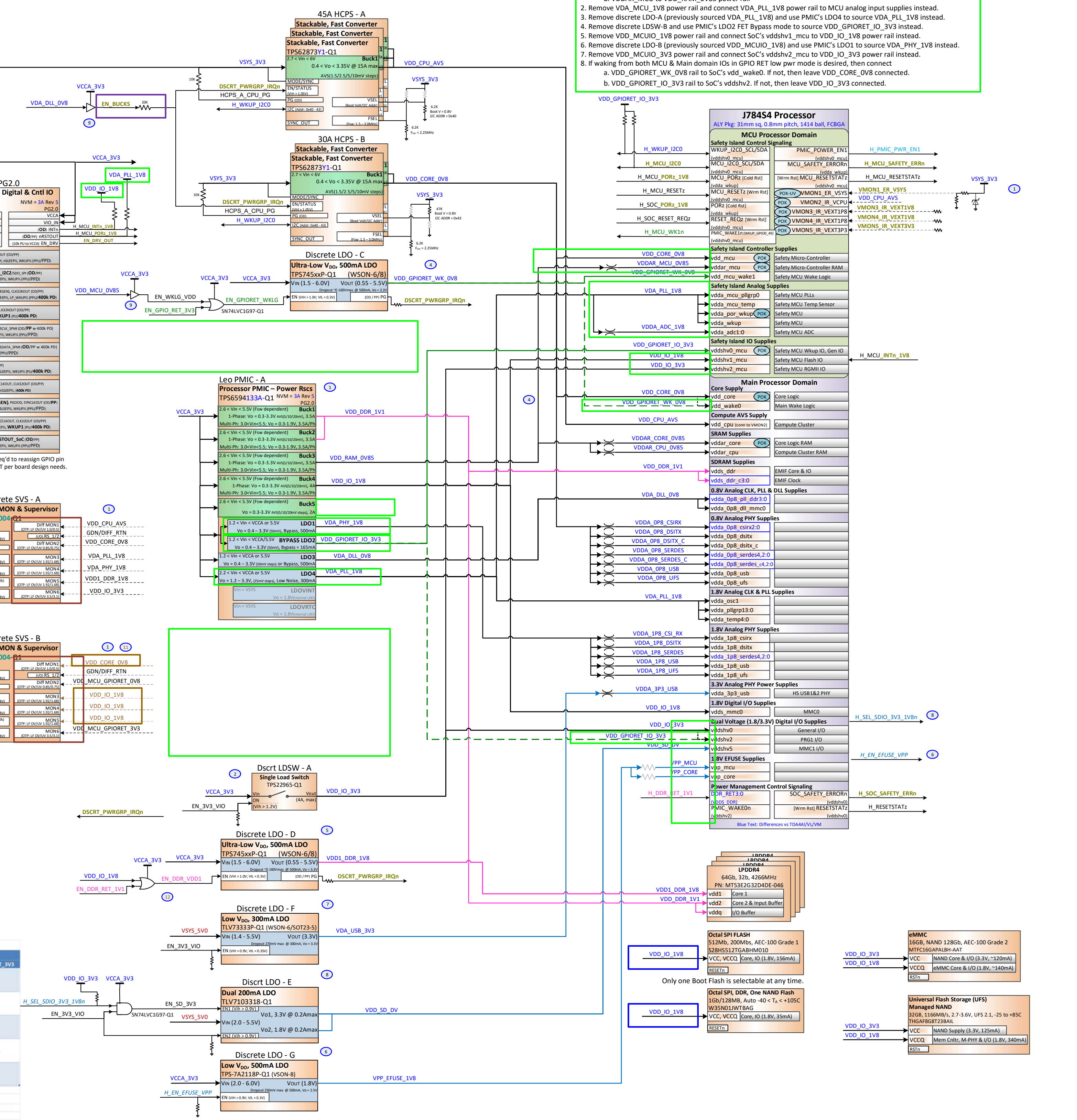
Features Supported (EVM Max Features):

1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
2. Functional Safety: ASIL-D capable sys w/ Grouped Main & MCU power rails
3. 4x SDRAMs: 32Gb, 4-Die, 32b, 4266MTs, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or Hyperflash & eMMC, UFS
5. Signaling Levels: MCU & Main Dual VIO
6. Low power modes:
   b. MCU GPIO Retention (needs 2 indep pwr rails & 1 cntrl signals min)
   c. DDR Retention/S2R (needs 1 add'l indep pwr rail & 1 cntrl signal min)
7. End Product Options:
   a. Compliant high-speed SD Card (needs 1 indep pwr rail & 1 VIO cntrl signal & discrete LDO needs Vin = 5V)
   b. Compliant USB 2.0 data eye (needs 5V, 1 indep pwr rail & discrete LDO needs Vin = 5V)
   c. HS SoC Efuse programming on-board (needs 1 indep pwr rail & 1 cntrl signal)

PDN-3G vs -3A Change List Summary:

1. Remove VDD_MCU_0V85 power rail then connect SoC input supply:
   a. VDD_MCU to VDD_CORE_0V8 power rail
   b. VDDAR_MCU to VDD_RAM_0V85 power rail
2. Remove VDA_MCU_1V8 power rail and connect VDA_PLL_1V8 power rail to MCU analog input supplies instead.
3. Remove discrete LDO-A (previously sourced VDA_PLL_1V8) and use PMIC's LDO4 to source VDA_PLL_1V8 instead.
4. Remove discrete LDSW-B and use PMIC's LDO2 FET Bypass mode to source VDD_GPIORET_IO_3V3 instead.
5. Remove VDD_MCUIO_1V8 power rail and connect SoC's vddshv1_mcu to VDD_IO_1V8 power rail instead.
6. Remove discrete LDO-B (previously sourced VDD_MCUIO_1V8) and use PMIC's LDO1 to source VDA_PHY_1V8 instead.
7. Remove VDD_MCUIO_3V3 power rail and connect SoC's vddshv2_mcu to VDD_IO_3V3 power rail instead.
8. If waking from both MCU & Main domain IOs in GPIO RET low pwr mode is desired, then connect
   a. VDD_GPIORET_WK_0V8 rail to SoC's vdd_wake0. If not, then leave VDD_CORE_0V8 connected.
   b. VDD_GPIORET_IO_3V3 rail to SoC's vddshv2. If not, then leave VDD_IO_3V3 connected.





Notes:

1) Functional Safety requires monitoring all "safety critical" power rails (i.e. VSYS_3V3 input, key SoC supplies) that could cause severe system failures. ASIL classification depends on the end product use case & what SoC resources a customer is using that are considered to be safety-related. SoC has internal OV & UV monitoring for key SoC MCU & Main voltage domains. The status is reported by SoC's Power OK (POK) status bits. Optional SoC voltage monitoring inputs (i.e. VMONx_IR_VEXTxxx) can be used to extend SoC's OV/UV monitoring to a few board level power rails if desired (i.e. load switch Vo = VDD_IO_3V3). The following SoC Main & SDRAM domains are classified as non-critical & do not require direct monitoring: VDDSHV5 (SD Card), VPP_CORE, VPP_MCU, VDDA_3P3_USB & VDD1_LPDDR4_1V8.

2) Load Switches (LdSw) have been used to create VDD_MCUIO_3V3, VDD_GPIORET_3V3 & VDD_IO_3V3 power rails from VCCA_3V3 to provide the following benefits:
   A) Correct SoC power supply sequencing by using PMIC resources (GPIO signals & power resource outputs) with desired start-up & shut-down timing delays per NVM settings.
   B) PMIC monitoring of "VCCA Over Voltage" (+5 to +10%) allows PMIC to disconnect 3.3V power rails from SoC if OV condition is detected.
   C) Enables low power modes (MCU Only, GPIO_RET & DDR_RET) since the different 3.3V power rails must be disabled independently for different low power modes.
   D) Connecting VCCA_3V3 directly to SoC 3.3V input supplies is ONLY recommended if low power modes are used and a full SoC power up seq is executed any time the VCCA_3V3/VSYS_3V3 is energized since partial powering of the SoC for extended time could negatively impact POH reliability.

3.1) PMIC NVM Rev 1 assigned multiple interface signals to GPIO8 with default NVM setting of GPIO_8 = DISABLE _WDOG function and required interface buffer circuitry, see PROC141E4_SCH for details.
   A) DISABLE_WDOG (NVM setting): PMIC latches logic level at GPIO8 pin on rising edge of PMIC's nRSTOUT = H_MCU_PORz_1V8 at end of power-up seq.
      a) High level at GPIO8 pin (SW-1/Jmpr-1 = closed) directs PMIC to disable Watch-Dog Timer (by setting WD_PWRHOLD bit to disable timer's long-window time-out) for development/debug.
      b) Low level at GPIO8 pin (SW-1/Jmpr-1 = open due to PMIC default internal pull-down R) enables Watch-Dog Timer (default setting enables timer's long-window time-out).
   B) After system SW boots, SW needs to reassign GPIO_8 = GPI function to operate with PDN's MAIN_PWRGRP_IRQ/_IRQn (asserted high or low) signal to allow PMIC to take action if a fault occurs.

3.2) PMIC NVM Rev2 & 3 changes are listed below. There are EVM board SCH/BOM impacts, see J784S4_EVM_...._PDN-3A v0.19 for details.
   1. PMIC VCCA input voltage level auto-detection that enables 1x PMIC PN to support PDNs using either 5V or 3.3V.
   2. PMIC internal Watchdog Timer is disabled at start-up. This allows GPIO8 function to be used as a PMIC internal configuration control. MCU SW will need to start watchdog timer as part of enabling full FuSa features.
   3. GPIO8 logic level selects the PDN type/scheme by latching level before the 3ms time step during power up sequence & directs PMIC to configure internal resources as follows:
      Low = Isolated PDN type directs PMIC to create MCU & SOC power groups; Enables BUCK5 per power up seq (Removes MCU SW write requirement needed in NVM Rev1 above.)
      High = Grouped PDN type directs PMIC create only MCU power group; Removes BUCK5 from pwr up seq (Allow SW to reassign Buck5 for peripheral devices that can be enabled after boot)

3.3) PMIC NVM Rev 4 has been optimized for end product production flow by enabling Watch Dog Timer to support FuSa by default, see J784S4_EVM_...._PDN-3A v0.20 & up & PROC141E5_SCH for details.
   GPIO9 has been used to support multiple interface signals as listed below.
   A) DISABLE_WDOG (optional): PMIC latches logic level at GPIO9 pin at transition from standby to active start-up sequence.
      a) High level at GPIO9 pin (SW-1/Jmpr-1 = closed) directs PMIC to disable Watch-Dog Timer (by setting WD_PWRHOLD bit to disable timer's long-window time-out).
      b) Low level at GPIO9 pin (SW-1/Jmpr-1 = open due to PMIC default internal pull-down R) enables Watch-Dog Timer (default setting enables timer's long-window time-out).
   B) EN_3V3_VIO (required): After PMIC NVM initialization, GPIO9 = GPO function to provide enable & disable control of load switch supplying VDD_IO_3V3 power rail.
      a) Disabling the WDOG timer is for development & debug tasks. Applying a pull-up R to disable WDOG timer will result in early enabling of discrete LDSW-A (VDD_IO_3V3), LD0-E (VDD_SD_DV) & LDO-F (VDA_USB_3V3). All of these supplies are 3.3V level and are part of the 1st group of supplies to be energized at the start of a power up seq. SoC will not be negatively impacted if these 3.3V supplies are enabled ahead of remaining 3.3V supplies sourced from PMIC and before the rest of SoC supplies begin a normal power up seq during temporary development & debugging activities.

4) GPIO Retention (aka GPIO_RET, IO_RET, IO Wake) low power mode requires:
   A) SoC SW executes command sequence that sets key PMIC register bits in order to enter GPIO_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
   B) After entering GPIO_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
      1. VDD_GPIORET_WK_0V8 supplying MCU's VDD_MCU_WAKE1 for MCU's 0.8V wake-up logic
      2. VDD_GPIORET_IO_3V3 supplying MCU's VDDSHV0_MCU for MCU's 3.3V IO toggle activity
   C) PDN system exits GPIO_RET state upon receiving logic toggles on SoC's MCU monitored IO signals ref to VDDSHV0_MCU supply. Then H_MCU_WAKE1n (= SoC's Open-Drain PMIC_WAKE1n, active low) signal connected to PMIC, GPIO_4 (= WKUP1 default function for Full Active or = WKUP2 for MCU Only destination state) is asserted and PMIC state machine transitions PDN system to desired targeted wake up state.
   D) The Open-Drain Buffer SN74LVC1G07DRLI (tri-states IO when power is OFF) connects PMIC_WAKE1n to SOC_PWR_WKn net at discrete open-drain FET node. It is needed to isolate the SoC output buffer from the always on VCCA_3V3 used as pull-up supply to prevent current bleeding into SoC during low power modes (MCU Only, DDR_RET) when VDD_GPIORET_3V3 is typically disabled.

5) DDR Retention (aka DDR_RET, Suspend-to-RAM, S2R) low power mode requires:
   A) PMIC PN to assign GPIO_6 = Regulator Enable (REGEN) function with an open-drain output buffer type per NVM default settings. The board level net H_DDR_RET_1V1 signal is pulled up to VDD_DDR_1V1 & connected to SoC's DDR_RET input. When this input is set high, SoC's EMIF IO buffers are set to high-Z state as part of entering DDR_RET mode.
   B) SoC SW executes command sequence that sets key PMIC register bits in order to enter DDR_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
   C) After entering DDR_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
      1. VDD_DDR_1V1 supplying both SoC EMIF & SDRAM IO voltages
      2. VDD1_DDR_1V8 supplying SDRAM only
   D) PDN system exits DDR_RET upon detecting a CAN_WAKE signal edge toggle on PMIC's GPIO_4 = LP_WKUP1 function per NVM settings that initiates exiting DDR_RET mode & restores Full Active processor operations.

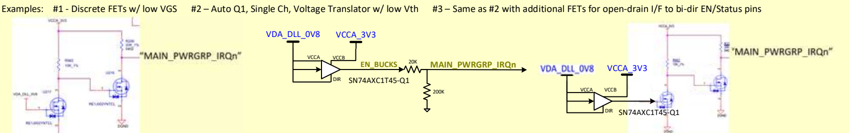
6) SoC devices come in two types: General Purpose (GP) & High Security (HS). All GP devices can leave the VPP domains unconnected per DM. Pre-programmed HS devices can also leave VPP domains unconnected if no additional EFUSE programming is needed. If customer desires capability for in-the-field updates, then on-board EFUSE programming will require an additional 1.8V, 150mA LDO. When disabled, this LDO's Vo will need a high impedance output. Recommended PNs: TPS73101-EP, fixed 1.8V TPS73118-Q1 or TLV70018-Q1. The EN_EFUSE_VPP control signal must be sourced from an SoC GPIO for this PDN (due to limited number of PMIC GPIOs). This allows SoC SW to control Efuse VPP voltage level by enabling & disabling dedicated LDO as needed to program High Security SoC Efuses (see SoC DM for details).

7) PDN shows SoC's VDA_3P3_USB domain supplied from a low noise LDO with a VSYS_5V input as preferred for optimal USB 2.0 data eye mask performance. If USB 2.0 I/F is not used or is only needed for development tasks, then the digital VDD_IO_3V3 rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_3V3 rail to support USB 2.0 I/F removes a discrete LDO & VSYS_5V input but could negatively impact data eye performance due to higher supply noise causing data eye mask violations.

8) PDN shows SoC's Main domain's VDDSHV5 supply being sourced from a dual voltage LDO with a VSYS_5V input as preferred for compliant high-speed SD card operation. If SD card is not used or only standard data rate operation is sufficient, then the digital VDD_IO_3V3 rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_3V3 rail to support SD Card operation removes dual voltage, discrete LDO & VSYS_5V input but will restrict data rates to standard 12Mb/s with VIO = 3.3V.

9) A low voltage translator with a VGS or VIH max spec less than 0.76V (-5% supply tol on 0.8V) is needed to ensure a 3.3V logic high level output. 3x different examples are shown below:
   #1 A discrete FET voltage translator with low VGS threshold below an input min 0.76V. EVM PROC141E2/E3_SCHs use discrete FET PN w/ low VGS but only industrial temp grade.
   #2 A single channel, voltage translator (SN74AXC1T45-Q1) that is automotive AEC-Q100 qualified, grade1 for -40 to +125C operation could be used as an alternative. Ensure valid logic levels are provided at both GPIO8 (as desc above) & discrete Buck's EN input pin (snap-shot shows Buck's internal bi-dir EN/STATUS circuitry).
      A.) The PMIC's GPIO8 has NVM default setting that enables a 400k internal pull-down. This should be sufficient to keep GPIO8 net from "floating" above GPIO's VIH min level when VDA_DLL_0V8 is disabled which causes the SN74AXC1T45-Q1 output to be tri-stated.
      B.) Customer may want to add a pull-down R on the board (showing a 200k below) just in case the PMIC's internal pull-down is not strong enough to ensure a low logic level.
   #3 A non-inverting FET stage (Ex 3, shown below) could be added to shunt the "MAIN_PWRGRP_IRQn" net to Gnd if items 2A or 2B are not sufficient.

   Examples: #1 - Discrete FETs w/ low VGS #2 – Auto Q1, Single Ch, Voltage Translator w/ low Vth #3 – Same as #2 with additional FETs for open-drain I/F to bi-dir EN/Status pins



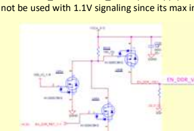
(OD buffer I/F needed for TPS6287x-Q1 buck connection using AEC-100 Translator)

10) Worst case analysis for very high thermal use cases could result in VCCA_3V3 load current in 15-18A range. This large load current range could lead to a 60 – 72mV voltage drop across Safety FET (Recm'd PN: NVMFS4C05N) for a max RDSon = 4mohm. The TPS22965-Q1 load switches have max RDSon = 27mohm with 4A max rating resulting in additional max drop of 108mV. SoC's 3.3V supply tolerance is +/-5% or 165mV. Total RDSon drops across Safety FET & Load Switches range from 168 – 180mV which exceed SoC's min voltage limit. For this reason, the Tulip buck input voltage will be moved from VCCA_3V3 to VSYS_3V3 since VDD_CPU_AVS & VDD_CORE_0V8 rails account for more than 70% of VCCA_3V3 worst case load currents.

11) If GPIO Retention low power mode is desired, then connect all SVS-B VMON inputs to existing MCU supplies (as shown) sourced from PMIC to enable 1x common PN for SVS-A & -B while avoiding false positives on "unconnected" VMONs. If an end product does not need GPIO Retention low power mode, then the 3x following components can be removed from the PDN: LDO-C, LDSW-B & SVS-B. Group the SoC input supplies according to he "PDN Features for Isolated Power Rails" table shown below using the "Standard Operation & MCU Only" assignments row.

12) The OR gate function enabling the discrete LDO supplying 1.8V to LPDDR4 VDD1 (Internal bias voltage) needs to revert back to original discrete FET OR gate circuitry (see PROC141E2_SCH or snap-shot below). Reason for reverting is due to the OR gate needing a max input voltage threshold less than 1.05V (-5% of 1.1V) since the EN_DDR_RET_1V1 signal is sourced from an open-drain PMIC GPIO with PU resistor to VDD_DDR_1V1 supply with +/-5% supply tolerance. In addition, the OR gate needs to remain energized during DDR Retention low power mode when only VDD_DDR_1V1 & VDD1_DDR_1V8 rails remain energized. Therefore, the OR gate supply must use VSYS_3V3 or VCCA_3V3 input supply that remains on in DDR Ret mode. The single logic gate IC (SN74LVC1G97-Q1) used for enabling other power resources interfaced to 3.3V signaling levels can not be used with 1.1V signaling since its max input voltage threshold for 3.3V supply is ~2.2V.

   Original discrete FET OR gate circuit used in PROC141E2_SCH:



13) The Safety Voltage Supervisor (SVS-A & SVS-B) supply connections need to be changed from "Always ON" VCCA_3V3 (=VSYS_3V3) to a "PMIC controlled" power rail to enable resetting of an asserted IRQn signal by power cycling SVS devices. During functional testing, it was discovered that an SVS's asserted IRQn could not be reset if MCU processor I2C comm with SVS devices is lost. This will happen if a MCU Power Error occurs (i.e. fault on a MCU supply) since this will cause the PMIC PFSM to transition the system to the desired Safe Recovery state (powers down all SoC supplies). However, if the SoC PDN's input voltage (VSYS_3V3) remains energized, then the energized SVS devices will maintain an asserted IRQn and the system will not be able to execute a SoC cold boot attempt due a previously asserted IRQn will cause the PMIC to abort an SoC power up sequence attempt. A SVS device power cycle will reset an asserted IRQn signal, enabling the desired SoC cold boot attempt. By replacing "Always ON" VCCA_3V3 supply connections with a PMIC controlled power rail (VDD_MCUIO_3V3), the SVS devices will have a power cycle event upon entering the Safe Recovery state (per table below). If a fault occurs on a Main domain supply, the PMIC will transition the system to MCU Only state which allows I2C comm to evaluate & potentially log the fault source. The MCU can use I2C comm to clear an asserted IRQn if a system cold boot attempt is desired to try restarting into the Full Active state since a fault might clear if it's due to a random noise event or temperature dependent. The SVS device's "ACTive" input connection will need to be connected to VDD since the new VDD_MCUIO_3V3 supply connection is enabled as part of the SoC power up seq.. This avoids driving a high logic signal into an unenergized device.

PDN State:	Active	MCU Only	Safe Recovery
	Main supplies = ON	Main supplies = OFF	Main supplies = OFF
	MCU supplies = ON	MCU supplies = ON	MCU supplies = OFF
	SVS-A = ON	SVS-A = ON	SVS-A = OFF
	SVS-B = ON	SVS-B = ON	SVS-B = OFF

14) PMIC 133A Rev 2 & higher supports "PDN Configuration Control" operation as follows:
During the first ~3-6ms of the SoC power up seq, PMIC's GPIO8 input logic must be held below PMIC's input VIL max to ensure PMIC will latch a low logic level. This directs PMIC's boot-time configuration to support "Isolated MCU & Main" PDN-3A thru -3F schemes by:
a) Creating 2x "MCU & SoC Power Groups" internal to PMIC for proper FuSa response by PFSM actions whenever any faults within either the MCU &/or Main (aka SOC) power rails
b) Including Buck5 to be energized during power up seq).

For "Grouped MCU & Main" PDN-3G thru -3M schemes, a pull-up resistor to VCCA_3V3 is connected to GPIO_8 to ensure a high logic level is latched by PMIC. This directs PMIC's boot-time configuration to support Grouped MCU & Main PDN schemes by:
a) Creating 1x "MCU Power Group" internal to PMIC for proper FuSa response by PFSM actions whenever any faults within either the grouped MCU & Main power rails
b) Excluding Buck5 from being energized during power up seq so that it can either be left unused without any board components or enabled by SW after boot for peripheral loads.

The Safety Voltage Supervisors (SVS-A & -B) IRQn pins, PMIC's GPIO_10 and all discrete power resources all connect to a new net "DSCRT_PWRGRP_IRQn" that gives FuSa coverage for all power rails sourced from discrete power resources. The PMIC continues to treat GPIO_10 input as "MCU_PWRGRP_IRQn" (legacy net name from PDN-3A scheme) which is the 1x PMIC internal power group for Grouped PDN schemes. The internal "MCU_PWR_GRP" will now comprehend both PMIC internal power resources & external discrete power resources. A fault on any of these resources will cause PMIC to shutdown all supplies as desired per FuSa requirements.

Modular PDNs support Flexible Feature Set Reductions

Feature Removals	Power Resource & Power Rail Removals	New Supply Mappings
HS SoC EFUSE Programming	Discrete LDO VPP_EFUSE_1V8	SoC: VPPs => No connects
Compliant, USB 2.0 data eye	Discrete LDO VDA_USB_3V3	SoC: VDDA_3P3_USB => filtered VDD_IO_3V3
Compliant, High-Speed SD Card	Discrete LDO VDD_SD_DV	SoC: VDDSHV5 => VDD_IO_3V3 or VDD_IO_1V8
DDR Retention low power mode	Discrete LDO VDD1_DDR_1V8	LPDDR4: VDD1 => VDD_IO_1V8
MCU GPIO Retention low power mode	Discrete LDO VDD_MCU_GPIORET_0V8	Isolated MCU & Main PDN Schemes: SoC: VDD_MCU_WAKE1 => VDD_MCU_0V85 Grouped MCU & Main PDN Schemes: SoC: VDD_MCU_WAKE1 => VDD_CORE_0V8
	Discrete LDSW VDD_MCU_GPIORET_3V3	Isolated MCU & Main PDN Schemes: SoC: VDDSHV0_MCU => VDD_MCUIO_3V3 or VDD_MCUIO_1V8 Grouped MCU & Main PDN Schemes: SoC: VDDSHV0_MCU => VDD_IO_3V3 or VDD_IO_1V8
	Discrete SVS	PMIC: GPIO_10 pulled-up to VCCA_3V3
Main GPIO Retention low power mode	Discrete LDO VDD_GPIORET_0V8	SoC: VDD_WAKE0 => VDD_CORE_0V8
	Discrete LDSW VDD_GPIORET_3V3	SoC: VDDSHV2 => VDD_IO_3V3 or VDD_IO_1V8
	Discrete SVS	PMIC: GPIO_10 pulled-up to VCCA_3V3

SoC Input Supply to Power Rail Groupings vs PDN Low Power Mode Features

PDN Features	Isolated MCU & Main PDN Power Rails							
	VDD_MCU_0V85	VDD_CORE_0V8	VDD_MCUIO_3V3	VDD_IO_1V8	VDD_IO_3V3	VDD1_DDR_1V8	VDD_GPIORET_0v8	VDD_GPIORET_3V3
Standard Operation & MCU Only	vdd_mcu vddar_mcu vdd_mcu_wake1	vdd_core vdd_wake0	vddshv0_mcu vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0 vddshv2			
DDR Retention	vdd_mcu vddar_mcu vdd_mcu_wake1	vdd_core vdd_wake0	vddshv0_mcu vddshv2_mcu	vdds_mmc0	vddshv0 vddshv2	DDR: vdd1		
GPIO Retention-MCU & Main	vdd_mcu vddar_mcu	vdd_core	vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0		vdd_mcu_wake1 vdd_wake0	vddshv0_mcu vddshv2
GPIO Retention-MCU	vdd_mcu vddar_mcu	vdd_core vdd_wake0	vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0 vddshv2		vdd_mcu_wake1	vddshv0_mcu
GPIO Retention-Main	vdd_mcu vddar_mcu vdd_mcu_wake1	vdd_core	vddshv0_mcu vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0		vdd_wake0	vddshv2

Notes:
1) Power rail names shown in "ALL CAPITAL LETTERS"
2) SoC input supplies shown in "all lower case letters"

J784S4 EVM Leo + 2x High-Current Pwr Stages(HCPS) PDN-3M

(All SoC PN variants: TDA4AP/VP/AH/VH)

(Power Rail & GPIO Mapping Overview)

Legend:

Power Rails <Pwr Rail Name>
PDN base
MCU Only/Safety Island
GPIO Retention
DDR_Retention (aka S2R)
End Product option
Peripheral loads (SW config'd after boot)

Control Signals: < Signals >
General cntrl & logic
(Italic = SW config'd after boot)
PDN base cntrl
Func Safety
MCU Only/Island
GPIO Retention
DDR_Retention (aka S2R)
End Product option
Peripheral comps
Debug/Development option

Note items
On-Chip "Pwr OK" Monitors (OV & UV)
On-Chip "Pwr OK" Monitors (UV only)
Provisioned In-Line Supply Filter
High-lighted diagram changes

Leo PMIC-A, PN TPS6594133ARWERQ1 (TI PN ID = 1, MP Buck Rails = 3, PG2.0 NVM ID = 3A Rev 5)
HCPS-A & B, Tulip PN TPS62873Y1QWRXSRQ1 (15A PN ID = 3, Jacinto7 Family ID = Y1)
Safety Voltage Supervisor, PN TPS389006004RTERQ1 (OTP ID = 004 = new common PN for use with Jacinto7 J784S4 PDN-3A scheme)

Features Supported (EVM Max Features):

1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
2. Functional Safety: ASIL-D capable sys w/ Grouped Main & MCU power rails
3. 4x SDRAMs: 32Gb, 4-Die, 32b, 4266MTs, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or Hyperflash & eMMC, UFS
5. Signaling Levels: MCU & Main Dual VIO
6. Low power modes:

V0.27 10/31/2024
1. Updated discrete buck's ENABLE input connections to more accurately show the 20k resistor located in-line to voltage translator output.
2. Updated Note 9, example #2 text & diag to show 20k resistor in-line with buck's ENABLE inputs.

V0.29 1/27/2025
1. Fixed power rail connections to OSPI memories by correctly changing name from VDD_MCUIO_1V8 to VDD_IO_1V8 for Grouped PDN scheme.

V0.32 5/15/2025, 5/22/2025
1. Added "Red Dashed Box" to high-light PMIC resources that are no longer needed and could be reassigned by system SW after boot-up.
2. Updated SVS-A & B to capture OV/UV threshold values per PN "004" default settings. Customers can adjust thresholds via I2C after boot as desired.

SW option to reassign PMIC resource after boot

PDN-3M vs -3A Change List Summary:

1. Remove VDD_MCU_0V85 power rail then connect SoC input supply:
   a. VDD_MCU to VDD_CORE_0V8 power rail
   b. VDDAR_MCU to VDD_RAM_0V85 power rail
2. Remove VDA_MCU_1V8 power rail and connect VDA_PLL_1V8 power rail to MCU analog input supplies instead.
3. Remove discrete LDO-A (previously sourced VDA_PLL_1V8) and use PMIC's LDO4 to source VDA_PLL_1V8 instead.
4. Remove VDD_MCUIO_1V8 power rail and connect SoC's vddshv1_mcu to VDD_IO_1V8 power rail instead.
5. Remove discrete LDO-B (previously sourced VDD_MCUIO_1V8) and use PMIC's LDO1 to source VDA_PHY_1V8 instead.
6. Remove VDD_MCUIO_3V3 power rail and connect SoC's vddshv2_mcu to VDD_IO_3V3 power rail instead.
7. If waking from both MCU & Main domain IOs in GPIO RET low pwr mode is desired, then connect
   a. VDD_GPIORET_WK_0V8 rail to SoC's vdd_wake0. If not, then leave VDD_CORE_0V8 connected.
   b. VDD_GPIORET_IO_3V3 rail to SoC's vddshv2. If not, then leave VDD_IO_3V3 connected.
8. Remove GPIO Ret power & VMON components (dscrt LDO-C, LDSW-B, SVS-B) then connect SoC input supply:
   a. VDD_MCU_WAKE1 to VDD_CORE_0V8 power rail (same rail as vdd_mcu)
   b. VDDSHV0_MCU to VDD_IO_3V3 power rail
   c. PMIC_WAKE1n & PMIC_WAKEn0 become No connects
9. Remove DDR Ret power component (dscrt LDO-D) then connect LPDDR input supply:
   a. VDD1 to VDD_IO_1V8 power rail
   b. Pull DDR_RETx inputs to Gnd with pull-down Rs
10. Remove compliant high-speed SD Card power component (dscrt LDO-E) then connect SoC input supply:
   a. VDDSHV5 to VDD_IO_3V3 power rail
11. Remove compliant USB 2.0 data eye power component (dscrt LDO-F) then connect analog filter input supplying SoC input:
   a. VDDA_3P3_USB to VDD_IO_3V3 power rail
12. Remove high-security Efuse programming power component (dscrt LDO-G) then leave SoC input supply:
   a. VPP_CORE & VPP_CPU become No Connects

Notes:

1) Functional Safety requires monitoring all "safety critical" power rails (i.e. VSYS_3V3 input, key SoC supplies) that could cause severe system failures. ASIL classification depends on the end product use case & what SoC resources a customer is using that are considered to be safety-related. SoC has internal OV & UV monitoring for key SoC MCU & Main voltage domains. The status is reported by SoC's Power OK (POK) status bits. Optional SoC voltage monitoring inputs (i.e. VMONx_IR_VEXTxxx) can be used to extend SoC's OV/UV monitoring to a few board level power rails if desired (i.e. load switch Vo = VDD_IO_3V3). The following SoC Main & SDRAM domains are classified as non-critical & do not require direct monitoring: VDDSHV5 (SD Card), VPP_CORE, VPP_MCU, VDDA_3P3_USB & VDD1_LPDDR4_1V8.

2) Load Switches (LdSw) have been used to create VDD_MCUIO_3V3, VDD_GPIORET_3V3 & VDD_IO_3V3 power rails from VCCA_3V3 to provide the following benefits:
   A) Correct SoC power supply sequencing by using PMIC resources (GPIO signals & power resource outputs) with desired start-up & shut-down timing delays per NVM settings.
   B) PMIC monitoring of "VCCA Over Voltage" (+5 to +10%) allows PMIC to disconnect 3.3V power rails from SoC if OV condition is detected.
   C) Enables low power modes (MCU Only, GPIO_RET & DDR_RET) since the different 3.3V power rails must be disabled independently for different low power modes.
   D) Connecting VCCA_3V3 directly to SoC 3.3V input supplies is ONLY recommended if low power modes are used and a full SoC power up seq is executed any time the VCCA_3V3/VSYS_3V3 is energized since partial powering of the SoC for extended time could negatively impact POH reliability.

3.1) PMIC NVM Rev 1 assigned multiple interface signals to GPIO8 with default NVM setting of GPIO_8 = DISABLE _WDOG function and required interface buffer circuitry, see PROC141E4_SCH for details.
   A) DISABLE_WDOG (NVM setting): PMIC latches logic level at GPIO8 pin on rising edge of PMIC's nRSTOUT = H_MCU_PORz_1V8 at end of power-up seq.
      a) High level at GPIO8 pin (SW-1/Jmpr-1 = closed) directs PMIC to disable Watch-Dog Timer (by setting WD_PWRHOLD bit to disable timer's long-window time-out) for development/debug.
      b) Low level at GPIO8 pin (SW-1/Jmpr-1 = open due to PMIC default internal pull-down R) enables Watch-Dog Timer (default setting enables timer's long-window time-out).
   B) After system SW boots, SW needs to reassign GPIO_8 = GPI function to operate with PDN's MAIN_PWRGRP_IRQ/_IRQn (asserted high or low) signal to allow PMIC to take action if a fault occurs.

3.2) PMIC NVM Rev2 & 3 changes are listed below. There are EVM board SCH/BOM impacts, see J784S4_EVM_..._PDN-3A v0.19 for details.
   1. PMIC VCCA input voltage level auto-detection that enables 1x PMIC PN to support PDNs using either 5V or 3.3V.
   2. PMIC internal Watchdog Timer is disabled at start-up. This allows GPIO8 function to be used as a PMIC internal configuration control. MCU SW will need to start watchdog timer as part of enabling full FuSa features.
   3. GPIO8 logic level selects the PDN type/scheme by latching level before the 3ms time step during power up sequence & directs PMIC to configure internal resources as follows:
      Low = Isolated PDN type directs PMIC to create MCU & SOC power groups; Enables BUCK5 per power up seq (Removes MCU SW write requirement needed in NVM Rev1 above.)
      High = Grouped PDN type directs PMIC create only MCU power group; Removes BUCK5 from pwr up seq (Allow SW to reassign Buck5 for peripheral devices that can be enabled after boot)

3.3) PMIC NVM Rev 4 has been optimized for end product production flow by enabling Watch Dog Timer to support FuSa by default, see J784S4_EVM_..._PDN-3A v0.20 & up & PROC141E5_SCH for details. GPIO9 has been used to support multiple interface signals as listed below.
   A) DISABLE_WDOG (optional): PMIC latches logic level at GPIO9 pin at transition from standby to active start-up sequence.
      a) High level at GPIO9 pin (SW-1/Jmpr-1 = closed) directs PMIC to disable Watch-Dog Timer (by setting WD_PWRHOLD bit to disable timer's long-window time-out).
      b) Low level at GPIO9 pin (SW-1/Jmpr-1 = open due to PMIC default internal pull-down R) enables Watch-Dog Timer (default setting enables timer's long-window time-out).
   B) EN_3V3_VIO (required): After PMIC NVM initialization, GPIO9 = GPO function to provide enable & disable control of load switch supplying VDD_IO_3V3 power rail.
      a) Disabling the WDOG timer is for development & debug tasks. Applying a pull-up R to disable WDOG timer will result in early enabling of discrete LDSW-A (VDD_IO_3V3), LD0-E (VDD_SD_DV) & LDO-F (VDA_USB_3V3). All of these supplies are 3.3V level and are part of the 1st group of supplies to be energized at the start of a power up seq. SoC will not be negatively impacted if these 3.3V supplies are enabled ahead of remaining 3.3V supplies sourced from PMIC and before the rest of SoC supplies begin a normal power up seq during temporary development & debugging activities.

4) GPIO Retention (aka GPIO_RET, IO_RET, IO Wake) low power mode requires:
   A) SoC SW executes command sequence that sets key PMIC register bits in order to enter GPIO_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
   B) After entering GPIO_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
      1. VDD_GPIORET_WK_0V8 supplying MCU's VDD_MCU_WAKE1 for MCU's 0.8V wake-up logic
      2. VDD_GPIORET_IO_3V3 supplying MCU's VDDSHV0_MCU for MCU's 3.3V IO toggle activity
   C) PDN system exits GPIO_RET state upon receiving logic toggles on SoC's MCU monitored IO signals ref to VDDSHV0_MCU supply. Then H_MCU_WAKE1n (= SoC's Open-Drain PMIC_WAKE1n, active low) signal connected to PMIC, GPIO_4 (= WKUP1 default function for Full Active or = WKUP2 for MCU Only destination state) is asserted and PMIC state machine transitions PDN system to desired targeted wake up state.
   D) The Open-Drain Buffer SN74LVC1G07DRLI (tri-states IO when power is OFF) connects PMIC_WAKE1n to SOC_PWR_WKn net at discrete open-drain FET node. It is needed to isolate the SoC output buffer from the always on VCCA_3V3 used as pull-up supply to prevent current bleeding into SoC during low power modes (MCU Only, DDR_RET) when VDD_GPIORET_3V3 is typically disabled.

5) DDR Retention (aka DDR_RET, Suspend-to-RAM, S2R) low power mode requires:
   A) PMIC PN to assign GPIO_6 = Regulator Enable (REGEN) function with an open-drain output buffer type per NVM default settings. The board level net H_DDR_RET_1V1 signal is pulled up to VDD_DDR_1V1 & connected to SoC's DDR_RET input. When this input is set high, SoC's EMIF IO buffers are set to high-Z state as part of entering DDR_RET mode.
   B) SoC SW executes command sequence that sets key PMIC register bits in order to enter DDR_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
   C) After entering DDR_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
      1. VDD_DDR_1V1 supplying both SoC EMIF & SDRAM IO voltages
      2. VDD1_DDR_1V8 supplying SDRAM only
   D) PDN system exits DDR_RET upon detecting a CAN_WAKE signal edge toggle on PMIC's GPIO_4 = LP_WKUP1 function per NVM settings that initiates exiting DDR_RET mode & restores Full Active processor operations.

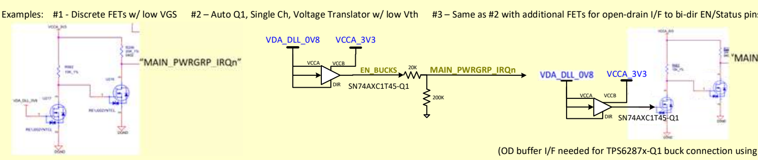
6) SoC devices come in two types: General Purpose (GP) & High Security (HS). All GP devices can leave the VPP domains unconnected per DM. Pre-programmed HS devices can also leave VPP domains unconnected if no additional EFUSE programming is needed. If customer desires capability for in-the-field updates, then on-board EFUSE programming will require an additional 1.8V, 150mA LDO. When disabled, this LDO's Vo will need a high impedance output. Recommended PNs: TPS73101-EP, fixed 1.8V TPS73118-Q1 or TLV70018-Q1. The EN_EFUSE_VPP control signal must be sourced from an SoC GPIO for this PDN (due to limited number of PMIC GPIOs). This allows SoC SW to control Efuse VPP voltage level by enabling & disabling dedicated LDO as needed to program High Security SoC Efuses (see SoC DM for details).

7) PDN shows SoC's VDA_3P3_USB domain supplied from a low noise LDO with a VSYS_5V input as preferred for optimal USB 2.0 data eye mask performance. If USB 2.0 I/F is not used or is only needed for development tasks, then the digital VDD_IO_3V3 rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_3V3 rail to support USB 2.0 I/F removes a discrete LDO & VSYS_5V input but could negatively impact data eye performance due to higher supply noise causing data eye mask violations.

8) PDN shows SoC's Main domain's VDDSHV5 supply being sourced from a dual voltage LDO with a VSYS_5V input as preferred for compliant high-speed SD card operation. If SD card is not used or only standard data rate operation is sufficient, then the digital VDD_IO_3V3 rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_3V3 rail to support SD Card operation removes dual voltage, discrete LDO & VSYS_5V input but will restrict data rates to standard 12Mb/s with VIO = 3.3V.

9) A low voltage translator with a VGS or VIH max spec less than 0.76V (-5% supply tol on 0.8V) is needed to ensure a 3.3V logic high level output. 3x different examples are shown below:
   #1 A discrete FET voltage translator with low VGS threshold below an input min 0.76V. EVM PROC141E2/E3_SCHs use discrete FET PN w/ low VGS but only industrial temp grade.
   #2 A single channel, voltage translator (SN74AXC1T45-Q1) that is automotive AEC-Q100 qualified, grade1 for -40 to +125C operation could be used as an alternative. Ensure valid logic levels are provided at both GPIO8 (as desc above) & discrete Buck's EN input pin (snap-shot shows Buck's internal bi-dir EN/STATUS circuitry).
      A.) The PMIC's GPIO8 has NVM default setting that enables a 400k internal pull-down. This should be sufficient to keep GPIO8 net from "floating" above GPIO's VIH min level when VDA_DLL_0V8 is disabled which causes the SN74AXC1T45-Q1 output to be tri-stated.
      B.) Customer may want to add a pull-down R on the board (showing a 200k below) just in case the PMIC's internal pull-down is not strong enough to ensure a low logic level.
   #3 A non-inverting FET stage (Ex 3, shown below) could be added to shunt the "MAIN_PWRGRP_IRQn" net to Gnd if items 2A or 2B are not sufficient.

Examples: #1 - Discrete FETs w/ low VGS   #2 – Auto Q1, Single Ch, Voltage Translator w/ low Vth   #3 – Same as #2 with additional FETs for open-drain I/F to bi-dir EN/Status pins



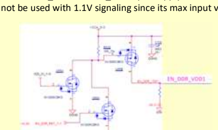
(OD buffer I/F needed for TPS6287x-Q1 buck connection using AEC-100 Translator)

10) Worst case analysis for very high thermal use cases could result in VCCA_3V3 load current in 15-18A range. This large load current range could lead to a 60 – 72mV voltage drop across Safety FET (Recm'd PN: NVMFS4C05N) for a max RDSon = 4mohm. The TPS22965-Q1 load switches have max RDSon = 27mohm with 4A max rating resulting in additional max drop of 108mV. SoC's 3.3V supply tolerance is +/-5% or 165mV. Total RDSon drops across Safety FET & Load Switches range from 168 – 180mV which exceed SoC's min voltage limit. For this reason, the Tulip buck input voltage will be moved from VCCA_3V3 to VSYS_3V3 since VDD_CPU_AVS & VDD_CORE_0V8 rails account for more than 70% of VCCA_3V3 worst case load currents.

11) If GPIO Retention low power mode is desired, then connect all SVS-B VMON inputs to existing MCU supplies (as shown) sourced from PMIC to enable 1x common PN for SVS-A & -B while avoiding false positives on "unconnected" VMONs. If an end product does not need GPIO Retention low power mode, then the 3x following components can be removed from the PDN: LDO-C, LDSW-B & SVS-B. Group the SoC input supplies according to he "PDN Features for Isolated Power Rails" table shown below using the "Standard Operation & MCU Only" assignments row.

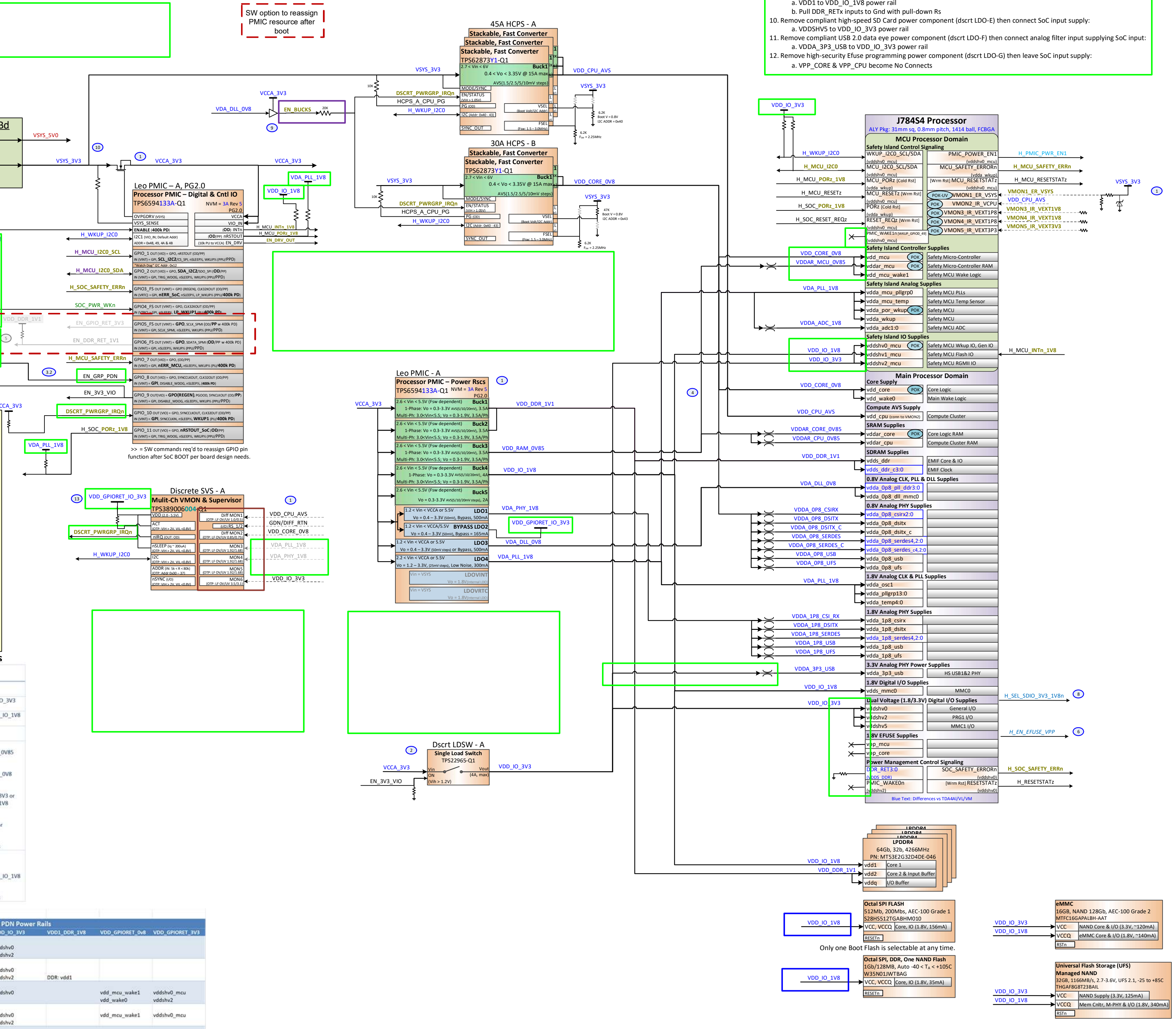
12) The OR gate function enabling the discrete LDO supplying 1.8V to LPDDR4 VDD1 (Internal bias voltage) needs to revert back to original discrete FET OR gate circuitry (see PROC141E2_SCH or snap-shot below). Reason for reverting is due to the OR gate needing a max input voltage threshold less than 1.05V (-5% of 1.1V) since the EN_DDR_RET_1V1 signal is sourced from an open-drain PMIC GPIO with PU resistor to VDD_DDR_1V1 supply with +/-5% supply tolerance. In addition, the OR gate needs to remain energized during DDR Retention low power mode when only VDD_DDR_1V1 & VDD1_DDR_1V8 rails remain energized. Therefore, the OR gate supply must use VSYS_3V3 or VCCA_3V3 input supply that remains on in DDR Ret mode. The single logic gate IC (SN74LVC1G97-Q1) used for enabling other power resources interfaced to 3.3V signaling levels can not be used with 1.1V signaling since its max input voltage threshold for 3.3V supply is ~2.2V.

Original discrete FET OR gate circuit used in PROC141E2_SCH:

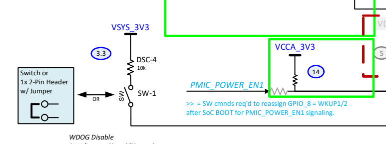


13) The Safety Voltage Supervisor (SVS-A & SVS-B) supply connections need to be changed from "Always ON" VCCA_3V3 (=VSYS_3V3) to a "PMIC controlled" power rail to enable resetting of an asserted IRQn signal by power cycling SVS devices. During functional testing, it was discovered that an SVS's asserted IRQn could not be reset if MCU processor I2C comm with SVS devices is lost. This will happen if a MCU Power Error occurs (i.e. fault on a MCU supply) since this will cause the PMIC PFSM to transition the system to the desired Safe Recovery state (powers down all SoC supplies). However, if the SoC PDN's input voltage (VSYS_3V3) remains energized, then the energized SVS devices will maintain an asserted IRQn and the system will not be able to execute a SoC cold boot attempt due a previously asserted IRQn will cause the PMIC to abort an SoC power up sequence attempt. A SVS device power cycle will reset an asserted IRQn signal, enabling the desired SoC cold boot attempt. By replacing "Always ON" VCCA_3V3 supply connections with a PMIC controlled power rail (VDD_MCUIO_3V3), the SVS devices will have a power cycle event upon entering the Safe Recovery state (per table below). If a fault occurs on a Main domain supply, the PMIC will transition the system to MCU Only state which allows I2C comm to evaluate & potentially log the fault source. The MCU can use I2C comm to clear an asserted IRQn if a system cold boot attempt is desired to
try restarting into the Full Active state since a fault might clear if it's due to a random noise event or temperature dependent. The SVS device's "ACTive" input connection will need to be connected to VDD since the new VDD_MCUIO_3V3 supply connection is enabled as part of the SoC power up seq.. This avoids driving a high logic signal into an unenergized device.

PDN State:	Active	MCU Only	Safe Recovery
	Main supplies = ON	Main supplies = OFF	Main supplies = OFF
	MCU supplies = ON	MCU supplies = ON	MCU supplies = OFF
	SVS-A = ON	SVS-A = ON	SVS-A = OFF
	SVS-B = ON	SVS-B = ON	SVS-B = OFF



Switch or 1x 2-Pin Header w/ Jumper
OR
SW-1
DSC-4 10k
WDOG Disable SW1/Jmpr = Closed/Shorted
PMIC_POWER_EN1
>> = SW cmnds req'd to reassign GPIO_8 = WKUP1/2 after SoC BOOT for PMIC_POWER_EN1 signaling.



14) PMIC 133A Rev 2 & higher supports "PDN Configuration Control" operation as follows:
During the first ~3ms of the SoC power up seq, before the VDA_DLL_0V8 rail is energized and enables CPU & CORE discrete bucks, the MAIN_PWRGRP_IRQn net must be held below PMIC's input VIL max to ensure PMIC will latch a low logic level. This directs PMIC's boot-time configuration to support "Isolated MCU & Main" PDN-3A thru -3F schemes by:
a) Creating 2x "MCU & SoC Power Groups" internal to PMIC for proper FuSa response by PFSM actions whenever any faults within either the MCU &/or Main (aka SOC) power rails
b) Including Buck5 to be energized during power up seq).

For "Grouped MCU & Main" PDN-3G thru -3M schemes, a pull-up resistor to VCCA_3V3 is connected to GPIO_8 to ensure a high logic level is latched by PMIC. This directs PMIC's boot-time configuration to support Grouped MCU & Main PDN schemes by:
a) Creating 1x "MCU Power Group" internal to PMIC for proper FuSa response by PFSM actions whenever any faults within either the grouped MCU & Main power rails
b) Excluding Buck5 from being energized during power up seq so that it can either be left unused without any board components or enabled by SW after boot for peripheral loads.

The Safety Voltage Supervisors (SVS-A & -B) IRQn pins, PMIC's GPIO_10 and all discrete power resources all connect to a new net "DSCRT_PWRGRP_IRQn" that gives FuSa coverage for all power rails sourced from discrete power resources. The PMIC continues to treat GPIO_10 input as "MCU_PWRGRP_IRQn" (legacy net name from PDN-3A scheme) which is the 1x PMIC internal power group for Grouped PDN schemes. The internal "MCU_PWR_GRP" will now comprehend both PMIC internal power resources & external discrete power resources. A fault on any of these resources will cause PMIC to shutdown all supplies as desired per FuSa requirements.

Modular PDNs support Flexible Feature Set Reductions

Feature Removals	Power Resource & Power Rail Removals	New Supply Mappings
HS SoC EFUSE Programming	Discrete LDO VPP_EFUSE_1V8	SoC: VPPs => No connects
Compliant, USB 2.0 data eye	Discrete LDO VDA_USB_3V3	SoC: VDDA_3P3_USB => filtered VDD_IO_3V3
Compliant, High-Speed SD Card	Discrete LDO VDD_SD_DV	SoC: VDDSHV5 => VDD_IO_3V3 or VDD_IO_1V8
DDR Retention low power mode	Discrete LDO VDD1_DDR_1V8	LPDDR4: VDD1 => VDD_IO_1V8
MCU GPIO Retention low power mode	Discrete LDO VDD_MCU_GPIORET_0V8	Isolated MCU & Main PDN Schemes: SoC: VDD_MCU_WAKE1 => VDD_MCU_0V85 Grouped MCU & Main PDN Schemes: SoC: VDD_MCU_WAKE1 => VDD_CORE_0V8
	Discrete LDSW VDD_MCU_GPIORET_3V3	Isolated MCU & Main PDN Schemes: SoC: VDDSHV0_MCU => VDD_MCUIO_3V3 or VDD_MCUIO_1V8 Grouped MCU & Main PDN Schemes: SoC: VDDSHV0_MCU => VDD_IO_3V3 or VDD_IO_1V8
	Discrete SVS	PMIC: GPIO_10 pulled-up to VCCA_3V3
Main GPIO Retention low power mode	Discrete LDO VDD_GPIORET_0V8	SoC: VDD_WAKE0 => VDD_CORE_0V8
	Discrete LDSW VDD_GPIORET_3V3	SoC: VDDSHV2 => VDD_IO_3V3 or VDD_IO_1V8
	Discrete SVS	PMIC: GPIO_10 pulled-up to VCCA_3V3

SoC Input Supply to Power Rail Groupings vs PDN Low Power Mode Features

PDN Features	Isolated MCU & Main PDN Power Rails							
	VDD_MCU_0V85	VDD_CORE_0V8	VDD_MCUIO_3V3	VDD_IO_1V8	VDD_IO_3V3	VDD1_DDR_1V8	VDD_GPIORET_0v8	VDD_GPIORET_3V3
Standard Operation & MCU Only	vdd_mcu vddar_mcu vdd_mcu_wake1	vdd_core vdd_wake0	vddshv0_mcu vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0 vddshv2			
DDR Retention	vdd_mcu vddar_mcu vdd_mcu_wake1	vdd_core vdd_wake0	vddshv0_mcu vddshv2_mcu	vdds_mmc0	vddshv0 vddshv2	DDR: vdd1		
GPIO Retention-MCU & Main	vdd_mcu vddar_mcu	vdd_core	vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0		vdd_mcu_wake1 vdd_wake0	vddshv0_mcu vddshv2
GPIO Retention-MCU	vdd_mcu vddar_mcu	vdd_core vdd_wake0	vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0 vddshv2		vdd_mcu_wake1	vddshv0_mcu
GPIO Retention-Main	vdd_mcu vddar_mcu vdd_mcu_wake1	vdd_core	vddshv0_mcu vddshv2_mcu	vdds_mmc0 DDR: vdd1	vddshv0		vdd_wake0	vddshv2

Notes:
1) Power rail names shown in "ALL CAPITAL LETTERS"
2) SoC input supplies shown in "all lower case letters"

TPS6594133A NVM | Revision History

Revision	Release Date	Comments
0.0	April 25, 2022	
1.0	August 8, 2022	
2.0	October 10, 2022	TI J784S4 EVM Samples
3.0	December 15, 2022	RTM'd in January 2023
4.0	Only released in sample units	
5.0	March 1, 2024	PCN released and all parts received after March 1st , 2024 contain Rev 5

Rev	Change	Impact of Change
1.0	GPIO Retention Entry/Exit Handling – If Wake signal triggers while being armed, PMIC will enter Retention and then immediately exit.	Prevents PMIC from getting stuck in Retention
	Power Down Sequence Timing Changes -Updated power down seq of VDA_DLL_0V8 to shift disabling from 2.5ms to 1.0ms due to ~1ms delay in VDA_DLL_0V8 RC discharge before VDD_CPU_AVS & VDD_CORE_0V8 are disabled by VDA_DLL_0V8 dropping below 0.6V FET Von threshold. -Updated power down seq of VDD_MCU_0V85 to shift disabling from 2.5ms to 2.0ms to ~align with disabling of VDD_CPU_AVS & VDD_CORE_0V8.	Overall sequence time remains the same. Better power down seq when using discrete component rails to align with J7 SoC DM recommended seq.
	At startup, all PMIC power resources/rails mapped to a single MCU_PWR_ERR group	• Enables 1x PMIC PN to support both Grouped & Isolated PDN board designs • Grouped MCU & Main PDNs (3G to 3M) need 1x PMIC power group to enable fault on any monitored rail to cause an orderly shutdown. • Isolated MCU & Main PDNs (3A to 3F) will need MCU SW to create 2x power groups (MCU & Main) by writing 0x1E to PMIC register 0x44

Rev	Change	Impact of Change
2.0	VCCA input voltage level auto-detection	Enables 1x PMIC PN to support PDNs with VCCA voltage of 5V or 3.3V
	Watchdog Timer disabled	• GPIO8 used for PMIC config control • MCU SW will need to start watchdog timer as part of enabling full FuSa features
	GPIO8 logic level latched before 3ms time step of power up sequence & directs PMIC to configure internal resources: • Low = Creates 2x power groups; Enables BUCK5 per power up seq • High = Creates 1x power group; Removes BUCK5 from power up seq	• Isolated MCU & Main PDNs (3A to 3F) need 2x power groups, use Buck5 for VDD_MCU_0V85 rail & connect MAIN_PWRGRP_IRQn to GPIO8 for discrete power resource monitoring. • Grouped MCU & Main PDNs (3G to 3M) need 1x power group, removes Buck5 from pwr up seq (Buck5 can be reassigned by SW config to supply a peripheral rail after SoC & SW boot-up) & connects GPIO8 to pull-up resistor to set logic high.

Rev	Change	Impact of Change
2.0	Removed any2ota sequence	PMIC OTA preparation sequence is no longer available. Unused during normal operation.
	Fixed GPIO10 response during normal operation	Prevents PMIC from getting stuck after MCU_PWRGRP_IRQn triggers a recovery attempt
3.0	Adjusted internal setting for improved BUCK reliability	No impact to function

Rev	Change	Impact of Change
4.0	Watchdog enabled by default with 1 sec long window	MCU SW must boot and configure watchdog within 1 second of nRSTOUT going high
	Change default GPIO9 function from GPIO to WD_DISABLE	GPIO9 starts as an input to set WD_PWRHOLD bit, then changes to an output. **In Development:** Customer has *option* to use external PU resistor to set WD_PWRHOLD =1 **In End Equipment:** No impact to function
	TO_ACTIVE sequence has 500us delay between LDO3 and BUCK5	In systems with split power groups, PMIC BUCK5 powers up fully before PMIC LDO3. Overall sequence time remains the same.
	LDO2 OV/UV Threshold changed from 5% to 10%	When used as 3.3V load switch, PG Window will match that of VCCA. Customer can tighten after boot.

*Error found EN_I2C_CRC sequence, only on Rev4

Rev 4 I2C_CRC_EN Error and Workaround

- **What**: Setting I2C_2 FSM Trigger high to enable the I2C CRC does not work on Rev 4 of TPS6594133A
- **Why:** Implementation of changes for watchdog and GPIO9 for disable watchdog pushed NVM over the memory limit
- **Affected Revisions:** Only Rev 4 is impacted. This was fixed in Rev 5
- **Software Workaround:** Instead of using the I2C_2 FSM trigger, please use SW workaround described on next page

NVM Rev 4 Summary of Changes

Item	Change	Impact
1	Watchdog enabled by default with 1 sec long window	MCU SW must boot and configure watchdog within 1 sec of nRSTOUT (SoC's MCU_PORz) going high
2	Change GPIO9's default NVM function from GPI to WD_DISABLE	GPIO9 starts as an input to set WD_PWRHOLD bit, then changes to an output. **In Development/Debug:** Customer has *option* to use external PU resistor to disable WD Timer by setting WD_PWRHOLD =1 **In End Equipment:** WD Timer enabled by default
3	TO_ACTIVE sequence adds 500us delay to LDO3 enable	Adds timing margin to ensure BUCK5 (SoC's VDD_MCU_0V85) powers up fully before Tulip buck (SoC's VDD_CORE_0V8) that is enabled by LDO3
4	LDO2 output OV/UV Threshold changed from 5% to 10%	When used as 3.3V load switch, PG Window will match that of VCCA since both are supplied by VSYS_3V3 input voltage from pre-regulator. Customer can tighten after boot.

Rev	Change	Impact of Change
5.0	Watchdog Long Window set to 13 minutes.	MCU SW must boot and configure watchdog within 13 minutes of nRSTOUT going high
	Fixed EN_I2C_CRC sequence error	MCU can use I2C_2 FSM Trigger to enable I2C CRC

J784S4 EVM Leo + 2x High-Current Pwr Stages(HCPS) PDN-3A

Rev	Date	By	Desc
V0.23	10/26/2023	BMc	1. Increase time btw pwr up seq Time Step #2 vs #3 to add 0.5ms margin btw VDD_MCU_0V85 vs VDD_CORE_0V8 for worst case per SoC errata i2406
V0.23b	10/27/2023	BMc	2. Updated PMIC PN NVM revision from v2 to v4
V0.23c	12/06/2023	BMc	3. Added new power up seq constraints list for quick reference as needed to align with Errata i2406 "IO Glitches during Pwr Up Seqs"
v0.29	2/07/2025	BMc	1. Corrected power up seq timing diagram to correctly show time btw pwr up seq Time Step #2 vs #3 as only 0.5ms (instead of 1.0ms).
v0.30	2/19/2025	BMc	1. Corrected diag to show SOC_PWR_EN (PMIC_ENABLE input) signal asserting low 0.1ms (PMIC's internal delay T_{DLY0}) before PMIC's state machine begins executing power down seq by 1st setting MCU_PORz & SOC_PORz low.
v0.31	3/21/2025	BMc	1. Corrected diag to show both VDD_GPIORET_IO_3V3 & VDD_IO_3V3 min enable time could be ~0.1ms after enabling signals (VDD_MCUIO_3V3 & EN_3V3_IO respectfully). 2. An "Immediate Shutdown/Power Down Seq" has recently been approved and will be add to an upcoming data manual version. This simplifies SoC power down to only require both PORz signals to be set low for 1-2us before disabling SoC input supplies in any order.

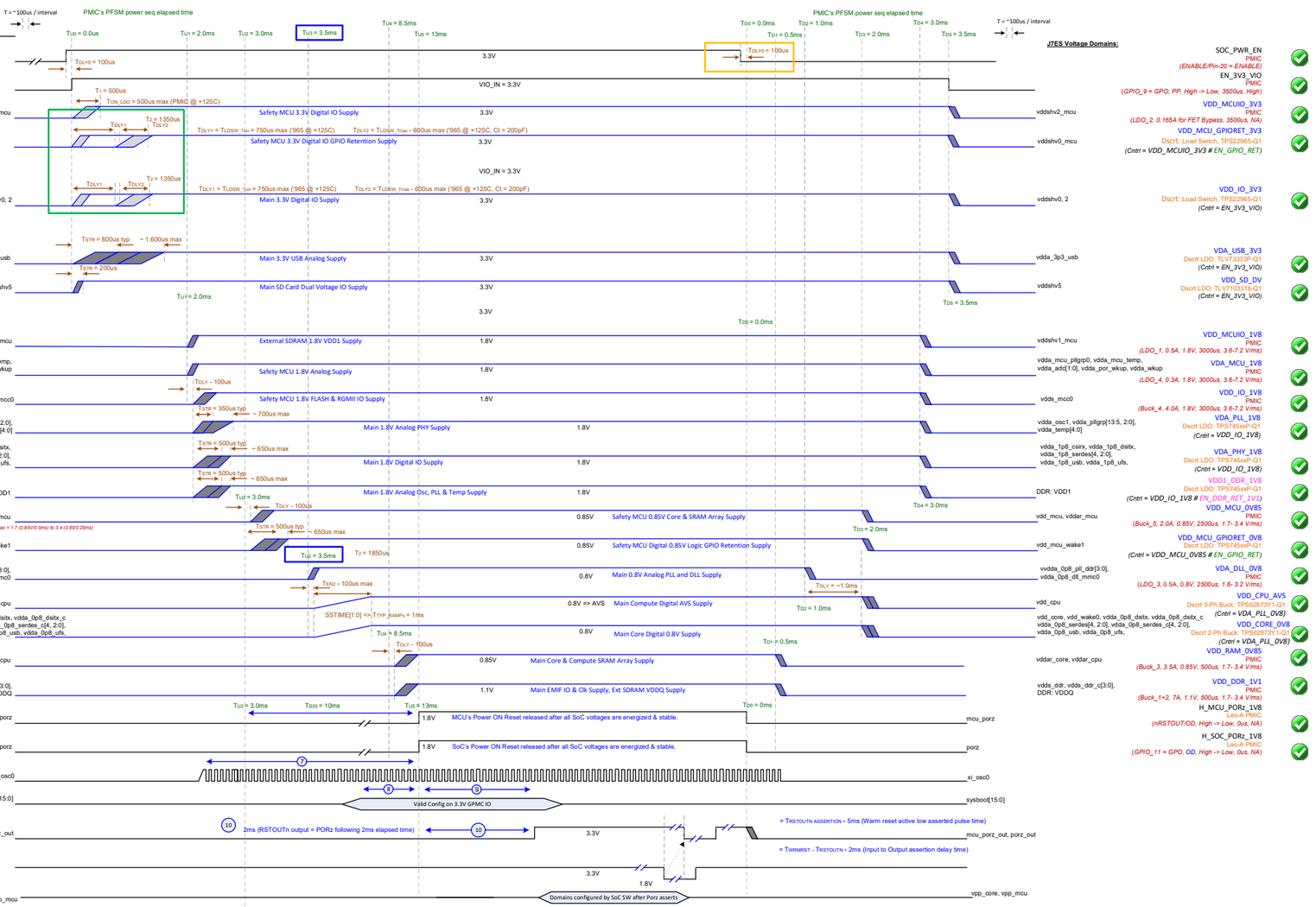
Legend:

System Elapsed Times
Device Timing Parameters
Board Power Rail – Active State / Control Signal Nets / SoC voltage domains
Board Power Rail – GPIO Retention / Control Signal Nets / SoC voltage domains
Board Power Rail – DDR Retention / Control Signal Nets / SoC voltage domains
Discrete Power Component
PMIC Power Component
NVM Settings: (Pwr Rsrc, Current Capacity, Boot Voltage, Delay After Enable [us], Slew Rate [mV/us])
(GPIO# = Function, Ref Voltage, Output Buffer Type, Logic @ T=0, Logic @ Elapsed time [us])
$ Indicates PMIC Control Signal & Power Resource and Board Power Rail counts that transition during power sequences
# = Boolean "OR"logic & = Boolean "AND" logic

Leo PMIC-A, PN TPS659413 3ARWERQ1 (TI PN ID = 1, MP Buck Rails = 3, PG2.0 NVM ID = 3A Rev 4 or higher)
HCPS-A & B, Tulip PN TPS62873Y1QWRXSRQ1 (15A PN ID = 3, Jacinto7 Family ID = Y1)
Safety Voltage Supervisor, PN TPS389006 004RTERQ1 (OTP ID = 004 = new common PN for use with Jacinto7 J784S4 PDN-3A scheme)

Verified per NVM file

PMIC Cntrl Count:	PMIC Pwr Rsc Count:	Power Rail Count:	Board Power & Logic Nets:	SoC Voltage Domains:	NVM Settings, Pwr-Up Seq
1$			SOC_PWR_EN		PMIC *(ENABLE/Pin-20 = ENABLE)*
2$			EN_3V3_VIO		PMIC *(GPIO_9 = GPO, VIO, PP, Low @ T0, High @ 0us)*
	1$	1$	VDD_MCUIO_3V3	vddshv2_mcu	PMIC *(LDO_2, 0.165A for FET Bypass, 0us, NA)*
	2$		VDD_MCU_GPIORET_3V3	vddshv0_mcu	Dscrt: Load Switch, TPS22965-Q1 *(Cntrl = VDD_MCUIO_3V3 # EN_GPIO_RET)*
		3$	VDD_IO_3V3	vddshv0, 2	Dscrt: Load Switch, TPS22965-Q1 *(Cntrl = EN_3V3_VIO)*
	4$		VDA_USB_3V3	vdda_3p3_usb	Dscrt LDO: TLV73333P-Q1 *(Cntrl = EN_3V3_VIO)*
	5$		VDD_SD_DV	vddshv5	Dscrt LDO: TLV7103318-Q1 *(Cntrl = EN_3V3_VIO)*
	2$	6$	VDD_MCUIO_1V8	vddshv1_mcu	PMIC *(LDO_1, 0.5A, 1.8V, 2000us, 3.6-7.2 V/ms)*
	3$	7$	VDA_MCU_1V8	vdda_mcu_pllgrp0, vdda_mcu_temp, vdda_adc[1:0], vdda_por_wkup, vdda_wkup	PMIC *(LDO_4, 0.3A, 1.8V, 2000us, 3.6-7.2 V/ms)*
	4$	8$	VDD_IO_1V8	vdds_mcc0	PMIC *(Buck_4, 4.0A, 1.8V, 2000us, 3.6-7.2 V/ms)*
		9$	VDA_PLL_1V8	vdda_osc1, vdda_pllgrp[13:5, 2:0], vdda_temp[4:0]	Dscrt LDO: TPS745xxP-Q1 *(Cntrl = VDD_IO_1V8)*
		10$	VDA_PHY_1V8	vdda_1p8_csirx, vdda_1p8_dsitx, vdda_1p8_serdes[4, 2:0], vdda_1p8_usb, vdda_1p8_ufs,	Dscrt LDO: TPS745xxP-Q1 *(Cntrl = VDD_IO_1V8)*
		11$	VDD1_DDR_1V8	DDR: VDD1	Dscrt LDO: TPS745xxP-Q1 *(Cntrl = VDD_IO_1V8 # EN_DDR_RET_1V1)*
	5$	12$	VDD_MCU_0V85	vdd_mcu, vddar_mcu	PMIC *(Buck_5, 2.0A, 0.85V, 3000us, 1.7- 3.4 V/ms)* *Slew Rate [V/ms] Min to Max = 1.7 (0.85V/0.5ms) to 3.4 (0.85V/0.25ms)*
		13$	VDD_MCU_GPIORET_0V8	vdd_mcu_wake1	Dscrt LDO: TPS745xxP-Q1 *(Cntrl = VDD_MCU_0V85 # EN_GPIO_RET)*
	6$	14$	VDA_DLL_0V8	vvdda_0p8_pll_ddr[3:0], vdda_0p8_dll_mmc0	PMIC *(LDO_3, 0.5A, 0.8V, 3500us, 1.6- 3.2 V/ms)*
	15$		VDD_CPU_AVS	vdd_cpu	Dscrt 3-Ph Buck: TPS62873Y1-Q1 *(Cntrl = VDA_PLL_0V8)*
		16$	VDD_CORE_0V8	vdd_core, vdd_wake0, vdda_0p8_dsitx, vdda_0p8_dsitx_c vdda_0p8_serdes[4, 2:0], vdda_0p8_usb, vdda_0p8_ufs,	Dscrt 2-Ph Buck: TPS62873Y1-Q1 *(Cntrl = VDA_PLL_0V8)*
	7$	17$	VDD_RAM_0V85	vddar_core, vddar_cpu	PMIC *(Buck_3, 3.5A, 0.85V, 8500us, 1.7- 3.4 V/ms)*
	8+9$	18$	VDD_DDR_1V1	vdds_ddr, vdds_ddr_c[3:0], DDR: VDDQ	PMIC *(Buck_1+2, 7A, 1.1V, 8500us, 1.7- 3.4 V/ms)*
3$			H_MCU_PORz_1V8	mcu_porz	Leo-A PMIC *(nRSTOUT/OD, Low -> High, 12,200us, NA)*
4$			H_SOC_PORz_1V8	porz	Leo-A PMIC *(GPIO_11 = GPO, OD, Low -> High, 12,200us, NA)*
			H_XI_OSC0	xi_osc0	
			H_SYSBOOT[15:0]	sysboot[15:0]	
			H_MCU_PORz_OUT/ H_SOC_PORz_OUT	mcu_porz_out, porz_out	
			H_RSTOUTn (System Warm Reset)		
19 *Not included in Power sequence***			VPP_EFUSE_1V8	vpp_core, vpp_mcu	Dscrt LDO: TLV73518P-Q1 *(Cntrl = H_EN_EFUSE_VPP from* SOC GPIO*)*



1.4.1 Power rails

NOTE: K3W1 devices are intended for use with low-cost PMIC. Depending on system needs, certain supply rails may be ganged. Power sequencing requirements are generally high to low and will follow a recommended sequence implemented by the PMIC.

The architecture will support any power sequence (with exception of array and DDR IO supplies, see exception descriptions below), but validation will be limited to those enforced by PMIC. External voltage supervisors (discrete or on PMIC) must be used to provide POR reset to teh device. On-chip POR circuitry provides redundant supply monitoring (in addition to any PMIC monitoring) for safety applications.

Power sequencing exceptions:

Due to specific analog IP restrictions, several power sequencing restrictions are required as follows.

RAM array supplies (I7es_arch_gap.41):

During active power ramp, the core supply must always lead the corresponding array supply during ramp-up and must lag the corresponding array supply during ramp-down such that VDD* (core) >= VDDAR* (array).

To meet lifetime reliability specs, during any other uncontrolled ramp down, ensure that the array supply (VDDA*) is not actively driven when the corresponding core (VDD*) is <=200mV.

DDR IO supplies (I7es_arch_gap.64):

During active power ramp up, the core supply must ramp to valid level before beginning DDR IO supply ramp (1.1V / 0.6V).

During active power ramp down, the DDR IO supplies (1.1V/0.6V) must ramp down before DDR logic VIL levels before the core supply begins to ramp down below valid level.

J7 SoC Errata Item i2406 | Power Sequence Limitations

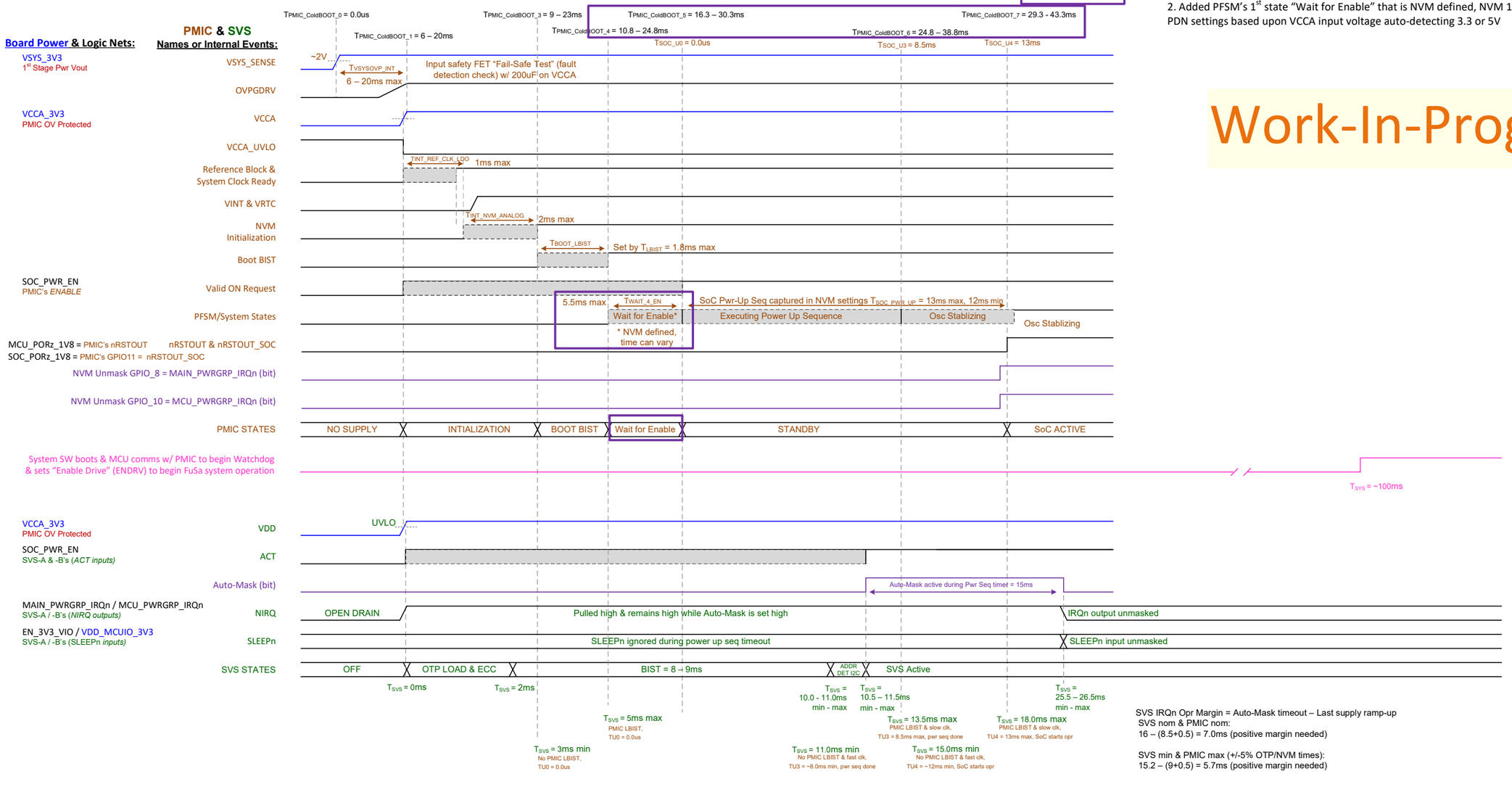
- Errata i2406 summary
  - In order to prevent random IO signal pulses & potential IO drive contention during the power up sequence
- New power-up seq constraints
  1. VDD_CORE must ramp-up before or from same power resource supplying VDD_WAKE0.
  2. VDD_MCU must ramp-up before or from same power resource supplying VDD_MCU_WAKE1.
  3. VDD_MCU should ramped-up based upon the Vnom level and power resource as follows:
     a) Vnom = 0.8V & same 0.8V power resource supplying all 0.8V core level supplies (VDD_CORE, VDD_WAKE0 & VDD_MCU_WAKE1) should ramp VDD_MCU simultaneously with all 0.8V core level supplies.
     b) Vnom = 0.85V & independent 0.85V power resource should ramp VDD_MCU 0.5ms before all 0.8V core level supplies.
  4. VDDAR_CPU or VDDAR_CORE supplies cannot be grouped with 0.85V VDD_MCU since they must ramp-up after VDD_CORE & VDD_CPU supplies.
  5. VDDAR_MCU & VDD_MCU_WAKE1 supply can be grouped with 0.85V VDD_MCU power resource.

Texas Instruments

TPS6594133A PMIC + TPS389006004 SVS Cold Boot-up Timing for PDN-3x

Leo PMIC-A, PN TPS659413**3A**RWERQ1 (TI PN ID = **1**, MP Buck Rails = **2**, PG2.0 NVM ID = **3A** **Rev 5**)
HCPS-A & B, Tulip PN TPS6287**3Y1**QWRXSRQ1 (15A PN ID = **3**, Jacinto7 Family ID = **Y1**)
Safety Voltage Supervisor, PN TPS389006**004**RTERQ1 (OTP ID = **004** = new common PN for use with J7 PDN-3x scheme)

Rev	Date	By	Desc
V0.1	5/21/2022	BMc	Initial capture of PMIC & SVS device initialization sequences vs SoC power up seq & release to active operations.
V0.2	5/24/2022	BMc	Updated SVS operation & added SVS PG set-up time margin calculations to ensure positive margin wrt PMIC's GPIO unmasking for MAIN & MCU_PWRGRP_PG/IRQn signaling at cold power up seq
V0.3	5/31/2022	BMc	Updated following 3rd PMIC & SVS power seq review
v0.4	6/2/2002	BMc	Updated 1. Functional opr of SVS device begins after OTP, BIST & I2C Addr completion (i.e. Pwr Seq timer, LF VMON) 2. Auto-Mask opr to includes masking of IRQn & SLEEPn pins and aligns to 1x Pwr Seq timer reg value
V0.5	6/30/2022	BMc	Increased Auto-Mask elapsed time-out from 5 to 15ms to ensure no false positives
V0.6	8/31/2022	BMc	Added "PMIC_ColdBOOT_#" power up step elapsed time stamps wrt VSYS_3V3 ramping up vs SoC PORz release to begin system SW boot.
V0.27	11/20/2024	BMc	1. Updated PMIC PN NVM revision from v4 to v5 2. Added PFSM's 1st state "Wait for Enable" that is NVM defined, NVM 133A requires 5.5ms max for capturing desired PDN settings based upon VCCA input voltage auto-detecting 3.3 or 5V



Work-In-Progress

SVS IRQn Opr Margin = Auto-Mask timeout – Last supply ramp-up
SVS nom & PMIC nom:
16 – (8.5+0.5) = 7.0ms (positive margin needed)

SVS min & PMIC max (+/-5% OTP/NVM times):
15.2 – (9+0.5) = 5.7ms (positive margin needed)