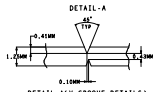
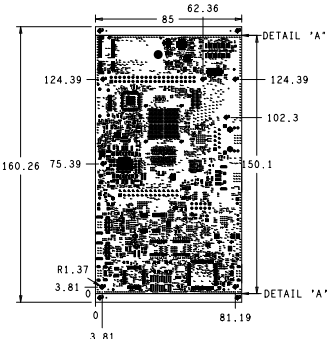


REVISIONS		
REV #	DESCRIPTION	DATE
REV E2		260922
CCN #		



FABRICATION NOTES:

- FABRICATE PCB IN ACCORDANCE WITH IPC-6012, CLASS 2; PER IPC-6011. PCB SHALL BE MANUFACTURED USING ITED 11804 OR EQUIVALENT.
- MATERIALS:**
 - LAMINATE AND PREPREG (8-STAGE) TO BE IN ACCORDANCE WITH IPC-4101/12E, (ENH TO 117).
 - COPPER FOIL TO BE IN ACCORDANCE WITH IPC-4101-180, UNLESS OTHERWISE SPECIFIED. THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC 6012B TABLE NO.3-1 AND 3-4.
- ALL HOLES SHALL BE LOCATED WITHIN 0.10MM DIAMETER OF TRUE POSITION. LAYERS TO LAYER REGISTRATION SHALL BE BETTER 0.250MM.
- ROW AND TRIST SHALL NOT EXCEED MORE THAN 0.175% OF THE DESIGN LENGTH.
- CONDUCTOR WEIGHT SHALL BE LESS THAN 20% FROM ITS ORIGINAL DATA. INCLUDE FOR MATCHING IMPEDANCE MISMATCH. SHALL APPROXIMATE THE MODIFIED WEIGHTS AND SPACING. TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAYERS.
- BOARD FINISHED SHALL BE ACCORDING TO IPC-6012 CLASS 2.
- AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
- FINISH:**
 - ALL UNCOATED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENIG. ELECTROLESS NICKEL/IMMERSION GOLD. ELECTROLESS NICKEL SHALL BE 3-5 MICROM. TYPICAL IMMERSION GOLD THICKNESS SHALL BE 0.04-0.06 MICROMS OF POLYMERIZABLE IMMERSION GOLD SURFACE THICKNESS.
 - APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-60-604, CLASS A, TO BOTH SIDES OF THE BOARD OVER BARE COPPER. THE MASK SHALL BE RECESSED AND COVERED WITH SOLDER MASK. ONLY SOLDER MASK FINISH THAT CAN BE RECESSED THIS SIDE SHALL BE REDUCED IF REQUIRED. ALL OTHER SOLDER MASK FINISHES SHALL BE IN AREA. RESIST COLOUR OF SOLDER MASK SHALL BE BLUE.
 - ENIG/ENMG SHALL BE WHITE. ENMG/ENMG SHALL BE NON-CONDUCTIVE EN. THERE SHALL BE NO SILKSCREEN ON ANY SOLDEABLE COMPONENT PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED IF THE SILK SCREEN FALLS ON SOLDEABLE AREAS.
 - SURFACE AND VTA HOLES FINISH SHALL NOT BE LESS THAN 20UM (0.0008"). THICKNESS OF LASER VTA'S PLATING SHALL NOT BE LESS THAN 10UM (0.0004") AND DRILLED VTA'S SHALL NOT BE LESS THAN 15UM (0.0006").
 - ALL HOLES SURROUNDED BY LAND $\ge 0.101^{\circ}$ SHALL BE COMPLIANT TO IPC6012, CLASS 2.
- MARKING:**
 - BOARD SHALL MEET THE REQUIREMENTS OF UL-796 WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE REPRODUCED IN SILKSCREEN.
- TEST REQUIREMENTS:**
 - 100% NET LIST ELECTRICAL VERIFICATION USING METRA SUPPLIED SPEC-D-306 NET LIST FOR SPENS AND SHORTS.
 - TRAVELING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
 - TEAR STRIPS SHALL BE ADDED ON VITS AND THROUGH HOLE PADS IN ALL INTERNAL AND OUTER LAYERS.
 - ALL UNCONNECTED VITS SHALL BE SUPPRESSED IF REQUIRED.
 - FINISHED PCB THICKNESS SHALL BE 0.204mm +/-0.005.
 - NEW TRACE REWORKING ON BOARD IS 0.0025mm (0.0001").
 - DRINK UL RESISTED E-FILE NUMBER SHALL BE PRINTED ON THE PCB SILKSCREEN.
 - VIA ON PAD SHALL BE RECESSED AND COP-PLATED.
 - FOR STACKUP DETAIL PROCESS_STACKUP.PDF SHALL BE REFERRED.



DRILL CHART, TOP TO BOTTOM		
FIGURE	SIZE	DEPTH
1	0.43	0.10
2	0.43	0.10
3	0.43	0.10
4	0.43	0.10
5	0.43	0.10
6	0.43	0.10
7	0.43	0.10
8	0.43	0.10
9	0.43	0.10
10	0.43	0.10
11	0.43	0.10
12	0.43	0.10
13	0.43	0.10
14	0.43	0.10
15	0.43	0.10
16	0.43	0.10
17	0.43	0.10
18	0.43	0.10
19	0.43	0.10
20	0.43	0.10
21	0.43	0.10
22	0.43	0.10
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25	0.43	0.10
26	0.43	0.10
27	0.43	0.10
28	0.43	0.10
29	0.43	0.10
30	0.43	0.10
31	0.43	0.10
32	0.43	0.10
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34	0.43	0.10
35	0.43	0.10
36	0.43	0.10
37	0.43	0.10
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39	0.43	0.10
40	0.43	0.10
41	0.43	0.10
42	0.43	0.10
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44	0.43	0.10
45	0.43	0.10
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51	0.43	0.10
52	0.43	0.10
53	0.43	0.10
54	0.43	0.10
55	0.43	0.10
56	0.43	0.10
57	0.43	0.10
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60	0.43	0.10
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66	0.43	0.10
67	0.43	0.10
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70	0.43	0.10
71	0.43	0.10
72	0.43	0.10
73	0.43	0.10
74	0.43	0.10
75	0.43	0.10
76	0.43	0.10
77	0.43	0.10
78	0.43	0.10
79	0.43	0.10
80	0.43	0.10
81	0.43	0.10
82	0.43	0.10
83	0.43	0.10
84	0.43	0.10
85	0.43	0.10
86	0.43	0.10
87	0.43	0.10
88	0.43	0.10
89	0.43	0.10
90	0.43	0.10
91	0.43	0.10
92	0.43	0.10
93	0.43	0.10
94	0.43	0.10
95	0.43	0.10
96	0.43	0.10
97	0.43	0.10
98	0.43	0.10
99	0.43	0.10
100	0.43	0.10

LAYER STACKUP	LAYER NAME	FINISHED Cu	X-SECTION	DIELECTRIC THICKNESS
PRIMARY SIDE SILKSCREEN				
PRIMARY SIDE SOLDERMASK				
L01	PRIMARY SIDE	1.474x		0.0030
L02	GROUND-PLANE-1	0.062x		0.0030
L03	INNER-SIGNAL-1	0.062x		0.0044
L04	GROUND-PLANE-2	0.062x		0.0030
L05	INNER-SIGNAL-2	0.062x		0.0044
L06	POWER-PLANE-1	0.062x		0.0030
L07	POWER-PLANE-2	0.062x		0.0044
L08	GROUND-PLANE-3	0.062x		0.0030
L09	INNER-SIGNAL-3	0.062x		0.0044
L10	GROUND-PLANE-4	0.062x		0.0030
L11	INNER-SIGNAL-4	0.062x		0.0044
L12	SECONDARY SIDE	1.474x		0.0030
SECONDARY SIDE SOLDERMASK				
SECONDARY SIDE SILKSCREEN				

IMPEDANCE SPECIFICATIONS							
SL#	TYPE	LAYER	TRACEDWIDTH (mil)	SPACING (mil)	IMPEDANCE (Ohms)	REF LAYER	
01	EDGE COUPLED MICROSTRIP	L1, L12	3.5	5.5	100	L2, L11	
02	EDGE COUPLED MICROSTRIP	L1, L12	6.0	5.5	50	L2, L11	
03	EDGE COUPLED MICROSTRIP	L1, L12	7.5	5.5	35	L2, L11	
04	EDGE COUPLED MICROSTRIP	L1, L12	10.0	5.5	25	L2, L11	
05	EDGE COUPLED MICROSTRIP	L3, L10	4.0	4.0	50	L2/L4, L2/L11	
06	EDGE COUPLED MICROSTRIP	L3, L10	7.5	4.0	25	L2/L4, L2/L11	
07	EDGE COUPLED MICROSTRIP	L3, L10	10.0	4.0	15	L2/L4, L2/L11	
08	EDGE COUPLED MICROSTRIP	L3, L10	15.0	4.0	10	L2/L4, L2/L11	
09	EDGE COUPLED MICROSTRIP	L3, L10	20.0	4.0	7.5	L2/L4, L2/L11	
10	EDGE COUPLED MICROSTRIP	L3, L10	25.0	4.0	6.0	L2/L4, L2/L11	
11	STRIPLINE	L3, L10	4.0	NA	50	L2/L4, L2/L11	
12	STRIPLINE	L3, L10	7.5	NA	25	L2/L4, L2/L11	
13	STRIPLINE	L3, L10	10.0	NA	15	L2/L4, L2/L11	
14	STRIPLINE	L3, L10	15.0	NA	10	L2/L4, L2/L11	
15	STRIPLINE	L3, L10	20.0	NA	7.5	L2/L4, L2/L11	
16	STRIPLINE	L3, L10	25.0	NA	6.0	L2/L4, L2/L11	

SIGNATURES	DATE	 TEXAS INSTRUMENTS	PROCL352
LAYOUT BY SK	260922		AM2A EVM BOARD
REVIEWED BY ZA	260922		
APPROVED BY AMB	260922		
		SIZE: D SCALE: NONE SHEET 1 OF 19	