KeyStone 1 Self Test Kit Release Note

Applies to Release 1.1

Publication Date: March 24, 2015

# Overview

This document is the Release Notes of KeyStone 1 Self Test Kit (STK). This software release gives users the ability to debug the KeyStone 1 device and test the performance of KeyStone device, the source code can also be used as reference for customer’s driver code development.

# Platform and Device Support

This release supports the Texas Instruments TMS320C6670, TMS320C6678 and TMS320TCI6614 high performance Multicore DSP KeyStone 1 System-on-Chip (SoC).

The release is tested and verified on the C66x DSP core of C6670 EVM, C6678 EVM, TCI6614 EVM.

# Dependencies

This release requires following software components and tools versions to successfully function:

* CCS5.4
* C6678 CSL in pdk\_C6678\_1\_1\_2\_6; C6670 CSL in pdk\_C6670\_1\_1\_2\_6; TCI6614 CSL in pdk\_tci6614\_1\_02\_01\_03.

# Releases

Below is a summary of the features of all modules.

## Memory Test

|  |  |
| --- | --- |
| **Features** | **Status** |
| Test Masters | All DSP cores, All EDMA TCs, IDMA |
| Tested memories | L1D, L1P, LL2, other core's L1 and LL2, SL2, DDR3, cache, prefetch buffer |
| Test algorithm | Data pattern filling; Addressing; Bit walking |
|  |  |
| DDR3 configuration | 64 bits x 1333MTS |

## Memory Performance

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Test Masters | DSP core, All EDMA TCs, IDMA |
| Tested memories | LL2, other core's L2, SL2, DDR3 |
| Cache/Prefetch buffer configuration cases | No cache and no prefetch; L1 cache and prefetchable; L1 + L2 cache and perfetchable |
| DSP core memory copy throughput | √ |
| DSP core read/write latency | √ |
| EDMA memory copy throughput | √ |
| EDMA transfer overhead | √ |
| EDMA test with different ACNT | √ |
| EDMA test with different Index | √ |
| IDMA memory copy throughput | √ |
| IDMA transfer overhead | √ |
|  |  |
| DDR3 configuration | 64 bits x 1333MTS |

## Multicore Navigator

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Test Masters | DSP core, QMSS Packet DMA, SRIO Packet DMA, PA packet DMA |
| Tested memories | LL2, SL2, DDR3 |
| Descriptor types | Host, Monolithic |
| linking RAM | Internal, External |
| Core Cycles for PUSH/POP operation through VBUSP and VBUSM | √ |
| Interrupt latency for queue pending | √ |
| descriptor accumulation latency | √ |
| descriptor Reclamation latency | √ |
| Packet DMA Throughput | √ |
| Packet DMA transfer overhead | √ |

## Timer

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| one-shot pulse and interrupt | √ |
| continual clock and interrupts | √ |
| square waves with special duty cycle | √ |
| watch-dog and exception | √ |

## SRIO

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Operations | SWRITE, NWRITE, NWRITE\_R, NREAD, message(type11), stream(type9); |
| Serdes lanes combination | 4x1x, 2x2x, 1x4x |
| Test with different memory buffer | LL2, SL2, DDR3 |
| Internal loopback | Digital Loopback, Serdes loopback |
| Test between two devices | External line loopback; forwarding back; transfer between two devices. |
| Throughput test | √ |
| Interrupts test | √ |
|  |  |
| Speed | 5Gbps, 3.125Gbps, 2.5Gbps, 1.25Gbps |

## HyperLink

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Test Master | DSP core, EDMA |
| Test with different memory buffer | LL2, SL2, DDR3 |
| Cache/Prefetch buffer configuration cases | No cache and no prefetch; L1 cache and prefetchable; L1 + L2 cache and perfetchable |
| Internal loopback | Serdes loopback |
| Test between two devices | √ |
| Integrity test | Data pattern filling; Addressing test |
| DSP core memory copy throughput | √ |
| DSP core read/write latency | √ |
| EDMA memory copy throughput | √ |
| EDMA transfer overhead | √ |
| Interrupts test | √ |
|  |  |
| Speed | 3.125Gbps, 5Gbps, 6.25Gbps |

## PCIE

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Test Master | DSP core, EDMA |
| Test with different memory buffer | LL2, SL2, DDR3 |
| Cache/Prefetch buffer configuration cases | No cache and no prefetch; L1 + L2 cache and perfetchable |
| Internal loopback | Serdes loopback |
| Test between two devices | √ |
| Integrity test | Data pattern filling; Addressing test |
| DSP core memory copy throughput | √ |
| DSP core read/write latency | √ |
| EDMA memory copy throughput | √ |
| EDMA transfer overhead | √ |
| Interrupts test | √ |
|  |  |
| Speed | 5Gbps, 2.5Gbps |

## GE (Gigabit Ethernet)

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Test with different memory buffer | LL2, SL2, DDR3 |
| Internal loopback | EMAC, SGMII, Serdes loopback |
| Test between two devices | External FIFO loopback, data from DSP 0 to DSP 1 |
| Throughput test | √ |
| Interrupts test | √ |
|  |  |
| Speed | 10Mbps, 100Mbps, 1000Mbps |

## SPI

|  |  |
| --- | --- |
| **Features** | **Status** |
| Test Masters | DSP core, EDMA |
| internal loopback | √ |
| FLASH test | Data pattern filling; Addressing |
| Max test Speed | 66MHz |

## UART

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Test Masters | DSP core, EDMA |
| internal loopback | √ |
| Tests between EVM and PC | Echo to PC; continuous data patterns transfer between EVM and PC |
| Max test Speed | 3Mbps |

## GPIO

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Direction | input, output |
| loopback test | √ |
| Interrupts | √ |

## VCP2

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Frame formats | All 3GPP frame formats |
| Performance | Channel density, DSP core cycles, VCP2 decoding time |
| Bit Error Rate checking | √ |

## Robust C66x CorePac

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Test masters | DSP core, EDMA, SRIO |
| Memory Protection | L1D, L1P, LL2, SL2, DDR, Reserved space |
| EDC | L1P, LL2, SL2, DDR |
| MPU (Peripherals protection) | √ |
| watch-dog and exception | √ |
| EDMA error handling | √ |
| Interrupt drop detection | √ |

## EMIF

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| NAND FLASH | √ |
| NOR FLASH | √ |

## AIF2

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| Antenna interface standards | CPRI, OBSAI |
| Radio Standards | LTE FDD/TDD, 5M/10M/20M; WCDMA |
| link rate | 2x, 4x, 8x |
| multiple links in parallel | 1~6 links |
| data buffer | LL2, SL2, DDR3 |
| Test data path | internal loopback, external loopback, two devices |

## I2C

|  |  |
| --- | --- |
| **Features, Test Cases** | **Status** |
| internal loopback | √ |
| EEPROM test | √ |
| I2C speed | 400K |

# New features and fixes

|  |  |
| --- | --- |
| **Module** | **New features and fixes** |
| Common functions | 1. Print device information including device type, speed grade, boot mode, required voltage, ID… 2. Common device, CPU, interrupt initialization functions. 3. Common test functions including memory test, memory copy, EDMA copy… |
| SPI | 1. save/restore flash content during test. 2. Support FLASH larger than 16MB. 3. fix CS selection and polarity bug in KeyStone\_SPI\_init\_drv.c/h |
| I2C | 1. save/restore EERPOM content during test. 2. add KeyStone\_I2C\_read\_follow\_write() in KeyStone\_I2C\_init\_drv.c |
| EMIF | save/restore flash content during test. |
| GE | Fixed SGMII and MDIO status check bug in KeyStone\_GE\_Init\_drv.c, GE\_debug.c and GE\_test.c. |
| HyperLink | add 5ms delay after enabling the power domain. |
| Timer | Add function to generate continual square waves. |
| Memory Test | optimize the data filling pattern |
| Memory Performance | add memory copy cases for SL2 and DDR |
| UART | to support selective interrupt enable for different case in KeyStone\_UART\_Interrupts\_Init(). |
| AIF2 | Fix SD\_PLL\_Bx\_STS check bug in AIF\_debug.c |
|  |  |