AM64x/AM243x EVM BOARD
PROC101D
TABLE OF CONTENTS

Revision Number

REV	D
VER	1.3

D-Note:-

SK/EVM is a device evaluation board or platform. The SK/EVM is not a reference design. In some cases the EVM implementation may deviate from the optimum solution to provide a better customer experience or provide flexibility for customers to be able to validate the SOC functionality. TI expects and recommends customers to carefully review and follow all requirements defined in the datasheet, silicon errata, and TRM when designing their custom board. The information found in the datasheet should always take precedence over the SK/EVM implementation.

R-Note:-

* Verify the DNI components configuration with respect to the EVM schematics (Use PDF) after completion of board design before board assembly.
* A standard 5% tolerance resistor can be used for most of the series and parallel pull resistor.
* Be sure to read through all the D-Notes (Design notes), R-Notes (Review notes) and CAD notes during board design and before start of board build. (Refer FAQs listed for additional details)

KEY LINKS TO COLLATERALS

Hardware Design Guide : https://www.ti.com/lit/an/sprad67a/sprad67a.pdf
Schematic Design and Review Checklist : https://www.ti.com/lit/an/spracu5c/spracu5c.pdf
DDR Board Design and Layout Guidelines : https://www.ti.com/lit/an/spracu1a/spracu1a.pdf
PMIC Power Solutions application note - > Powering the AM64x with the TPS65220 or TPS65219 PMIC https://www.ti.com/lit/pdf/slvafe9
Using LP8733xx and TPS65218xx PMICs to Power AM64x and AM243x Sitara Processors https://www.ti.com/lit/pdf/slda059
EVM/SKs (Starter Kits) for reference : TMDS64EVM, SK-AM64B

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Title	TABLE OF CONTENTS	
Size C	Variant Name = PROC101D(004) TMDS64EVM	Rev D
Date: Wednesday, June 12, 2024	Sheet 1 of 40	

REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	11th MARCH 2022	Drafted from "PROC101B_SCH" document.	Mistral Design Team	AJIT MB	AJIT MB
0.2	11th MARCH 2022	Removed Voltage Monitor circuit & added RC Delay Circuit for power down sequence requirement Fixed Power down sequence issue seen on AM243x REV B	Mistral Design Team	AJIT MB	AJIT MB
0.3	11th MARCH 2022	Updated schematics to support PG2 Silicon	Mistral Design Team	AJIT MB	AJIT MB
1.0	30th MARCH 2022	Baselined and Released	Mistral Design Team	AJIT MB	AJIT MB
1.1	5th AUG 2022	Updated SoC Part Number and OPN Details Updated SoC Symbol for Reserved pins	Mistral Design Team	AJIT MB	AJIT MB
1.2	27 NOV 2023	Reduced the switching frequency of U30 to 440 Khz for compliance testing (R.E) Resized the Inductors (L5 & L6), Capacitors (C69, C71, C81 & C82) for the change in SW frequency of U30	Mistral Design Team	AJIT MB	AJIT MB
1.3	12 JUNE 2024	Updated SoC Part Number, Enabled Voltage ratings for all the capacitors and added Design Review notes Moved to DNI : R67, R444, R65, C184, C262, C133, C134, Y1 Moved to Mount : R66, R193, R479, R480, R483, R484, R485, R646, R181, R176, R169, R172, R173, R180, R179, R178, R240, R367, R102 C148 4.7uF changed to 1uF; C149 1uF changed to 4.7uF; C243 1uF changed to 2.2uF. R404 , R389-22E_1% changed to 0E ; R405-10K changed to 10K,1%; R167-100K changed to 10K; R428-3.48K_0.1% changed to 3.48K_1%; R427- 16.5K_0.1% changed to 16.5K_1%; R431, R576 - 10K_1% changed to Std 10K; R696- 1K_1% changed to Std 1K; R157-10E_1% changed to 0E; R70,R349,R110 - 11K_1% changed to 10K_1%.	Mistral Design Team		

LINKS TO KEY FAQs

https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1185502/faq-am6442-am6441-am6422-am6421-am6412-am6411-custom-board-hardware-design-collaterals-to-get-started
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am62x-am62ax-am62px-custom-board-hardware-design---collaterals-for-reference-during-schematic-design-and-schematics-review
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1337853/faq-am6442--am6441-am6422-am6421-am6412-am6411-custom-board-hardware-design---guidelines-for-reuse-of-tmds64evm-schematics
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1274160/faq-am6442-am6441-am6422-am6421-am6412-am6411-custom-board-hardware-design---faqs-related-to-processor-collaterals-functioning-peripherals-interface-and-evm-starter-kit

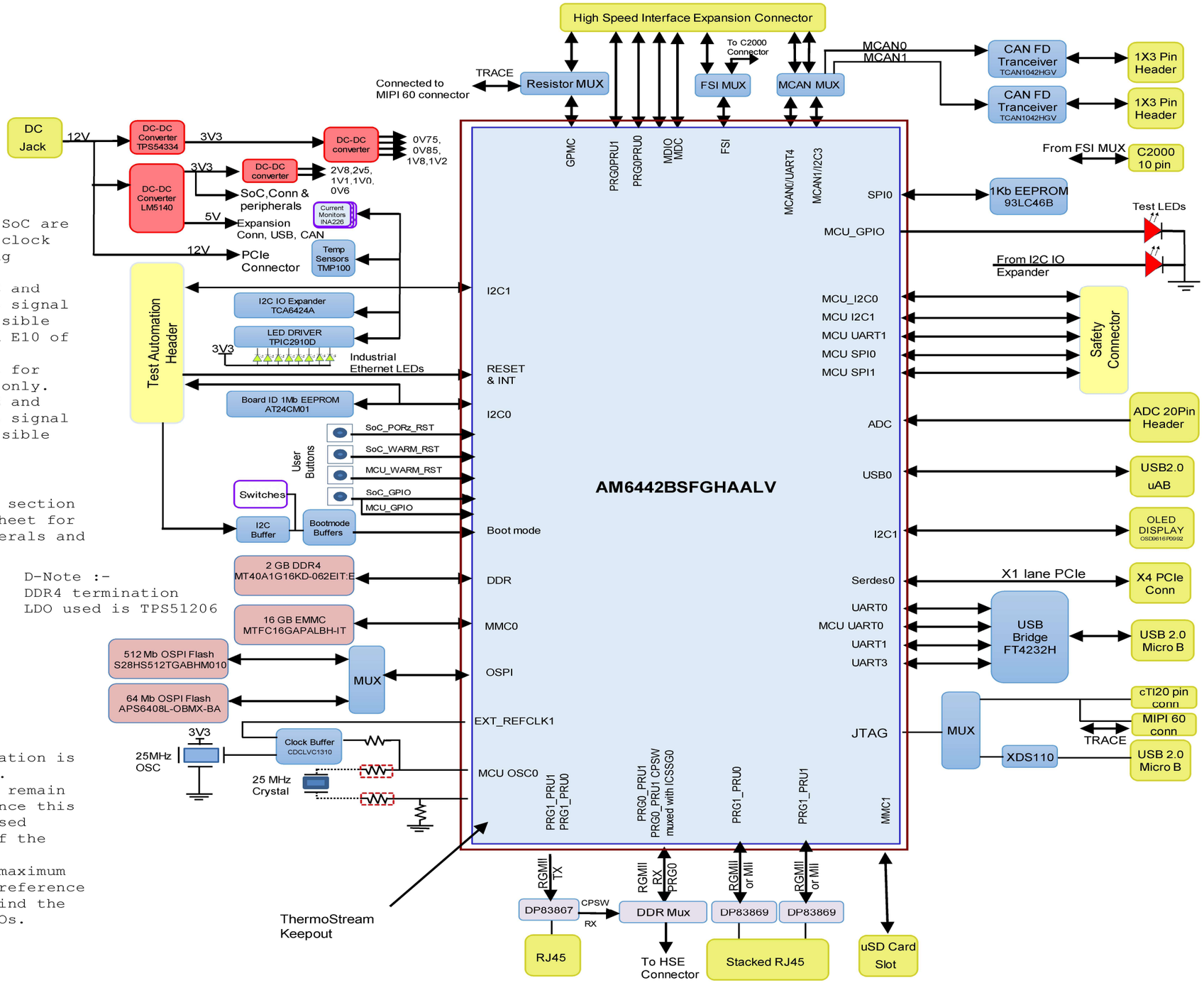
BLOCK DIAGRAM_AM64x_EVM

D-Note
Pin (**OBSCLK**) D17 of the SoC are main domain Observation clock output for test and debug purposes only.
Add a TP near to the SoC and provision to isolate the signal for testing whenever possible
Pins (MCU_**OBSCLK**) C6 and E10 of the SOC are MCU Domain Observation clock output for test and debug purposes only.
Add a TP near to the SoC and provision to isolate the signal for testing whenever possible

D-Note
Refer Device Comparison section of the processor data sheet for supported cores, peripherals and memory size

D-Note :-
DDR4 termination
LDO used is TPS51206

D-Note :-
Drive strength configuration is currently not supported.
The drive strength must remain in the default state since this is the only condition used during timing closure of the peripherals.
The devices are set to maximum drive strength. Please reference to the IBIS model to find the drive strength of the IOs.



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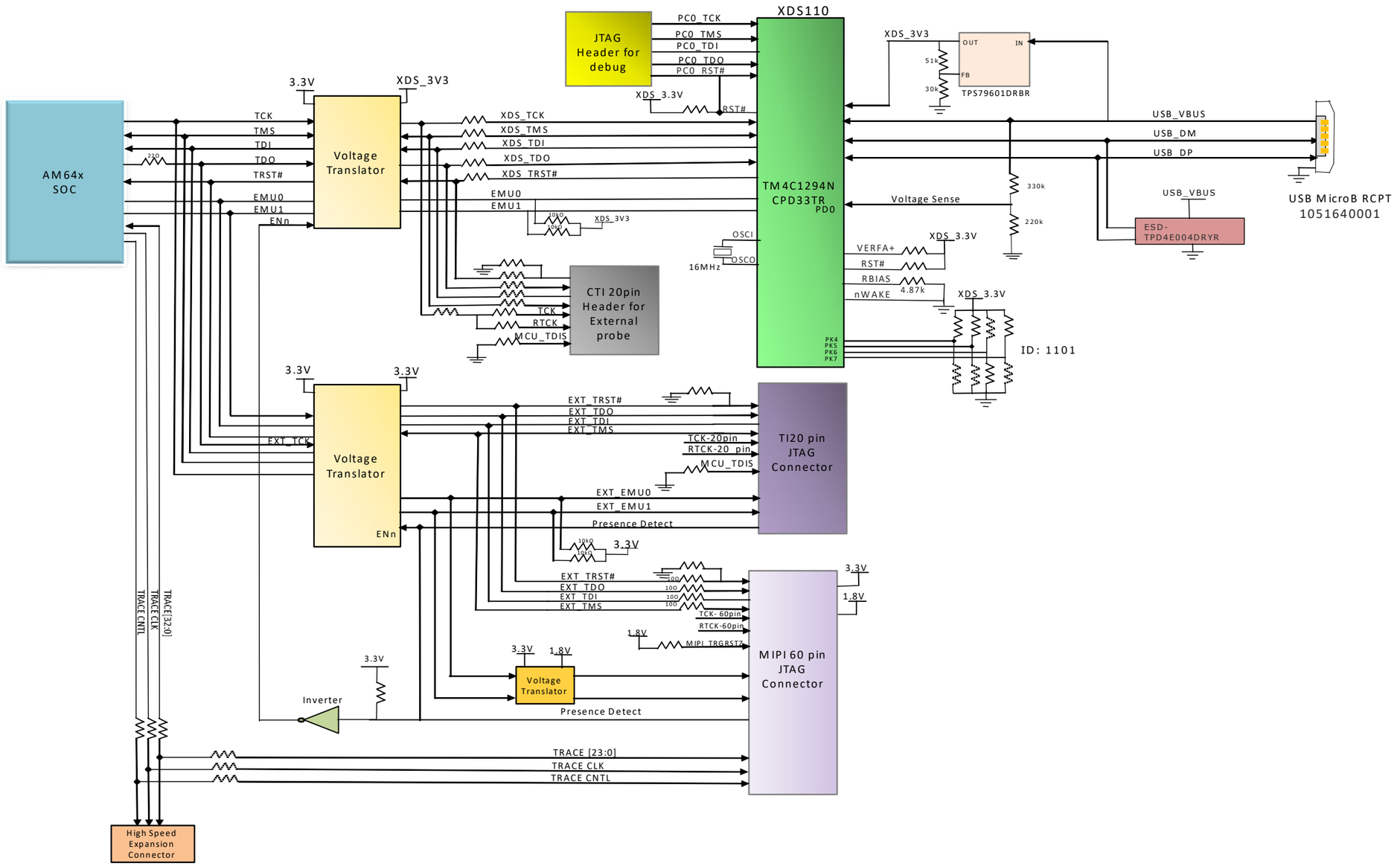
Title	BLOCK DIAGRAM_CP BOARD	
Size: C	Variant Name = PROC101D(004) TMDS64EVM	Rev: D
Date: Wednesday, June 12, 2024	Sheet 3 of 40	

BLOCK DIAGRAM_XDS110



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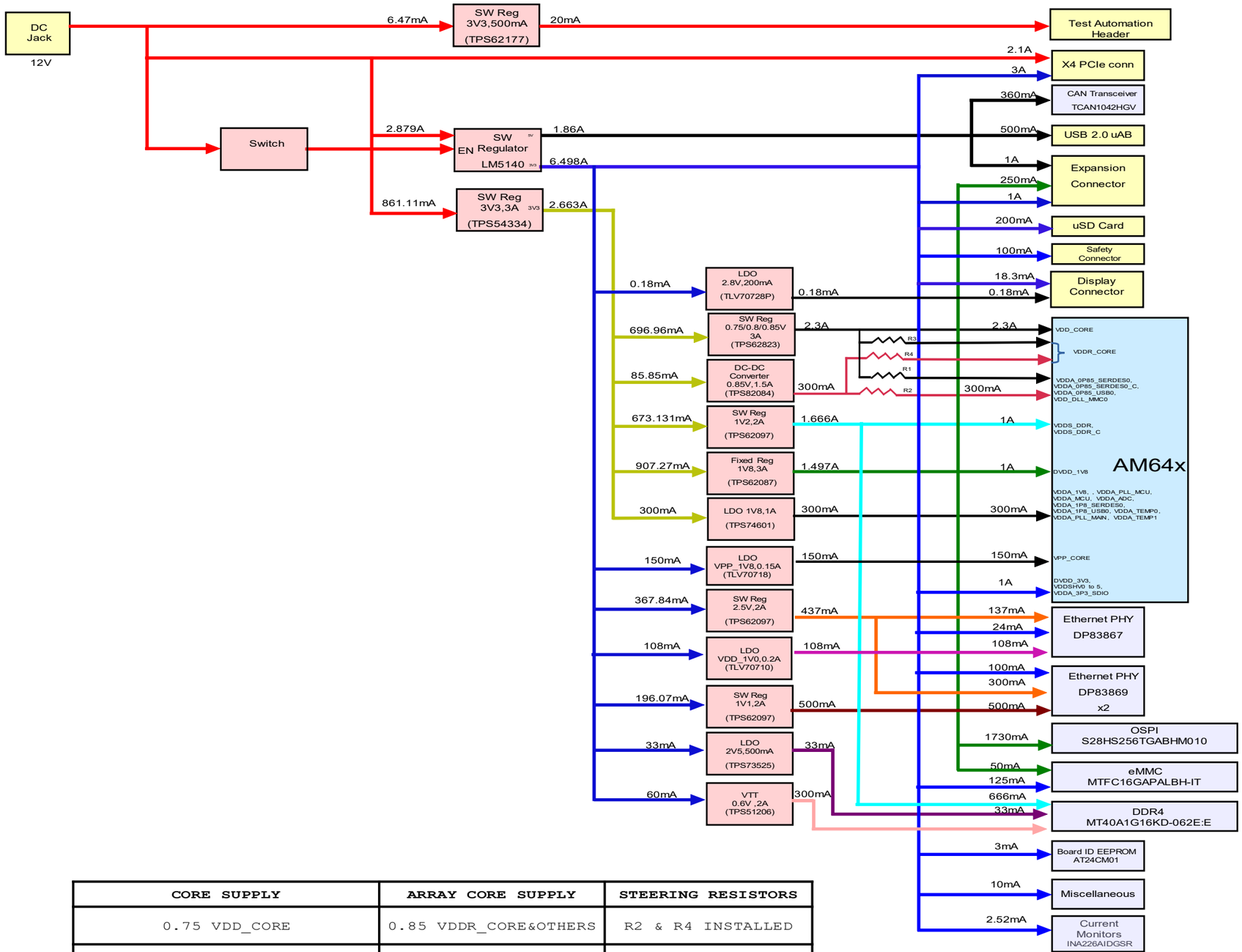
Title	BLOCK DIAGRAM_XDS110	
Size: C	Variant Name = PROC101D(004) TMDS64EVM	Rev: D
Date: Wednesday, June 12, 2024	Sheet 4 of 40	

POWER FLOW DIAGRAM



CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.85 VDD_CORE,VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED

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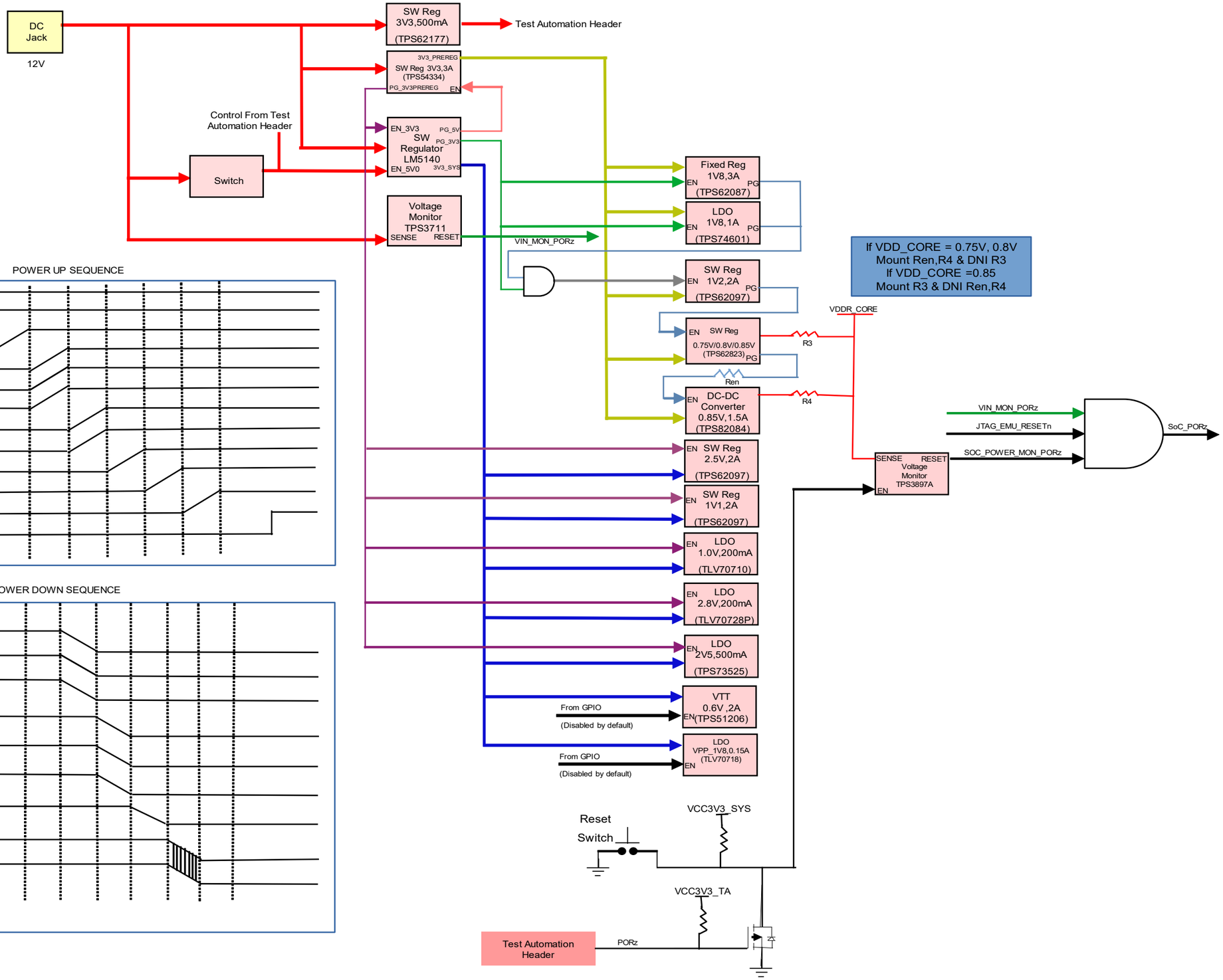
Title	POWER FLOW DIAGRAM	
Size: C	Variant Name = PROC101D(004) TMDS64EVM	Rev: D
Date: Wednesday, June 12, 2024	Sheet 5 of 40	

POWER SEQUENCE



POWER UP SEQUENCE

POWER DOWN SEQUENCE

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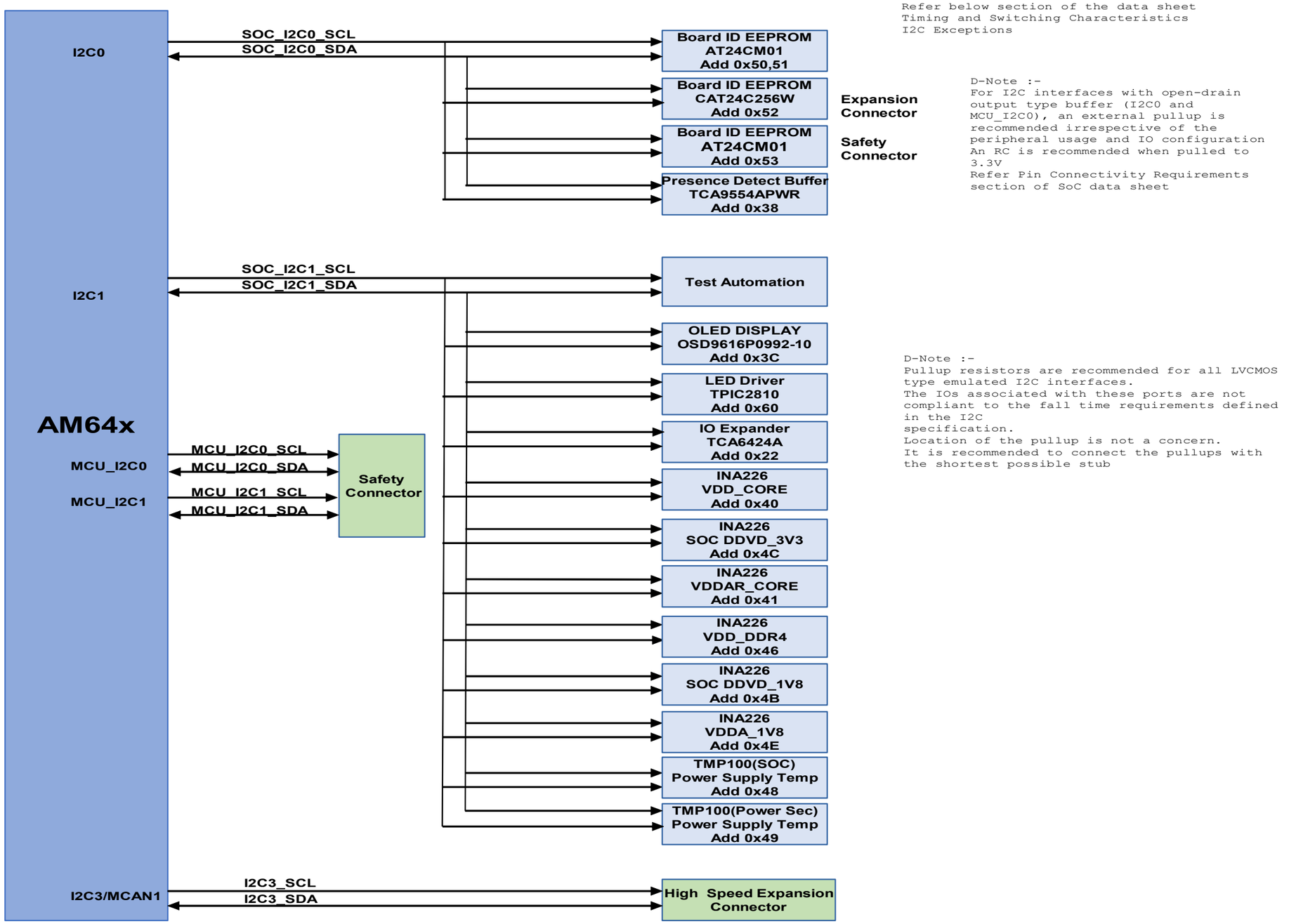
Title	POWER SEQUENCE	
Size: C	Variant Name = PROC101D(004) TMDS64EVM	Rev: D
Date: Wednesday, June 12, 2024	Sheet 6 of 40	

GPIO MAPPING TABLE

S.NO	GPIO DESCRIPTION	GPIO NETNAME	REQUIRED ON	FUNCTIONALITY	GPIO USED	SoC Muxed Signal Name	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE
1	EMMC RESET Control GPIO	GPIO_eMMC_RSTn	GP EVM	Reset	IO EXPANDER- P00		OUTPUT	HIGH	LOW
2	OSPI RESET Control GPIO	GPIO_OSPI_RSTn	GP EVM	Reset	GPIO013	OSPI0_CS2	OUTPUT	HIGH	LOW
3	CPSW RGMII1 RESET Control GPIO	GPIO_CPSW1_RST	GP EVM	Reset	IO EXPANDER- P02		OUTPUT	HIGH	LOW
4	PRG1 RGMII1 Ethernet PHY RESET Control GPIO	GPIO_RGMII1_RST	GP EVM	Reset	IO EXPANDER- P03		OUTPUT	HIGH	LOW
5	PRG1 RGMII2 Ethernet PHY RESET Control GPIO	GPIO_RGMII2_RST	GP EVM	Reset	IO EXPANDER- P04		OUTPUT	HIGH	LOW
6	PRG1 RGMII1 Ethernet PHY Link Detection GPIO	PRG1_ETH1_LED_LINK	GP EVM	Link Detection	PRG1_PRU0_GPO8		INPUT	LOW	HIGH
7	PRG1 RGMII2 Ethernet PHY Link Detection GPIO	PRG1_ETH2_LED_LINK	GP EVM	Link Detection	PRG1_PRU1_GPO8		INPUT	LOW	HIGH
8	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	GP EVM	Interrupt	Connected to PRG1_RGMII_INT via 0E res		INPUT	HIGH	LOW
9	PRG1 Ethernet PHY 1Interrupt	PRG1_RGMII_INT	GP EVM	Interrupt	GPIO1_70	EXTINTn	INPUT	HIGH	LOW
10	PRG1 Ethernet PHY 2Interrupt			Interrupt			INPUT	HIGH	LOW
11	PCIe RESET Control GPIO	GPIO_PCIe_RST_OUT	GP EVM	Reset	IO EXPANDER- P05		OUTPUT	LOW	HIGH
12	SD card load switch enable control	MMC1_SD_EN	GP EVM	Load SW Enable	IO EXPANDER- P06		OUTPUT	HIGH	LOW
13	One GPIO is required to control the Mux select between HSE and FSI Connector	FSI_FET_SEL	GP EVM	Mux Seleection	IO EXPANDER- P07		OUTPUT	PREFERABLE	PREFERABLE
14	One GPIO is required to enable Standby mode in CAN tranceiver	MCAN0_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P10		OUTPUT	LOW	HIGH
15	One GPIO is required to enable Standby mode in CAN tranceiver	MCAN1_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P11		OUTPUT	LOW	HIGH
16	One GPIO is required to control the Mux select between HSE and Ethernet PHY	CPSW_FET_SEL	GP EVM	Mux Seleection	IO EXPANDER- P12		OUTPUT	PREFERABLE	PREFERABLE
17	MDC/MDIO FET Switch Select for Mux	PRG1_RGMII2_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P14		OUTPUT	PREFERABLE	PREFERABLE
18	VTT 0.6V regulator Enable	VTT_EN	GP EVM	VTT 0.6V regulator Enable	GPIO0_12	OSPI0_CSn1	OUTPUT	LOW	HIGH
19	TEST GPIO1 from Test Automation Connector/ GPIO for GP board push button	TEST GPIO1/GPIO1_43	GP EVM	GPIO for communications with AM64x	GPIO1_43	SPI0_CS1	INPUT	HIGH	LOW
20	TEST GPIO2 from Test Automation Connector	TEST GPIO2	GP EVM	GPIO for communications with AM64x	IO EXPANDER- P15		INPUT	HIGH	LOW
21	OLED Display RESET GPIO	GPIO_OLED_RESETn	GP EVM	Reset	IO EXPANDER- P16		OUTPUT	LOW	HIGH
22	IO Expander Interrupt	IO_EXP_INTn	GP EVM	Interrupt	GPIO1_78	MMC1_SDWP	INPUT	HIGH	LOW
23	VPP 1.8V regulator Enable	VPP_LDO_EN	GP EVM	VPP 01.8V regulator Enable	IO EXPANDER- P17		OUTPUT	LOW	HIGH
24	One GPIO is required to control the Mux select between HSE and CAN Interface	CAN_MUX_SEL	GP EVM	Mux Seleection	IO EXPANDER- P01		OUTPUT	LOW	HIGH
25	User LED	TEST_LED1	GP EVM	Test	IO EXPANDER- P20		OUTPUT	LOW	HIGH
26	User LED	TEST_LED2	GP EVM	Test	MCU_SPI1_CS0	MCU_GPIO0_5	OUTPUT	LOW	HIGH
27	One GPIO to enable the PCIe Clock generator outputs	CDC_OE1/E4	GP EVM	Clock output enable	IO EXPANDER- P21		OUTPUT	HIGH	HIGH

I2C TREE



R-Note :-
Refer below section of the data sheet
Timing and Switching Characteristics
I2C Exceptions

D-Note :-
For I2C interfaces with open-drain output type buffer (I2C0 and MCU_I2C0), an external pullup is recommended irrespective of the peripheral usage and IO configuration
An RC is recommended when pulled to 3.3V
Refer Pin Connectivity Requirements section of SoC data sheet

R-Note :-
Add - Indicates Address

D-Note :-
Pullup resistors are recommended for all LVCMOS type emulated I2C interfaces.
The IOs associated with these ports are not compliant to the fall time requirements defined in the I2C specification.
Location of the pullup is not a concern.
It is recommended to connect the pullups with the shortest possible stub

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TEXAS INSTRUMENTS MISTRAL

Title	I2C TREE	
Size	Variant Name = PROC101D(004) TMDS64EVM	Rev
C		D
Date: Wednesday, June 12, 2024	Sheet 8 of 40	

SoC POWER

D-Note :-
Recommend implementing the voltage monitoring functionality using VMON_VSYS for early detection of supply failure
It is meant to be a power-fail indicator for the main input (higher) voltage rail that enters the PCB. For example, 5, 12, or 24 volts.
The error associated with this monitor would require you to set the threshold significantly lower than the nominal to avoid false trigger
Refer System Power Supply Monitor Design Guidelines section of the data sheet

VMAIN
VCC_5V0
R604 DNI
R314 100K
D-Note :-
Use 1% tolerance resistor
VDDA_SYS_MON
R315 11K_1%
DGND

D-Note :-
Changing the core voltage is not allowed after the device has been released from reset. If you turn off the core supply, we expect you to turn off all power rails and ramp them down per the power-down sequence and wait until all supply rails decay below 300mv before turning on power again.

D-Note :-
Add a filter cap Refer System Power Supply Monitor Design Guidelines section of SoC data sheet

D-Note :-
VDDAR_0P85_SERDES0, VDDA_1V8_SERDES
Refer usage note in the Pin connectivity table

D-Note :-
VDDA_3P3_SDIO Connect to output of load switch when UHS-I speed is used

U23O

VDD_CORE: J10, J12, K9, K11, L8, L12, M9, M11, N8, N10, P9
VDD_DDR4: F7, G6, H7, J6, K7, L6
VDDA_1V8: G11, L11, P12, P13, P11, T12, R14, R15, H15, R13, J15, K14, H13, L10, M13, K13
VDDAR_0P85_SERDES0
VDDAR_0P85_USB0
VDDA_1V8_SERDES
VDDA_1V8_USB0
VDD_MMC1
SoC_DVDD3V3
VDDS_MMC0/ADC0_VREFP
SOC_DVDD1V8
VDDR_CORE
VDDA_CORE

VDDA_TEMP0
VDDA_TEMP1
VDDA_0P85_SERDES0
VDDA_0P85_SERDES0_C
VDDA_0P85_USB0
VDDA_1P8_SERDES0
VDDA_1P8_USB0
VDDA_3P3_SDIO
VDDA_3P3_USB0
ADC0_REFP
VDDS_MMC0
VDDS_OSC
VDDR_CORE
VDD_MMC0

VDDSHV_MCU: F9, G8, G10
VDDSHV0: F11, G12, G14
VDDSHV1: M7, N6, P7
VDDSHV2: R8, R10, T9
VDDSHV3: P14, P15
VDDSHV4: M14, M15
VDDSHV5: L14, L15
VMON_1P8_MCU: K16
VMON_1P8_SOC: E12
VMON_3P3_MCU: F13
VMON_3P3_SOC: F14
VMON_VSYS: K10
VDDS_DDR_C: J8
VDDA_ADC: J13
VDDA_MCU: K12
VPP: G15
VDD_DLL_MMC0: H14
VDDA_PLL0: N12
VDDA_PLL1: H9
VDDA_PLL2: J11

SoC_DVDD3V3
SOC_DVDD1V8
VDDSHV_SD_IO
VDDA_1V8_MCU
VDDA_1V8_USB0
VDDA_ADC
VDDA_1V8_MCU
VPP_1V8
VDD_DLL_MMC0
VDDA_PLL0
VDDA_PLL1
VDDA_PLL2

AM6442BSFGHAALV

D-Note :-
VDDSHV_SD_IO
Refer pin connectivity table when SD card interface is not used

R-Note
Connecting 1.8V supply source directly to VPP continuously is not allowed

D-Note :-
Select a capacitor with ESR < 1 O.
Ensure the PCB loop inductance is < 2.5 nH
Select 0201 package or smallest possible package
Refer SoC Data sheet

U23N

CAP_VDDS_MCU: H10
CAP_VDDS0: H12
CAP_VDDSHV_MMC1: K15
CAP_VDDS1: T7
CAP_VDDS2: R11
CAP_VDDS3: N14
CAP_VDDS4: M16
CAP_VDDS5: L13

VDDSHV_SD_IO
C289 1uF 6.3V
C390 1uF 6.3V
C400 3.3uF 6.3V
C298 1uF 6.3V
C348 1uF 6.3V
C357 1uF 6.3V
C396 1uF 6.3V
C391 1uF 6.3V
DGND

AM6442BSFGHAALV

D-Note :-
Increase voltage rating to 10V or 16V to include the effect of DC bias

VDD_CORE
VDDR_CORE
VDDAR_CORE
VDDA_CORE
R106 DNI
R3
R297 0E
R4
R1
R78 DNI
R75 0E
R2

CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.85 VDD_CORE,VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED

SOC_DVDD1V8
VDDS_MMC0/ADC0_VREFP
VDDA_ADC
R698 DNI
R699 0E

D Note :-
Mount R699 and DNI R698 when SR2.0 Device is used
Mount R698 and DNI R699 when SR1.0 Device is used
Currently shipped device are SR2.0

D-Note :-
Refer pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used. It is acceptable to have the supplies connected and all the USB pins left unconnected provided the USB driver is not initialized any time and the USB calibration procedure does not happen. Grounding the USB supplies as per pin connectivity requirements when not used saves power when low power is a critical requirement.

D-Note :-
A Trace connected to SOC is effectively an antenna that will pick up noise.
A potential will be generated on the signal when noise couples into the antenna.
This potential will be largest on the highest impedance end of the signal.
By placing a pull-up or pull-down near the SoC pin, we force the highest potential to the open-circuit end of the signal rather than the SoC end of the signal.

CORE SUPPLY

VDDA_CORE — FB4 — VDDAR_0P85_SERDES0
26E
D-Note :-
Ferrite is optional when SERDES0 is not used

VDDAR_0P85_SERDES0
C91 0.1uF 16V
C92 0.1uF 16V
C93 0.1uF 16V
C356 0.01uF 25V
C344 0.01uF 25V
C362 0.01uF 25V
DGND

VDDAR_0P85_SERDES0
C88 4.7uF 10V
DGND

D-Note :-
Bulk caps are optional when SERDES0 is not used

VDDA_CORE — FB16 — VDDAR_0P85_USB0
26E

VDDAR_0P85_USB0
C358 0.1uF 16V
C350 0.01uF 25V
DGND

VDDAR_0P85_USB0
C341 4.7uF 10V
DGND

VDDA_CORE — FB17 — VDD_DLL_MMC0
26E

VDD_DLL_MMC0
C365 0.1uF 16V
C373 0.01uF 25V
DGND

VDD_DLL_MMC0
C377 4.7uF 10V
DGND

1.8V Analog SUPPLY

VDDA_1V8 — FB3 — VDDA_PLL2
120E

VDDA_PLL2
C75 0.1uF 16V
C347 0.01uF 25V
DGND

VDDA_PLL2
C74 4.7uF 10V
DGND

1.8V Analog SUPPLY

VDDA_1V8 — FB5 — VDDA_1V8_MCU
120E

VDDA_1V8_MCU
C387 0.1uF 16V
C353 0.01uF 25V
DGND

VDDA_1V8_MCU
C103 4.7uF 10V
DGND

VDDA_1V8 — FB15 — VDDA_PLL0
120E

VDDA_PLL0
C340 0.1uF 16V
C355 0.01uF 25V
DGND

VDDA_PLL0
C327 4.7uF 10V
DGND

VDDA_1V8 — FB20 — VDDA_1V8_USB0
120E

VDDA_1V8_USB0
C399 0.1uF 16V
C380 0.01uF 25V
DGND

VDDA_1V8_USB0
C398 4.7uF 10V
DGND

VDDA_1V8 — FB13 — VDDA_PLL1
120E

VDDA_PLL1
C300 0.1uF 16V
C322 0.01uF 25V
DGND

VDDA_PLL1
C299 4.7uF 10V
DGND

VDDA_1V8 — FB18 — VDDA_ADC
120E

VDDA_ADC
C368 0.1uF 16V
DGND

VDDA_ADC
C363 4.7uF 10V
DGND

VDDA_1V8 — FB6 — VDDA_1V8_SERDES
120E
D-Note :-
Ferrite is optional when SERDES0 is not used

VDDA_1V8_SERDES
C121 0.1uF 16V
C375 0.01uF 25V
DGND

VDDA_1V8_SERDES
C120 4.7uF 10V
DGND

D-Note :-
Bulk caps are optional when SERDES0 is not used

D-Note :-
Common SOC LVCMOS IO interface guidelines
1. Most of the SOC IOs are not fail-safe. No input should be applied before supply ramps.
2. SOC LVCMOS inputs have minimum slew rate requirements specified
3. SOC IO buffers are off during Reset. A pull is required near to the attached device being driven by the SOC IOs
4. Any SOC IO that has a trace connected and not being actively driven needs a parallel pull. When adding pull is not feasible, ensure the traces are routed away from noisy signals

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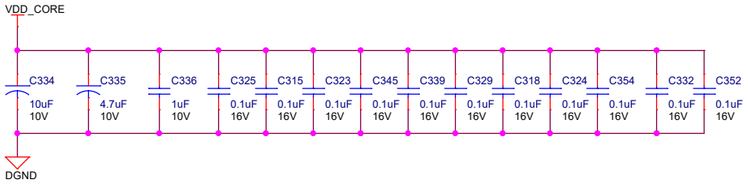
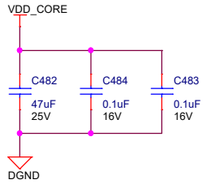
TEXAS INSTRUMENTS
MISTRAL

Title	SOC POWER	
Size	Variant Name = PROC101D(004) TMDS64EVM	Rev
C		D
Date: Wednesday, June 12, 2024	Sheet 9 of 40	

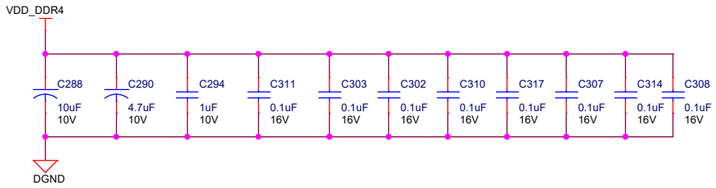
SOC POWER SUPPLIES - DECAPS



Cad Note :- Place 0.1 uF caps near to SoC pins

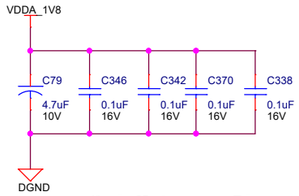


Cad Note :-
To place after current sense resistor on VDD_CORE plane

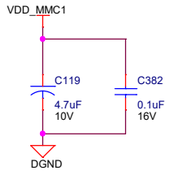


Cad Note :- Place 0.1 uF caps near to SoC pins

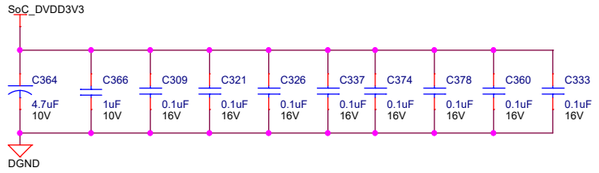
VDD ARRAY CORE



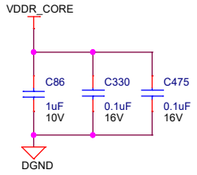
VDDA_3P3_SDIO

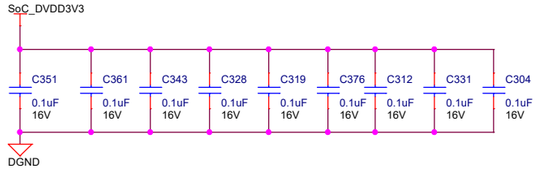


Cad Note :- Place 0.1 uF caps near to SoC pins

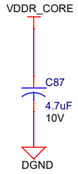


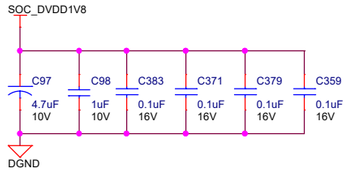
Cad Note :- Place 0.1 uF caps near to SoC pins

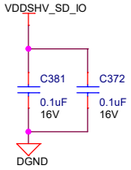




Cad Note :- Place 0.1 uF caps near to SoC pins

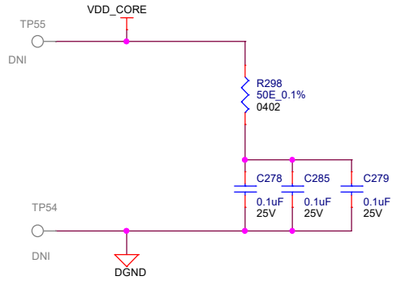


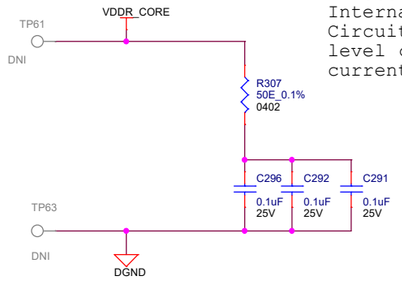




Cad Note :- Place 0.1 uF caps near to SoC pins

Core & Array Core Supply Kelvin Sensing



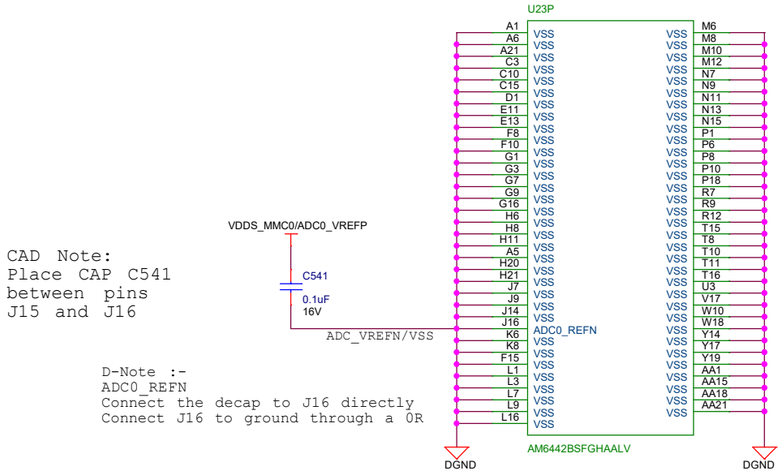


R-Note :-
Internal testing
Circuit for testing of noise level on the low voltage/high current power rails

Designed for TI by Mistral Solutions Pvt Ltd

Title	SOC POWER CAPS	
Size C	Variant Name = PROC101D(004) TMDS64EVM	Rev D
Date: Wednesday, June 12, 2024	Sheet 10 of 40	

SoC POWER - VSS



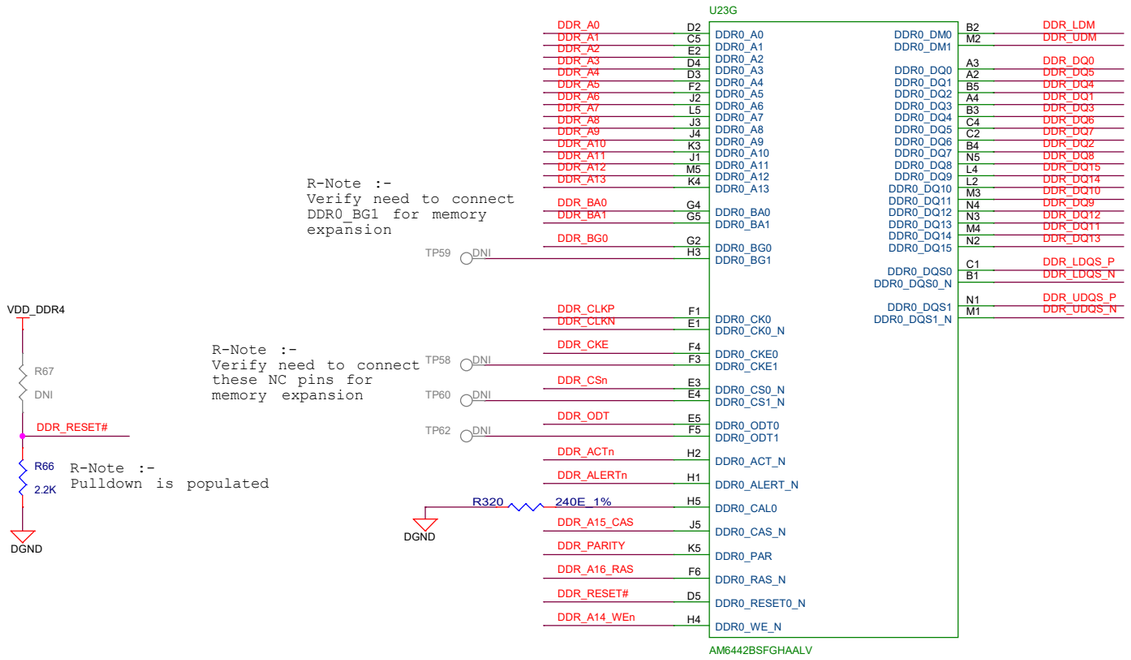
CAD Note:
Place CAP C541
between pins
J15 and J16

D-Note :-
ADC0_REFN
Connect the decap to J16 directly
Connect J16 to ground through a 0R

Designed for TI by Mistral Solutions Pvt Ltd

Title	SOC VSS	
Size: C	Variant Name = PROC101D(004) TMDS64EVM	Rev: D
Date: Wednesday, June 12, 2024	Sheet 11 of 40	

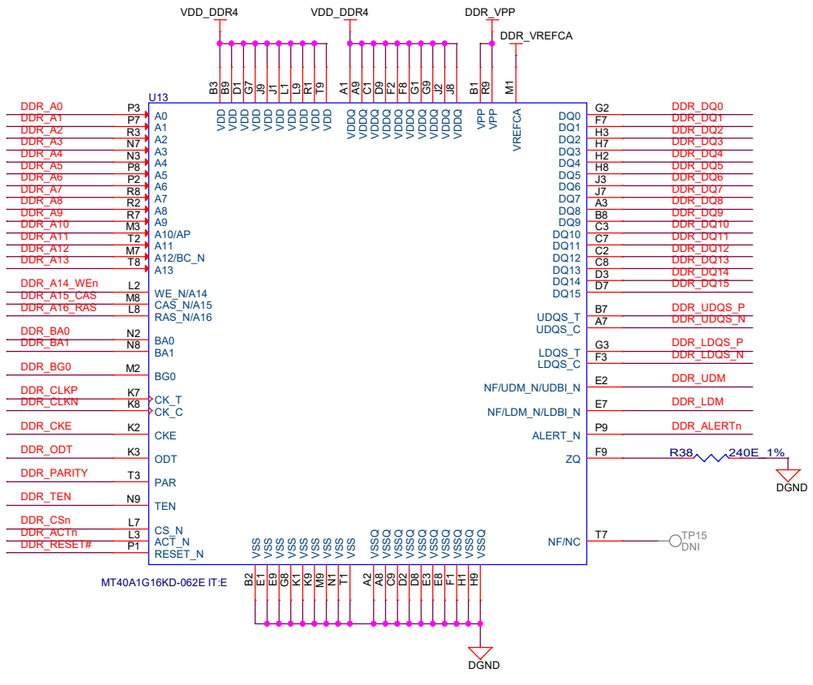
SoC DDR INTERFACE

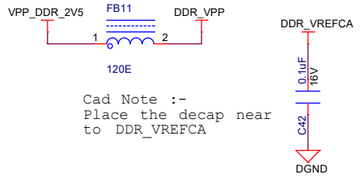


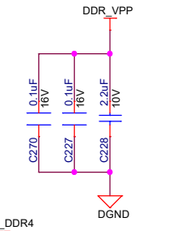
D-Note :-

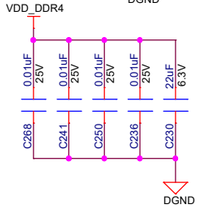
DDR DQ Lines Swapped With Data Byte

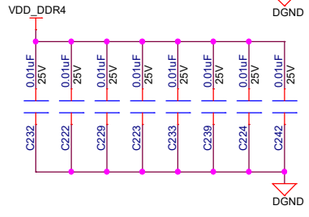
DDR4 DEVICE



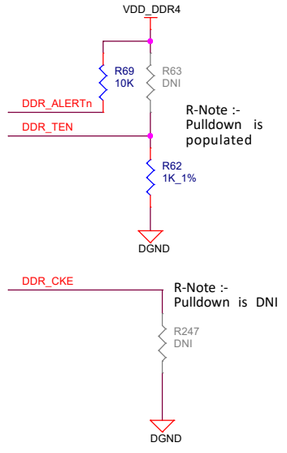


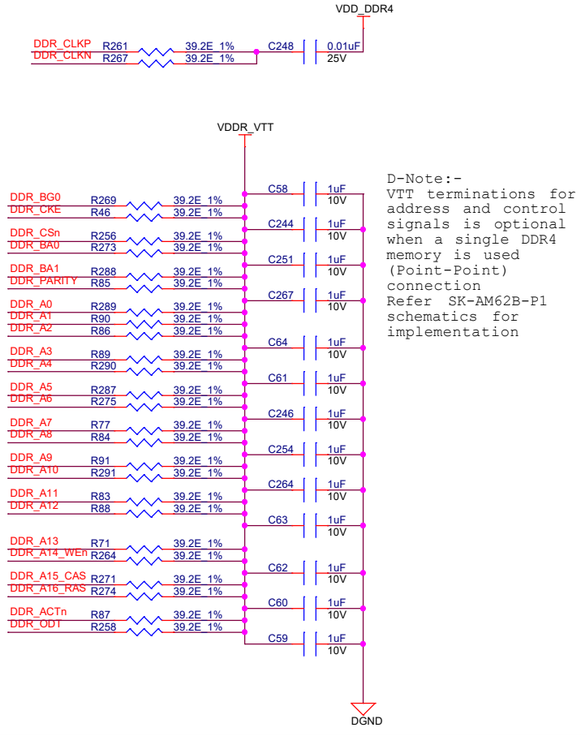






DDR TERMINATION





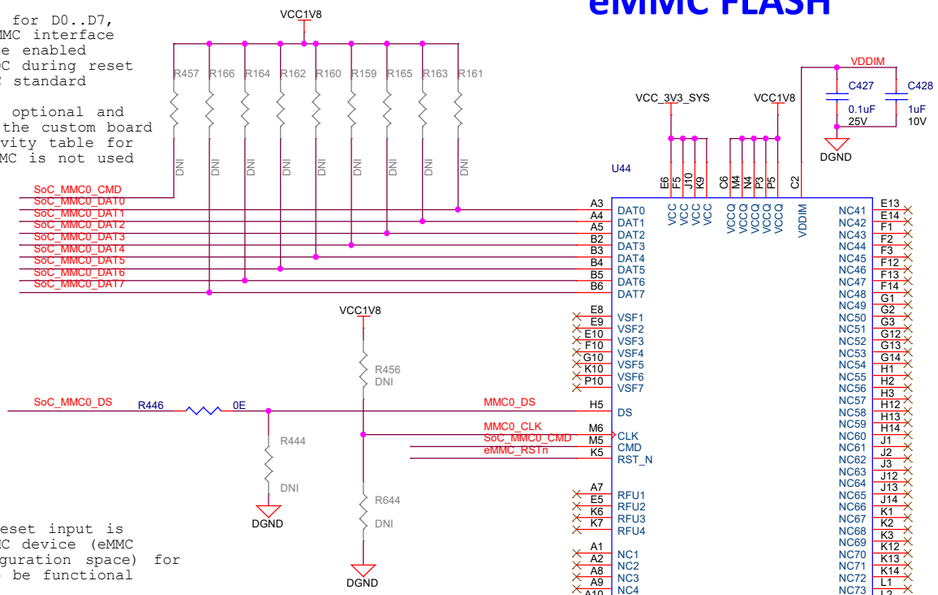
Designed for TI by Mistral Solutions Pvt Ltd

Title	DDR INTERFACE		
Size	Variant Name = PROC101D(004) TMDS64EVM		Rev
C			D
Date:	Wednesday, June 12, 2024	Sheet 12 of 40	

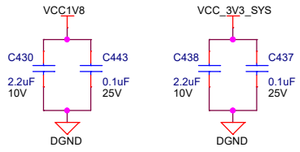
eMMC FLASH

D-Note :-
This family of processor implements a hard and dedicated PHY for eMMC interface.
The pull required for D0..D7, Clock and other eMMC interface control signals are enabled internal to the SOC during reset
Refer pin connectivity table for guidelines when eMMC is not used

D-Note :-
The pulls required for D0..D7, Clock and other eMMC interface control signals are enabled internal to the SOC during reset and are eMMC JEDEC standard compliant
External pullup is optional and can be deleted on the custom board
Refer pin connectivity table for guidelines when eMMC is not used



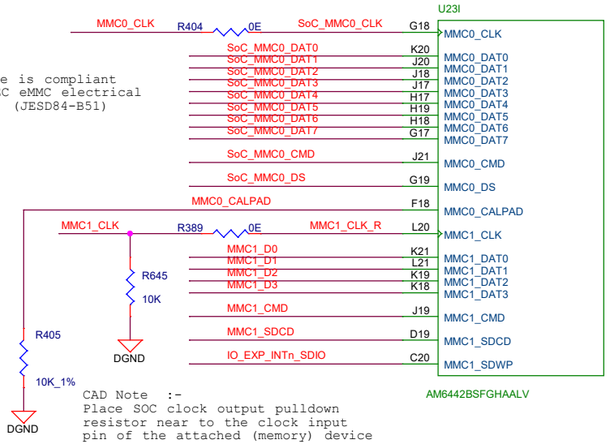
D-Note :-
Add additional decaps as required
Refer SK-AM62P-LP schematics



D-Note :-
Ensure eMMC_RSTn Reset input is enabled in the eMMC device (eMMC non-volatile configuration space) for the reset logic to be functional

SOC - MMC INTERFACE

D-Note :-
0E provision on MMC0_CLK
Helps improve signal integrity



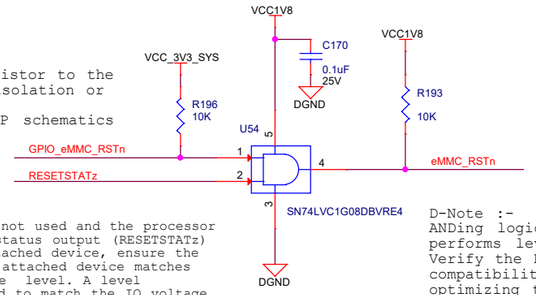
D-Note :-
MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51)

R-Note :-
What is the reason we selected pulldown instead of pullup for EMMC, SD card or other peripherals?
Because there are cases where the clock is stopped or paused in a low logic state and the pull-down option is consistent with this logic state.

CAD Note :-
Place SOC clock output pulldown resistor near to the clock input pin of the attached (memory) device

eMMC FLASH RESET

D-Note :-
Add a series resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics



D-Note :-
In case ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level. A resistor divider could be used alternatively, provided optimum impedance value of the resistor divider is selected. If too high the rise/fall time of the eMMC reset input could be slow and introduce too much delay. If too low it will cause the AM62x to source too much steady-state current during normal operation.

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation

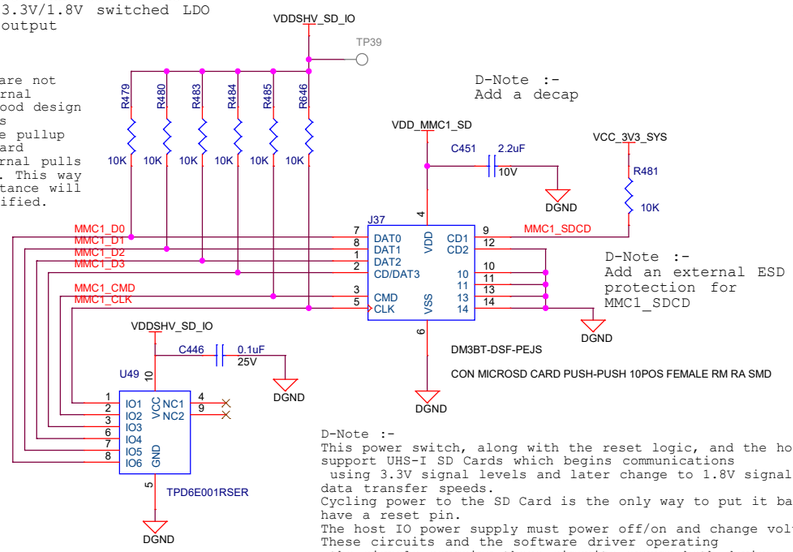
D-Note :-
The GPIO reset option makes it possible for software to reset the attached device (eMMC or OSPI or SD card or OLDI0 or EPHY) without resetting the entire processor if there is a case where the peripheral becomes unresponsive.

D-Note :-
You could eliminate the GPIO option and only use the reset output (Warm or Cold), where software forces a warm reset if the peripheral becomes unresponsive. However, this will reset the entire device rather than trying to recover the specific peripheral without resetting the entire device.

SD CARD INTERFACE

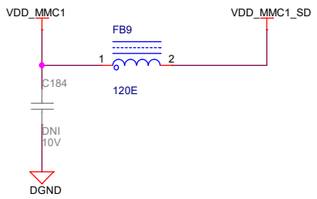
D-Note :-
For UHS-I operation, the pullups are recommended to be connected to the 3.3V/1.8V switched LDO output

D-Note :-
Ensure internal pullups are not configured when 10K external pullups are used. As a good design practice, a 47K pullup is recommended to ensure the pullup value is within the SD card specification, when internal pulls are enabled unexpectedly. This way the resulting pull resistance will still be within the specified.



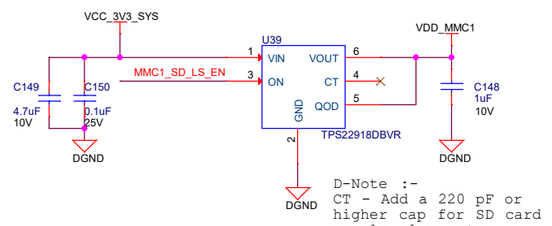
D-Note :-
Add a decap

D-Note :-
Add an external ESD protection for MMC1_SDCD



D-Note :-
Add a series resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics

D-Note :-
Anding logic could be optimized to 2 input AND gate
Use RESETSTATz and the SoC IO as inputs



D-Note :-
CT - Add a 220 pF or higher cap for SD card supply slew rate control

D-Note :-
This power switch, along with the reset logic, and the host IO power supply circuit is required to support UHS-I SD Cards which begins communications using 3.3V signal levels and later change to 1.8V signal levels when changing to one of the faster data transfer speeds.
Cycling power to the SD Card is the only way to put it back into 3.3V mode since SD Cards do not have a reset pin.
The host IO power supply must power off/on and change voltage at the same time as the SD Card.
These circuits and the software driver operating the signals sourcing these circuits ensure both devices are off, or on and operating at the same IO voltage at the same time.

Off Page Connections

From & To IO Expander

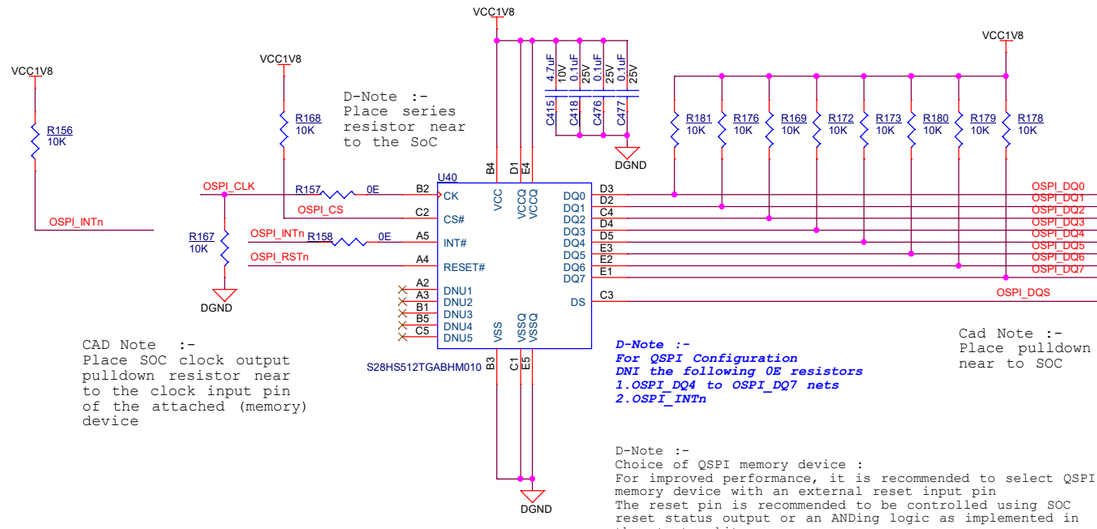
- [33] IO_EXP_INTn_SDIO <<> IO_EXP_INTn_SDIO
- [33] GPIO_eMMC_RSTn <<> GPIO_eMMC_RSTn
- [33] MMC1_SD_EN <<> MMC1_SD_EN

Designed for TI by Mistral Solutions Pvt Ltd

Title	eMMC FLASH_SDCARD INTERFACE	
Size: C	Variant Name = PROC101D(004) TMDS64EVM	Rev: D
Date: Wednesday, June 12, 2024	Sheet 13 of 40	

OSPI FLASH

R-Note :-
SOC IO buffers are off during power-up. A pullup is recommended near to the attached device, to hold the attached device IOs in a known state.
Use of Pullups are attached device dependent



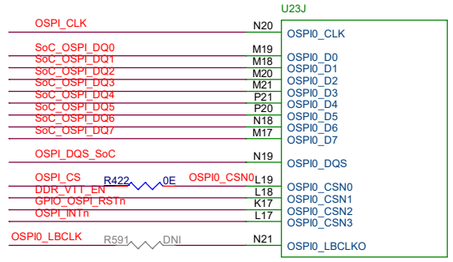
D-Note :-
Choice of QSPI memory device :
For improved performance, it is recommended to select QSPI memory device with an external reset input pin
The reset pin is recommended to be controlled using SOC reset status output or an ANDing logic as implemented in the starter kit

D-Note :-
These 0R resistors are used for configuring QSPI and OSPI
This is optional during custom board design

To Route DQS to LBCLK0	To Route DQS to SOC's DQS
Mount R591 & R600	DNI R591 & R600

SOC OSPI INTERFACE

D-Note :-
Connecting OSPI interface to multiple devices is not recommended or supported

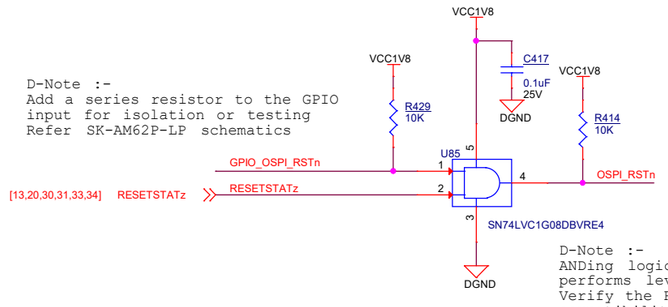


Cad Note :-

Place R591 close to the ball with as little trace as possible

D-Note :-
External loopback clock series resistors are DNI when DQS is connected

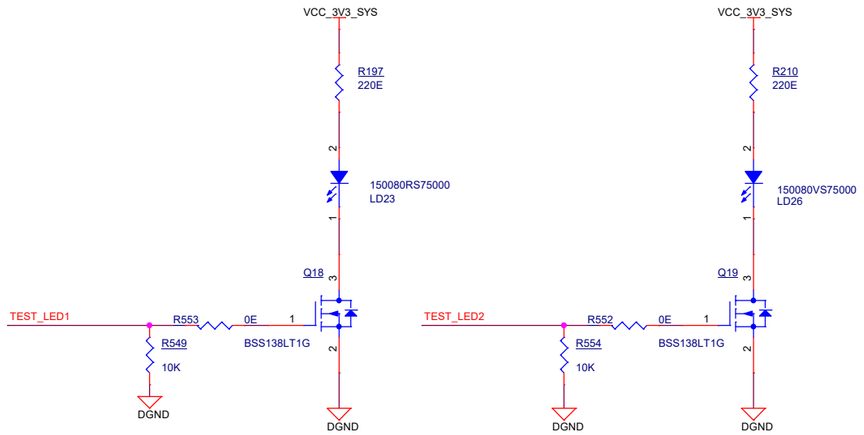
OSPI FLASH RESET



D-Note :-
Add a series resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation

USER TEST LED



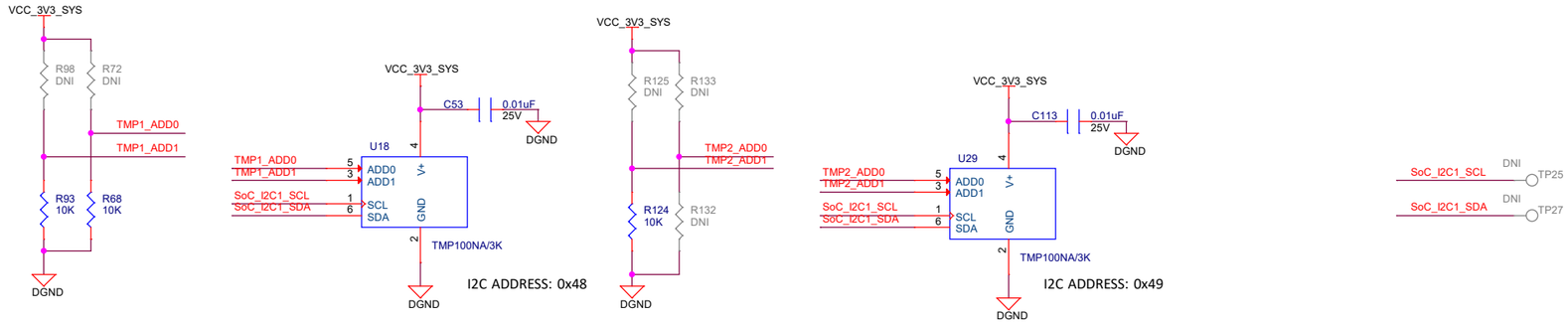
Off Page Connections

TEST_LED1 → TEST_LED1 [33]
TEST_LED2 → TEST_LED2 [34]
DDR_VTT_EN → DDR_VTT_EN [33]
To Level Translator

Designed for TI by Mistral Solutions Pvt Ltd

Title	OSPI	
Size: C	Variant Name = PROC101D(004) TMDS64EVM	Rev: D
Date: Wednesday, June 12, 2024	Sheet 14 of 40	

DIGITAL TEMPERATURE SENSOR

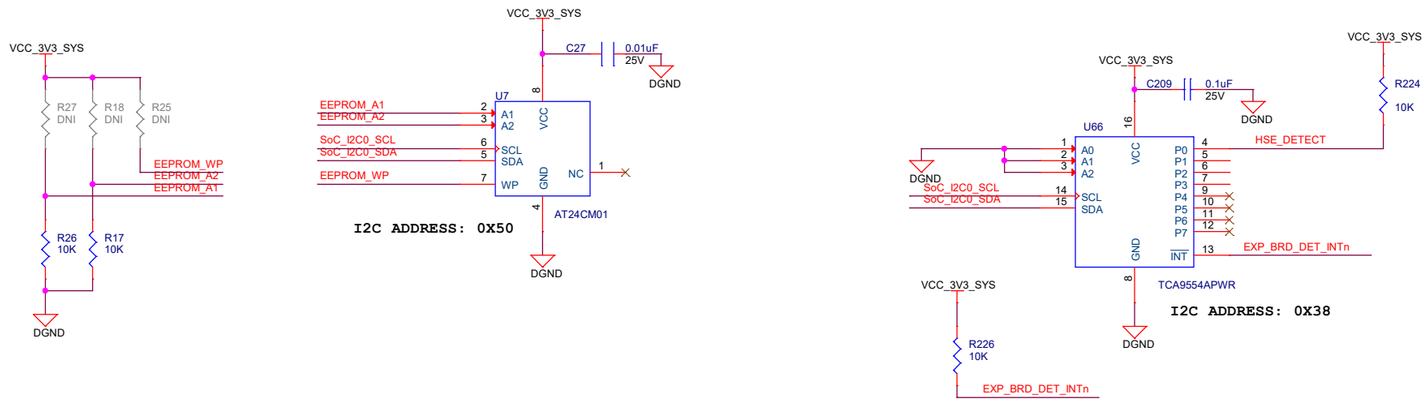


Cad Note :- PLACE TEMP SENSOR CLOSE TO SoC

Cad Note :- PLACE TEMP SENSOR CLOSE TO CORE POWER SECTION

BOARD ID EEPROM

BOARD PRESENCE DETECT CIRCUIT



Off Page Connections

HSE_DETECT — HSE_DETECT [27]

SoC_I2C1_SDA, SoC_I2C1_SCL — SoC_I2C1_SDA [19,21,29,30,31,32,33], SoC_I2C1_SCL [19,21,29,30,31,32,33]

SoC_I2C0_SDA, SoC_I2C0_SCL — SoC_I2C0_SDA [27,29,33], SoC_I2C0_SCL [27,29,33]

Designed for TI by Mistral Solutions Pvt Ltd

Title	EEPROM,PRESENCE DETECTION & TEMP SENSOR	
Size: C	Variant Name = PROC101D(004) TMDS64EVM	Rev: D
Date: Wednesday, June 12, 2024	Sheet 15 of 40	

CPSW3G RGMII 1 - ETHERNET PHY

Decaps

VDD_1V0: C51 0.1uF 25V, C39 0.1uF 25V, C41 0.1uF 25V, C36 0.1uF 25V, C259 1uF 10V, C253 1uF 10V, C274 1uF 10V, C238 1uF 10V, C263 10uF 10V → DGND

VCC_3V3_SYS: C275 0.1uF 25V, C44 0.1uF 25V, C35 0.1uF 25V, C52 1uF 10V, C266 1uF 10V, C237 1uF 10V, C281 10uF 10V → DGND

VDD_2V5: C38 0.1uF 25V, C43 0.1uF 25V, C249 1uF 10V, C261 1uF 10V, C258 10uF 10V → DGND

D-Note :-
The caps and values used are as per the EPHY data sheet recommendations

D-Note :-
Add 10 nF cap for each supply rail Refer EPHY data sheet

D-Note :-
Provide provision for Series resistor based on EPHY for RX signals near to EPHY

D-Note :-
XI clock Input amplitude allowed is 1.8V irrespective of the IO supply Use a CAP DIVIDER when the clock amplified is 3.3V

D-Note :-
VDDA1P8
These are LDO outputs Do not short. Add individual TPs for testing

D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

U15 DP83867IRRGZ

CPSW_RGMII1_TD0	28	TX_D0
CPSW_RGMII1_TD1	27	TX_D1
CPSW_RGMII1_TD2	26	TX_D2
CPSW_RGMII1_TD3	25	TX_D3
CPSW_RGMII1_TXC	29	GTX_CLK
CPSW_RGMII1_TX_CTL	37	TX_EN/TX_CTRL
CPSW_RGMII1_RD0	33	RX_D0
CPSW_RGMII1_RD1	34	RX_D1
CPSW_RGMII1_RD2	35	RX_D2
CPSW_RGMII1_RD3	36	RX_D3
CPSW_RGMII1_RXC	32	RX_CLK
CPSW_RGMII1_RX_CTL	38	RX_DV/RX_CTRL
CPSW_RGMII1_ETH1_CLK	15	XI
	14	XO
	20	JTAG_CLK
	22	JTAG_TMS
	23	JTAG_TDI
	21	JTAG_TDO
CPSW_RGMII1_ETH1_CLK_OUT	18	CLK_OUT
CPSW_RGMII1_MDC	16	MDC
CPSW_RGMII1_MDIO	17	MDIO
CPSW_RGMII_INTn	44	INT/PWDN
CPSW_RGMII1_ETH1_RBIAS	12	RBIAS
CPSW_RGMII1_RESETn	43	RESET_N

VCC_3V3_SYS, TP11, VDD_2V5, VDD_1V0 → VDDIO (19, 33, 41), VDDA1P8 (13, 48), VDDA2P5 (3, 9), VDD1P0 (6, 24, 31, 42)

TD_P_A	1	CPSW_ETH1_D0P
TD_M_A	2	CPSW_ETH1_D0M
TD_P_B	4	CPSW_ETH1_D1P
TD_M_B	5	CPSW_ETH1_D1M
TD_P_C	7	CPSW_ETH1_D2P
TD_M_C	8	CPSW_ETH1_D2M
TD_P_D	10	CPSW_ETH1_D3P
TD_M_D	11	CPSW_ETH1_D3M
LED_0	47	CPSW_ETH1_LED0
LED_1	46	CPSW_ETH1_LED_1000
LED_2	45	CPSW_ETH1_LED_ACT
GPIO_0	39	CPSW_ETH1_GPIO_0
GPIO_1	40	CPSW_ETH1_GPIO_1

TP9, GND → 49 → DGND

TP16, R81 DNI, R79 2.2K, R42 2.2K, R70 10K 1% → DGND

D-Note :-
Add a parallel 22 pF cap These changes are for Ethernet compliance test performance improvement

PRG1_RGMII_INTn — R250 0E — CPSW_RGMII_INTn

RJ45 with Integrated Mangnetics

VCC_3V3_SYS — FB26 — DNI

R-Note :-
Ferrite is DNI

J14

CPSW_ETH1_D0P	9	J1
CPSW_ETH1_D0M	10	J2
CPSW_ETH1_D1P	7	J3
CPSW_ETH1_D1M	8	J6
CPSW_ETH1_D2P	5	J4
CPSW_ETH1_D2M	6	J5
CPSW_ETH1_D3P	3	J7
CPSW_ETH1_D3M	4	J8
	1	
	2	
	SH1 15	
	SH2 16	

D-Note :-
Refer to DP83867ERGZ-R-EVM when using LAN Discrete Transformer Module and RJ45 connector

VCC_3V3_SYS → R76 220E → CPSW_ETH1_LED1 (11), CPSW_ETH1_LED2 (12), CPSW_ETH1_LED3 (13), (14)

YELLOW / GREEN — RIGHT LED

YELLOW / GREEN — LEFT LED

CON_RJ45-14_LPJG16314A4NL

C287 1000pF 2KV, R299 1M → CPSW_EARTH, DGND

STRAPPING RESISTORS

VCC_3V3_SYS

R56	R51	R39	R32	R33	R41	R35	
DNI	DNI	5.76K_1%	DNI	DNI	DNI	DNI	
R54	R52	R249	R31	R34	R251	R36	
DNI	DNI	2.49K_1%	DNI	DNI	DNI	DNI	

CPSW_RGMII1_RD0, CPSW_RGMII1_RD2, CPSW_RGMII1_RX_CTL, CPSW_ETH1_LED_1000, CPSW_ETH1_LED_ACT, CPSW_ETH1_GPIO_0, CPSW_ETH1_GPIO_1

PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx & Rx Clock Skew = 2.0ns

CPSW_ETHERNET PHY- 1 SPEED & ACTIVITY LED 's DRIVERS

CPSW_ETH1_LED1 — Q13 — R286 0E — CPSW_ETH1_LED_ACT — BSS138LT1G

VCC_3V3_SYS — R234 220E — CPSW_ETH1_LED2 — Q12 — R230 0E — CPSW_ETH1_GPIO_0 — BSS138LT1G

VCC_3V3_SYS — R37 220E — CPSW_ETH1_LED3 — Q3 — R30 0E — CPSW_ETH1_LED_1000 — BSS138LT1G

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation

CPSW3G EPHY - 1 RESET

VCC_3V3_SYS, VCC_3V3_SYS — R242 10K, C220 0.1uF 25V → DGND

[16,33] GPIO_CPSW1_RST, PORz_OUT → U69 SN74LVC1G08DBVRE4 → CPSW_RGMII1_RESETn

R241 DNI, R240 10K → DGND

CPSW RGMII 1 ETHERNET PHY SIGNALS & HSE CON SIGNALS

VCC_3V3_SYS — C276 0.1uF 25V, C284 0.1uF 25V, C260 0.1uF 25V → DGND

U75 TS3DDR3812RUAR

PRG0_PRU1_GPO7/CPSW_RGMII1_RD0	2	A0	B0 41 CPSW_RGMII1_RD0
PRG0_PRU1_GPO9/CPSW_RGMII1_RD1	3	A1	B1 39 CPSW_RGMII1_RD1
PRG0_PRU1_GPO10/CPSW_RGMII1_RD2	4	A2	B2 38 CPSW_RGMII1_RD2
PRG0_PRU1_GPO17/CPSW_RGMII1_RD3	5	A3	B3 36 CPSW_RGMII1_RD3
PRG0_PRU0_GPO9/CPSW_RGMII1_RX_CTL	6	A4	B4 34 CPSW_RGMII1_RX_CTL
PRG0_PRU0_GPO10/CPSW_RGMII1_RXC	7	A5	B5 32 CPSW_RGMII1_RXC
			C0 42 HSE_PRG0_PRU1_GPO7
			C1 40 HSE_PRG0_PRU1_GPO9
			C2 37 HSE_PRG0_PRU1_GPO10
			C3 35 HSE_PRG0_PRU1_GPO17
			C4 33 HSE_PRG0_PRU0_GPO9
			C5 31 HSE_PRG0_PRU0_GPO10
	11	A6	B6 29
	12	A7	B7 27
	13	A8	B8 25
	14	A9	B9 23
	15	A10	B10 21
	16	A11	B11 19
			C6 28
			C7 26
			C8 24
			C9 22
			C10 20
			C11 18
CPSW_FET_EN	8	EN	
CPSW_FET_SEL	9	SEL1	
	10	SEL2	
	1, 17, 30	VCC	
	43	GND	

VCC_3V3_SYS — R278 10K — CPSW_FET_EN; R292 10K → DGND

D-Note :-
Terminate unused IOs

TS3DDR3812RUAR Truth Table

EN	SEL1	SEL2	FUNCTION
L	X	X	A0 to A11, B0 to B11, and C0 to C11 are Hi-Z
H	L	L	A0 to A5 = B0 to B5 and A6 to A11 = B6 to B11
H	L	H	A0 to A5 = B0 to B5 and A6 to A11 = C6 to C11
H	H	L	A0 to A5 = C0 to C5 and A6 to A11 = B6 to B11
H	H	H	A0 to A5 = C0 to C5 and A6 to A11 = C6 to C11

Off Page Connections

From Processor

[27]	PRG0_PRU1_GPO7/CPSW_RGMII1_RD0	PRG0_PRU1_GPO7/CPSW_RGMII1_RD0
[27]	PRG0_PRU1_GPO9/CPSW_RGMII1_RD1	PRG0_PRU1_GPO9/CPSW_RGMII1_RD1
[27]	PRG0_PRU1_GPO10/CPSW_RGMII1_RD2	PRG0_PRU1_GPO10/CPSW_RGMII1_RD2
[27]	PRG0_PRU1_GPO17/CPSW_RGMII1_RD3	PRG0_PRU1_GPO17/CPSW_RGMII1_RD3
[27]	PRG0_PRU0_GPO9/CPSW_RGMII1_RX_CTL	PRG0_PRU0_GPO9/CPSW_RGMII1_RX_CTL
[27]	PRG0_PRU0_GPO10/CPSW_RGMII1_RXC	PRG0_PRU0_GPO10/CPSW_RGMII1_RXC

From Processor

[27]	CPSW_RGMII1_TD0	CPSW_RGMII1_TD0
[27]	CPSW_RGMII1_TD1	CPSW_RGMII1_TD1
[27]	CPSW_RGMII1_TD2	CPSW_RGMII1_TD2
[27]	CPSW_RGMII1_TD3	CPSW_RGMII1_TD3
[27]	CPSW_RGMII1_TX_CTL	CPSW_RGMII1_TX_CTL
[27]	CPSW_RGMII1_TXC	CPSW_RGMII1_TXC
[13,17,18,20,34]	PORz_OUT	PORz_OUT
[17,18,34]	PRG1_RGMII_INTn	PRG1_RGMII_INTn

From IO Expander

[16,33]	GPIO_CPSW1_RST	GPIO_CPSW1_RST
[33]	CPSW_FET_SEL	CPSW_FET_SEL

From Clock Buffer

[31]	CPSW_RGMII1_ETH1_CLK	CPSW_RGMII1_ETH1_CLK

To HSE Connector

[27]	HSE_PRG0_PRU1_GPO7	HSE_PRG0_PRU1_GPO7
[27]	HSE_PRG0_PRU1_GPO9	HSE_PRG0_PRU1_GPO9
[27]	HSE_PRG0_PRU1_GPO10	HSE_PRG0_PRU1_GPO10
[27]	HSE_PRG0_PRU1_GPO17	HSE_PRG0_PRU1_GPO17
[27]	HSE_PRG0_PRU0_GPO9	HSE_PRG0_PRU0_GPO9
[27]	HSE_PRG0_PRU0_GPO10	HSE_PRG0_PRU0_GPO10

From Processor

[17,27]	CPSW_RGMII1_MDIO	CPSW_RGMII1_MDIO
[17,27]	CPSW_RGMII1_MDC	CPSW_RGMII1_MDC

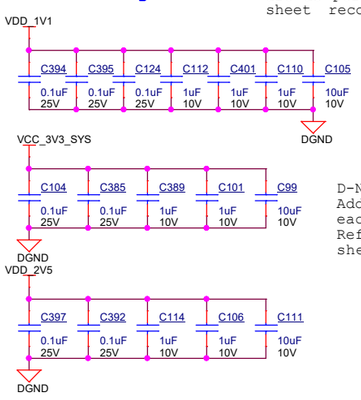
Designed for TI by Mistral Solutions Pvt Ltd

Title	CPSW RGMII_1 ETHERNET PHY	
Size C	Variant Name = PROC101D(004) TMDS64EVM	Rev D
Date: Wednesday, June 12, 2024	Sheet 16 of 40	

ICSSG RGMII 2 - ETHERNET PHY

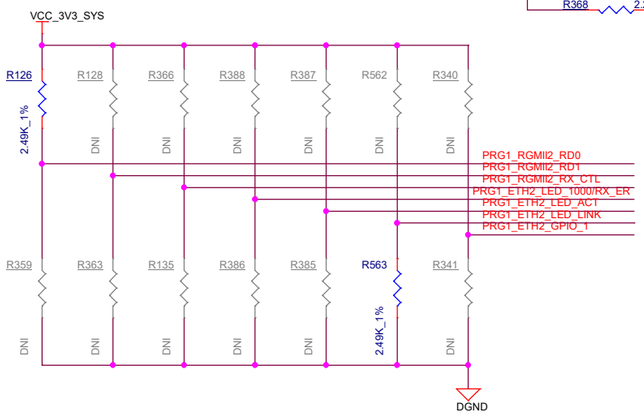
Decaps

D-Note :-
The caps and values used are as per the EPHY data sheet recommendations

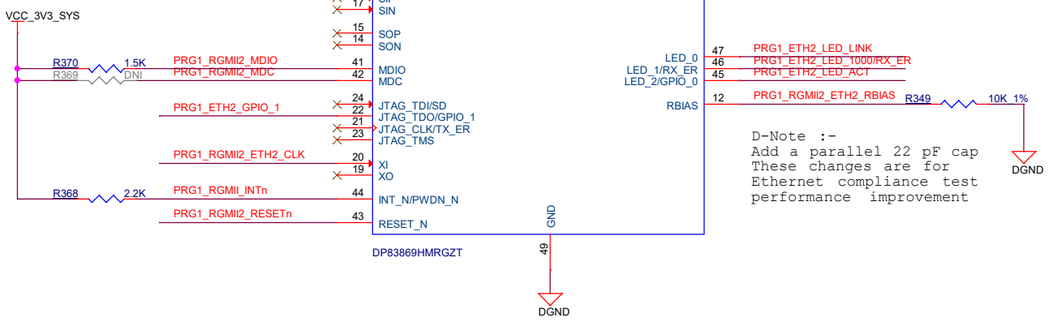


D-Note :-
Add 10 nF cap for each supply rail
Refer EPHY data sheet

STRAPPING RESISTORS



PHY_ADDRESS = 00011
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X
RGMII to Copper (1000BaseT/100Base-TX/10Base-Te)

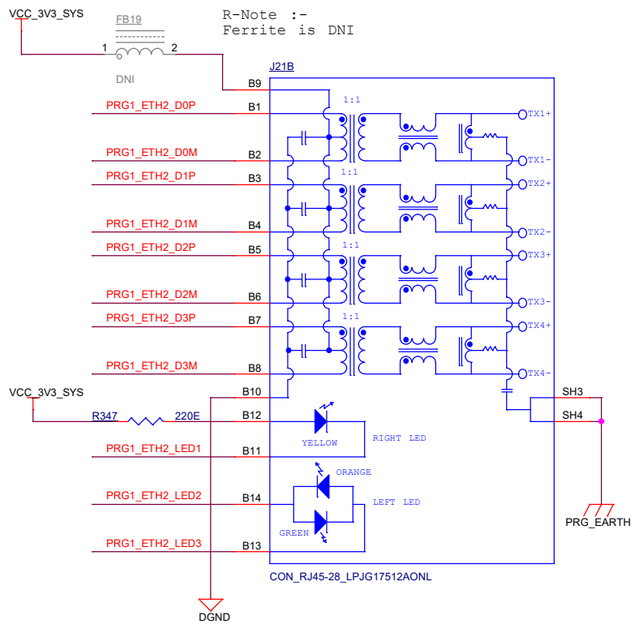


D-Note :-
VDDA1P8
These are LDO outputs
Do not short. Add individual TPs for testing

D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

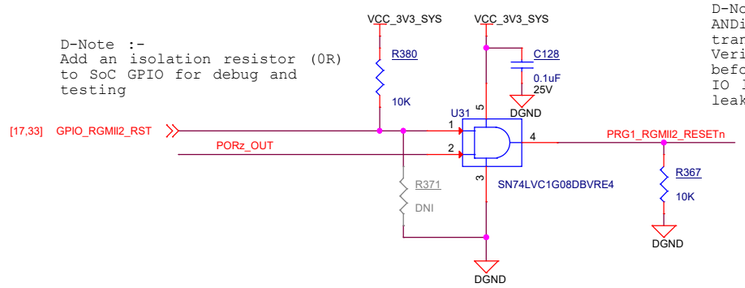
D-Note :-
Add a parallel 22 pF cap
These changes are for Ethernet compliance test performance improvement

Dual RJ45 CON With Integrated Magnetics



D-Note :-
Refer to DP83867ERGZ-R-EVM when using LAN Discrete Transformer Module and RJ45 connector

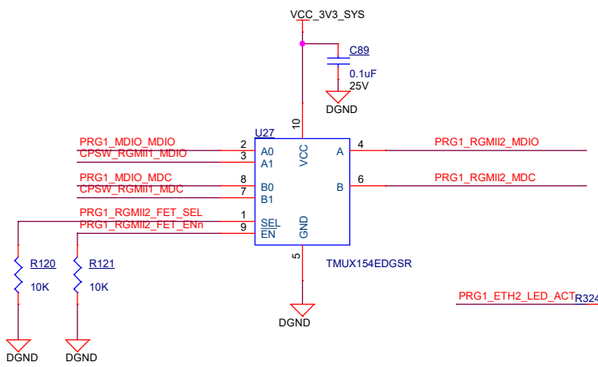
PRG1 (ICSSG) ETH2 RESET



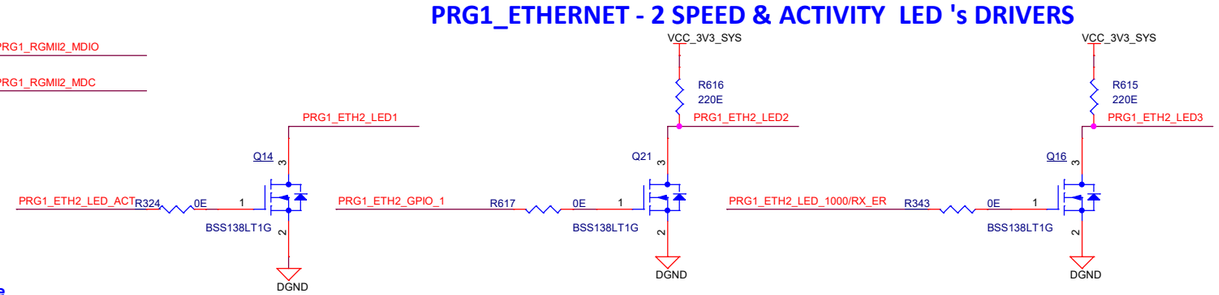
D-Note :-
Add an isolation resistor (0R) to SoC GPIO for debug and testing

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation

PRG1 MDC/MDIO FET SWITCH



PRG1_ETHERNET - 2 SPEED & ACTIVITY LED 's DRIVERS



TMUX154EDGSR Truth Table

SEL	$\overline{EN}$	FUNCTION
X	H	Disconnet
L	L	A = A0 B = B0
H	L	A = A1 B = B1

Off Page Connections

To Processor	[16,18,34] PRG1_RGMII_INTn	PRG1_RGMII_INTn
	[27] PRG1_RGMII2_RD0	PRG1_RGMII2_RD0
	[27] PRG1_RGMII2_RD1	PRG1_RGMII2_RD1
	[27] PRG1_RGMII2_RD2	PRG1_RGMII2_RD2
	[27] PRG1_RGMII2_RD3	PRG1_RGMII2_RD3
	[27] PRG1_RGMII2_RXC	PRG1_RGMII2_RXC
	[27] PRG1_RGMII2_RX_CTL	PRG1_RGMII2_RX_CTL
	[27] PRG1_ETH2_LED_LINK	PRG1_ETH2_LED_LINK
	[27] PRG1_ETH2_LED_1000/RX_ER	PRG1_ETH2_LED_1000/RX_ER
From Processor	[27] PRG1_RGMII2_TD0	PRG1_RGMII2_TD0
	[27] PRG1_RGMII2_TD1	PRG1_RGMII2_TD1
	[27] PRG1_RGMII2_TD2	PRG1_RGMII2_TD2
	[27] PRG1_RGMII2_TD3	PRG1_RGMII2_TD3
	[27] PRG1_RGMII2_TXC	PRG1_RGMII2_TXC
	[27] PRG1_RGMII2_TX_CTL	PRG1_RGMII2_TX_CTL
	[13,16,18,20,34] PORz_OUT	PORz_OUT
	[18,27] PRG1_MDIO_MDIO	PRG1_MDIO_MDIO
	[18,27] PRG1_MDIO_MDC	PRG1_MDIO_MDC
From CPSW	[16,27] CPSW_RGMII1_MDIO	CPSW_RGMII1_MDIO
	[16,27] CPSW_RGMII1_MDC	CPSW_RGMII1_MDC
From IO Expander	[17,33] GPIO_RGMII2_RST	GPIO_RGMII2_RST
	[33] PRG1_RGMII2_FET_SEL	PRG1_RGMII2_FET_SEL
From Clock Buffer	[31] PRG1_RGMII2_ETH2_CLK	PRG1_RGMII2_ETH2_CLK

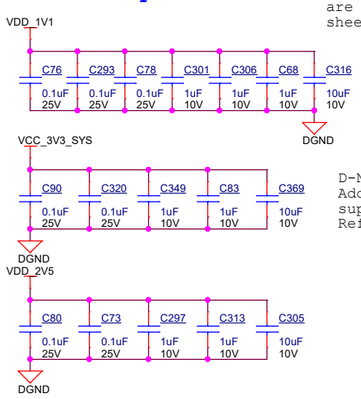
Designed for TI by Mistral Solutions Pvt Ltd

Title	ICSSG1 RGMII_2 ETHERNET PHY	
Size C	Variant Name = PROC101D(004) TMDS64EVM	Rev D
Date: Wednesday, June 12, 2024	Sheet 17 of 40	

ICSSG RGMII 1 - ETHERNET PHY

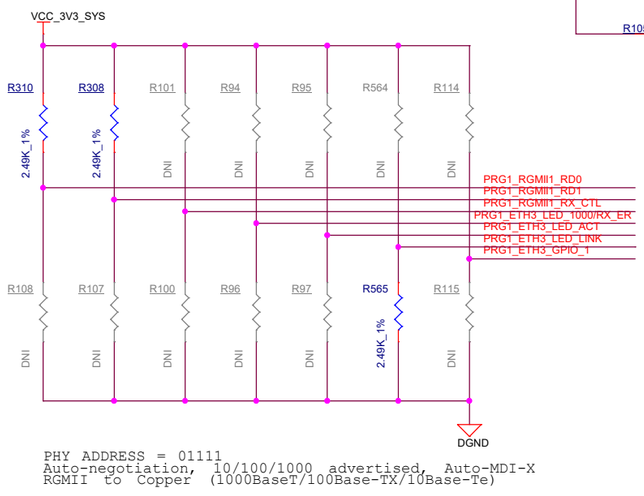
Decaps

D-Note :-
The caps and values used are as per the EPHY data sheet recommendations



D-Note :-
Add 10 nF cap for each supply rail
Refer EPHY data sheet

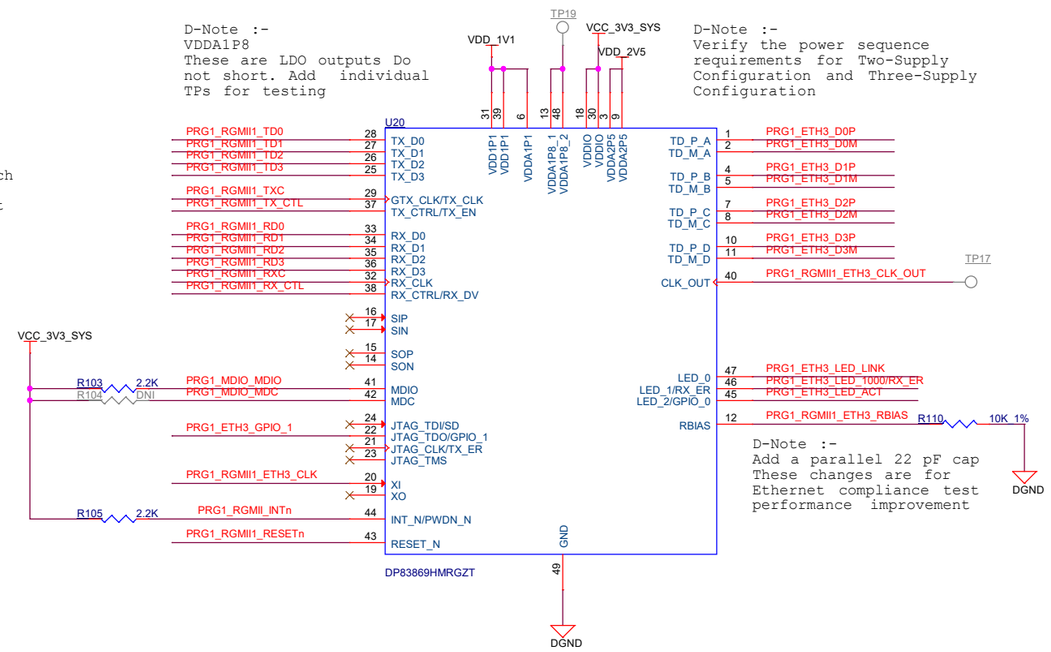
STRAPPING RESISTORS



PHY ADDRESS = 01111
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X
RGMII to Copper (1000BaseT/100Base-TX/10Base-Te)

D-Note :-
VDDA1P8
These are LDO outputs Do not short. Add individual TPs for testing

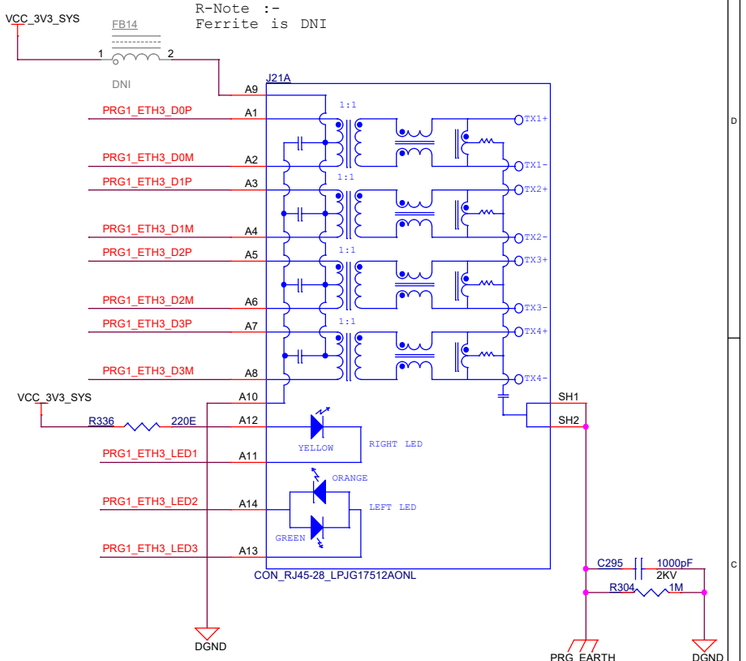
D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration



D-Note :-
Add a parallel 22 pF cap These changes are for Ethernet compliance test performance improvement

Dual RJ45 CON With Integrated Magnetics

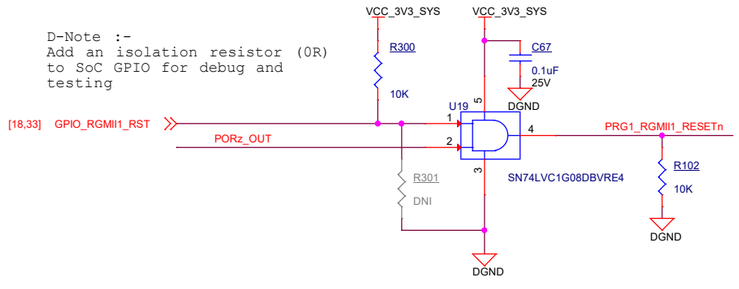
R-Note :-
Ferrite is DNI



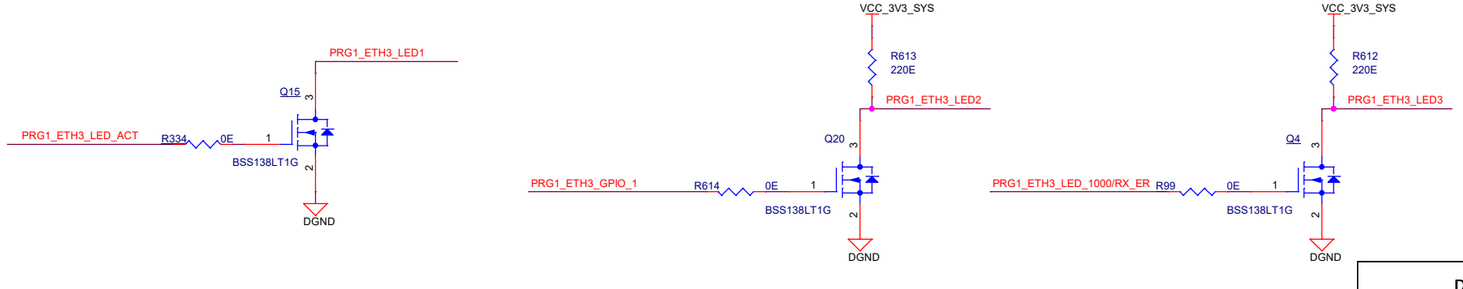
PRG1 (ICSSG) ETH1 RESET

D-Note :-
Add an isolation resistor (0R) to SoC GPIO for debug and testing

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation



PRG1_ETHERNET - 3 SPEED & ACTIVITY LED 's DRIVERS



Off Page Connections

To Processor	[16,17,34]	PRG1_RGMII_INTn	PRG1_RGMII_INTn
	[27]	PRG1_RGMII1_RD0	PRG1_RGMII1_RD0
	[27]	PRG1_RGMII1_RD1	PRG1_RGMII1_RD1
	[27]	PRG1_RGMII1_RD2	PRG1_RGMII1_RD2
	[27]	PRG1_RGMII1_RD3	PRG1_RGMII1_RD3
	[27]	PRG1_RGMII1_RXC	PRG1_RGMII1_RXC
	[27]	PRG1_RGMII1_RX_CTL	PRG1_RGMII1_RX_CTL
	[13,16,17,20,34]	PORz_OUT	PORz_OUT
	[27]	PRG1_ETH3_LED_LINK	PRG1_ETH3_LED_LINK
	[27]	PRG1_ETH3_LED_1000/RX_ER	PRG1_ETH3_LED_1000/RX_ER
From Processor	[27]	PRG1_RGMII1_TD0	PRG1_RGMII1_TD0
	[27]	PRG1_RGMII1_TD1	PRG1_RGMII1_TD1
	[27]	PRG1_RGMII1_TD2	PRG1_RGMII1_TD2
	[27]	PRG1_RGMII1_TD3	PRG1_RGMII1_TD3
	[27]	PRG1_RGMII1_TXC	PRG1_RGMII1_TXC
	[27]	PRG1_RGMII1_TX_CTL	PRG1_RGMII1_TX_CTL
From Processor (MDC & MDIO Pins are common to both ICSSG PHY, This to be verified)	[17,27]	PRG1_MDIO_MDIO	PRG1_MDIO_MDIO
	[17,27]	PRG1_MDIO_MDC	PRG1_MDIO_MDC
From IO Expander	[18,33]	GPIO_RGMII1_RST	GPIO_RGMII1_RST
From Clock Buffer	[31]	PRG1_RGMII1_ETH3_CLK	PRG1_RGMII1_ETH3_CLK

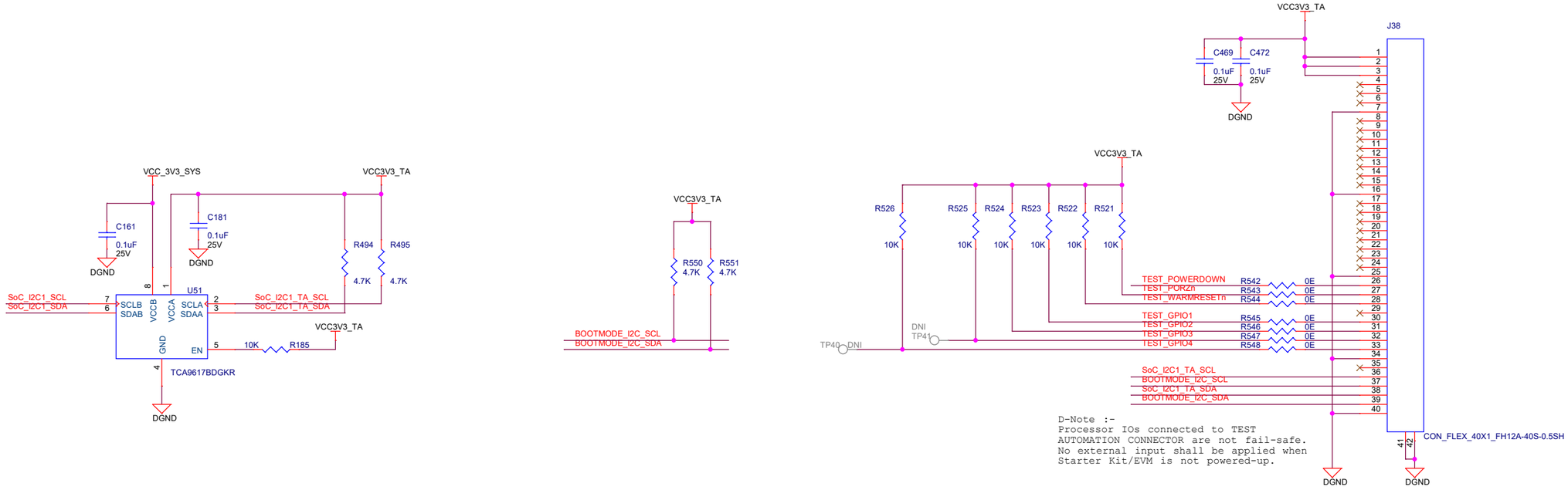
Designed for TI by Mistral Solutions Pvt Ltd

Title	ICSSG2 RGMII_1 ETHERNET PHY	
Size	Variant Name = PROC101D(004) TMDS64EVM	Rev
C		D
Date: Wednesday, June 12, 2024	Sheet 18 of 40	

TEST AUTOMATION

D-Note :-
Refer SK-AM62P-LP implementation for the latest updates

40-PIN AUTOMATION HEADER



D-Note :-
Processor IOs connected to TEST AUTOMATION CONNECTOR are not fail-safe. No external input shall be applied when Starter Kit/EVM is not powered-up.

TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on GPIO0_13_INTn Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to I/O Expander to Communicate with SoC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

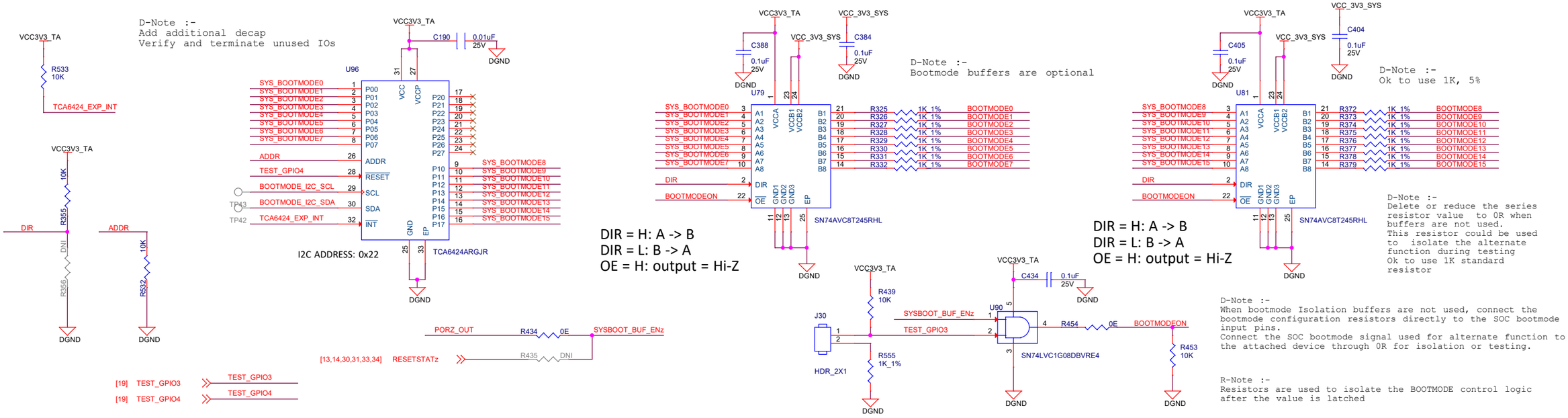
Off Page Connections

To Processor	[15,21,29,30,31,32,33] SoC_I2C1_SCL [15,21,29,30,31,32,33] SoC_I2C1_SDA	SoC_I2C1_SCL SoC_I2C1_SDA
To Bootmode Buffer	[20] BOOTMODE_I2C_SCL [20] BOOTMODE_I2C_SDA	BOOTMODE_I2C_SCL BOOTMODE_I2C_SDA
To Debounce Ckt	[35] TEST_PORZn	TEST_PORZn
To High Side SW	[37] TEST_POWERDOWN	TEST_POWERDOWN
To Debounce Ckt	[35] TEST_WARMRESETn	TEST_WARMRESETn
To Debounce Ckt	[35] TEST_GPIO1	TEST_GPIO1
To IO Expander	[33] TEST_GPIO2	TEST_GPIO2
To EN Boot Mode Buffer	[20] TEST_GPIO3	TEST_GPIO3
To RST Boot Mode Buffer	[20] TEST_GPIO4	TEST_GPIO4

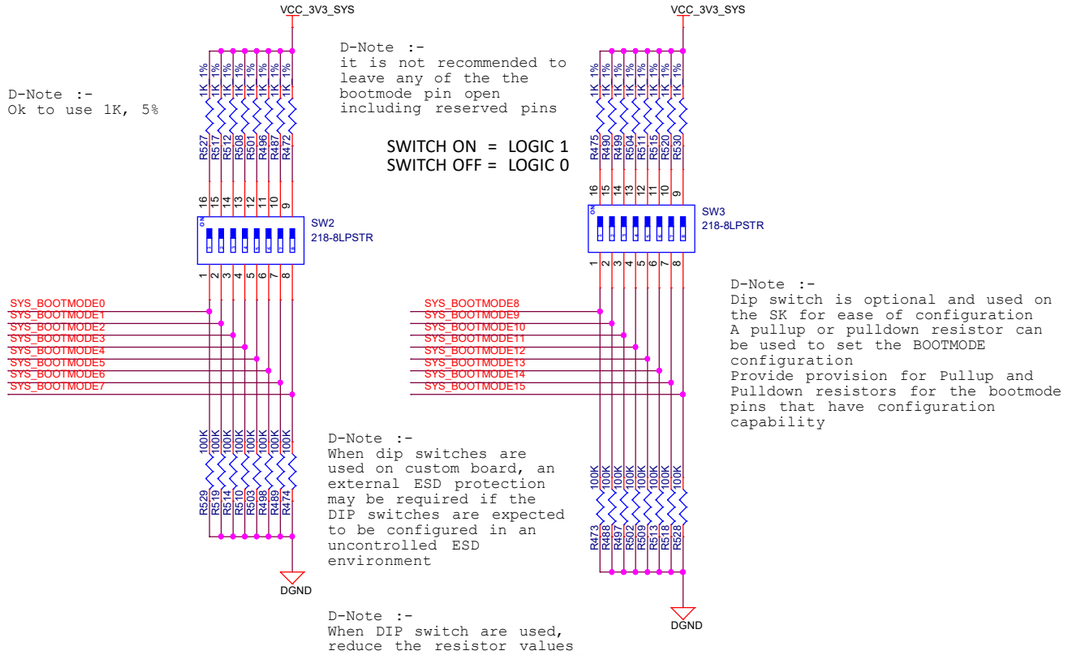
Designed for TI by Mistral Solutions Pvt Ltd

Title	TEST AUTOMATION	
Size: C	Variant Name = PROC101D(004) TMDS64EVM	Rev: D
Date: Wednesday, June 12, 2024	Sheet 19 of 40	

BOOT MODE BUFFER & DIP SWITCHES



BOOTMODE CONFIGURATION RESISTORS AND BOOTMODE SWITCHES



BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. MMC0 - eMMC
4. CPSW Ethernet Slave
5. USB Host
6. USB Device
7. UART
8. Ethernet

Off Page Connections

From Processor

[28] BOOTMODE0 → BOOTMODE0
[28] BOOTMODE1 → BOOTMODE1
[28] BOOTMODE2 → BOOTMODE2
[28] BOOTMODE3 → BOOTMODE3
[28] BOOTMODE4 → BOOTMODE4
[28] BOOTMODE5 → BOOTMODE5
[28] BOOTMODE6 → BOOTMODE6
[28] BOOTMODE7 → BOOTMODE7
[28] BOOTMODE8 → BOOTMODE8
[28] BOOTMODE9 → BOOTMODE9
[28] BOOTMODE10 → BOOTMODE10
[28] BOOTMODE11 → BOOTMODE11
[28] BOOTMODE12 → BOOTMODE12
[28] BOOTMODE13 → BOOTMODE13
[28] BOOTMODE14 → BOOTMODE14
[28] BOOTMODE15 → BOOTMODE15
[13,16,17,18,34] PORz_OUT → PORz_OUT

From Test Automation Header

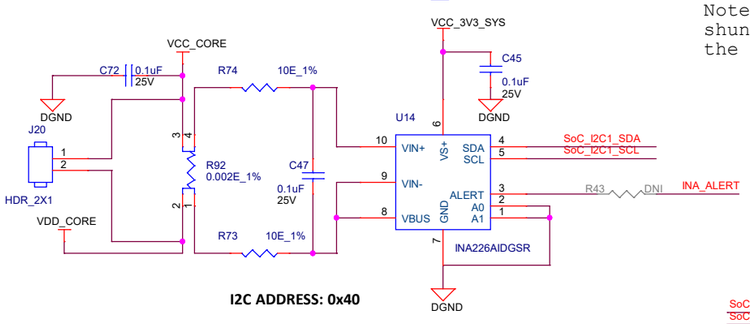
[19] BOOTMODE_I2C_SCL → BOOTMODE_I2C_SCL
[19] BOOTMODE_I2C_SDA → BOOTMODE_I2C_SDA

Designed for TI by Mistral Solutions Pvt Ltd

Title	BOOT MODE BUFFER & SWITCHES	
Size C	Variant Name = PROC101D(004) TMDS64EVM	Rev D
Date: Wednesday, June 12, 2024	Sheet 20 of 40	

CURRENT MONITORING DEVICES

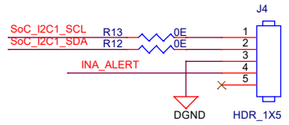
VDD_CORE



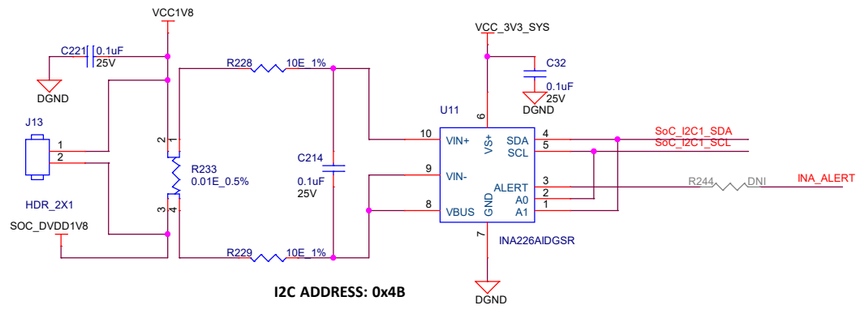
I2C ADDRESS: 0x40

D-Note :-
Note the supply rail name change across the shunt when optimizing the design (Deleting the current sense)

CAD Note :-
Follow Kelvin connection for Current Sensing when using 2 terminal resistors

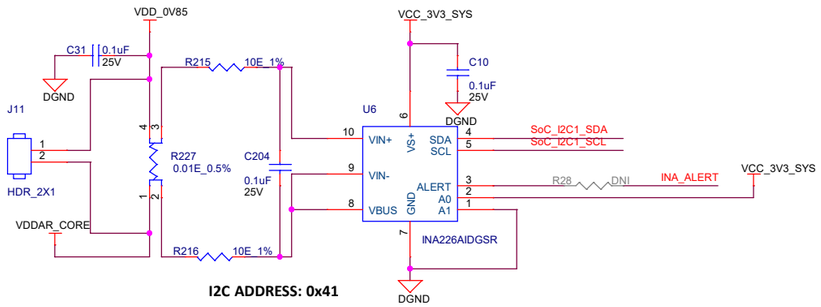


SoC_DVDD1V8



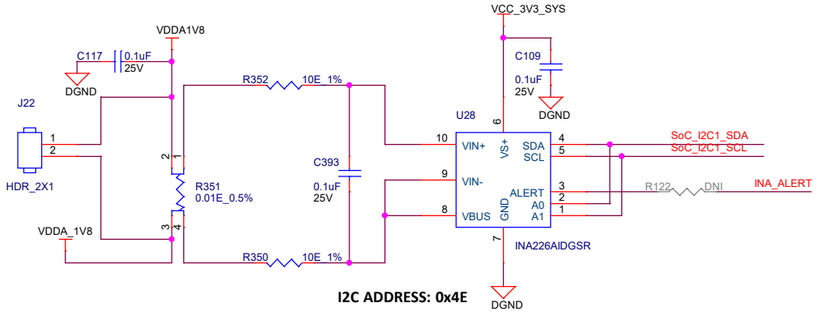
I2C ADDRESS: 0x4B

VDDAR_CORE



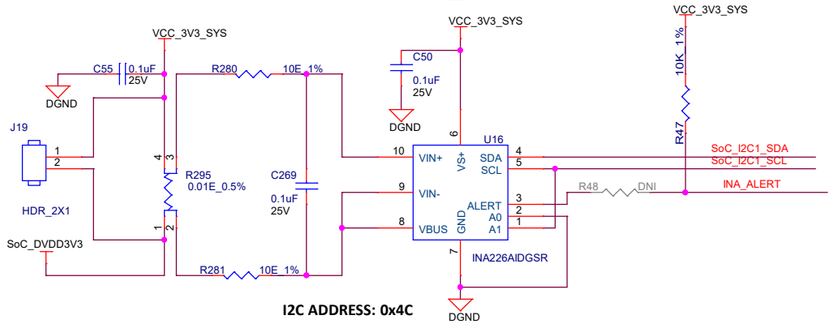
I2C ADDRESS: 0x41

VDDA_1V8



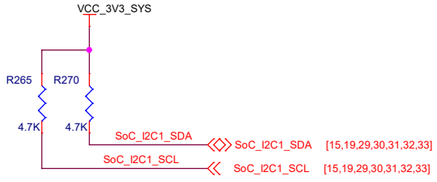
I2C ADDRESS: 0x4E

SoC_DVDD3V3

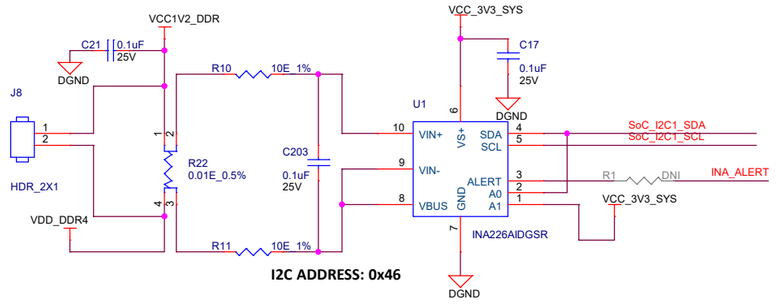


I2C ADDRESS: 0x4C

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VDD_0V85	VDDAR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8	SoC_DVDD1V8	4B
VDDA1V8	VDDA_1V8	4E
VCC1V2_DDR	VDD_DDR4	46



VDD_DDR4



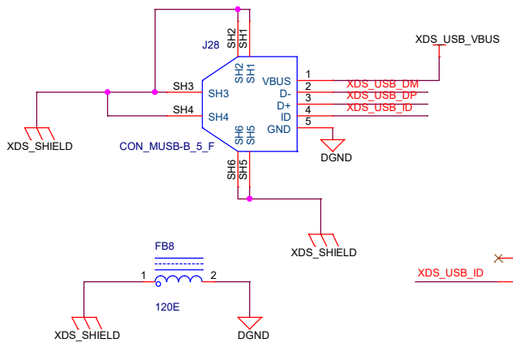
I2C ADDRESS: 0x46

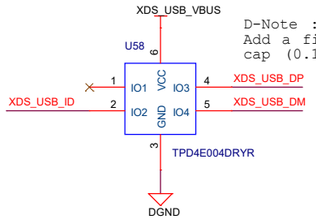
Designed for TI by Mistral Solutions Pvt Ltd

Title	CURRENT MONITORING DEVICES	
Size C	Variant Name = PROC101D(004) TMDS64EVM	Rev D
Date: Wednesday, June 12, 2024	Sheet 21 of 40	

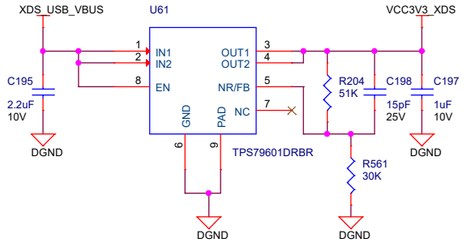
XDS110 POWER

USB Connector



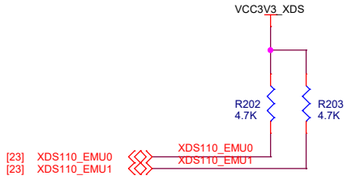


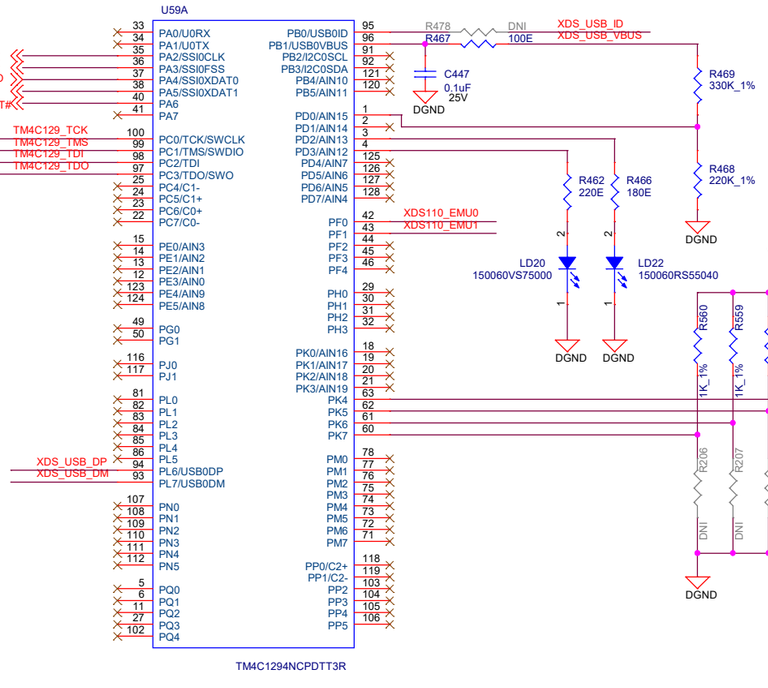
D-Note :-
Add a filter cap (0.1uF)



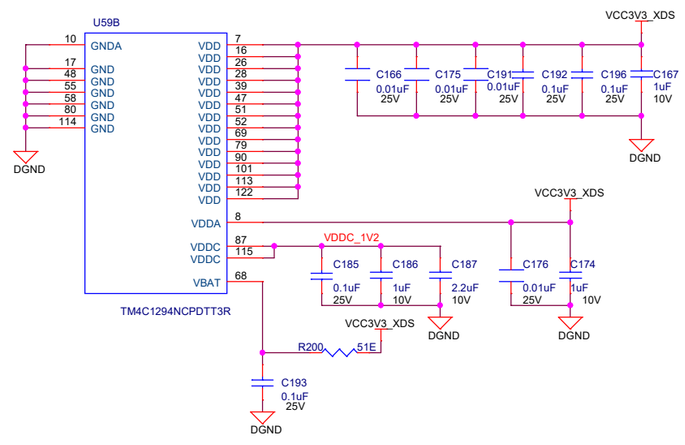
D-Note :-
Please follow SK-AM62P-LP EVM implementations for latest updates on XDS110

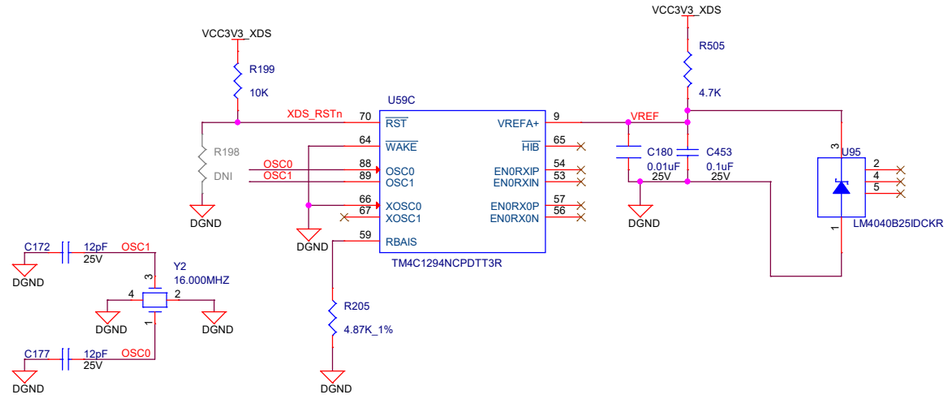
XDS110 DEBUGGER





This will indicate the unique ID of the Debugger



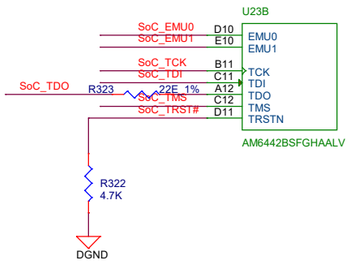


Designed for TI by Mistral Solutions Pvt Ltd

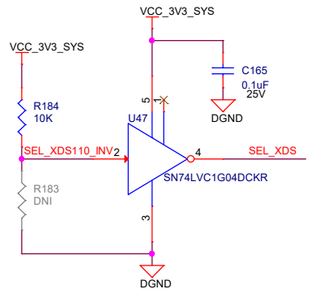
Title	XDS110 DEBUGGER	
Size: C	Variant Name = PROC101D(004) TMDS64EVM	Rev: D
Date: Wednesday, June 12, 2024	Sheet 22 of 40	

JTAG BUFFER

JTAG SoC SECTION

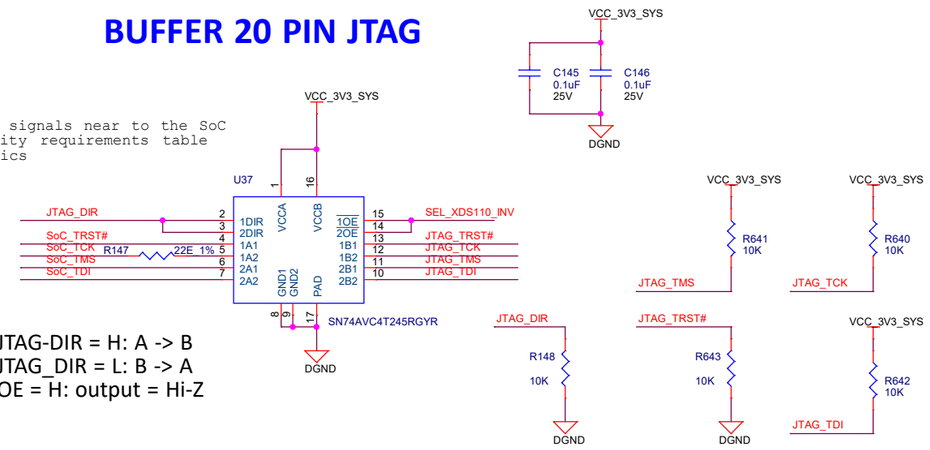


D-Note :-
Place pulls on JTAG
signals near to the SoC
Refer AM62P schematics



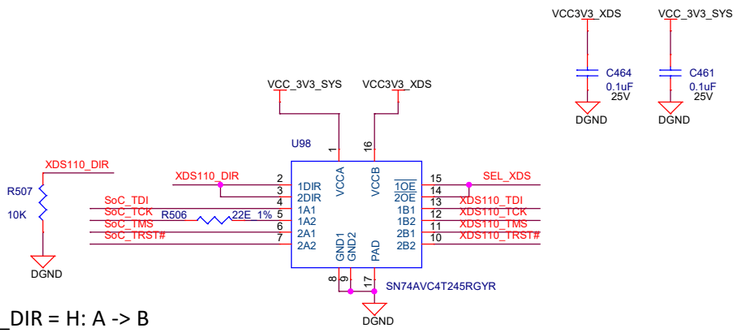
BUFFER 20 PIN JTAG

D-Note :-
Place pulls on JTAG signals near to the SoC
Refer Pin connectivity requirements table
Refer AM62P schematics

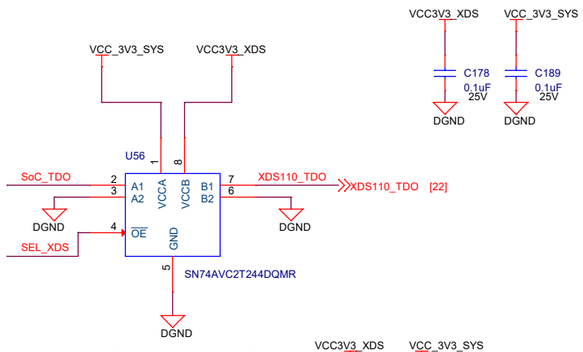


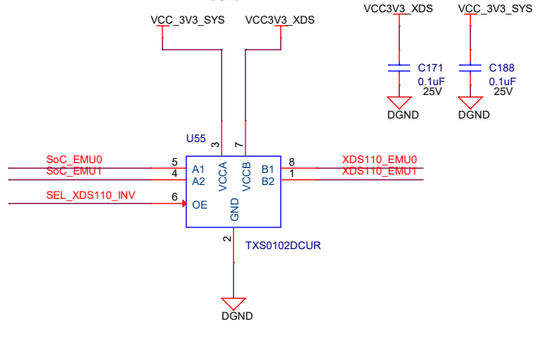
JTAG-DIR = H: A -> B
JTAG_DIR = L: B -> A
OE = H: output = Hi-Z

BUFFER XDS110

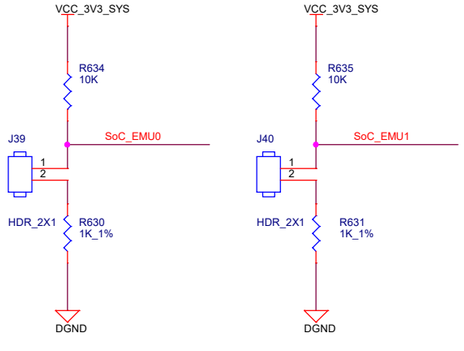


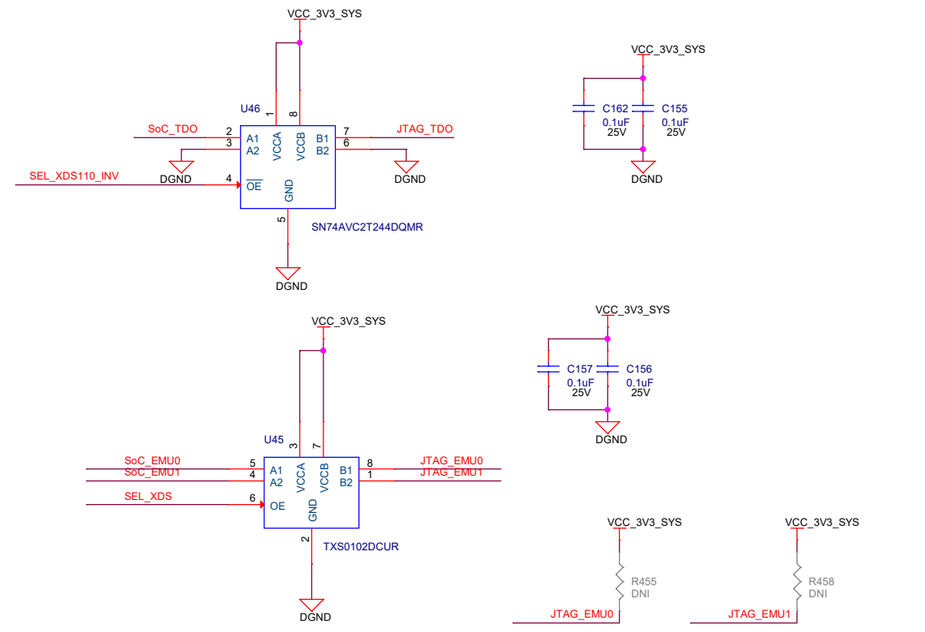
XDS110_DIR = H: A -> B
XDS110_DIR = L: B -> A
OE = H: output = Hi-Z





Placement of Buffers U37, U46, U56 and U98
to be changed to reduce
Stub length of the JTAG signals.
These buffers need to be placed closer
to the cTI-20pin connector -J25





Off Page Connections

From XDS1100 Debugger

[24] SEL_XDS110_INV		SEL_XDS110_INV
[24] JTAG_EMU0		JTAG_EMU0
[24] JTAG_EMU1		JTAG_EMU1
[22] XDS110_TDI		XDS110_TDI
[22] XDS110_TCK		XDS110_TCK
[22] XDS110_TMS		XDS110_TMS
[22] XDS110_TRST#		XDS110_TRST#
[24] JTAG_TDI		JTAG_TDI
[24] JTAG_TCK		JTAG_TCK
[24] JTAG_TMS		JTAG_TMS
[24] JTAG_TRST#		JTAG_TRST#
[24] JTAG_TDO		JTAG_TDO
[22] XDS110_EMU0		XDS110_EMU0
[22] XDS110_EMU1		XDS110_EMU1

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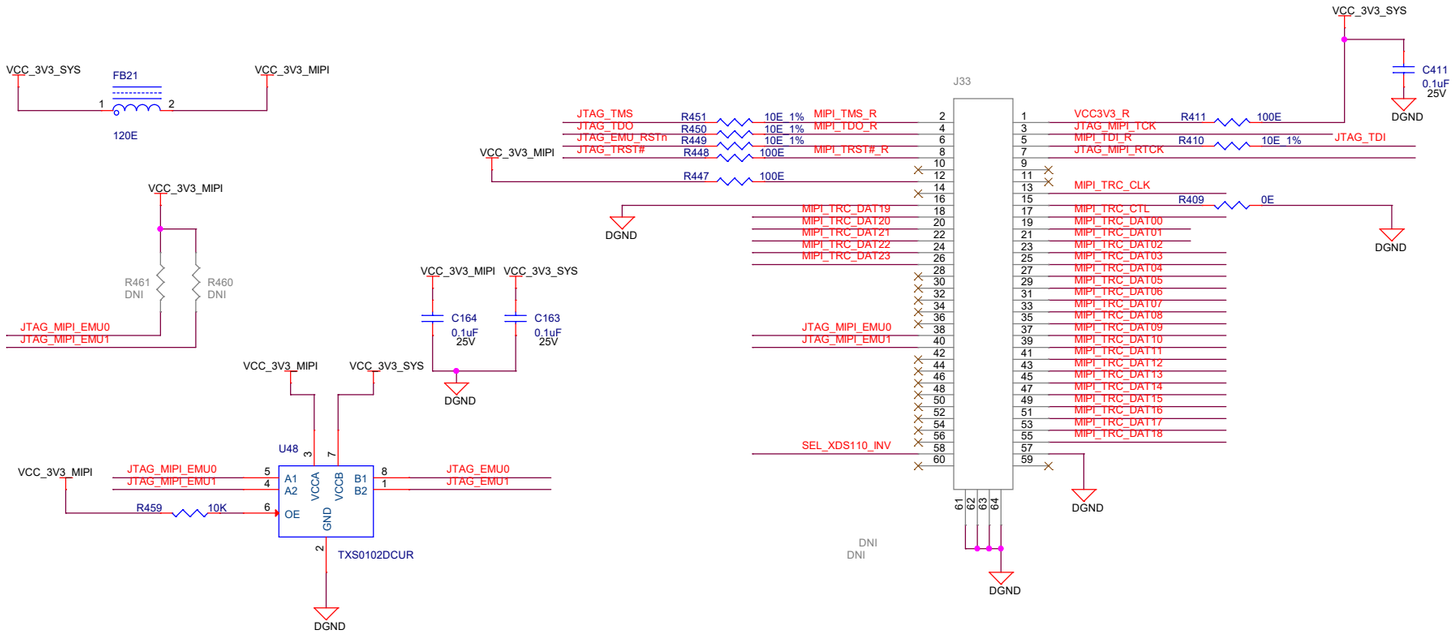
TEXAS INSTRUMENTS MISTRAL

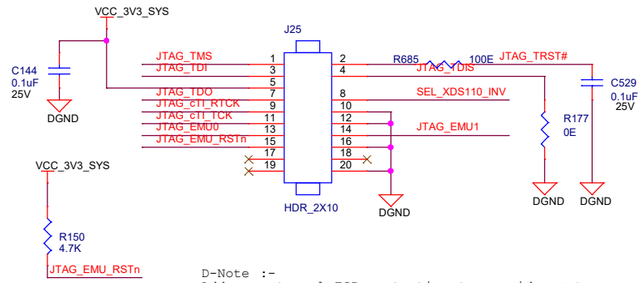
Title	JTAG BUFFER	
Size	Variant Name = PROC101D(004) TMDS64EVM	Rev
C		D
Date: Wednesday, June 12, 2024	Sheet 23 of 40	

MIPI 60 PIN CONNECTOR



JTAG 20 PIN cTI CONNECTOR

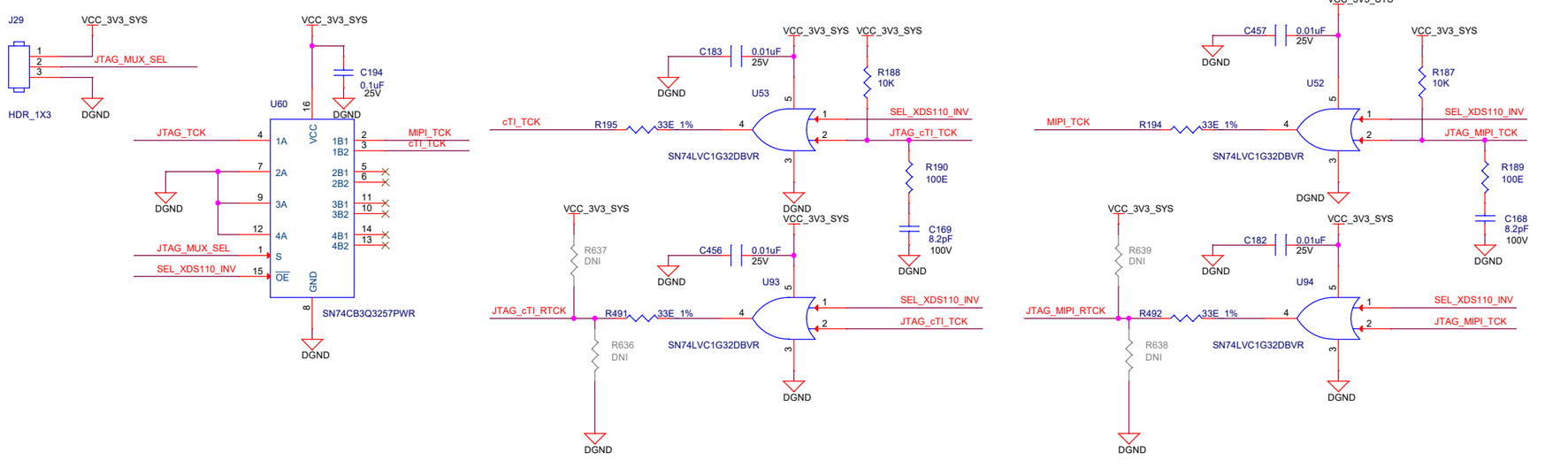
D-Note :-
Place pulls on the JTAG signals near to the SoC
Refer SoC data sheet for Pin Connectivity
Requirements



D-Note :-
Add an external ESD protection to provide system level ESD protection
when external connector is used for debug
Follow the connectivity table for connecting the required pulls for the SOC JTAG interface
Add Test points, and external ESD protection when JTAG connector is not used

D-Note :-
TRSTn is the reset to the JTAG logic. For normal operation, this is pulled low, and thus the JTAG remains in reset as it is not being used. When a JTAG pod is connected, the pod will eventually drive this signal high to release the JTAG logic from reset and enable a JTAG connection.

JTAG CLOCK BUFFER



Off Page Connections

From JTAG Buffer

[23] SEL_XDS110_INV
[23] JTAG_TDO
[23] JTAG_EMU0
[23] JTAG_EMU1
[23] JTAG_TDI
[23] JTAG_TCK
[23] JTAG_TMS
[23] JTAG_TRST#
[35] JTAG_EMU_RSTn

From SoC GPMC

[28] MIPI_TRC_DAT05
[28] MIPI_TRC_DAT04
[28] MIPI_TRC_DAT03
[28] MIPI_TRC_DAT02
[28] MIPI_TRC_DAT01
[28] MIPI_TRC_DAT00
[28] MIPI_TRC_CTL
[28] MIPI_TRC_CLK

[28] MIPI_TRC_DAT11
[28] MIPI_TRC_DAT10
[28] MIPI_TRC_DAT09
[28] MIPI_TRC_DAT13
[28] MIPI_TRC_DAT12
[28] MIPI_TRC_DAT08
[28] MIPI_TRC_DAT07
[28] MIPI_TRC_DAT06

[28] MIPI_TRC_DAT21
[28] MIPI_TRC_DAT20
[28] MIPI_TRC_DAT19
[28] MIPI_TRC_DAT18
[28] MIPI_TRC_DAT17
[28] MIPI_TRC_DAT16
[28] MIPI_TRC_DAT15
[28] MIPI_TRC_DAT14

[28] MIPI_TRC_DAT23
[28] MIPI_TRC_DAT22

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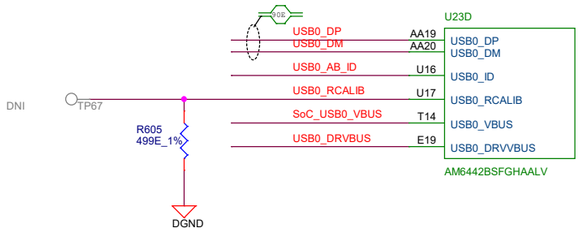
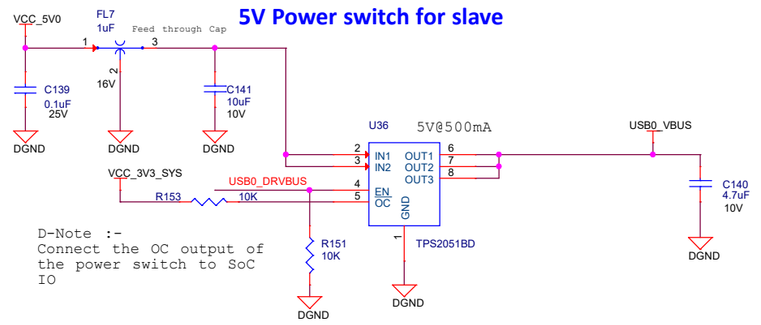
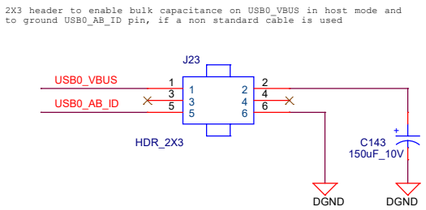
Title	MIPI 60 PIN CONNECTOR	
Size C	Variant Name = PROC101D(004) TMDS64EVM	Rev D
Date: Wednesday, June 12, 2024	Sheet 24 of 40	

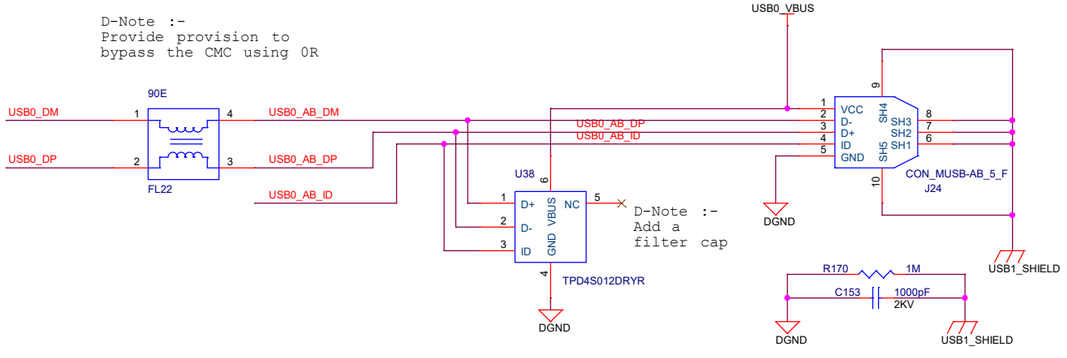
USB 2.0 INTERFACE

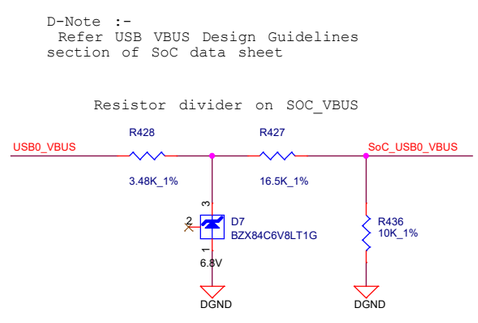






Micro USB 2.0 AB Connector

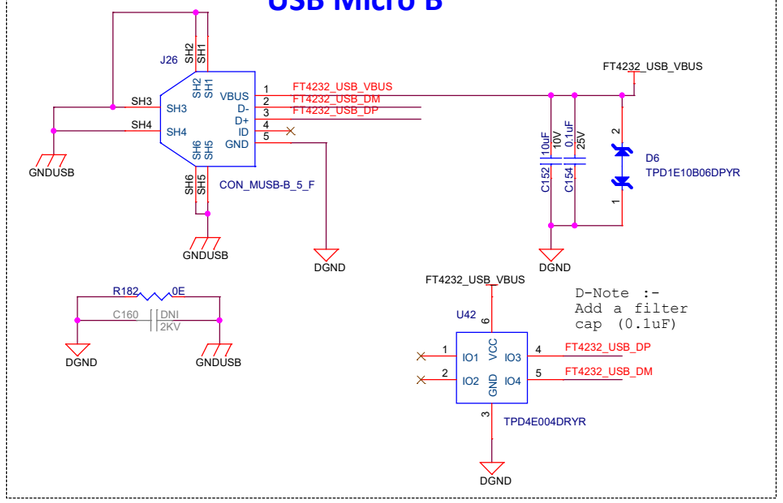




Designed for TI by Mistral Solutions Pvt Ltd

Title	USB 2.0 INTERFACE	
Size: C	Variant Name = PROC101D(004) TMDS64EVM	Rev: D
Date: Wednesday, June 12, 2024	Sheet 25 of 40	

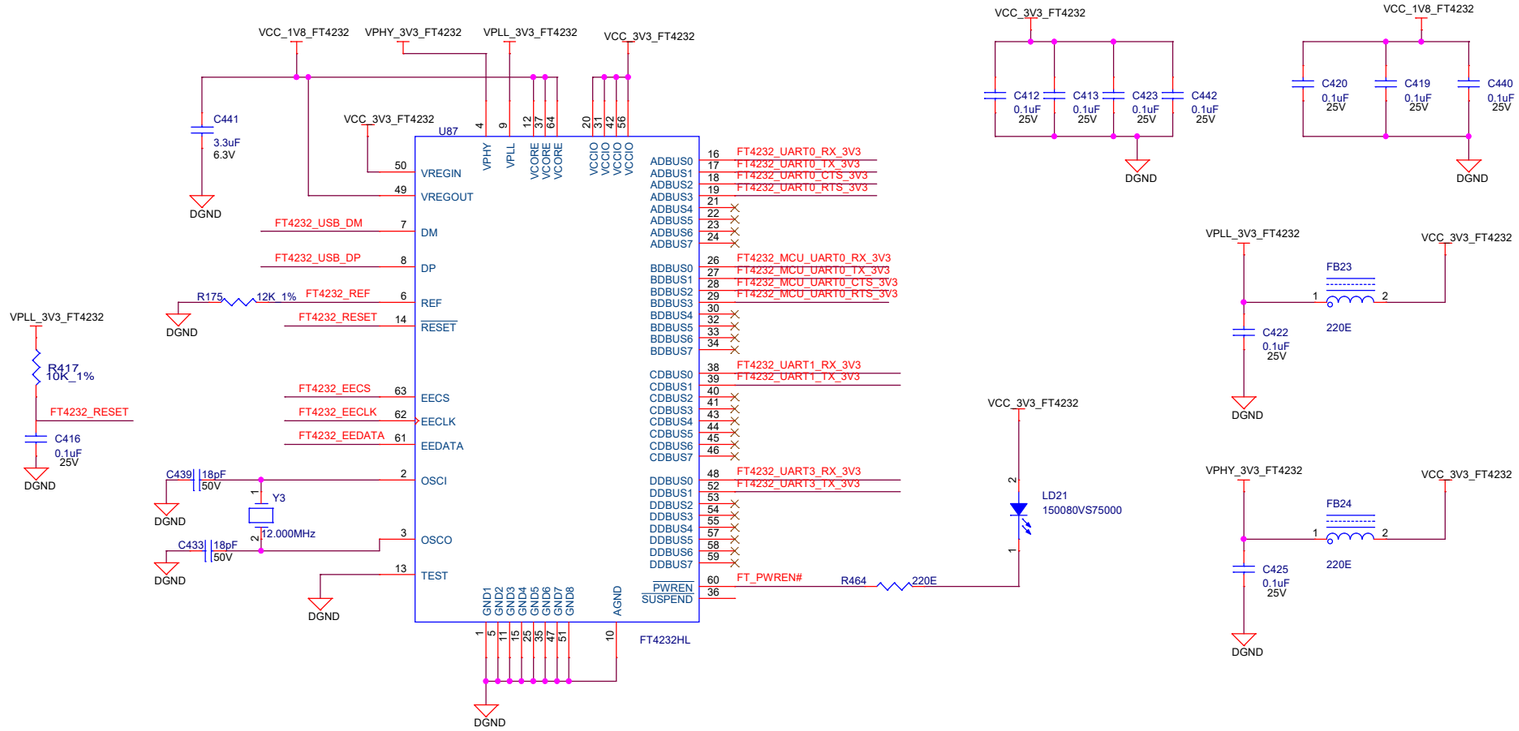
USB Micro B



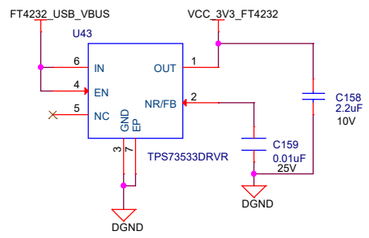
FT4232 UART

D-Note :-
Follow SK-AM62P-LP SK implementations for latest updates on FT4232

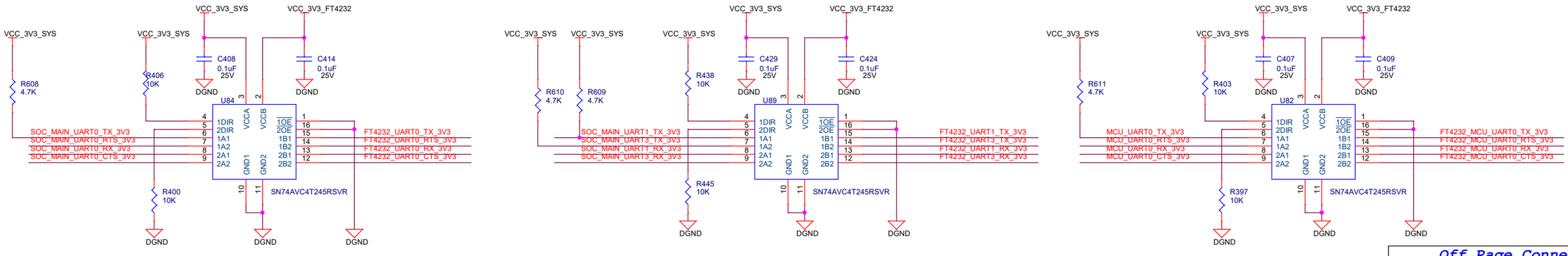
R-Note:-
Verify the implementation with the device manufacturer



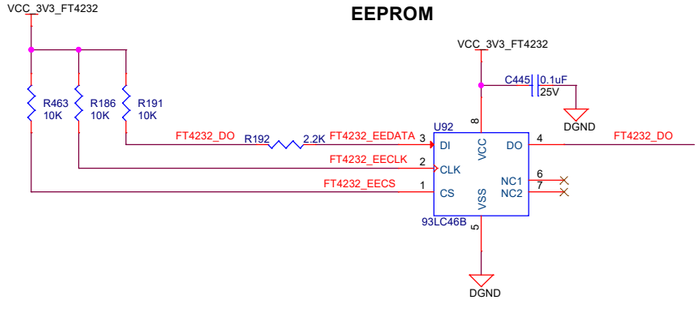
FT4232: 5V to 3.3V@500mA LDO



FT4232 LEVEL TRANSLATOR



EEPROM



Off Page Connections

SOC_MAIN_UART0_RX_3V3 → SOC_MAIN_UART0_RX_3V3 [29]
SOC_MAIN_UART0_TX_3V3 → SOC_MAIN_UART0_TX_3V3 [29]
SOC_MAIN_UART0_RTS_3V3 → SOC_MAIN_UART0_RTS_3V3 [29]
SOC_MAIN_UART0_CTS_3V3 → SOC_MAIN_UART0_CTS_3V3 [29]

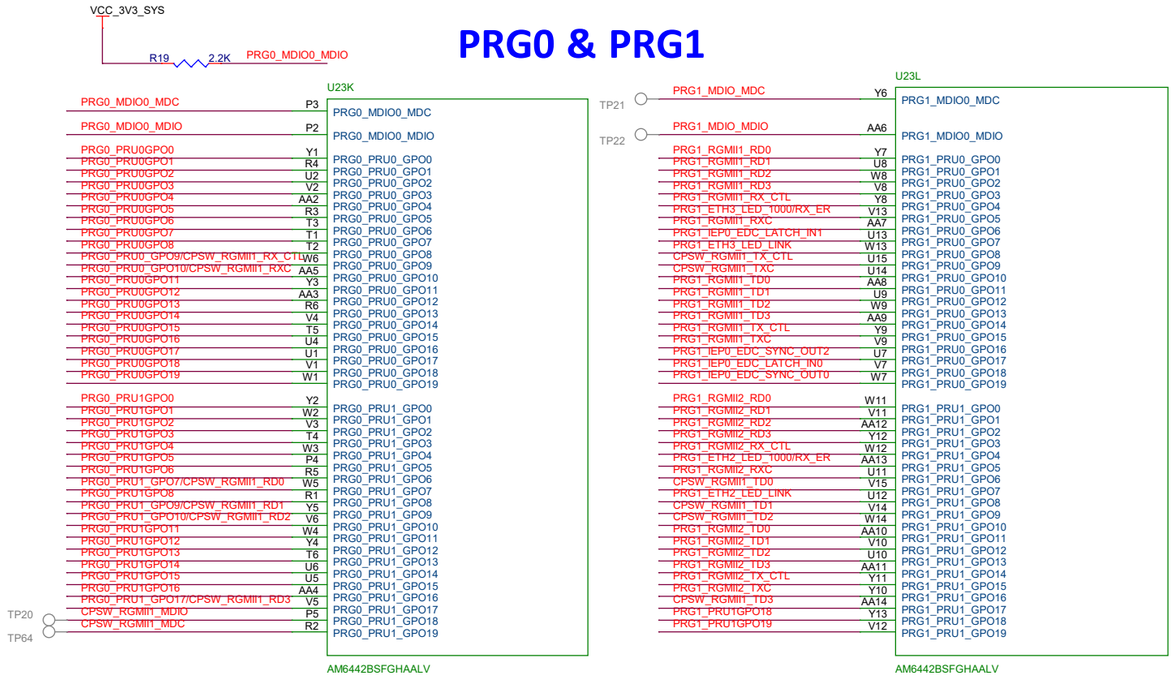
MCU_UART0_RX_3V3 → MCU_UART0_RX_3V3 [34]
MCU_UART0_TX_3V3 → MCU_UART0_TX_3V3 [34]
MCU_UART0_RTS_3V3 → MCU_UART0_RTS_3V3 [34]
MCU_UART0_CTS_3V3 → MCU_UART0_CTS_3V3 [34]

SOC_MAIN_UART1_RX_3V3 → SOC_MAIN_UART1_RX_3V3 [29]
SOC_MAIN_UART1_TX_3V3 → SOC_MAIN_UART1_TX_3V3 [29]
SOC_MAIN_UART3_TX_3V3 → SOC_MAIN_UART3_TX_3V3 [29]
SOC_MAIN_UART3_RX_3V3 → SOC_MAIN_UART3_RX_3V3 [29]

Designed for TI by Mistral Solutions Pvt Ltd

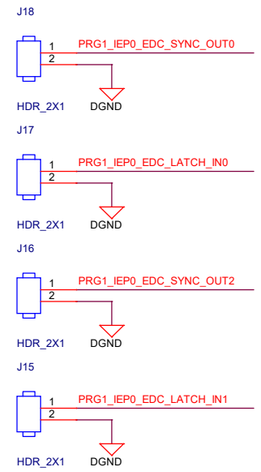
Title	FT4232 UART TO USB BRIDGE	
Size: C	Variant Name = PROC101D(004) TMDS64EVM	Rev: D
Date: Wednesday, June 12, 2024	Sheet 26 of 40	

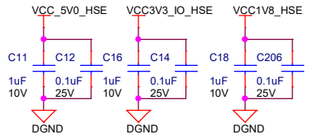
PRG0 & PRG1



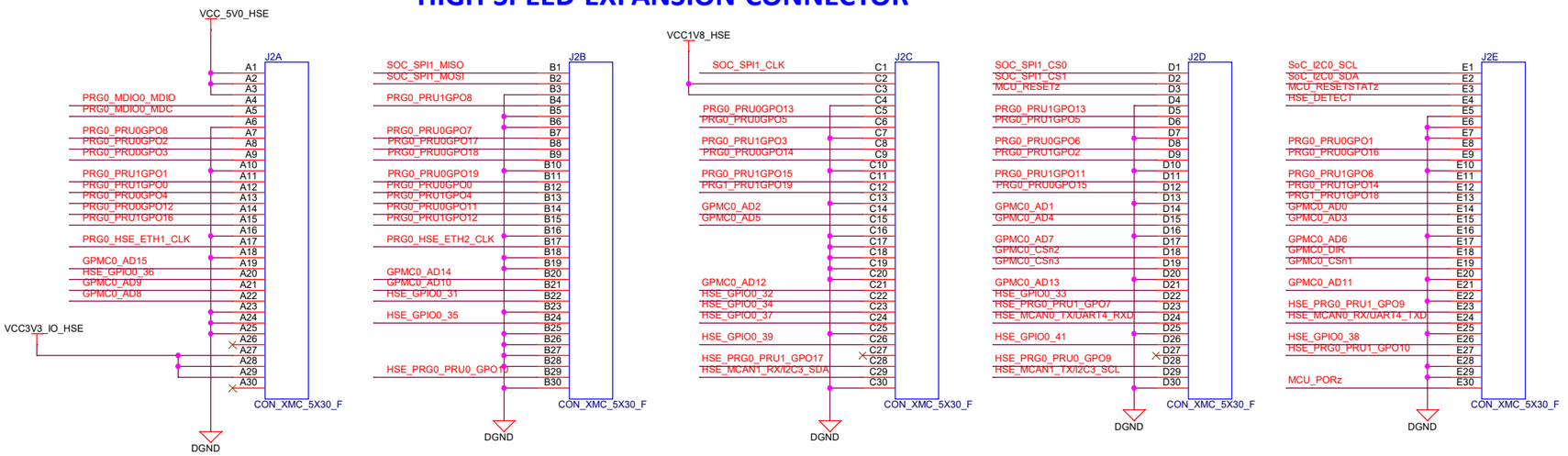
D-Note :-
Add series resistors 22 R on the Ethernet interface TX (TDx) signals near to the SoC

SYNC TP





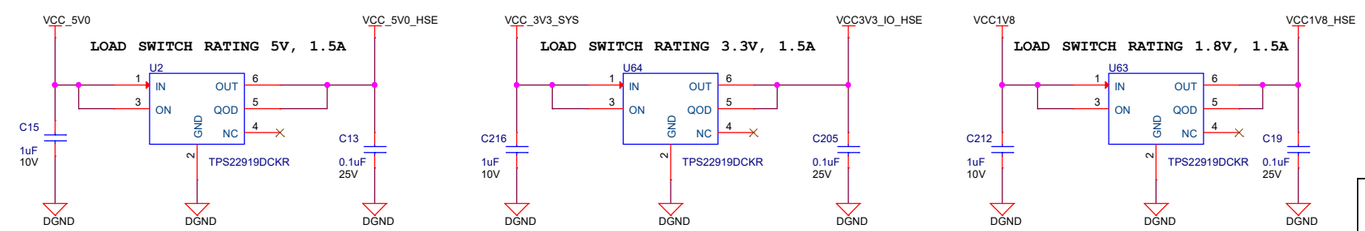
HIGH SPEED EXPANSION CONNECTOR



D-Note :-
Any SoC IO that has a trace connected but not being driven actively needs to be connected to an external pull.
When adding pull is not feasible, ensure the traces are routed away from noisy signals

D-Note:-
Processor IOs connected to HSEC are not fail-safe.
No external input shall be driven when Starter Kit is not powered-up.

HSE CONNECTOR LOAD SWITCHES



D-Note :-
These supplies are always ON. Take Ensure the board is off during connection to avoid hot plug of the attached devices.

Off Page Connections

To Presence Detect Buffer
[15] HSE_DETECT

From Processor GPMC
[28] GPMC0_CSn1
[28] GPMC0_CSn2
[28] GPMC0_CSn3
[28] GPMC0_DIR

From FSI mux
[28] GPMC0_AD8
[28] GPMC0_AD9
[28] GPMC0_AD10
[28] GPMC0_AD14
[28] GPMC0_AD15
[28] HSE_GPIO0_36

From Processor GPMC resistor muxed with MIPI
[28] GPMC0_AD0
[28] GPMC0_AD1
[28] GPMC0_AD2
[28] GPMC0_AD3
[28] GPMC0_AD4
[28] GPMC0_AD5
[28] GPMC0_AD6
[28] GPMC0_AD7
[28] GPMC0_AD11
[28] GPMC0_AD12
[28] GPMC0_AD13
[28] HSE_GPIO0_31
[28] HSE_GPIO0_32
[28] HSE_GPIO0_33
[28] HSE_GPIO0_34
[28] HSE_GPIO0_35
[28] HSE_GPIO0_37
[28] HSE_GPIO0_38
[28] HSE_GPIO0_39
[28] HSE_GPIO0_41

From Processor
[34] MCU_PORz
[34,35] MCU_RESETz
[34] MCU_RESETSTATZ

[29] HSE_MCAN0_RX/UART4_TXD
[29] HSE_MCAN0_TX/UART4_RXD
[29] HSE_MCAN1_RX/I2C3_SDA
[29] HSE_MCAN1_TX/I2C3_SCL

[29] SOC_SPI1_CLK
[29] SOC_SPI1_MOSI
[29] SOC_SPI1_MISO
[29] SOC_SPI1_CS0
[29] SOC_SPI1_CS1
[15,29,33] SoC_I2C0_SCL
[15,29,33] SoC_I2C0_SDA

From clock Buffer
[31] PRG0_HSE_ETH1_CLK
[31] PRG0_HSE_ETH2_CLK

To and from ICSSG1 RGMII 2 Ethernet PHY
[17] PRG1_RGMII2_RD0
[17] PRG1_RGMII2_RD1
[17] PRG1_RGMII2_RD2
[17] PRG1_RGMII2_RD3
[17] PRG1_RGMII2_RXC
[17] PRG1_RGMII2_RX_CTL
[17] PRG1_ETH2_LED_1000/RX_ER
[17] PRG1_RGMII2_TD0
[17] PRG1_RGMII2_TD1
[17] PRG1_RGMII2_TD2
[17] PRG1_RGMII2_TD3
[17] PRG1_RGMII2_TXC
[17] PRG1_RGMII2_TX_CTL

To and from ICSSG2 RGMII 1 Ethernet PHY
[17,18] PRG1_MDIO_MDIO
[17,18] PRG1_MDIO_MDC
[18] PRG1_ETH3_LED_LINK
[17] PRG1_ETH2_LED_LINK
[18] PRG1_RGMII1_RD0
[18] PRG1_RGMII1_RD1
[18] PRG1_RGMII1_RD2
[18] PRG1_RGMII1_RD3
[18] PRG1_RGMII1_RXC
[18] PRG1_RGMII1_RX_CTL
[18] PRG1_ETH3_LED_1000/RX_ER
[18] PRG1_RGMII1_TD0
[18] PRG1_RGMII1_TD1
[18] PRG1_RGMII1_TD2
[18] PRG1_RGMII1_TD3
[18] PRG1_RGMII1_TXC
[18] PRG1_RGMII1_TX_CTL

From MUX To HSE
[16] HSE_PRG0_PRU1_GPO7
[16] HSE_PRG0_PRU1_GPO9
[16] HSE_PRG0_PRU1_GPO10
[16] HSE_PRG0_PRU1_GPO17
[16] HSE_PRG0_PRU0_GPO9
[16] HSE_PRG0_PRU0_GPO10

[16,17] CPSW_RGMII1_MDIO
[16,17] CPSW_RGMII1_MDC

To MUX From SoC
[16] PRG0_PRU1_GPO7/CPSW_RGMII1_RD0
[16] PRG0_PRU1_GPO9/CPSW_RGMII1_RD1
[16] PRG0_PRU1_GPO10/CPSW_RGMII1_RD2
[16] PRG0_PRU1_GPO17/CPSW_RGMII1_RD3
[16] PRG0_PRU0_GPO9/CPSW_RGMII1_RX_CTL
[16] PRG0_PRU0_GPO10/CPSW_RGMII1_RXC

From CPSW RGMII 1 PHY
[16] CPSW_RGMII1_TD0
[16] CPSW_RGMII1_TD1
[16] CPSW_RGMII1_TD2
[16] CPSW_RGMII1_TD3
[16] CPSW_RGMII1_TX_CTL
[16] CPSW_RGMII1_TXC

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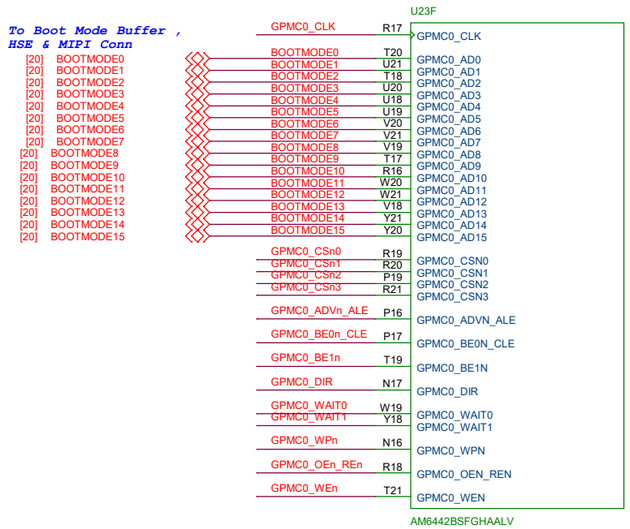
Title	HSE CONNECTOR	
Size	Variant Name = PROC101D(004) TMDS64EVM	Rev
C		D
Date: Wednesday, June 12, 2024	Sheet 27 of 40	

GPMC

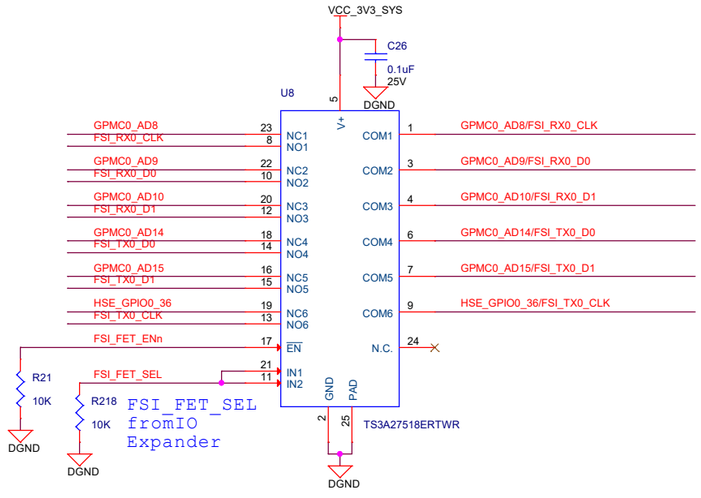
D-Note :-
SOC IO buffers for signals used for GPMC interface are disabled during reset
The required pulls for the interfaced signals are provided on the GPMC interface card

D-Note :-
Shorting of bootmode inputs (IOs) is not recommended or allowed since the IOs have alternate functions that could be configured after boot
Shorting the bootmode pins directly to VCC or ground directly is not recommended
Connect each of the bootmode pins through separate resistor
Choose the bootmode resistor value based on the use case (10K or similar)

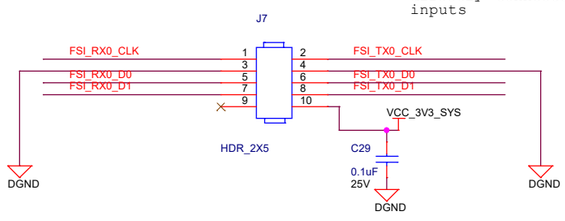
D-Note :-
Add a series resistor 0R when used as GPMC0_CLK



GPMC TO FSI & HSE CONNECTOR



FSI CONNECTOR



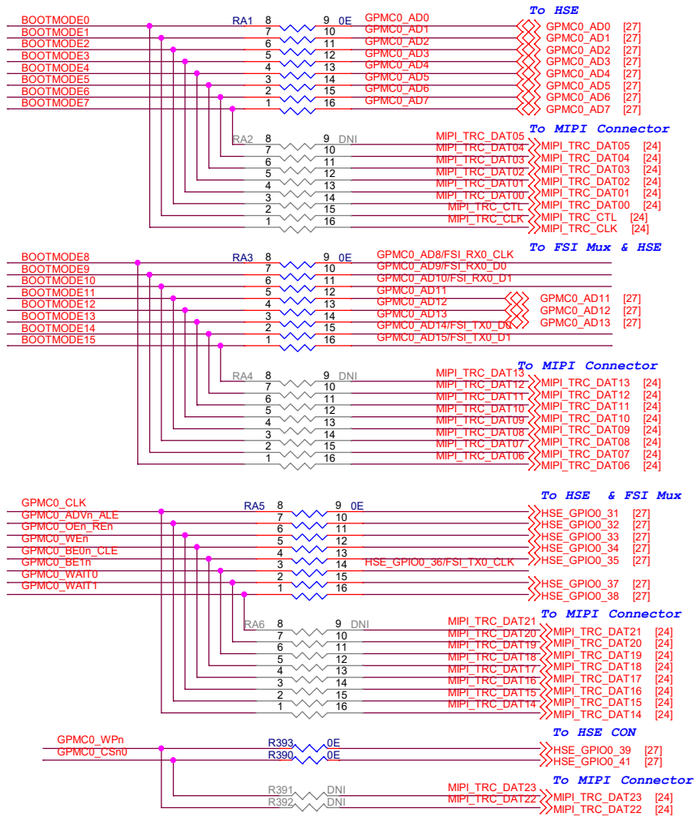
D-Note :-
An external ESD protection is recommended when these IOs are directly connected to external inputs

D-Note :-
Processor IOs connected to TEST FSI CONNECTOR are not fail-safe.
No external input shall be applied when Starter Kit/EVM is not powered-up.

TS3A27518ERTWR Truth Table

EN#	IN1	IN2	NC1/2/3 TO COM1/2/3 & COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM14/5/6 & COM4/5/6 TO NC4/5/6	NO1/2/3 TO COM1/2/3 & COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM14/5/6 & COM4/5/6 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

0- Ohm Res MUX between HSE Connector and TRACE Funct i onality
-For HSE Connector RA1 , RA3 , RA5 , R393 & R390 Should be installed and RA2, RA4 ,RA6 , R391& R392 Should be DNI'd.
-For TRACE RA2, RA4 ,RA6 , R391& R392 Should be Installed and RA1 , RA3 , RA5 , R393 & R390 Should be DNI'd.



Off Page Connections

From IO Expander
[33] FSI_FET_SEL — FSI_FET_SEL

To HSE Connector
[27] GPMC0_CSn1 — GPMC0_CSn1
[27] GPMC0_CSn2 — GPMC0_CSn2
[27] GPMC0_CSn3 — GPMC0_CSn3
[27] GPMC0_DIR — GPMC0_DIR

From FSI mux To HSE Connector
[27] GPMC0_AD8 — GPMC0_AD8
[27] GPMC0_AD9 — GPMC0_AD9
[27] GPMC0_AD10 — GPMC0_AD10
[27] GPMC0_AD14 — GPMC0_AD14
[27] GPMC0_AD15 — GPMC0_AD15
[27] HSE_GPIO0_36 — HSE_GPIO0_36

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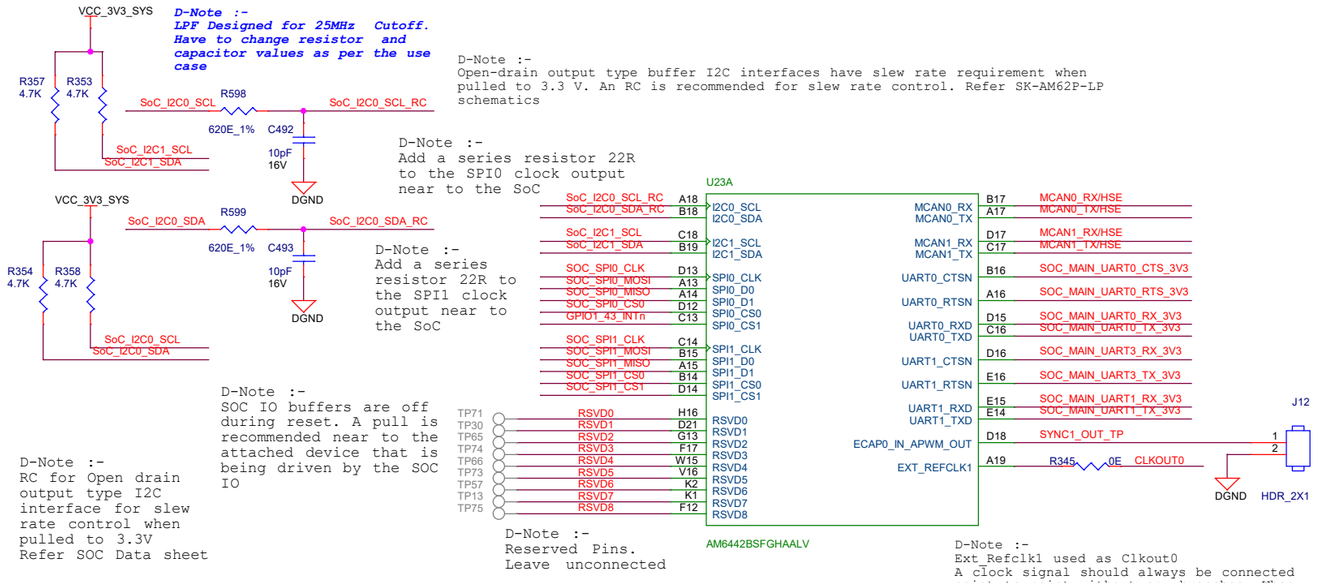
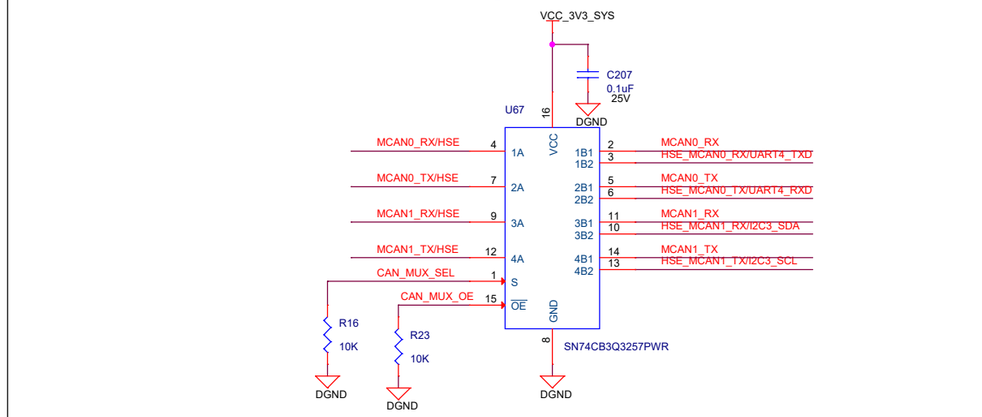
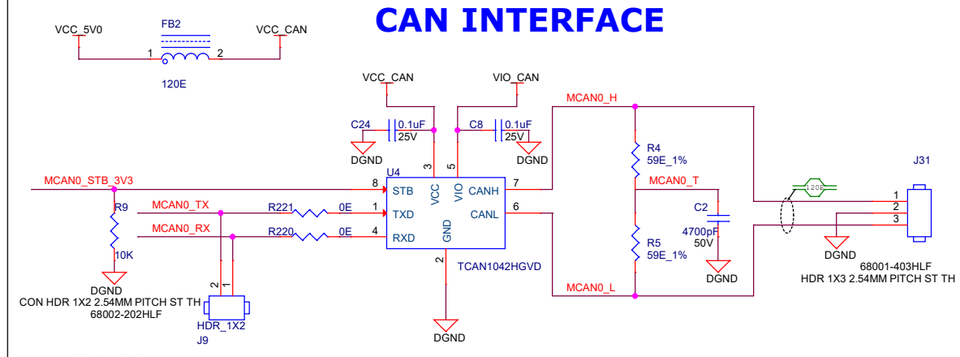
Title	GPMC	
Size C	Variant Name = PROC101D(004) TMDS64EVM	Rev D
Date: Wednesday, June 12, 2024	Sheet 28 of 40	



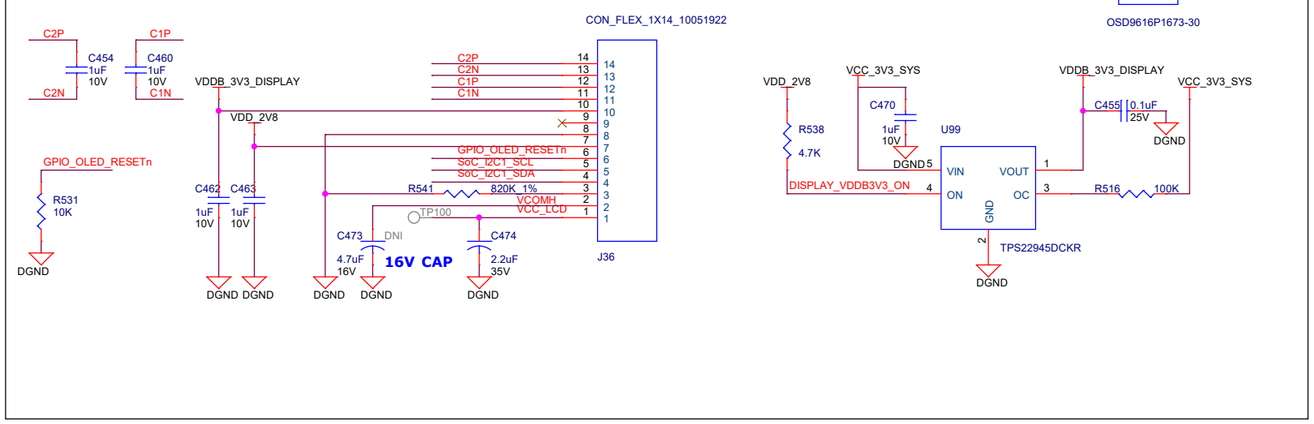
HSE/CAN MUX



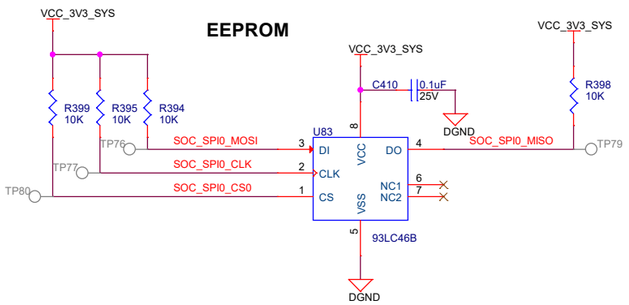
CAN INTERFACE



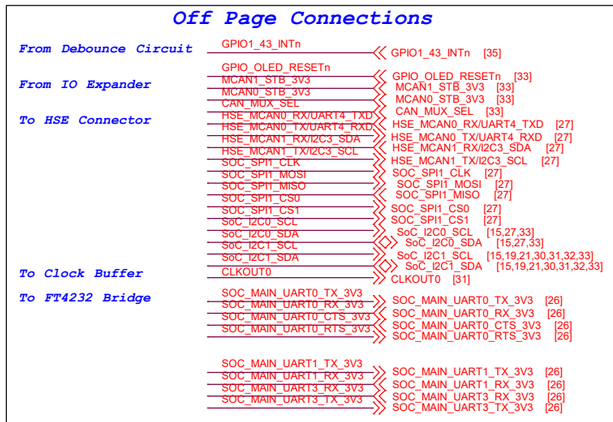
DISPLAY CONNECTOR



SPI EEPROM



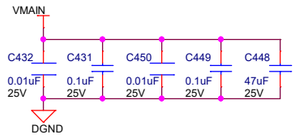
Off Page Connections

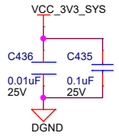


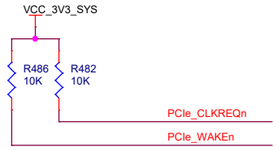
PROC101D(004) TMDS64EVM

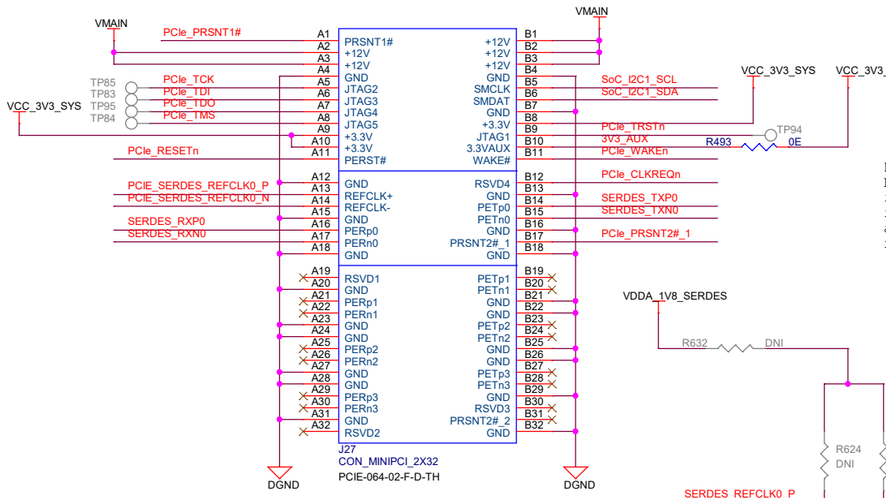
Project : <Project Name>	Designed for TI by Mistral Solutions Pvt Ltd	Title: CAN & DISPLAY INTERFACE
		Size: C — Document Number: MS_TI_MAXIE_APPLICATION_CARD_SCH_REVA — Rev: D
		Date: Wednesday, June 12, 2024 — Sheet 29 of 40

x4 Lane PCIe Connector



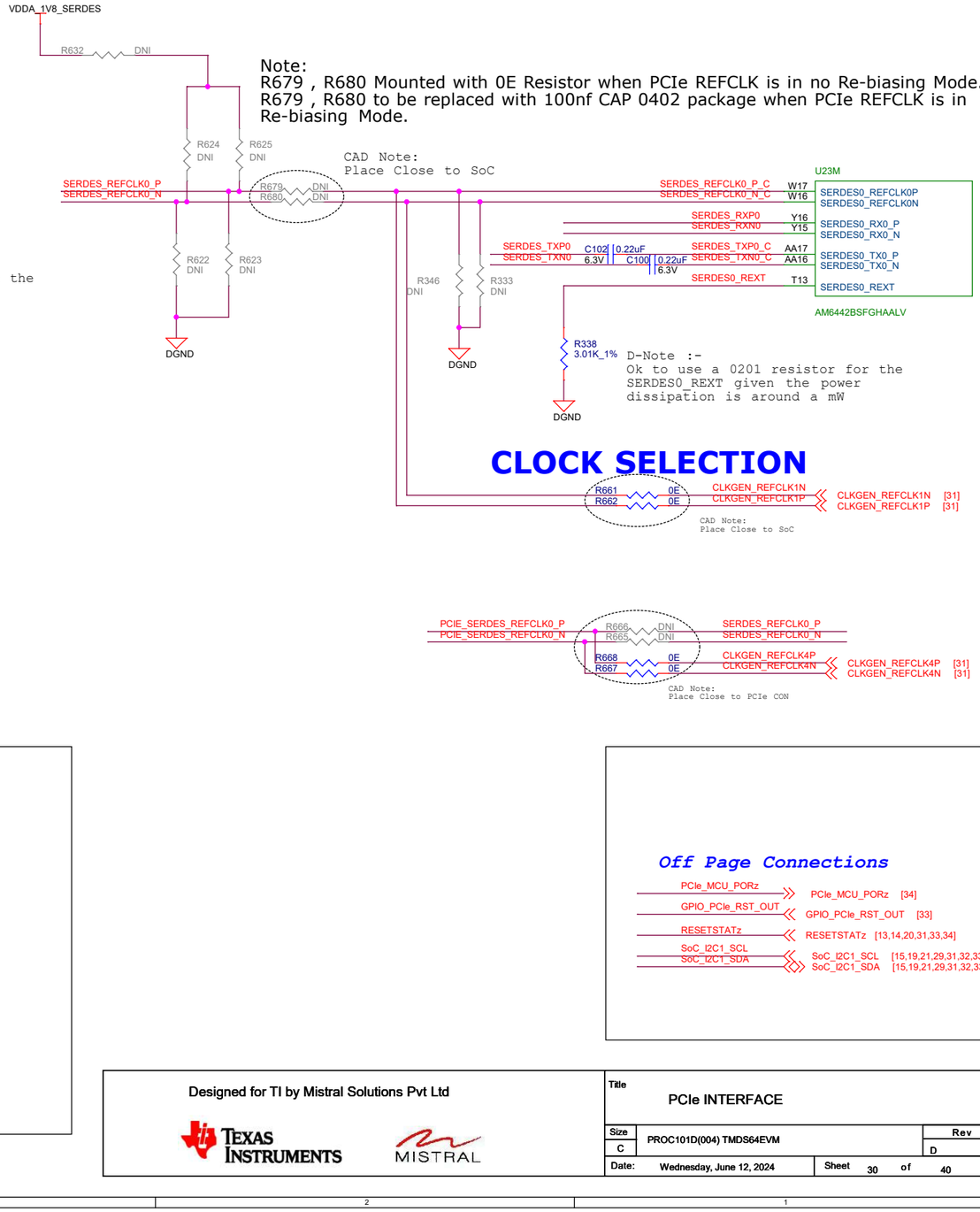






D-Note :-
Errata i2326 PCIe refclk Applicable?
i2326 does not apply when PCIe refclk is from an external source. It only applies if SK-AM64B is generating the refclk.

D-Note :-
SERDES0 inputs are not fail-safe.
If clock or data inputs are available before the SOC supply ramps, VDDR_CORE rail could be affected causing booting issues based on t



Note:
R679 , R680 Mounted with 0E Resistor when PCIe REFCLK is in no Re-biasing Mode.
R679 , R680 to be replaced with 100nf CAP 0402 package when PCIe REFCLK is in Re-biasing Mode.

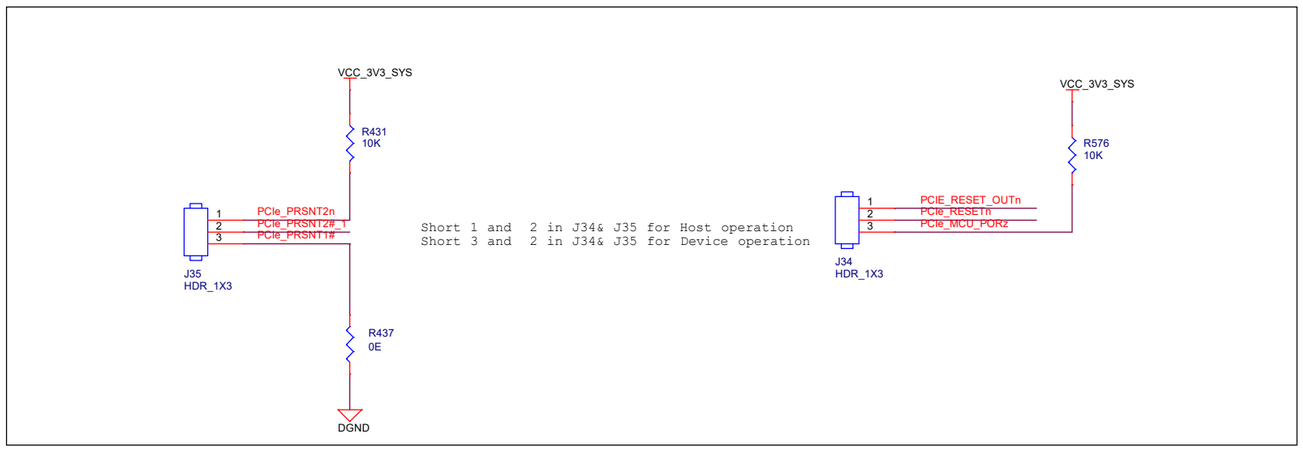
D-Note :-
Ok to use a 0201 resistor for the SERDES0_REXT given the power dissipation is around a mW

PCIe Reset

D-Note :-
Add a series resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics

CLOCK SELECTION

RC OR EP MODE SELECTION



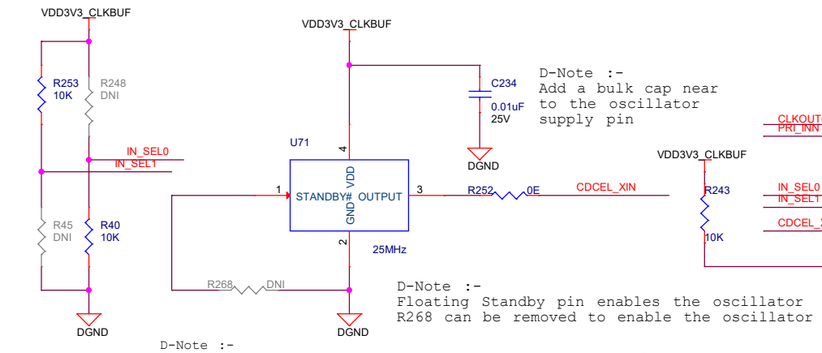
Off Page Connections

PCIe_MCU_PORz → PCIe_MCU_PORz [34]
GPIO_PCIe_RST_OUT → GPIO_PCIe_RST_OUT [33]
RESETSTATz → RESETSTATz [13,14,20,31,33,34]
SoC_I2C1_SCL → SoC_I2C1_SCL [15,19,21,29,31,32,33]
SoC_I2C1_SDA → SoC_I2C1_SDA [15,19,21,29,31,32,33]

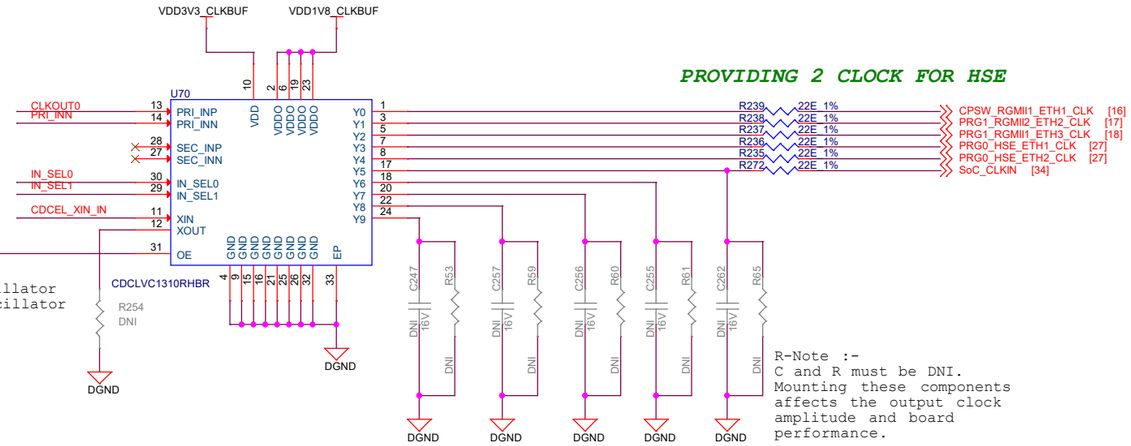
Designed for TI by Mistral Solutions Pvt Ltd

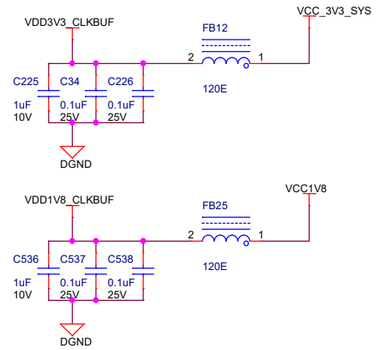
Title	PCIe INTERFACE		
Size C	PROC101D(004) TMDS64EVM		Rev D
Date: Wednesday, June 12, 2024		Sheet 30 of 40	

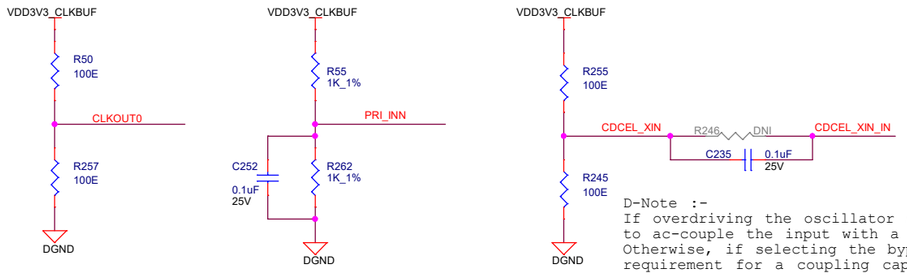
REFERENCE INPUT SELECTION



ETHERNET PHY CLOCK BUFFER



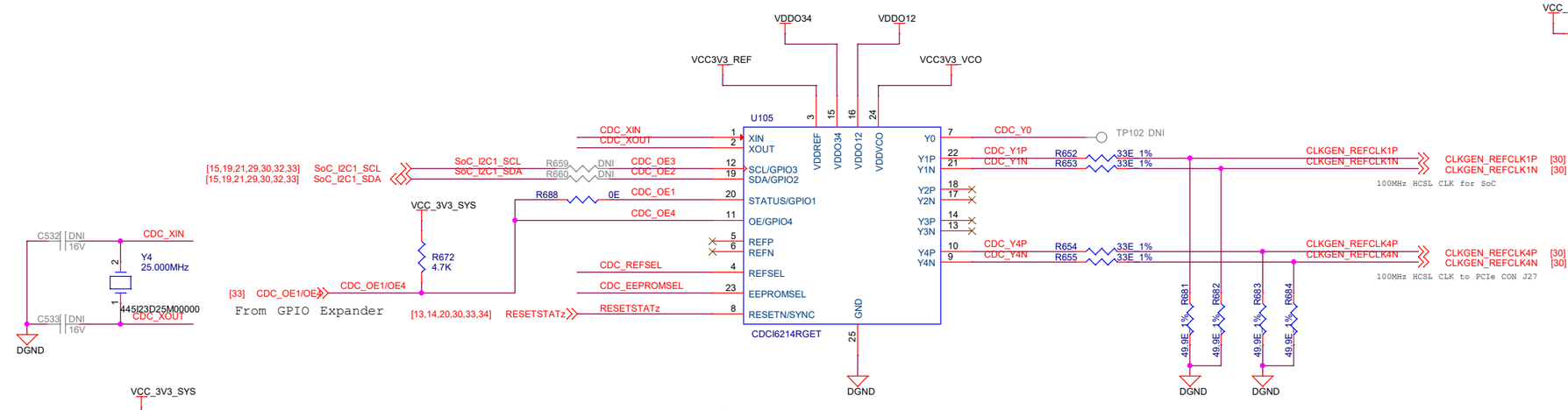


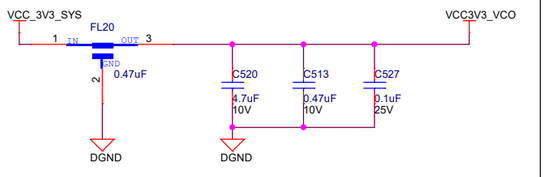


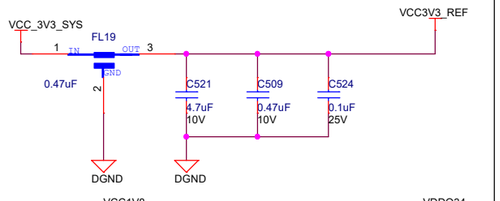
Off Page Connections

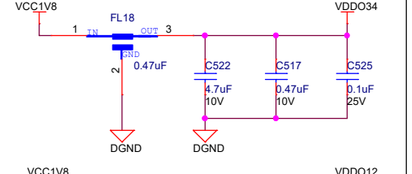
From SoC — CLKOUT0 — CLKOUT0 [29]

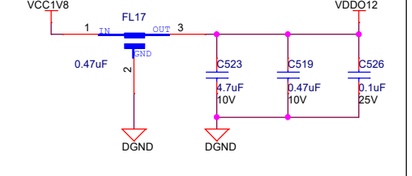
PCIe Clock HCSL (100MHz)

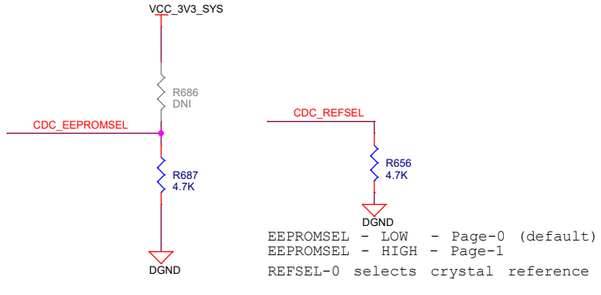












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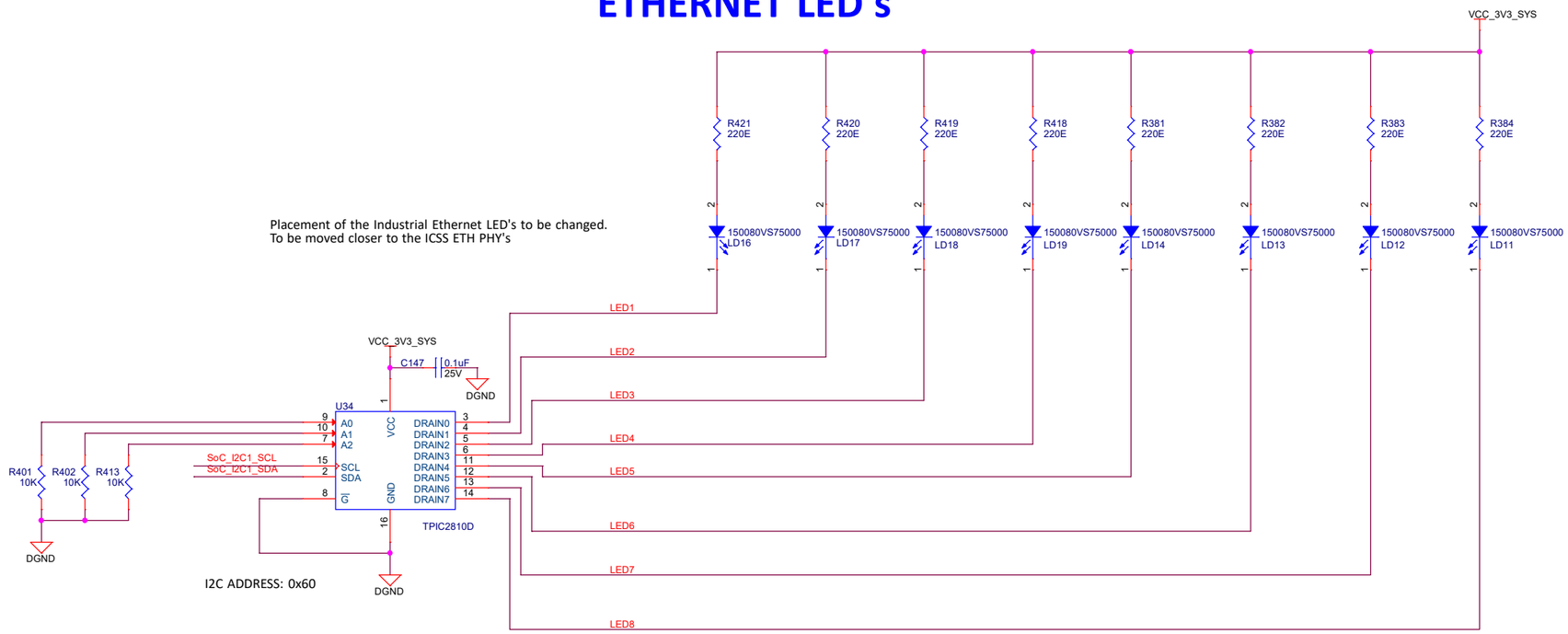
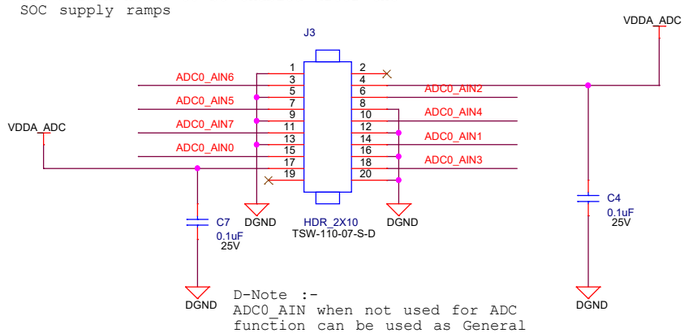
Title	ETHERNET PHY & PCIe CLOCK GENERATOR	
Size: C	Variant Name = PROC101D(004) TMDS64EVM	Rev: D
Date: Wednesday, June 12, 2024	Sheet 31 of 40	

ETHERNET LED's



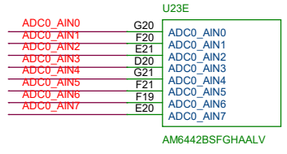
ADC CONNECTOR

D-Note :-
ADC inputs are not fail-safe. No input voltage should be apply before the SOC supply ramps. The SOC functionality could be affected if ADC inputs are applied before the SOC supply ramps
Use a FET or similar switch to control the input voltage in case they are available before the SOC supply ramps
The Switch needs to be enabled after the SOC supply ramps



D-Note :-
ADC0_AIN when not used for ADC function can be used as General Purpose Input
The assignment of each ADC0 pin to the GPIO1 module is defined in the ADC0 Signal Description table found in the data sheet.

D-Note :-
For connecting the ADC0 signals, Refer Pin connectivity table when entire ADC0 is not used or any ADC input is not used



Off Page Connections

SoC_I2C1_SCL
SoC_I2C1_SDA
SoC_I2C1_SCL [15,19,21,29,30,31,33]
SoC_I2C1_SDA [15,19,21,29,30,31,33]

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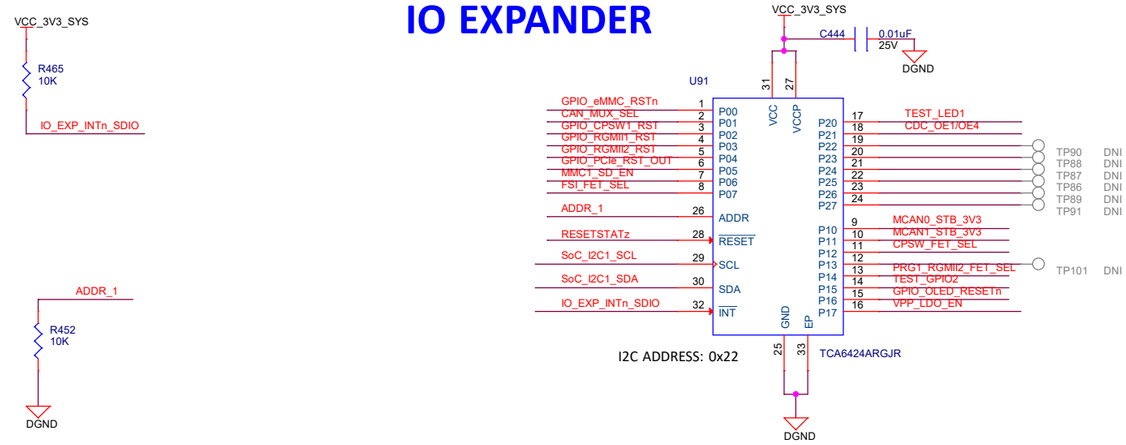
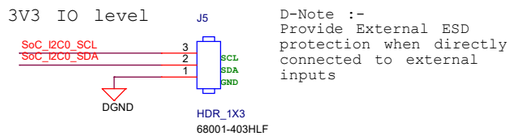
Title	ETHERNET LEDs	
Size C	Variant Name = PROC101D(004) TMDS64EVM	Rev D
Date: Wednesday, June 12, 2024	Sheet 32 of 40	

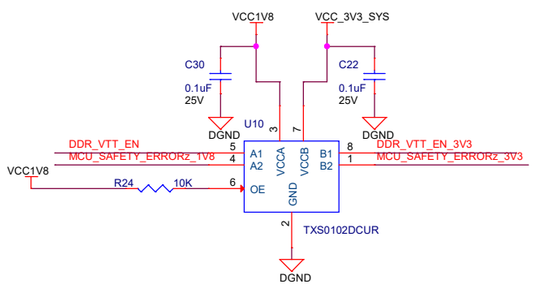
IO EXPANDER



I2C TEST HEADER



LEVEL TRANSLATOR



Off Page Connections

GPIO_eMMC_RSTn → GPIO_eMMC_RSTn [13]
GPIO_PCIe_RST_OUT → GPIO_PCIe_RST_OUT [30]
GPIO_CPSW1_RST → GPIO_CPSW1_RST [16]
GPIO_RGMII1_RST → GPIO_RGMII1_RST [18]
GPIO_RGMII2_RST → GPIO_RGMII2_RST [17]

MMC1_SD_EN → MMC1_SD_EN [13]
FSI_FET_SEL → FSI_FET_SEL [28]

MCAN1_STB_3V3 → MCAN1_STB_3V3 [29]
MCAN0_STB_3V3 → MCAN0_STB_3V3 [29]
CPSW_FET_SEL → CPSW_FET_SEL [16]

PRG1_RGMII2_FET_SEL → PRG1_RGMII2_FET_SEL [17]
TEST_GPIO2 → TEST_GPIO2 [19]
GPIO_OLED_RESETn → GPIO_OLED_RESETn [29]
VPP_LDO_EN → VPP_LDO_EN [38]

CAN_MUX_SEL → CAN_MUX_SEL [29]
TEST_LED1 → TEST_LED1 [14]
CDC_OE1/OE4 → CDC_OE1/OE4 [31]
RESETSTATz → RESETSTATz [13,14,20,30,31,34]

SoC_I2C1_SDA → SoC_I2C1_SDA [15,19,21,29,30,31,32]
SoC_I2C1_SCL → SoC_I2C1_SCL [15,19,21,29,30,31,32]

SoC_I2C0_SDA → SoC_I2C0_SDA [15,27,29]
SoC_I2C0_SCL → SoC_I2C0_SCL [15,27,29]

From Safety Connector: MCU_SAFETY_ERRORz_3V3 → MCU_SAFETY_ERRORz_3V3 [34]

From SoC OSPI Section: DDR_VTT_EN → DDR_VTT_EN [14]

To Processor: MCU_SAFETY_ERRORz_1V8 → MCU_SAFETY_ERRORz_1V8 [34]
To VTT Reg: DDR_VTT_EN_3V3 → DDR_VTT_EN_3V3 [39]
To SoC MMC: IO_EXP_INTn_SDIO → IO_EXP_INTn_SDIO [13]

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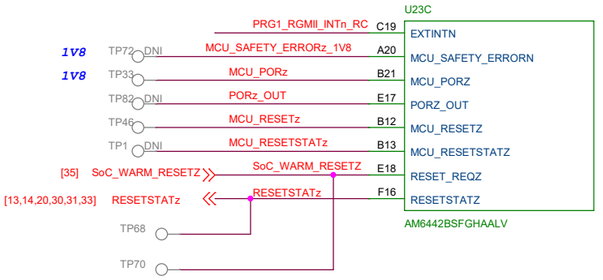
TEXAS INSTRUMENTS MISTRAL

Title	IO EXPANDER	
Size: C	Variant Name = PROC101D(004) TMDS64EVM	Rev: D
Date: Wednesday, June 12, 2024	Sheet 33 of 40	

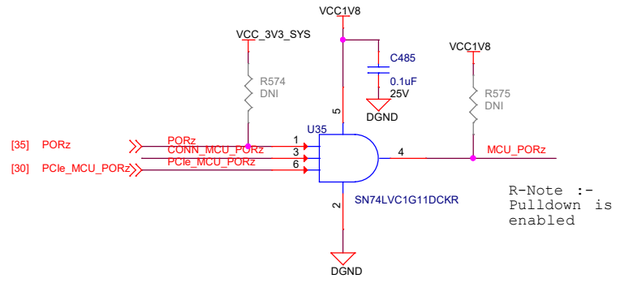
SOC-MCU_GENERAL

SOC RESET

D-Note :-
MCU_SAFETY_ERRORz_1V8
Provision for a pulldown
Populate when attached
device is connected
Refer SOC data sheet pin
connectivity requirements

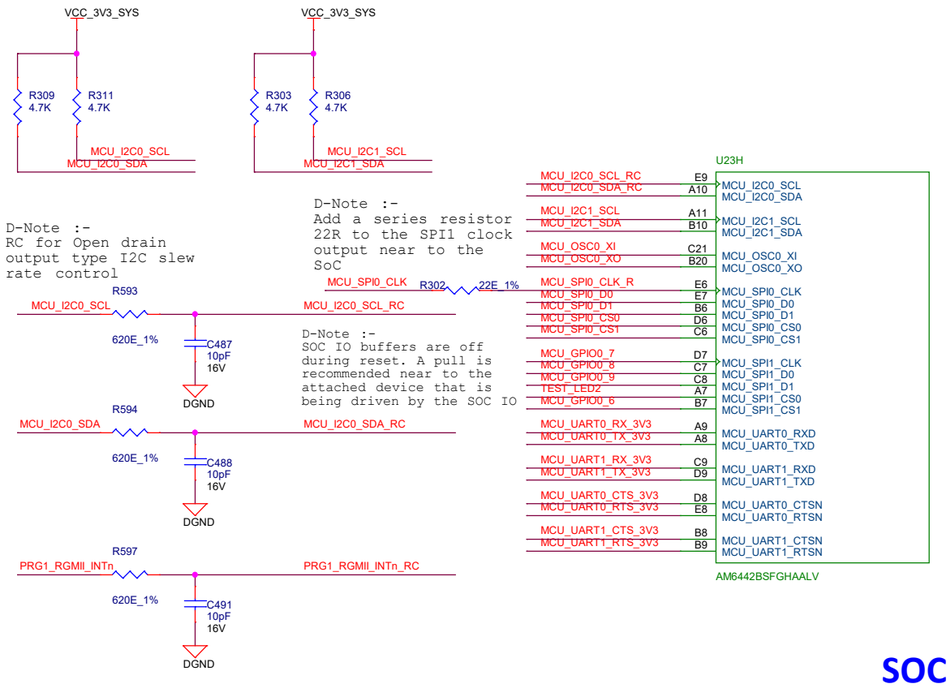


D-Note :-
It is recommended to connect the output from logic gate or discrete buffer (with fast rise time) as MCU_PORz input rather than slow rising open drain output (could glitch internally).



R-Note :-
Pulldown is enabled

D-Note :-
Not connecting a valid MCU_PORz could cause unpredictable and probably random behavior, since the device is not getting a valid reset, internal circuits would be in random states. Slow rising reset signal could cause glitches internal to the SOC reset circuit. Use a discrete buffer and have the fast rising output of the buffer drive the MCU_PORz is recommended

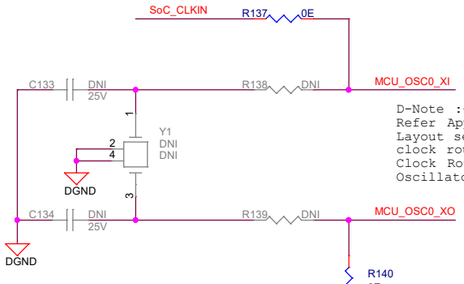


SOC - MCU (SAFETY) CONNECTOR

CRYSTAL FOR SOC MCU_OSC0

LPF Designed for 25MHz Cutoff
Have to change resistor and capacitor values accordingly

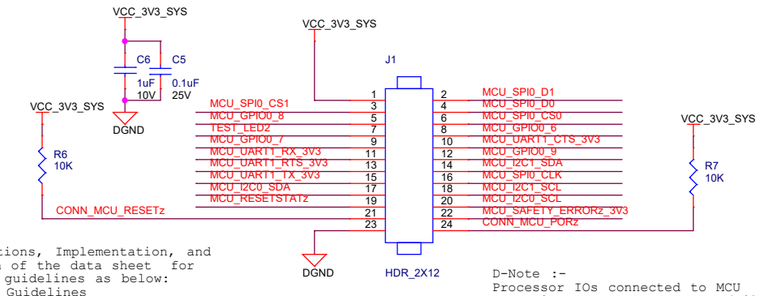
D-Note :-
Connect the 25 MHz crystal directly to the SOC Xi and Xo pins (No Series or parallel resistors are recommended).
The internal oscillator implements AGC (Automatic Gain Control) for amplitude control
Match the SOC and the EPHY crystal specs



D-Note :-
MCU_OSC0 has been validated only with a 25 MHz clock source, so that is the only frequency supported.
The datasheet shows MCU_OSC0 not starting until after the core voltage because there are some cases where the oscillator may not start until VDD_CORE is valid.
In most cases it will start as early as VDDS_OSC0, but this may not always be the case.
This diagram in the datasheet is showing the maximum start-up time, which must include the case where the delay is based on VDD_CORE being valid.

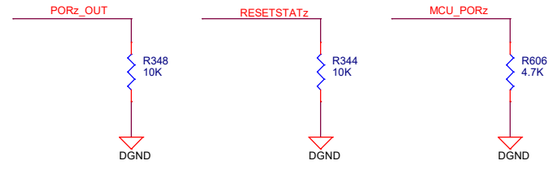
D-Note :-
Refer Applications, Implementation, and Layout section of the data sheet for clock routing guidelines as below:
Clock Routing Guidelines
Oscillator Routing

D-Note :-
XO should be grounded when an external oscillator is used
Refer SOC data sheet



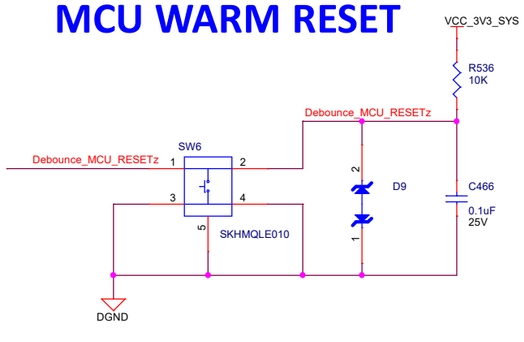
D-Note :-
Processor IOs connected to MCU expansion CONNECTOR are not fail-safe. No external input shall be applied when Starter Kit/EVM is not powered-up

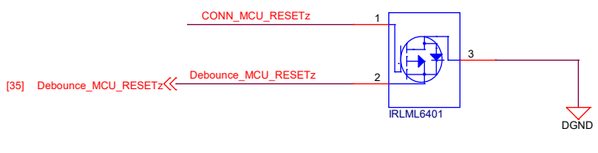
D-Note :-
MCU_PORz pulldown is used to hold the SOC in reset during power-up



D-Note :-
Pull-down resistors on PORz_OUT and RESETSTATz are provided to keep the signal low until the processor is released from reset during the power-up sequence

MCU WARM RESET





D-Note :-
No HFOSC0 registers are required to be changed. These registers should remain in their default state. Select the appropriate crystal circuit components that are compliant to the values defined in the MCU_OSC0 Crystal Circuit Requirements table. Read the Load Capacitance and Shunt Capacitance sections to select the appropriate crystal circuit components.

Off Page Connections

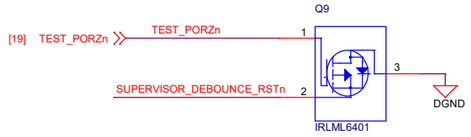
To HSE Connector
To level translator From Level Translator
To Boot Mode Section
From ICSSG Phy1&2
To User LED From Push button Switch

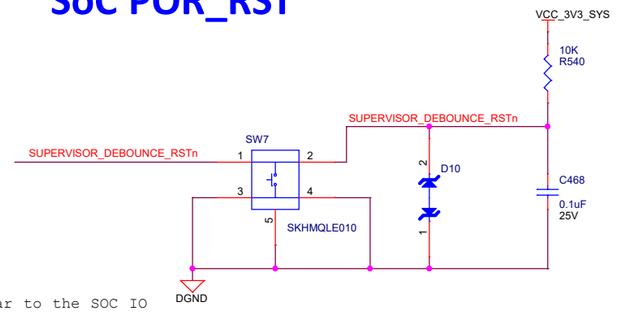
MCU_PORz
MCU_RESETz
MCU_RESETSTATz
MCU_PORz [27]
MCU_RESETz [27,35]
MCU_RESETSTATz [27]
MCU_SAFETY_ERRORz_3V3
MCU_SAFETY_ERRORz_1V8
MCU_SAFETY_ERRORz_3V3 [33]
MCU_SAFETY_ERRORz_1V8 [33]
PORz_OUT
PORz_OUT [13,16,17,18,20]
PRG1_RGMII_INTn
PRG1_RGMII_INTn [16,17,18]
TEST_LED2
MCU_GPIO0_6
TEST_LED2 [14]
MCU_GPIO0_6 [35]
SoC_CLKIN
MCU_UART0_TX_3V3
MCU_UART0_RX_3V3
MCU_UART0_CTS_3V3
MCU_UART0_RTS_3V3
SoC_CLKIN [31]
MCU_UART0_TX_3V3 [26]
MCU_UART0_RX_3V3 [26]
MCU_UART0_CTS_3V3 [26]
MCU_UART0_RTS_3V3 [26]

Designed for TI by Mistral Solutions Pvt Ltd

Title	MCU GENERAL & SAFETY CONNECTOR	
Size C	Variant Name = PROC101D(004) TMDS64EVM	Rev D
Date: Wednesday, June 12, 2024	Sheet 34 of 40	

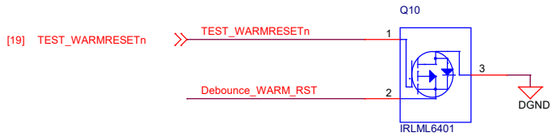
SoC POR_RST

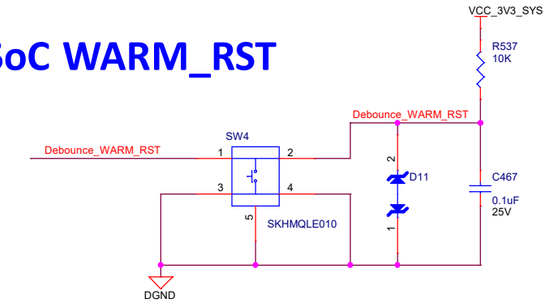




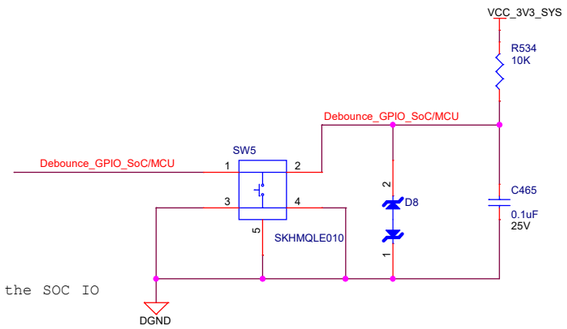
Cad Note :-
Place ESD diode near to the SOC IO

SoC WARM_RST





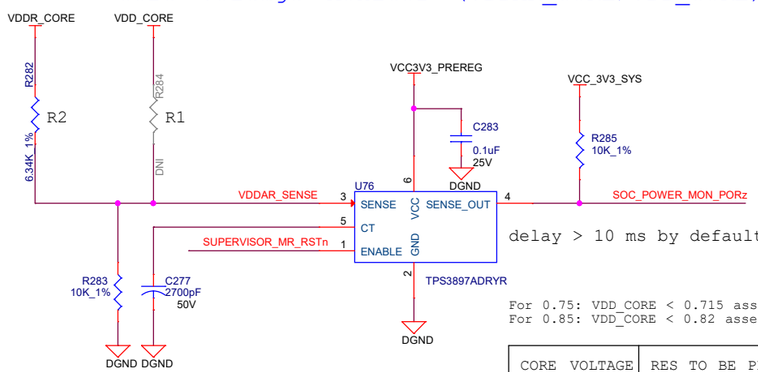
Cad Note :-
Place ESD diode near to the SOC IO



Cad Note :-
Place ESD diode near to the SOC IO

VOLTAGE SUPERVISOR

Core Voltage Monitor (VDDAR_CORE/VDD_CORE)

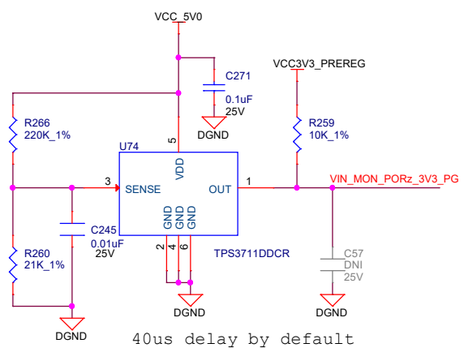


delay > 10 ms by default

For 0.75: VDD_CORE < 0.715 assert PORz
For 0.85: VDD_CORE < 0.82 asserts PORz

CORE VOLTAGE	RES TO BE PLACED
0.75V	R1 = 4.3K
0.85V	R2 = 6.34K

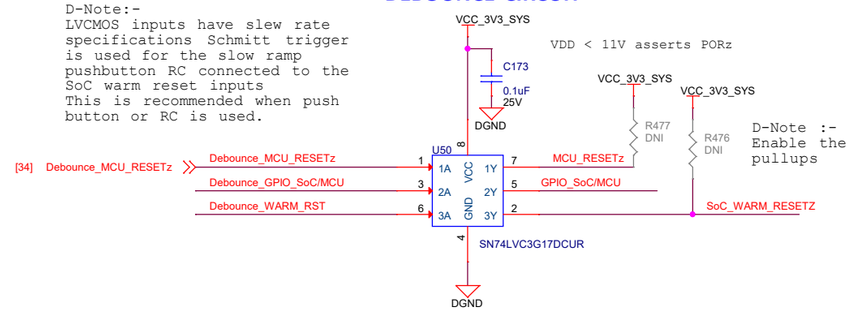
5V OUTPUT MONITOR (VCC_5V0)

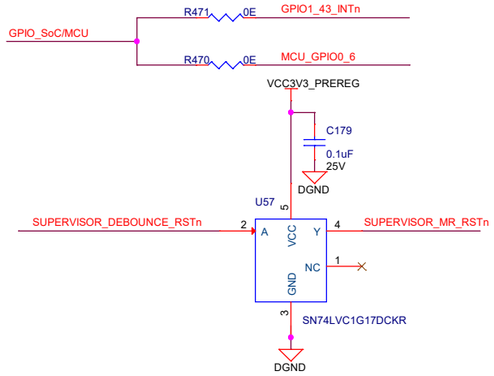


40us delay by default
VDD < 4.6 asserts PORz

DEBOUNCE CIRCUIT

D-Note:-
LVCMOS inputs have slew rate specifications Schmitt trigger is used for the slow ramp pushbutton RC connected to the SoC warm reset inputs
This is recommended when push button or RC is used.



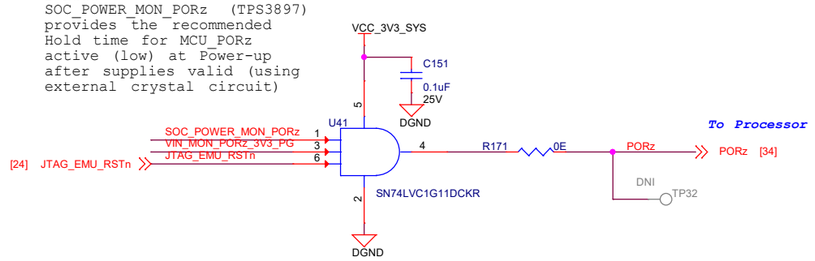


Off Page Connections

To Processor

VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG [37,39]
SoC_WARM_RESETZ	SoC_WARM_RESETZ [34]
GPIO1_43_INTn	GPIO1_43_INTn [29]
MCU_RESETz	MCU_RESETz [27,34]
MCU_GPIO0_6	MCU_GPIO0_6 [34]

D-Note :-
SOC_POWER_MON_PORz (TPS3897) provides the recommended Hold time for MCU_PORz active (low) at Power-up after supplies valid (using external crystal circuit)



D-Note :-
MCU_PORz input have a maximum rise/fall time requirements when PMIC_POWERGOOD or similar signal is connected to the MCU_PORz. Adjust the pullup to minimize the rise time (100..200 ns) when using open drain output.
MCU_PORz is fail-safe and 3.3v tolerant. Therefore, you can pull the MCU_PORz signal to 1.8V or 3.3V.

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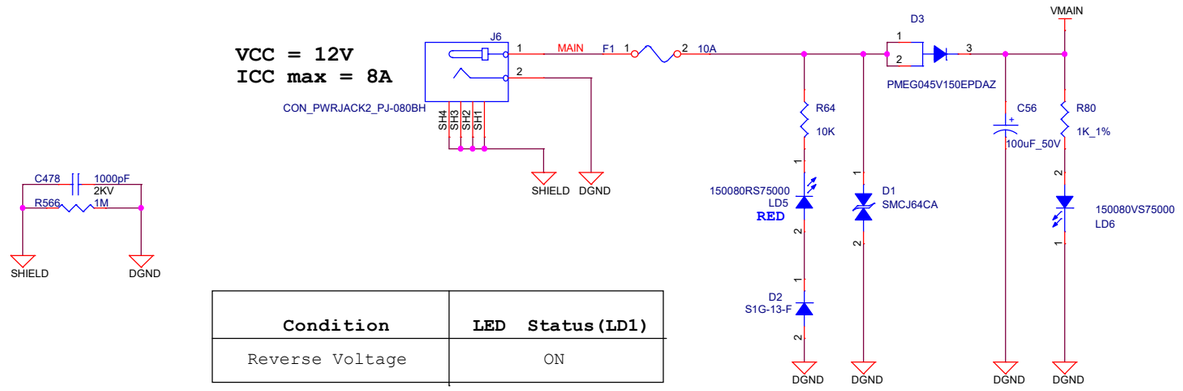
TEXAS INSTRUMENTS MISTRAL

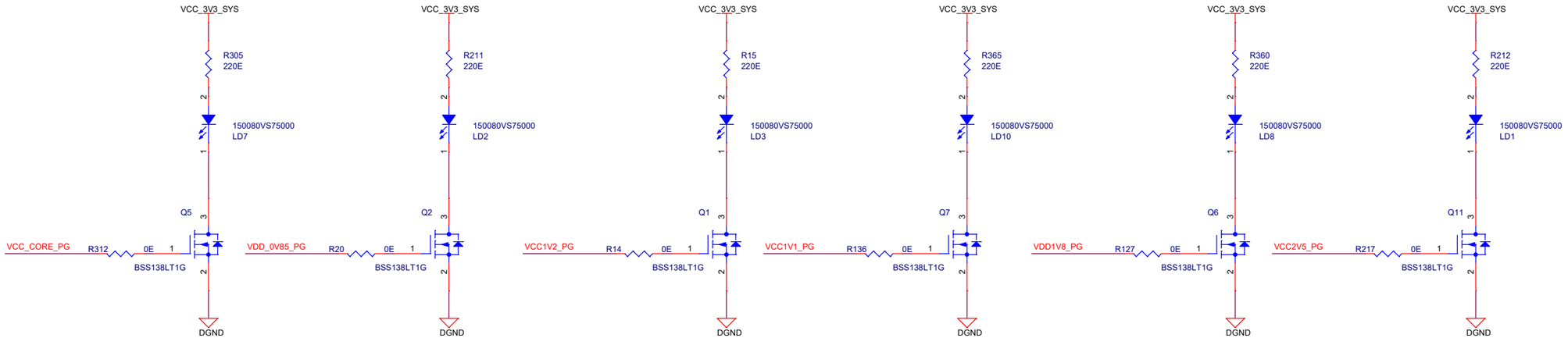
Title	DEBOUNCE CIRCUIT & VOLTAGE SUPERVISOR	
Size	Variant Name = PROC101D(004) TMDS64EVM	Rev
C		D
Date: Wednesday, June 12, 2024	Sheet 35 of 40	

MAIN INPUT 12V DC

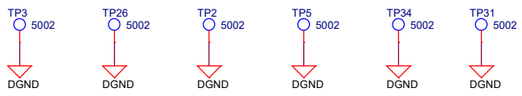


Condition	LED Status(LD1)
Reverse Voltage	ON

POWER INDICATION LED's



Ground test points



Off Page Connections

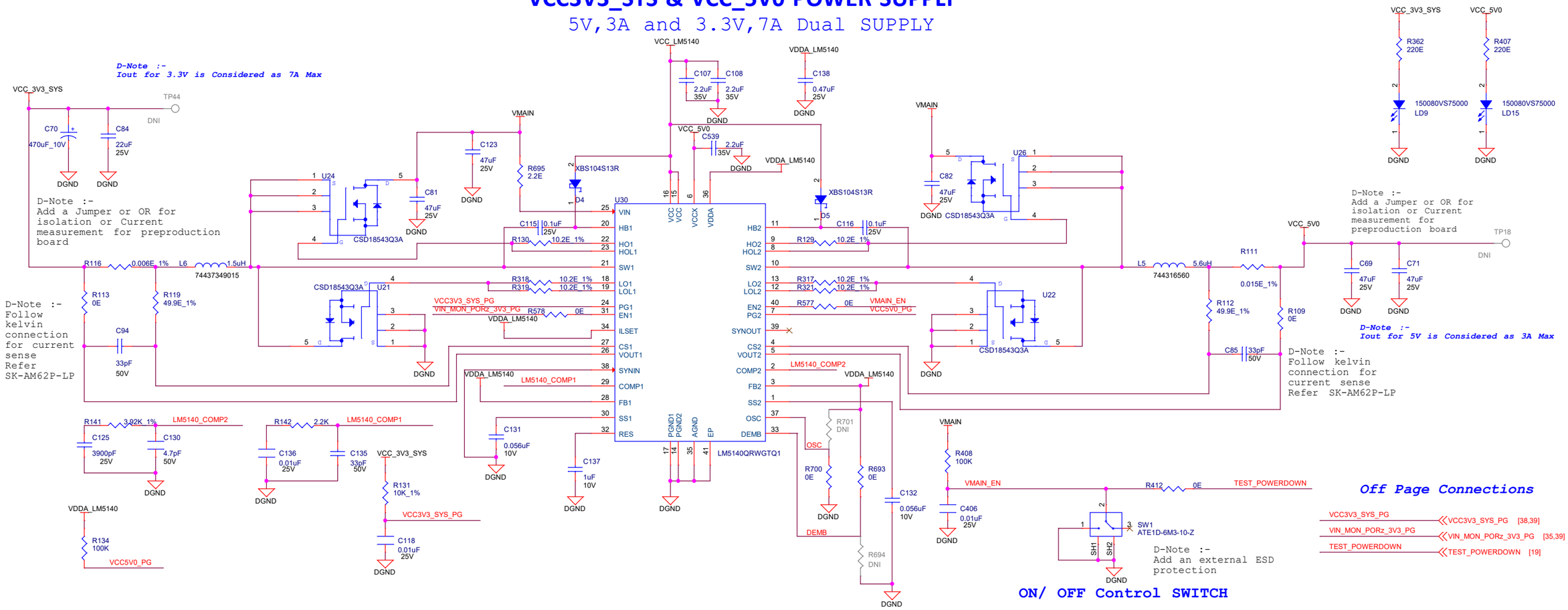
VCC_CORE_PG	VCC_CORE_PG	[37,38]
VDD_0V85_PG	VDD_0V85_PG	[38]
VCC1V2_PG	VCC1V2_PG	[38]
VCC1V1_PG	VCC1V1_PG	[39]
VDD1V8_PG	VDD1V8_PG	[38]
VCC2V5_PG	VCC2V5_PG	[39]

Designed for TI by Mistral Solutions Pvt Ltd

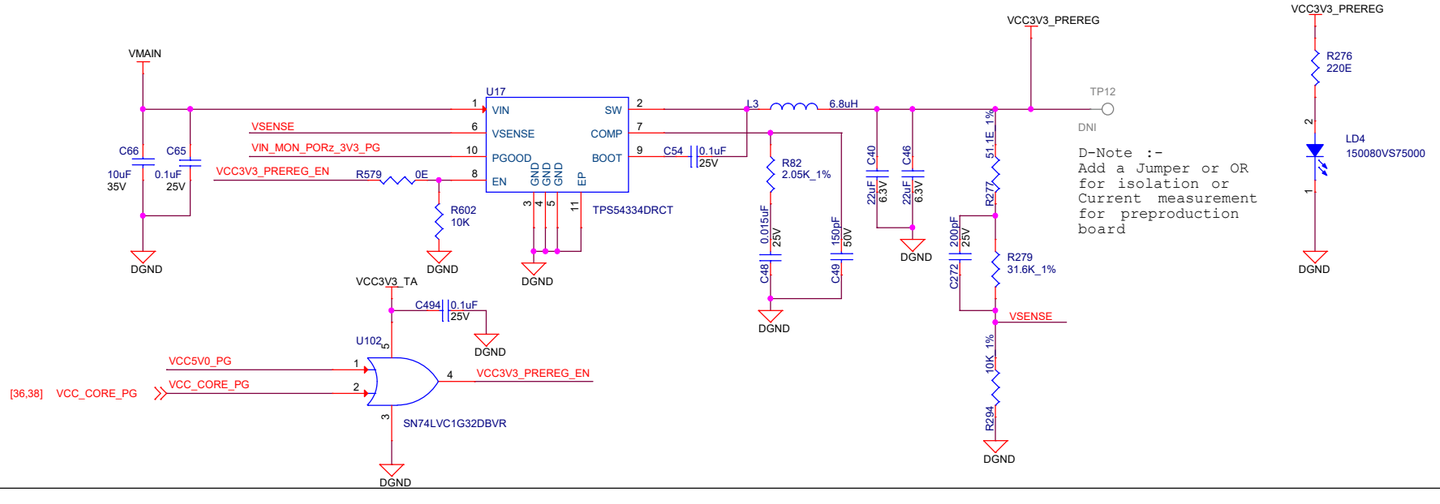
Title	MAIN 12V POWERSUPPLY	
Size: C	Variant Name = PROC101D(004) TMDS64EVM	Rev: D
Date: Wednesday, June 12, 2024	Sheet 36 of 40	

VCC3V3_SYS & VCC_5V0 POWER SUPPLY

5V,3A and 3.3V,7A Dual SUPPLY



PREREG 3.3V, 3.0AMPS SUPPLY



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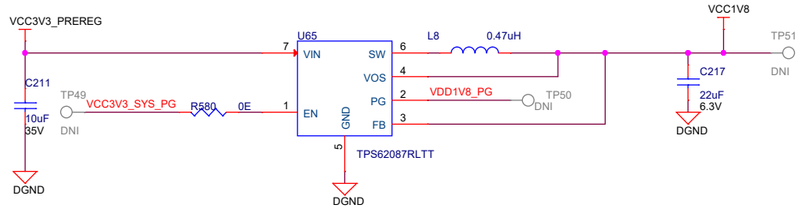
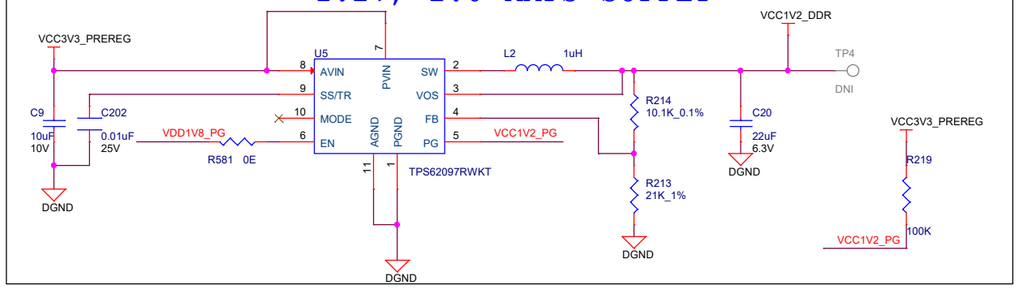
Title	DUAL & PREREG REGULATOR	
Size C	Variant Name = PROC101D(004) TMDS64EVM	Rev D
Date: Wednesday, June 12, 2024	Sheet 37 of 40	

SoC POWER SUPPLIES

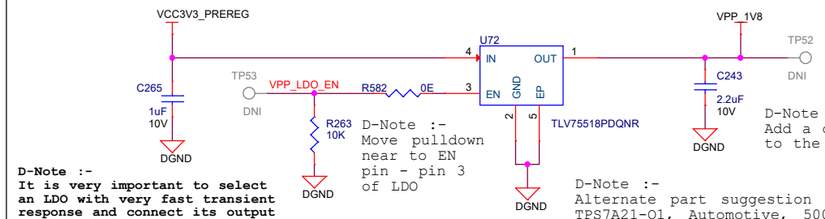
1.8V IO, 3.0 AMPS SUPPLY



1.2V, 2.0 AMPS SUPPLY



1.8V VPP, 0.5 AMP SUPPLY



D-Note :-
Add a series resistor to the VPP supply pin for isolation or testing

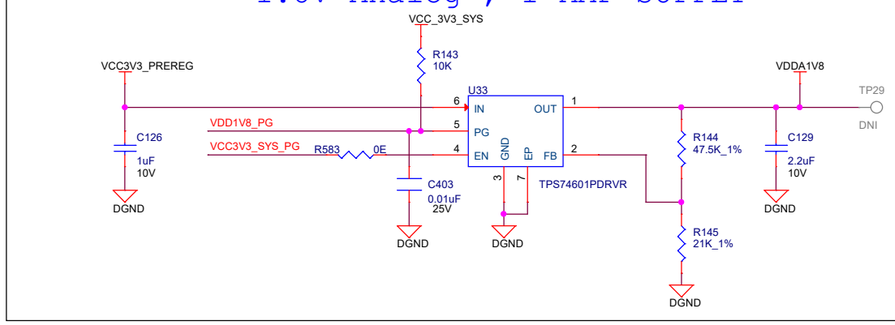
D-Note :-
Move pulldown near to EN pin - pin 3 of LDO

D-Note :-
Add a decap 0.1 uF near to the SoC VPP pin

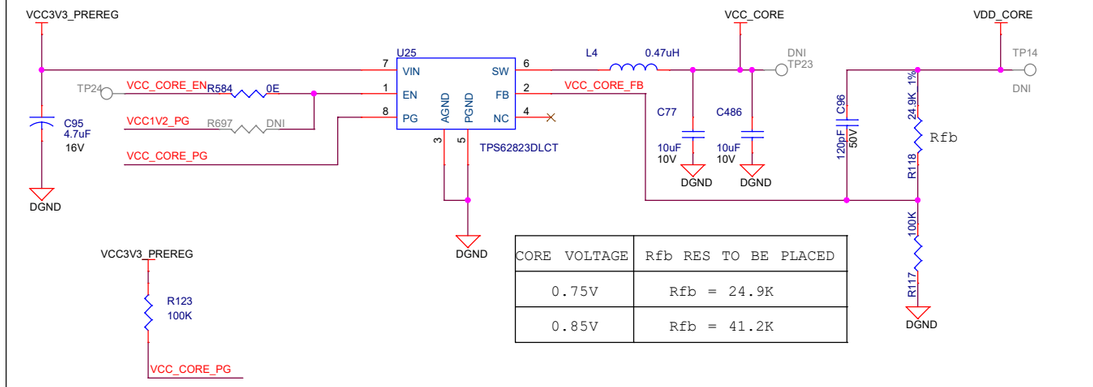
D-Note :-
It is very important to select an LDO with very fast transient response and connect its output to the VPP pin with a low loop inductance path to ensure it is able to source the high transient load, where the VPP pin never drops below the minimum operating voltage.

D-Note :-
Alternate part suggestion
TPS7A21-Q1, Automotive, 500mA, low-noise ultra-low-IQ high-PSRR low-dropout (LDO) voltage regulator

1.8V Analog , 1 AMP SUPPLY

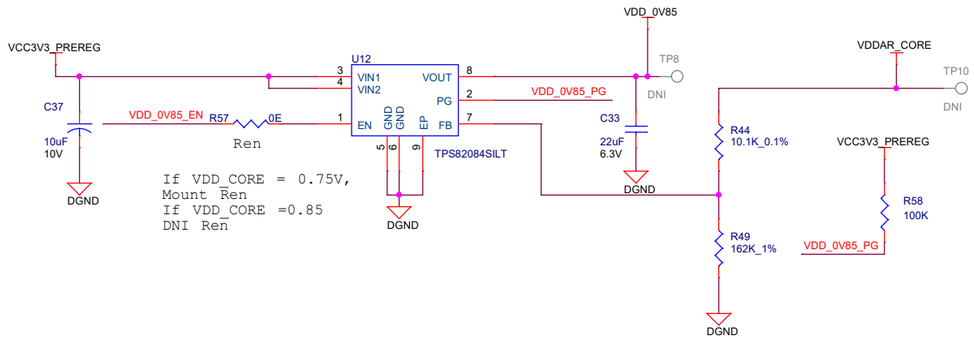


0.75 /0.85V, 3.0 AMPS SUPPLY



CORE VOLTAGE	Rfb RES TO BE PLACED
0.75V	Rfb = 24.9K
0.85V	Rfb = 41.2K

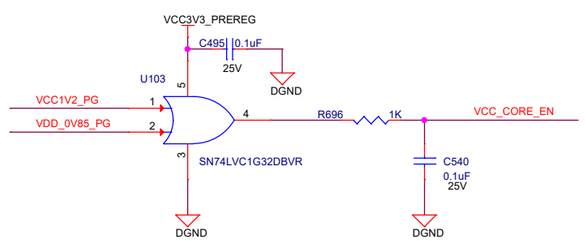
0.85 V, 1.5 AMPS SUPPLY

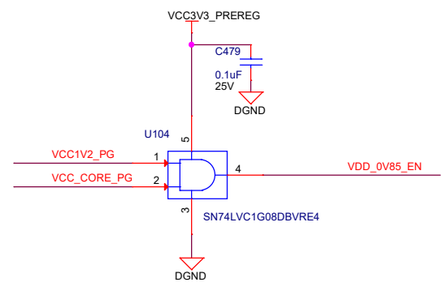


If VDD_CORE = 0.75V,
Mount Ren
If VDD_CORE =0.85
DNI Ren

D-Note :-
An alternative way to source the VPP is to use an external supply. The required caps and termination/Discharge resistor are recommended to be placed near to the SoC VPP pin.
SOC GPIO output can be used to control or time the external power supply output

D-Note :-
Given the transient current requirement during eFuse programming, using load switch or FET switch may not be a recommended approach,
It is recommended to use an LDO. A load or FET switch is likely to have too much voltage drop that can't be compensated like when using an LDO.





Off Page Connections

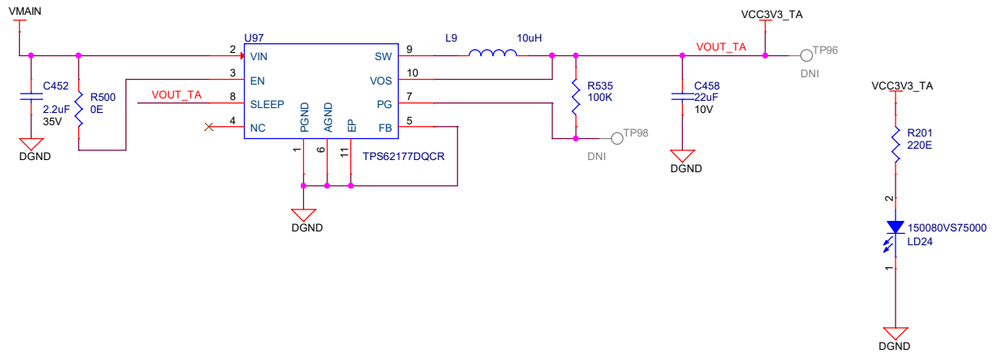
[36,37]	VCC_CORE_PG	VCC_CORE_PG
[36]	VDD_0V85_PG	VDD_0V85_PG
[36]	VCC1V2_PG	VCC1V2_PG
[36]	VDD1V8_PG	VDD1V8_PG
[33]	VPP_LDO_EN	VPP_LDO_EN
[35,37,39]	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG
[37,39]	VCC3V3_SYS_PG	VCC3V3_SYS_PG

Designed for TI by Mistral Solutions Pvt Ltd

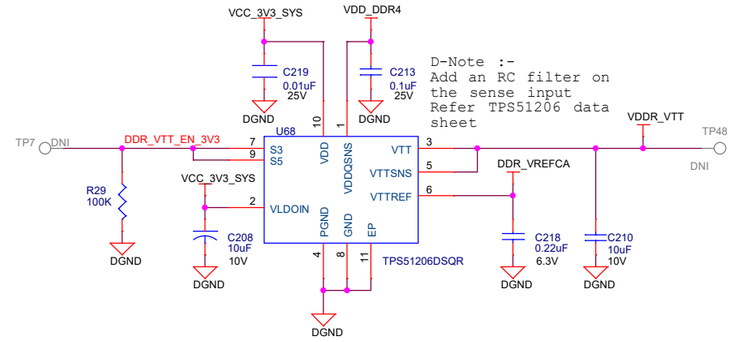
Title	SoC POWER SUPPLY	
Size: C	Variant Name = PROC101D(004) TMDS64EVM	Rev: D
Date: Wednesday, June 12, 2024	Sheet 38 of 40	

PERIPHERAL POWER SUPPLIES

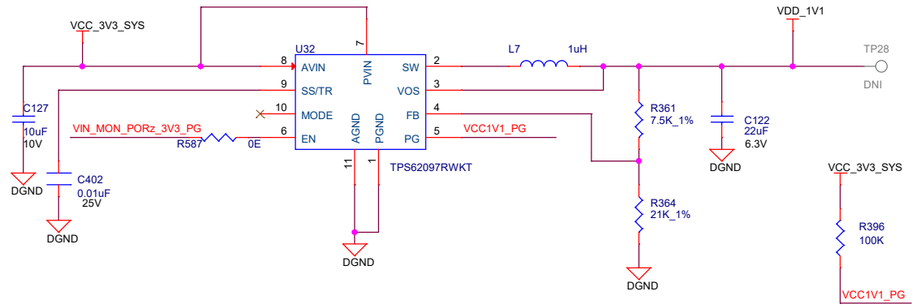
TEST AUTOMATION BOARD POWER SUPPLY



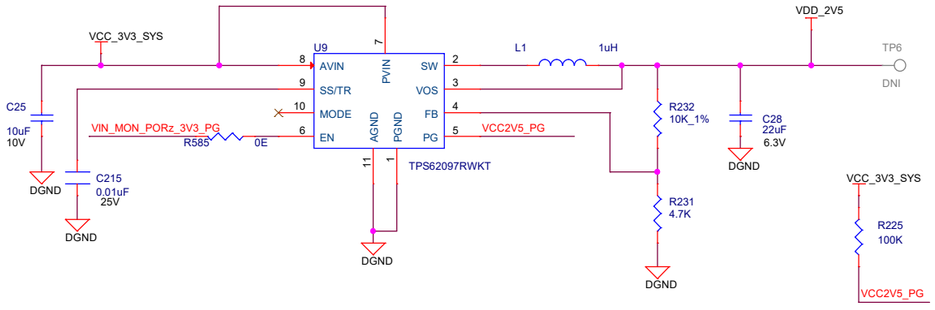
VTT SUPPLY FOR DDR4



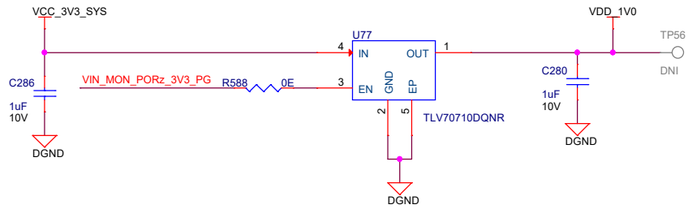
1.1 V ETHERNET PHY (DP83869) POWER SUPPLY



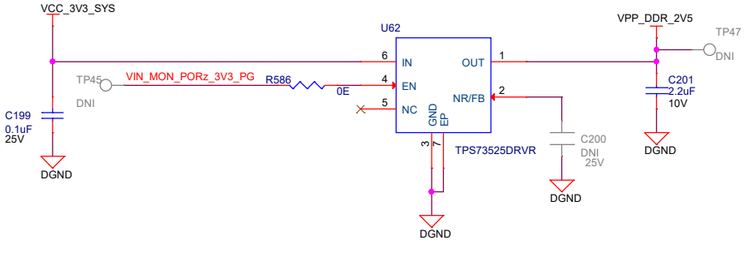
2.5 V, 2.0 AMPS SUPPLY



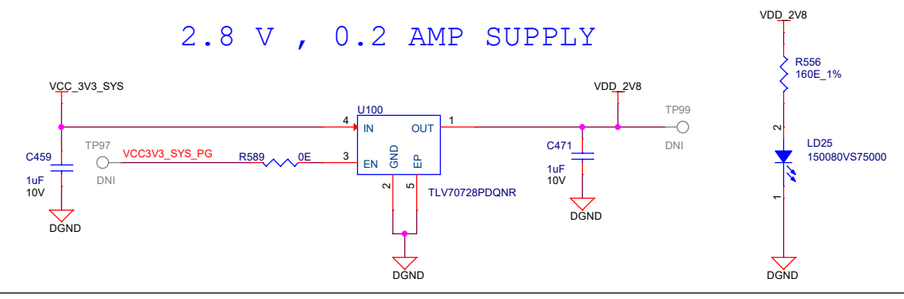
1.0 V ETHERNET PHY (DP83867) POWER SUPPLY



2.5V, 0.5 AMP SUPPLY



2.8 V , 0.2 AMP SUPPLY



Off Page Connections

[33] DDR_VTT_EN_3V3
[36] VCC2V5_PG
[36] VCC1V1_PG
[37,38] VCC3V3_SYS_PG
[35,37] VIN_MON_PORz_3V3_PG

DDR_VTT_EN_3V3
VCC2V5_PG
VCC1V1_PG
VCC3V3_SYS_PG
VIN_MON_PORz_3V3_PG

Designed for TI by Mistral Solutions Pvt Ltd

Title	PERIPHERAL POWER SUPPLY	
Size: C	Variant Name = PROC101D(004) TMDS64EVM	Rev: D
Date: Wednesday, June 12, 2024	Sheet 39 of 40	

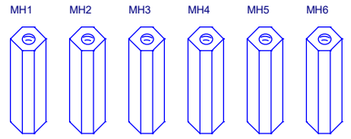
MOUNTING HARDWARE

R-Note :-
Refer STRAP CONFIGURATION OF ETHERNET PHYS page of the SK schematics

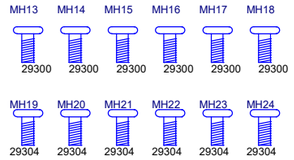
ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

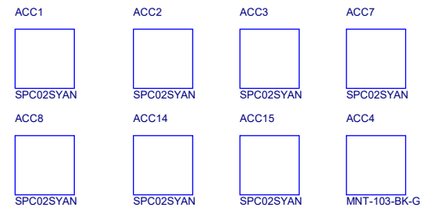
STANDOFFs



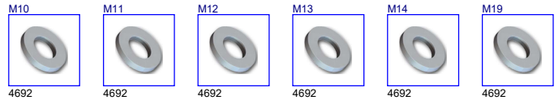
SCREWS



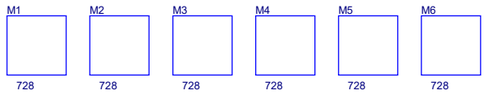
JUMPERs



WASHER's



RUBBER FEET



FIDUCIALS

FID1 DNI
FID2 DNI
FID3 DNI

TI EVM FLYERS

ACC11 SZZC019i
ACC12 SSZZ027

Socket & Processor as Accessories

ACC10 DNI
ACC13 DNI

BARE PCB

PROC101
PROC101D

LABELS

Board Serial No.

LBL1 PCB LABEL DNI

Assembly Revision

LBL3 PCB LABEL DNI

ORDERABLE PART NO

LBL2 PCB LABEL DNI

Orderable part number	
Variant	**Label Text**
001	TMDS64GPEVM
002	TMDS243GPEVM
003	TMDS64HSEVM
004	TMDS64EVM
005	TMDS243EVM

LOGOs

PCB LOGO DNI — Texas Intruments
PCB LOGO DNI — For Evaluation only; not FCC approved for resale
PCB LOGO DNI — WEEE Mark
PCB LOGO DNI — CE Mark

Designed for TI by Mistral Solutions Pvt Ltd

Title	HARDWARE SCHEMATICS	
Size C	Variant Name = PROC101D(004) TMDS64EVM	Rev D
Date: Wednesday, June 12, 2024	Sheet 40 of 40	