Application Report
SPRABN2–March 2019

AM335x schematic checklist

Catalog Processors

ABSTRACT

This application report highlights board design recommendations when using the AM335x family of devices. The recommendations are intended to supplement the information provided in the device-specific technical reference manual and data sheet. It is not an all-encompassing list, but rather a succinct reference for board designers that highlights certain caveats and care-abouts related to different use cases.

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1 Introduction

This application report applies to the AM335x family of devices listed on the AM335x Cortex-A8 Overview. On this overview page are links to TI hardware designs based on AM335x.

For more information, see the device-specific product pages that contain up-to-date information and resources, including application reports and user's guides to facilitate schematic and board design.

2 Recommendations Specific to AM335x

2.1 Unused Signals

Signals on interfaces that are unused can typically be left as no connect. Many of the IOs have a Pad Control Register that provides control over the input capabilities of the I/O (RXACTIVE field in each conf_<module>_<pin> register). For more details, see the *Control Module* chapter of the *AM335x and AMIC110 Sitara™ Processors Technical Reference Manual*. In initialization, software should disable the I/Os that are no connects (RXACTIVE=0) as soon as possible. This RXACTIVE field defaults to "input active" for most signals, which means there is a potential for some leakage during powerup of the chip if the input floats to a mid-supply level before the software can initialize the I/O. This should only be a concern if you are attempting to power up the design with a minimum power consumption. Most designs should be able to tolerate this small amount of leakage in each floating I/O until the software has a change to disable it. After disabling the I/O, no leakage will occur.

2.2 System Issues

2.2.1 Pinmux

All pinmux settings must be verified using the TI Pinmux tool to ensure valid IOSets have been used. The tool can be downloaded from Pin Mux Tool.

2.2.2 Pullups

- Ensure all pullups connected to AM335x are pulled up to the correct I/O voltage to avoid any leakage between the I/O rails of AM335x. Each terminal has an associated voltage used to power its I/O cell. This can be found in the AM335x data sheet, in the Ball Characteristics table under the "ZCE Power/ ZCZ Power" column.
  - For example, if you want to pull up terminal SPI0_CS0 in any mux mode (gpio0_5, i2c1_scl, and so forth), pull up the signal to VDDSHV6.

2.2.3 General Debug

Output clocks CLKOUT1 and CLKOUT2 are present on terminals XDMA_EVENT_INTR0 and XDMA_EVENT_INTR1. If these are not used in your design, it is good to have test points on these signals to be able to monitor internal clocks.

2.2.4 Warm Reset

Be sure to check the device-specific TRM uses for warm reset. The warm reset signal should be used as an input (for example, connected to a push button) or output (to reset external devices during a POR). It cannot be used for both because of an errata with the clocking of the debounce circuitry.

2.2.5 Peripheral Clocking

Several peripheral clocks are required to have RXACTIVE bit set as input because they are used to retime read data returning to the device. We also recommend a series resistor located as close to the device as possible to reduce reflections on the clock. For the following peripherals, the associated signals should have a series resistor (33 Ω) in line as close to the processor as possible when used in master mode (AM335x drives the clock).

- GPMC - GPMC_CLK
- MMC - MMC_CLK
- SPI - SPI_CLK
- McASP (all clocks and frame syncs)

2.3 Low-Power Considerations

If you are designing for low power, here are some tips to help you optimize your design:

- The TPS65217C and TPS65217D do not support RTC-only mode. TPS65218 does.
- On early prototype boards, it is recommended to include small shunt resistors in the voltage rail paths of each of the following rails of AM335x: VDD_MPU, VDD_CORE, VDDS, VDDSHV1-6, VDDS_DDR. This will help you measure the power consumption of each rail and potential pinpoint high power consumption during development. You may also want to add these shunt resistors for other devices power supplies to be able to measure power for key devices. The AM335x EVMs have examples of these shunt resistors.
  - For production, these shunt resistors should be removed from the design (turned into a continuous plane), especially for designs using Smart Reflex.
- Only GPIO0 signals are capable of wakeup signaling (to wakeup from DeepSleep or RTC modes). Connect wakeup sources only to these GPIOs (GPIO0_0 to GPIO0_31).

- For your main clock (24 MHz, and so forth) you can use either a crystal or a LVCMOS square wave clock. There is a power benefit to using a crystal because there is hardware inside the chip that can shutoff the crystal entirely during DeepSleep0 (DS0). When using a square wave clock there is unfortunately no mechanism for automatically turning the clock off and on, which results in additional current consumption.
- If your design uses VTT you should use a pin from GPIO bank 0 to control the regulator. This will enable the regulator to be switched off during DS0.
- The Cortex-M3 uses I2C0 for communication with the Power Management IC (PMIC) for purposes of reducing the voltage during DS0.

2.4 Clocking

- If you do not need RTC-only mode and the RTC timer feature, you do not need to include a 32 KHz crystal. The 32 KHz reference can come from the high frequency clock. Leave the RTC_XTALIN/RTC_XTALOUT pins as NC.
- Per Advisory 1.0.30 in the device Silicon Errata, VSS_OSC and VSS_RTC should be connected to system ground.
- It is preferable to always have bias and dampening resistors that can help tune the crystal later. For more details, see the *Clock Specifications* section of the device-specific data sheet.

2.5 General DDR Guidelines

These guidelines are applicable for all DDR designs:

- It is very important to follow the DDR routing guidelines for your DDR type in the AM335x data sheet. These guidelines are very important to ensure a proper DDR design.
- Ensure resistor for DDR_VTP is a high precision resistor as specified in the data sheet. A 49.9 Ω 1% resistor is less expensive than a 50 Ω 2% resistor and can be used for the DDR_VTP pin for cost sensitive designs.
- When using a resistor divider for DDR_VREF, ensure resistors are high precision resistors as specified in the device-specific data sheet
- Allow for adequate decoupling capacitors on the DDR power rails both at the AM335x as well as the DDR SDRAM device(s)

2.5.1 DDR2

DDR_VREF can be derived using a resistor divider with decoupling to both DDR supply and ground. Follow the recommendations as documented in the *DDR2 Routing Guidelines* section in the device-specific data sheet.

2.5.2 DDR3

- For point-to-point DDR3 topologies (single x16 DDR3 IC), VTT termination is not needed. Designs using two x8 DDR3 IC's may wish to consider using a termination regulator such as the TPS51200 for the address/control signals.
- If using VTT termination:
  - Do not use VTT termination for DDR_RESET. It should be connected directly from the AM335x to DDR.
  - If VTT regulator is disabled during low power modes (by programming EN=0 using the TPS51200), DDR_CKE should not be connected to termination resistors. The active discharge capability of the regulator can cause a brief dip on this signal, which can be problematic. This would likely be true of any VTT regulator with active discharge capability.
  - Termination for clock signals is VDDS_DDR (along with an AC coupling capacitor), whereas, all other signals need to use VTT for the termination voltage. For more details, see the device-specific data sheet.

- If not using VTT termination, VREF should be obtained using a resistor divider (10Kohm 1%) with capacitive decoupling to ground, and should be used as a reference for both CA and DQ pins on the memory, as well as the VREF signal on AM335x. Be sure to use high precision (1%) resistors as specified in the data sheet. When not using VTT, be especially sure to follow the routing guidelines in the device-specific data sheet.

2.6 MultiMedia Card/ (MMC)

- Include a 33 Ω series resistor on MMCx_CLK (as close to the processor as possible). This signal is used as an input on read transactions. The resistor eliminates possible signal reflections on the signal that can cause false clock transitions.
  - This also requires you to set RXACTIVE=1 in the pinmux configuration for the MMC_CLK signal.
- When connecting a device (card or eMMC), include 10k pullups on RST#, CMD, and all DAT signals.

2.7 Inter-Integrated Circuit (I2C)

- Pullups on both I2C signals (I2C_DATA and I2C_CLK) should be 4.7K. Ensure the pullups connect to the correct I/O voltage rail. For more information, see Section 2.2.2.
- If you are planning to use TI's software Processor SDK, be sure to connect I2C0 to the PMIC, as this is the port used for PMIC control.

2.8 LCD

Be sure to consult the silicon errata for the proper pinout of the LCD interface. There is a usage note titled, "LCD: Color Assignments of LCD_DATA Terminals" in the device Silicon Errata.

Note that the AM335x EVM "fixes" the pin mapping through a CPLD on the daughterboard, so be extra careful to get the proper mapping!

- A good example of a 24-bit hookup comes from the AM335x Starter Kit shown in Figure 1.

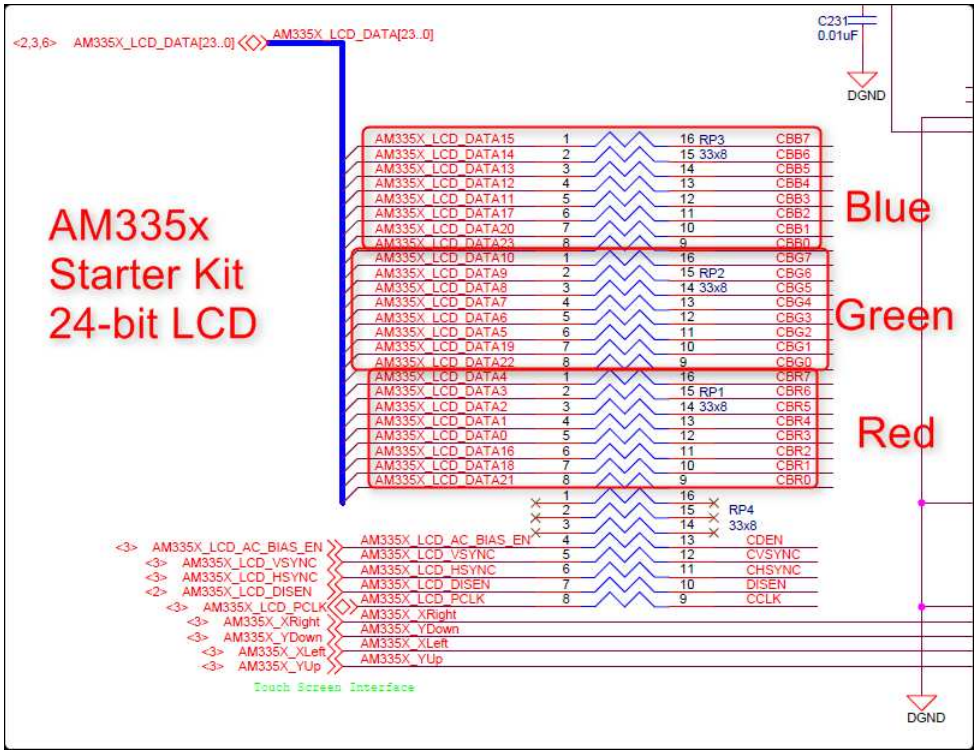

Figure 1. AM335x Starter Kit, 24-Bit LCD

- A good example of a 16-bit hookup comes from the BeagleBone Black that is shown in Figure 2. In this case, the other LCD pins were preserved for use by capes.

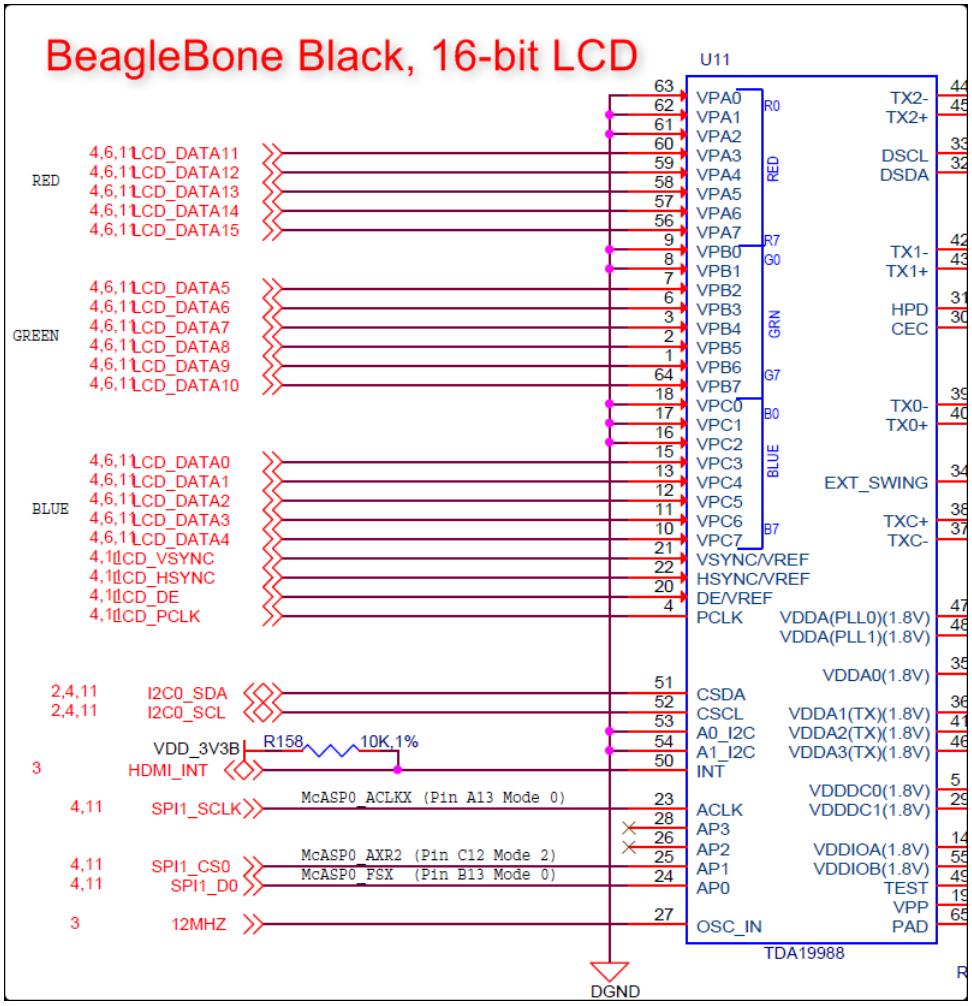

Figure 2. BeagleBone Black, 16-Bit LCD

- Notice that Red and Blue swap positions depending on whether you are outputting in 16-bit mode vs 24-bit mode (that is, the errata).

2.9 Power

- AM335x Power Solution

Table 1. AM335x Power Solutions

	TPS65217x				TPS65218	TPS65910x		TPS650250
	A	B	C	D		A	A3	
Battery Charger	Yes				No	No		No
Boost	WLED Backlighting				No	5 V Boost		No
AM335x OPP	OPP40, OPP100	OPP50, OPP100, OPP120, Turbo, Nitro			OPP50, OPP100, OPP120, Turbo, Nitro	OPP50, OPP100, OPP120, Turbo, Nitro		OPP50, OPP100
Power	3 DCDC @ 1.2A 4 LDO				3 DCDC@ 1.8 V 1 DCDC @ 1.6A 2 Low-q DCDC for RTC 1 LDO and 3 LSW	2 DCDC @ 1.5A 1 DCDC @ 1A 9 LDO		1 DCDC @ 1.6A 2 DCDC @ 0.8A 3 LDO
Input Voltage Range	2.7 - 5.8 V				2.5 - 6.5 V	2.7 - 5.5 V		2.5 - 6.5 V
DVFS/Smart Reflex	Yes				Yes	Yes		No
RTC-Only Mode	Yes		No		Yes	Yes		No
DDR	DDR2, LPDDR1		DDR3	DDR3L	DDR3, DDR3L	DDR2, LPDDR1	DDR3	DDR2, LPDDR1, DDR3
Package	48-pin QDN, 6 mm x 6 mm				32-pin QFN, 5 mm x 5 mm	48-pin QFN, 6 mm x 6 mm		32-pin QFN, 5 mm x 5 mm
T_A	- 40°C to 105°C				- 40°C to 85°C	- 40°C to 85°C		- 40°C to 85°C

- Check the product pages on each device-specific application report when connecting the PMIC to AM335x. Also check the device-specific data sheet for specific part numbers to be used for the AM335x.
  - *Powering the AM335x With the TPS65217x*
  - *Powering the AM335x With the TPS650250*
  - *TPS65910x User's Guide for AM335x Processors User's Guide*
  - *TPS65910x Schematic Checklist*
- Ensure current capabilities of DCDC switchers and LDOs meet the maximum demand of all devices that are attached. You can find the maximum current draw of all AM335x I/O rails in the data sheet. If these rails from the PMIC also power other devices, the maximum current draw of these devices need to be taken into consideration as well.
- Ensure I2C0 is used for communication to PMIC. All TI software distributions (Processor SDK, and so forth) assumes the use of this interface with the PMIC.

2.10 Touchscreen

- Recommend adding 0ohm resistor to VDDA_ADC in case you need to add a filter for noise on the ADC.
- Check out the sampling voltage must not exceed the voltage of reference. Otherwise, it will affect the whole TSC_ADC system. For example, if you add pull up to 3.0 V at the last four channel, this will lead to the abnormal work of the whole system, including the first four.
- If the AM335x ADC/Touchscreen is not used, connect all TSC_ADC terminals (VREFP, VREFN, AIN[7:0], VDDA_ADC, and VSSA_ADC) to same ground as all VSS terminals.

2.10.1 If ADC/Touchscreen is not Used

- Connect all TSC_ADC terminals (VREFP, VREFN, AIN[7:0], VDDA_ADC, and VSSA_ADC) to same ground as all VSS terminals.

2.11 USB

For more details, see *High-speed interface layout guidelines*.

The AM335x USB0_ID and USB1_ID terminals should never be connected to any external voltage source. These terminals should be open-circuit when the respective USB port is configured to operate in USB peripheral mode, or should be connected to ground when the respective USB port is configured to operate in USB host mode.

USBx_DP and USB_DM should never have any series resistors or capacitance on these signals. These signals should be straight traces to the connector with no stubs or test points.

Typical connections for a USB peripheral:

- USBx_DP and USBx_DM are connected directly to the USB connector
- USBx_CE can be used if supporting charging. This generally would be connected to the enable of a charging source for the battery.
- USBx_ID can be left unconnected
- USBx_DRVVBUS is not used and can be left unconnected
- USBx_VBUS should be connected directly to the VBUS pin on the USB connector

Typical connections for a USB host:

- USBx_DP and USBx_DM are connected directly to the USB connector
- USBx_CE is typically not used and can be left unconnected
- USDx_ID should be grounded
- USBx_DRVVBUS should be connected to the enable of the 5 V VBUS power source.
- USBx_VBUS should be connected to the output of the 5 V VBUS power source

Typical connections for a USB host with USB hub:

- USBx_DP and USBx_DM are connected directly to the USB hub upstream port. The hub then distributes these signals to the downstream ports as needed.
- USBx_CE is typically not used and can be left unconnected
- USDx_ID should be grounded to enable host mode.
- USBx_DRVVBUS should be connected to the enable of the 5 V VBUS power source.
- USBx_VBUS should be connected to the output of the 5 V VBUS power source. It is also connected to the VBUS detect on the hub, which allows the hub to selectively enable or disable typically through a power switch to each downstream port.

2.11.1 If USB0 or USB1 is not Used

- If USB0 or USB1 is not used:
  - Connect the respective VDDA1P8V_USB terminal to any 1.8-V power supply and the respective VDDA3P3V_USB terminal to any 3.3-V power supply. If the system does not have a 3.3-V power supply, the VDDA3P3V_USB terminal may be connected to ground.
  - The OTG_PWRDN and CM_PWRDN bits in the respective USB_CTRL register can be used to power down the unused USB PHY to minimize power supply leakage current. These bits default to the powered-up state after the AM335x device has been reset. The USB PHY can be powered down by setting both of these bits to "1".
  - The respective VBUS, ID, DP, and DM terminals may be connected to ground or left floating.
  - The respective CE terminal should be left floating.

2.12 External Interrupt (EXTINTn)

This signal is active high for PG1.0 and active low for PG2.x. Boards designed to support all silicon revisions may want contain population options for both in case you move between different revisions of the AM335x during development. New designs are expected to use only PG2.1.

This signal connects directly to the Cortex-A8 interrupt controller, which as a result makes this a level sensitive pin. It is recommended to consider using a GPIO signal instead of EXTINTn. The GPIO pins offer more flexibility with respect to polarity as well as the ability to be edge triggered.

2.13 Ethernet

While no series resistors are required for MII/RMII/RGMII, it is prudent include zero-Ω stuff options for the TX and RX lines. Ideally, these option resistors should be as small as possible (0402 or smaller recommended) and should be placed as close to the transmitter as possible.

2.14 RTC

Table 2 describes what to do with each pin related to RTC functionality. Three use case scenarios are provided:

- RTC-only mode: If you will be using the low power RTC-only mode. This use case allows low power operation of the AM335x by allowing only the RTC power supply to be ON while all the remaining supplies are OFF.
- RTC timer functionality but no RTC-only mode: If you will be using the RTC feature but do not need RTC-only mode. This use case allows you to use the Real Time clocking features (keeping time), but you do not need to support the low power RTC-only mode.

- RTC feature disabled: If you will never use the RTC features. In this use case, the RTC functions are fully disabled.

Table 2. RTC

Pin	Function	RTC-Only Mode	RTC Timer Functionality but no RTC-Only Mode	RTC Feature Disabled
VDDS_RTC	1.8 V power supply	Always on RTC 1.8 V power supply	Any AM335x 1.8 V power supply (3)	Any AM335x 1.8 V power supply (3)
CAP_VDD_RTC	RTC core voltage input/LDO output (1)	1 uF decoupling capacitor to VSS	VDD_CORE (3)	VDD_CORE (4)
RTC_KALDO_ENn	Internal LDO enable input	VSS	VDDS_RTC	VDDS_RTC
RTC_PWRONRSTn	RTC power on reset input	1.8 V RTC power on reset (2)	1.8 V PWRONRSTn (5)	VSS
PMIC_POWER_EN	PMIC power enable output	PMIC power enable input	No Connect	No Connect
EXT_WAKEUP	External wakeup input	1.8 V wakeup event signal	VSS	VSS
	For information on power up sequencing, see the *AM335x Sitara™ Processors* data sheet	Figure 6-2 thru 6-4	Figure 6-5	Figure 6-6

(1) The CAP_VDD_RTC terminal operates as an input to the RTC core voltage domain when the internal RTC LDO is disabled by connecting the RTC_KALDO_ENn terminal to VDDS_RTC.

(2) If the internal RTC LDO is disabled,CAP_VDD_RTC should be sourced from an external 1.1-V power supply.

(3) RTC_PWRONRSTn should be asserted for at least 1ms for internal RTC LDO output voltage stabilized when internal RTC LDO is enabled.

(4) VDDS_RTC can be ramped independent of other power supplies if PMIC_POWER_EN functionality is not required. If VDDS_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE.

(5) RTC_PWRONRSTn high level must be 1.8 V. It cannot be 3.3 V. If tied together with PWRONRSTn, both reset inputs high level must be 1.8 V

(6) If using an external LVCMOS input for the 32 kHz clock it must be 1.8 V amplitude since this pin is related to VDDS_RTC.

(7) For more information, see the *Preferred Power-Supply Sequencing With Dual-Voltage I/Os Configured as 3.3 V*, *Alternate Power-Supply Sequencing With Dual-Voltage I/Os Configured as 3.3 V* and the *Power-Supply Sequencing With Dual-Voltage I/Os Configured as 1.8 V* figures in the *AM335x Sitara™ Processors* data manual.

(8) For more information, see the *Power-Supply Sequencing With Internal RTC LDO Disabled* figure in the *AM335x Sitara™ Processors* data manual.

(9) For more information, see the *Power-Supply Sequencing With RTC Feature Disabled* figure in the *AM335x Sitara™ Processors* data manual.

- If a 1.8 volt LVCMOS clock source is used rather than a crystal circuit:
  - Connect the clock source to the RTC_XTALIN terminal, leave the RTC_XTALOUT terminal open-circuit, and connect VSS_RTC to VSS if using the ZCZ package option.

2.14.1 If RTC is not Used

- If the AM335x RTC is not used:
  - Leave the RTC_XTALIN and RTC_XTALOUT terminals open-circuit, and connect VSS_RTC to VSS if using the ZCZ package.

3 References

- Texas Instruments: *AM335x and AMIC110 Sitara™ processors technical reference manual*
- Texas Instruments: *Powering the AM335x with the TPS65217x*
- Texas Instruments: *Powering the AM335x with the TPS650250*
- Texas Instruments: *TPS65910x user's guide for AM335x processors*
- Texas Instruments: *TPS65910x schematic checklist*
- Texas Instruments: *AM335x Sitara™ processors data manual*
- Texas Instruments: *High-speed interface layout guidelines*

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