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 /\*

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 \*/

/dts-v1/;

#include <dt-bindings/phy/phy.h>

#include <dt-bindings/mux/ti-serdes.h>

#include <dt-bindings/leds/common.h>

#include <dt-bindings/gpio/gpio.h>

#include <dt-bindings/net/ti-dp83867.h>

#include "k3-am642.dtsi"

/ {

    compatible = "ti,am642-evm", "ti,am642";

    model = "Texas Instruments AM642 EVM-C";

    chosen {

        stdout-path = "serial2:115200n8";

        bootargs = "console=ttyS2,115200n8 earlycon=ns16550a,mmio32,0x02800000";

    };

    aliases {

        ethernet2 = &icssg1\_emac0;

        ethernet3 = &icssg1\_emac1;

    };

    memory@80000000 {

        device\_type = "memory";

        /\* 2G RAM \*/

        reg = <0x00000000 0x80000000 0x00000000 0x80000000>;

    };

    reserved-memory {

        #address-cells = <2>;

        #size-cells = <2>;

        ranges;

        secure\_ddr: optee@9e800000 {

            reg = <0x00 0x9e800000 0x00 0x01800000>; /\* for OP-TEE \*/

            alignment = <0x1000>;

            no-map;

        };

        main\_r5fss0\_core0\_dma\_memory\_region: r5f-dma-memory@a0000000 {

            compatible = "shared-dma-pool";

            reg = <0x00 0xa0000000 0x00 0x100000>;

            no-map;

        };

        main\_r5fss0\_core0\_memory\_region: r5f-memory@a0100000 {

            compatible = "shared-dma-pool";

            reg = <0x00 0xa0100000 0x00 0xf00000>;

            no-map;

        };

        /\*

        main\_r5fss0\_core1\_dma\_memory\_region: r5f-dma-memory@a1000000 {

            compatible = "shared-dma-pool";

            reg = <0x00 0xa1000000 0x00 0x100000>;

            no-map;

        };

        main\_r5fss0\_core1\_memory\_region: r5f-memory@a1100000 {

            compatible = "shared-dma-pool";

            reg = <0x00 0xa1100000 0x00 0xf00000>;

            no-map;

        };

        \*/  //commented by user

        main\_r5fss1\_core0\_dma\_memory\_region: r5f-dma-memory@a2000000 {

            compatible = "shared-dma-pool";

            reg = <0x00 0xa2000000 0x00 0x100000>;

            no-map;

        };

        main\_r5fss1\_core0\_memory\_region: r5f-memory@a2100000 {

            compatible = "shared-dma-pool";

            reg = <0x00 0xa2100000 0x00 0xf00000>;

            no-map;

        };

        /\*

        main\_r5fss1\_core1\_dma\_memory\_region: r5f-dma-memory@a3000000 {

            compatible = "shared-dma-pool";

            reg = <0x00 0xa3000000 0x00 0x100000>;

            no-map;

        };

        main\_r5fss1\_core1\_memory\_region: r5f-memory@a3100000 {

            compatible = "shared-dma-pool";

            reg = <0x00 0xa3100000 0x00 0xf00000>;

            no-map;

        };

        \*/  //commented by user

        mcu\_m4fss\_dma\_memory\_region: m4f-dma-memory@a4000000 {

            compatible = "shared-dma-pool";

            reg = <0x00 0xa4000000 0x00 0x100000>;

            no-map;

        };

        mcu\_m4fss\_memory\_region: m4f-memory@a4100000 {

            compatible = "shared-dma-pool";

            reg = <0x00 0xa4100000 0x00 0xf00000>;

            no-map;

        };

        rtos\_ipc\_memory\_region: ipc-memories@a5000000 {

            reg = <0x00 0xa5000000 0x00 0x00800000>;

            alignment = <0x1000>;

            no-map;

        };

    };

    evm\_12v0: fixedregulator-evm12v0 {

        /\* main DC jack \*/

        compatible = "regulator-fixed";

        regulator-name = "evm\_12v0";

        regulator-min-microvolt = <12000000>;

        regulator-max-microvolt = <12000000>;

        regulator-always-on;

        regulator-boot-on;

    };

    vsys\_5v0: fixedregulator-vsys5v0 {

        /\* output of LM5140 \*/

        compatible = "regulator-fixed";

        regulator-name = "vsys\_5v0";

        regulator-min-microvolt = <5000000>;

        regulator-max-microvolt = <5000000>;

        vin-supply = <&evm\_12v0>;

        regulator-always-on;

        regulator-boot-on;

    };

    vsys\_3v3: fixedregulator-vsys3v3 {

        /\* output of LM5140 \*/

        compatible = "regulator-fixed";

        regulator-name = "vsys\_3v3";

        regulator-min-microvolt = <3300000>;

        regulator-max-microvolt = <3300000>;

        vin-supply = <&evm\_12v0>;

        regulator-always-on;

        regulator-boot-on;

    };

    vdd\_mmc1: fixed-regulator-sd {

        /\* TPS2051BD \*/

        compatible = "regulator-fixed";

        regulator-name = "vdd\_mmc1";

        regulator-min-microvolt = <3300000>;

        regulator-max-microvolt = <3300000>;

        regulator-boot-on;

        enable-active-high;

        vin-supply = <&vsys\_3v3>;

        //gpio = <&exp1 6 GPIO\_ACTIVE\_HIGH>;  //commented by user

    };

    vddb: fixedregulator-vddb {

        compatible = "regulator-fixed";

        regulator-name = "vddb\_3v3\_display";

        regulator-min-microvolt = <3300000>;

        regulator-max-microvolt = <3300000>;

        vin-supply = <&vsys\_3v3>;

        regulator-always-on;

        regulator-boot-on;

    };

    /\* commented by user

    leds {

        compatible = "gpio-leds";

        led-0 {

            label = "am64-evm:red:heartbeat";

            gpios = <&exp1 16 GPIO\_ACTIVE\_HIGH>;

            linux,default-trigger = "heartbeat";

            function = LED\_FUNCTION\_HEARTBEAT;

            default-state = "off";

        };

    };\*/

/\* commented by user

    mdio\_mux: mux-controller {

        compatible = "gpio-mux";

        #mux-control-cells = <0>;

        //mux-gpios = <&exp1 12 GPIO\_ACTIVE\_HIGH>;  //commented by user

    };

    mdio\_mux\_1: mdio-mux-1 {

        compatible = "mdio-mux-multiplexer";

        mux-controls = <&mdio\_mux>;

        mdio-parent-bus = <&cpsw3g\_mdio>;

        #address-cells = <1>;

        #size-cells = <0>;

        mdio@1 {

            reg = <0x1>;

            #address-cells = <1>;

            #size-cells = <0>;

            cpsw3g\_phy3: ethernet-phy@3 {

                reg = <3>;

                tx-internal-delay-ps = <250>;

                rx-internal-delay-ps = <2000>;

            };

        };

    };\*/

    transceiver1: can-phy0 {

        compatible = "ti,tcan1042";

        #phy-cells = <0>;

        max-bitrate = <5000000>;

        //standby-gpios = <&exp1 8 GPIO\_ACTIVE\_HIGH>;

    };

    transceiver2: can-phy1 {

        compatible = "ti,tcan1042";

        #phy-cells = <0>;

        max-bitrate = <5000000>;

        //standby-gpios = <&exp1 9 GPIO\_ACTIVE\_HIGH>;

    };

    icssg1\_eth: icssg1-eth {

            status = "disabled";        //added by user

        compatible = "ti,am642-icssg-prueth";

        pinctrl-names = "default";

        //pinctrl-0 = <&icssg1\_rgmii1\_pins\_default>;  commented by user

        sram = <&oc\_sram>;

        ti,prus = <&pru1\_0>, <&rtu1\_0>, <&tx\_pru1\_0>, <&pru1\_1>, <&rtu1\_1>, <&tx\_pru1\_1>;

        firmware-name = "ti-pruss/am65x-sr2-pru0-prueth-fw.elf",

                "ti-pruss/am65x-sr2-rtu0-prueth-fw.elf",

                "ti-pruss/am65x-sr2-txpru0-prueth-fw.elf",

                "ti-pruss/am65x-sr2-pru1-prueth-fw.elf",

                "ti-pruss/am65x-sr2-rtu1-prueth-fw.elf",

                "ti-pruss/am65x-sr2-txpru1-prueth-fw.elf";

        ti,pruss-gp-mux-sel = <2>,  /\* MII mode \*/

                      <2>,

                      <2>,

                      <2>,  /\* MII mode \*/

                      <2>,

                      <2>;

        ti,mii-g-rt = <&icssg1\_mii\_g\_rt>;

        ti,mii-rt = <&icssg1\_mii\_rt>;

        ti,pa-stats = <&icssg1\_pa\_stats>;

        iep = <&icssg1\_iep0>,  <&icssg1\_iep1>;

        interrupt-parent = <&icssg1\_intc>;

        interrupts = <24 0 2>, <25 1 3>;

        interrupt-names = "tx\_ts0", "tx\_ts1";

        dmas = <&main\_pktdma 0xc200 15>, /\* egress slice 0 \*/

               <&main\_pktdma 0xc201 15>, /\* egress slice 0 \*/

               <&main\_pktdma 0xc202 15>, /\* egress slice 0 \*/

               <&main\_pktdma 0xc203 15>, /\* egress slice 0 \*/

               <&main\_pktdma 0xc204 15>, /\* egress slice 1 \*/

               <&main\_pktdma 0xc205 15>, /\* egress slice 1 \*/

               <&main\_pktdma 0xc206 15>, /\* egress slice 1 \*/

               <&main\_pktdma 0xc207 15>, /\* egress slice 1 \*/

               <&main\_pktdma 0x4200 15>, /\* ingress slice 0 \*/

               <&main\_pktdma 0x4201 15>, /\* ingress slice 1 \*/

               <&main\_pktdma 0x4202 0>, /\* mgmnt rsp slice 0 \*/

               <&main\_pktdma 0x4203 0>; /\* mgmnt rsp slice 1 \*/

        dma-names = "tx0-0", "tx0-1", "tx0-2", "tx0-3",

                "tx1-0", "tx1-1", "tx1-2", "tx1-3",

                "rx0", "rx1";

        ethernet-ports {

            #address-cells = <1>;

            #size-cells = <0>;

            icssg1\_emac0: port@0 {

                reg = <0>;

                //phy-handle = <&icssg1\_phy1>;  //commented by user

                phy-mode = "rgmii-id";

                ti,syscon-rgmii-delay = <&main\_conf 0x4110>;

                /\* Filled in by bootloader \*/

                local-mac-address = [00 00 00 00 00 00];

                status = "disabled";

            };

            icssg1\_emac1: port@1 {

                reg = <1>;

                ti,syscon-rgmii-delay = <&main\_conf 0x4114>;

                /\* Filled in by bootloader \*/

                local-mac-address = [00 00 00 00 00 00];

                status = "disabled";

            };

        };

    };

};

&mcu\_pmx0 {

        cust\_mcugpio0\_pins\_default: cust-mcugpios-default {

        pinctrl-single,pins = <

                        //TEMP\_ALERT(E7 – MCU\_SPI0\_D0)   MCU\_GPIO0\_10 int

                        //GPIO\_PHY3\_RST(C6 – MCU\_SPI0\_CS1)  MCU\_GPIO0\_12 o/p

                        //GPIO\_eMMC\_RSTn – (D7 – MCU\_SPI1\_CLK)  MCU\_GPIO0\_7 o/p

                        //VPP\_1V8\_EN – (C8 – MCU\_SPI0\_D1) Used fpr prog OTP.    MCU\_GPIO0\_9 o/p

                        //GPIO\_EXP2\_INT\_N – (B7 – MCU\_SPI1\_CS1)   interrupt for Button press   MCU\_GPIO0\_6 int

        >;

    };

};

&main\_pmx0 {

    main\_mmc1\_pins\_default: main-mmc1-pins-default {

        pinctrl-single,pins = <

            AM64X\_IOPAD(0x0294, PIN\_INPUT\_PULLUP, 0) /\* (J19) MMC1\_CMD \*/

            AM64X\_IOPAD(0x028c, PIN\_INPUT\_PULLDOWN, 0) /\* (L20) MMC1\_CLK \*/

            AM64X\_IOPAD(0x0288, PIN\_INPUT\_PULLUP, 0) /\* (K21) MMC1\_DAT0 \*/

            AM64X\_IOPAD(0x0284, PIN\_INPUT\_PULLUP, 0) /\* (L21) MMC1\_DAT1 \*/

            AM64X\_IOPAD(0x0280, PIN\_INPUT\_PULLUP, 0) /\* (K19) MMC1\_DAT2 \*/

            AM64X\_IOPAD(0x027c, PIN\_INPUT\_PULLUP, 0) /\* (K18) MMC1\_DAT3 \*/

            AM64X\_IOPAD(0x0298, PIN\_INPUT\_PULLUP, 0) /\* (D19) MMC1\_SDCD \*/

            AM64X\_IOPAD(0x029c, PIN\_INPUT, 0) /\* (C20) MMC1\_SDWP \*/

            AM64X\_IOPAD(0x0290, PIN\_INPUT, 0) /\* MMC1\_CLKLB \*/

        >;

    };

    main\_uart0\_pins\_default: main-uart0-pins-default {

        pinctrl-single,pins = <

            //AM64X\_IOPAD(0x0238, PIN\_INPUT, 0) /\* (B16) UART0\_CTSn \*/ //Commented by user

            //AM64X\_IOPAD(0x023c, PIN\_OUTPUT, 0) /\* (A16) UART0\_RTSn \*/  //Commented by user

            AM64X\_IOPAD(0x0230, PIN\_INPUT, 0) /\* (D15) UART0\_RXD \*/

            AM64X\_IOPAD(0x0234, PIN\_OUTPUT, 0) /\* (C16) UART0\_TXD \*/

        >;

    };

    main\_spi0\_pins\_default: main-spi0-pins-default {

        pinctrl-single,pins = <

            AM64X\_IOPAD(0x0210, PIN\_INPUT, 0) /\* (D13) SPI0\_CLK \*/

            AM64X\_IOPAD(0x0208, PIN\_INPUT, 0) /\* (D12) SPI0\_CS0 \*/

            AM64X\_IOPAD(0x0214, PIN\_INPUT, 0) /\* (A13) SPI0\_D0 \*/

            //AM64X\_IOPAD(0x0218, PIN\_INPUT, 0) /\* (A14) SPI0\_D1 \*/ // commented by user

        >;

    };

    main\_i2c1\_pins\_default: main-i2c1-pins-default {

        pinctrl-single,pins = <

            AM64X\_IOPAD(0x0268, PIN\_INPUT\_PULLUP, 0) /\* (C18) I2C1\_SCL \*/

            AM64X\_IOPAD(0x026c, PIN\_INPUT\_PULLUP, 0) /\* (B19) I2C1\_SDA \*/

        >;

    };

    main\_i2c0\_pins\_default: main-i2c0-pins-default {

        pinctrl-single,pins = <

            AM64X\_IOPAD(0x0260, PIN\_INPUT\_PULLUP, 0) /\* (A18) I2C0\_SCL \*/

            AM64X\_IOPAD(0x0264, PIN\_INPUT\_PULLUP, 0) /\* (B18) I2C0\_SDA \*/

        >;

    };

    mdio1\_pins\_default: mdio1-pins-default {

        pinctrl-single,pins = <

            AM64X\_IOPAD(0x01fc, PIN\_OUTPUT, 4) /\* (R2) PRG0\_PRU1\_GPO19.MDIO0\_MDC \*/

            AM64X\_IOPAD(0x01f8, PIN\_INPUT, 4) /\* (P5) PRG0\_PRU1\_GPO18.MDIO0\_MDIO \*/

        >;

    };

    rgmii1\_pins\_default: rgmii1-pins-default {

        pinctrl-single,pins = <

            AM64X\_IOPAD(0x01cc, PIN\_INPUT, 4) /\* (W5) PRG0\_PRU1\_GPO7.RGMII1\_RD0 \*/

            AM64X\_IOPAD(0x01d4, PIN\_INPUT, 4) /\* (Y5) PRG0\_PRU1\_GPO9.RGMII1\_RD1 \*/

            AM64X\_IOPAD(0x01d8, PIN\_INPUT, 4) /\* (V6) PRG0\_PRU1\_GPO10.RGMII1\_RD2 \*/

            AM64X\_IOPAD(0x01f4, PIN\_INPUT, 4) /\* (V5) PRG0\_PRU1\_GPO17.RGMII1\_RD3 \*/

            AM64X\_IOPAD(0x0188, PIN\_INPUT, 4) /\* (AA5) PRG0\_PRU0\_GPO10.RGMII1\_RXC \*/

            AM64X\_IOPAD(0x0184, PIN\_INPUT, 4) /\* (W6) PRG0\_PRU0\_GPO9.RGMII1\_RX\_CTL \*/

            AM64X\_IOPAD(0x0124, PIN\_OUTPUT, 4) /\* (V15) PRG1\_PRU1\_GPO7.RGMII1\_TD0 \*/

            AM64X\_IOPAD(0x012c, PIN\_OUTPUT, 4) /\* (V14) PRG1\_PRU1\_GPO9.RGMII1\_TD1 \*/

            AM64X\_IOPAD(0x0130, PIN\_OUTPUT, 4) /\* (W14) PRG1\_PRU1\_GPO10.RGMII1\_TD2 \*/

            AM64X\_IOPAD(0x014c, PIN\_OUTPUT, 4) /\* (AA14) PRG1\_PRU1\_GPO17.RGMII1\_TD3 \*/

            AM64X\_IOPAD(0x00e0, PIN\_OUTPUT, 4) /\* (U14) PRG1\_PRU0\_GPO10.RGMII1\_TXC \*/

            AM64X\_IOPAD(0x00dc, PIN\_OUTPUT, 4) /\* (U15) PRG1\_PRU0\_GPO9.RGMII1\_TX\_CTL \*/

        >;

    };

//rgmii2\_pins\_default: rgmii2-pins-default {

       // pinctrl-single,pins = <

            //AM64X\_IOPAD(0x0108, PIN\_INPUT, 4) /\* (W11) PRG1\_PRU1\_GPO0.RGMII2\_RD0 \*/

            //AM64X\_IOPAD(0x010c, PIN\_INPUT, 4) /\* (V11) PRG1\_PRU1\_GPO1.RGMII2\_RD1 \*/

            //AM64X\_IOPAD(0x0110, PIN\_INPUT, 4) /\* (AA12) PRG1\_PRU1\_GPO2.RGMII2\_RD2 \*/

            //AM64X\_IOPAD(0x0114, PIN\_INPUT, 4) /\* (Y12) PRG1\_PRU1\_GPO3.RGMII2\_RD3 \*/

           //AM64X\_IOPAD(0x0120, PIN\_INPUT, 4) /\* (U11) PRG1\_PRU1\_GPO6.RGMII2\_RXC \*/

            //AM64X\_IOPAD(0x0118, PIN\_INPUT, 4) /\* (W12) PRG1\_PRU1\_GPO4.RGMII2\_RX\_CTL \*/

            //AM64X\_IOPAD(0x0134, PIN\_OUTPUT, 4) /\* (AA10) PRG1\_PRU1\_GPO11.RGMII2\_TD0 \*/

           // AM64X\_IOPAD(0x0138, PIN\_OUTPUT, 4) /\* (V10) PRG1\_PRU1\_GPO12.RGMII2\_TD1 \*/

           // AM64X\_IOPAD(0x013c, PIN\_OUTPUT, 4) /\* (U10) PRG1\_PRU1\_GPO13.RGMII2\_TD2 \*/

            //AM64X\_IOPAD(0x0140, PIN\_OUTPUT, 4) /\* (AA11) PRG1\_PRU1\_GPO14.RGMII2\_TD3 \*/

            //AM64X\_IOPAD(0x0148, PIN\_OUTPUT, 4) /\* (Y10) PRG1\_PRU1\_GPO16.RGMII2\_TXC \*/

           // AM64X\_IOPAD(0x0144, PIN\_OUTPUT, 4) /\* (Y11) PRG1\_PRU1\_GPO15.RGMII2\_TX\_CTL \*/

       // >;

    //};

    main\_usb0\_pins\_default: main-usb0-pins-default {

        pinctrl-single,pins = <

            AM64X\_IOPAD(0x02a8, PIN\_OUTPUT, 0) /\* (E19) USB0\_DRVVBUS \*/

        >;

    };

    ospi0\_pins\_default: ospi0-pins-default {

        pinctrl-single,pins = <

            AM64X\_IOPAD(0x0000, PIN\_OUTPUT, 0) /\* (N20) OSPI0\_CLK \*/

            AM64X\_IOPAD(0x002c, PIN\_OUTPUT, 0) /\* (L19) OSPI0\_CSn0 \*/

            AM64X\_IOPAD(0x000c, PIN\_INPUT, 0) /\* (M19) OSPI0\_D0 \*/

            AM64X\_IOPAD(0x0010, PIN\_INPUT, 0) /\* (M18) OSPI0\_D1 \*/

            AM64X\_IOPAD(0x0014, PIN\_INPUT, 0) /\* (M20) OSPI0\_D2 \*/

            AM64X\_IOPAD(0x0018, PIN\_INPUT, 0) /\* (M21) OSPI0\_D3 \*/

            AM64X\_IOPAD(0x001c, PIN\_INPUT, 0) /\* (P21) OSPI0\_D4 \*/

            AM64X\_IOPAD(0x0020, PIN\_INPUT, 0) /\* (P20) OSPI0\_D5 \*/

            AM64X\_IOPAD(0x0024, PIN\_INPUT, 0) /\* (N18) OSPI0\_D6 \*/

            AM64X\_IOPAD(0x0028, PIN\_INPUT, 0) /\* (M17) OSPI0\_D7 \*/

            AM64X\_IOPAD(0x0008, PIN\_INPUT, 0) /\* (N19) OSPI0\_DQS \*/

        >;

    };

    main\_ecap0\_pins\_default: main-ecap0-pins-default {

        pinctrl-single,pins = <

            AM64X\_IOPAD(0x0270, PIN\_INPUT, 0) // (D18) ECAP0\_IN\_APWM\_OUT

        >;

    };

/\*

    main\_mcan0\_pins\_default: main-mcan0-pins-default {

        pinctrl-single,pins = <

            AM64X\_IOPAD(0x0254, PIN\_INPUT, 0) // (B17) MCAN0\_RX

            AM64X\_IOPAD(0x0250, PIN\_OUTPUT, 0) // (A17) MCAN0\_TX

            AM64X\_IOPAD(0x0238, PIN\_INPUT, 0) // (B16) UART0\_CTSn  //Commented by user

        >;

    };

    main\_mcan1\_pins\_default: main-mcan1-pins-default {

        pinctrl-single,pins = <

            AM64X\_IOPAD(0x025c, PIN\_INPUT, 0) // (D17) MCAN1\_RX

            AM64X\_IOPAD(0x0258, PIN\_OUTPUT, 0) // (C17) MCAN1\_TX

        >;

    };

\*/ //Commented by user

/\*  icssg1\_mdio1\_pins\_default: icssg1-mdio1-pins-default {

        pinctrl-single,pins = <

            AM64X\_IOPAD(0x015c, PIN\_OUTPUT, 0) // (Y6) PRG1\_MDIO0\_MDC

            AM64X\_IOPAD(0x0158, PIN\_INPUT, 0) // (AA6) PRG1\_MDIO0\_MDIO

        >;

    };\*/    //commented by user

/\*

    icssg1\_rgmii1\_pins\_default: icssg1-rgmii1-pins-default {

        pinctrl-single,pins = <

            AM64X\_IOPAD(0x00b8, PIN\_INPUT, 2) // (Y7) PRG1\_PRU0\_GPO0.PRG1\_RGMII1\_RD0

            AM64X\_IOPAD(0x00bc, PIN\_INPUT, 2) // (U8) PRG1\_PRU0\_GPO1.PRG1\_RGMII1\_RD1

            AM64X\_IOPAD(0x00c0, PIN\_INPUT, 2) // (W8) PRG1\_PRU0\_GPO2.PRG1\_RGMII1\_RD2

            AM64X\_IOPAD(0x00c4, PIN\_INPUT, 2) // (V8) PRG1\_PRU0\_GPO3.PRG1\_RGMII1\_RD3

            AM64X\_IOPAD(0x00d0, PIN\_INPUT, 2) // (AA7) PRG1\_PRU0\_GPO6.PRG1\_RGMII1\_RXC

            AM64X\_IOPAD(0x00c8, PIN\_INPUT, 2) // (Y8) PRG1\_PRU0\_GPO4.PRG1\_RGMII1\_RX\_CTL

            AM64X\_IOPAD(0x00e4, PIN\_INPUT, 2) // (AA8) PRG1\_PRU0\_GPO11.PRG1\_RGMII1\_TD0

            AM64X\_IOPAD(0x00e8, PIN\_INPUT, 2) // (U9) PRG1\_PRU0\_GPO12.PRG1\_RGMII1\_TD1

            AM64X\_IOPAD(0x00ec, PIN\_INPUT, 2) // (W9) PRG1\_PRU0\_GPO13.PRG1\_RGMII1\_TD2

            AM64X\_IOPAD(0x00f0, PIN\_INPUT, 2) // (AA9) PRG1\_PRU0\_GPO14.PRG1\_RGMII1\_TD3

            AM64X\_IOPAD(0x00f8, PIN\_INPUT, 2) // (V9) PRG1\_PRU0\_GPO16.PRG1\_RGMII1\_TXC

            AM64X\_IOPAD(0x00f4, PIN\_INPUT, 2) // (Y9) PRG1\_PRU0\_GPO15.PRG1\_RGMII1\_TX\_CTL

        >;

    };\*/

    //icssg1\_iep0\_pins\_default: icssg1-iep0-pins-default {

       // pinctrl-single,pins = <

        //    AM64X\_IOPAD(0x0104, PIN\_OUTPUT, 2) /\* (W7) PRG1\_PRU0\_GPO19.PRG1\_IEP0\_EDC\_SYNC\_OUT0 \*/

       // >;

   // };

    customgpio1\_pins\_default: customgpio1-default-pins {

        pinctrl-single,pins = <

            AM64X\_IOPAD(0x0160, PIN\_INPUT\_PULLUP, 7) /\* (Y1) PRG0\_PRU0\_GPO0.GPIO1\_0  LCD-BCKLIGHT\*/

            //AM64X\_IOPAD(0x0208, PIN\_INPUT, 7) /\* (D12) SPI0\_CS0.GPIO1\_42 LCD\_CS\*/

            AM64X\_IOPAD(0x020c, PIN\_INPUT, 7) /\* (C13) SPI0\_CS1.GPIO1\_43 LCD\_RST\*/

            AM64X\_IOPAD(0x0218, PIN\_INPUT, 7) /\* (A14) SPI0\_D1.GPIO1\_46  LCD\_D/C\*/

        >;

    };

};

//Added by user

&main\_rti1 {

     status = "disabled";

};

&main\_uart0 {

    status = "okay";

    pinctrl-names = "default";

    pinctrl-0 = <&main\_uart0\_pins\_default>;

};

/\* main\_uart1 is reserved for firmware usage \*/

&main\_uart1 {

    status = "reserved";

};

//added by user

&mcu\_uart0{

    status = "disabled";

    pinctrl-names = "default";

    //pinctrl-0 = <&mcu\_uart0\_pins\_default>;

};

//added by user

&mcu\_uart1{

    status = "disabled";

    pinctrl-names = "default";

    //pinctrl-0 = <&mcu\_uart1\_pins\_default>;

};

&main\_i2c0 {

    status = "okay";

    pinctrl-names = "default";

    pinctrl-0 = <&main\_i2c0\_pins\_default>;

    clock-frequency = <400000>;

};

&main\_i2c1 {

    status = "okay";

    pinctrl-names = "default";

    pinctrl-0 = <&main\_i2c1\_pins\_default>;

    clock-frequency = <400000>;

/\*

    exp1: gpio@22 {

        compatible = "ti,tca6424";

        reg = <0x22>;

        gpio-controller;

        #gpio-cells = <2>;

        gpio-line-names = "GPIO\_eMMC\_RSTn", "CAN\_MUX\_SEL",

                  "GPIO\_CPSW1\_RST", "GPIO\_RGMII1\_RST",

                  "GPIO\_RGMII2\_RST", "GPIO\_PCIe\_RST\_OUT",

                  "MMC1\_SD\_EN", "FSI\_FET\_SEL",

                  "MCAN0\_STB\_3V3", "MCAN1\_STB\_3V3",

                  "CPSW\_FET\_SEL", "CPSW\_FET2\_SEL",

                  "PRG1\_RGMII2\_FET\_SEL", "TEST\_GPIO2",

                  "GPIO\_OLED\_RESETn", "VPP\_LDO\_EN",

                  "TEST\_LED1", "TP92", "TP90", "TP88",

                  "TP87", "TP86", "TP89", "TP91";

    };\*/

    /\* osd9616p0899-10 \*/

    /\*display@3c {

        compatible = "solomon,ssd1306fb-i2c";

        reg = <0x3c>;

        reset-gpios = <&exp1 14 GPIO\_ACTIVE\_LOW>;

        vbat-supply = <&vddb>;

        solomon,height = <16>;

        solomon,width = <96>;

        solomon,com-seq;

        solomon,com-invdir;

        solomon,page-offset = <0>;

        solomon,prechargep1 = <2>;

        solomon,prechargep2 = <13>;

    };\*/ /\* Commented By user\*/

};

&main\_gpio0 {

};

&main\_gpio1 {

    status = "okay";

        pinctrl-names = "default";

        pinctrl-0 = <&customgpio1\_pins\_default>;

        gpio-controller;

};

/\* mcu\_gpio0 is reserved for mcu firmware usage \*/

&mcu\_gpio0 {

    //status = "reserved";

    status = "okay";

        pinctrl-names = "default";

        pinctrl-0 = <&cust\_mcugpio0\_pins\_default>;

        gpio-controller;

};

&main\_spi0 {

    status = "okay";

    pinctrl-names = "default";

    pinctrl-0 = <&main\_spi0\_pins\_default>;

    //ti,pindir-d0-out-d1-in;  //commented by user

    //ti,pindir-d0-out-d1-out;  //added by user

    ti,pindir-d0-out-d1-in = <1>;  //commented by user

    ti,spi-num-cs = <1>;        //added by user

    cs-gpios = <0>;     //added by user

    //no-cs;

    /\*commented by user

    eeprom@0 {

        compatible = "microchip,93lc46b";

        reg = <0>;

        spi-max-frequency = <1000000>;

        spi-cs-high;

        data-size = <16>;

    };\*/

       spidev@0 {

           status = "okay";

               //compatible = "spidev";

               //compatible = "linux,spidev";

               compatible = "rohm,dh2228fv";

               spi-max-frequency = <1000000>;

               reg = <0>;

           //spi-cs-high;

       };

};

&sdhci0 {

    /\* emmc \*/

    bus-width = <8>;

    non-removable;

    ti,driver-strength-ohm = <50>;

    disable-wp;

/\*  mmc-ddr-1\_8v;\*/     /\* disabling all the UHS modes  added by user\*/

/\*  max-frequency   = <50000000>;\*/

/\*  sd-uhs-sdr50;\*/

    //sd-uhs-sdr104;

    //sd-uhs-ddr50;

    /delete-property/mmc-ddr-1\_8v;

    /delete-property/mmc-hs200-1\_8v;

    no-1-8-v; /\* disabling all the UHS modes  added by user\*/

    sd-uhs-sdr50;  //added by user

};

&sdhci1 {

    /\* SD/MMC \*/

    vmmc-supply = <&vdd\_mmc1>;

    pinctrl-names = "default";

    bus-width = <4>;

    pinctrl-0 = <&main\_mmc1\_pins\_default>;

    ti,driver-strength-ohm = <50>;

    disable-wp;

    no-1-8-v; /\* disabling all the UHS modes  added by user\*/

    sd-uhs-sdr50;  //added by user

};

&usbss0 {

    ti,vbus-divider;

    ti,usb2-only;

};

&usb0 {

    status = "disabled";        //ADDED by user

    dr\_mode = "otg";

    maximum-speed = "high-speed";

    pinctrl-names = "default";

    pinctrl-0 = <&main\_usb0\_pins\_default>;

};

&cpsw3g {

    pinctrl-names = "default";

    pinctrl-0 = <&rgmii1\_pins\_default>;

             //&rgmii2\_pins\_default>;  //commented by user

    /\* Map HW8\_TS\_PUSH to GENF1 \*/

    cpts@3d000 {

        ti,pps = <7 1>;

    };

};

&cpsw\_port1 {

    phy-mode = "rgmii-rxid";

    phy-handle = <&cpsw3g\_phy0>;  //commented by user

};

/\*

&cpsw\_port2 {

    phy-mode = "rgmii-rxid";

    phy-handle = <&cpsw3g\_phy3>;

};

\*/ //commented by user

&cpsw3g\_mdio {

    //status = "okay";

    pinctrl-names = "default";

    status = "disabled";

    pinctrl-0 = <&mdio1\_pins\_default>;

    cpsw3g\_phy0: ethernet-phy@0 {

        reg = <0>;

        ti,rx-internal-delay = <DP83867\_RGMIIDCTL\_2\_00\_NS>;

        ti,fifo-depth = <DP83867\_PHYCR\_FIFO\_DEPTH\_4\_B\_NIB>;

    };

};

&tscadc0 {

    /\* ADC is reserved for R5 usage \*/

    status = "reserved";

};

&ospi0 {

    pinctrl-names = "default";

    pinctrl-0 = <&ospi0\_pins\_default>;

    flash@0 {

        compatible = "jedec,spi-nor";

        reg = <0x0>;

        spi-tx-bus-width = <4>;     //old 8 changed to 4 by user

        spi-rx-bus-width = <4>;     //old 8 changed to 4 by user

        spi-max-frequency = <25000000>;

        cdns,tshsl-ns = <60>;

        cdns,tsd2d-ns = <60>;

        cdns,tchsh-ns = <60>;

        cdns,tslch-ns = <60>;

        cdns,read-delay = <4>;

        partitions {

            compatible = "fixed-partitions";

            #address-cells = <1>;

            #size-cells = <1>;

            partition@0 {

                label = "ospi.tiboot3";

                reg = <0x0 0x80000>;

            };

            partition@80000 {

                label = "ospi.tispl";

                reg = <0x80000 0x200000>;

            };

            partition@280000 {

                label = "ospi.u-boot";

                reg = <0x280000 0x400000>;

            };

            partition@680000 {

                label = "ospi.env";

                reg = <0x680000 0x40000>;

            };

            partition@6c0000 {

                label = "ospi.env.backup";

                reg = <0x6c0000 0x40000>;

            };

            partition@700000 {

                label = "ospi.dtb";

                reg = <0x700000 0x100000>;

            };

            partition@800000 {

                label = "ospi.kernel";

                reg = <0x800000 0x1400000>;

            };

            partition@1c00000 {

                label = "ospi.rootfs";

                reg = <0x1c00000 0x23c0000>;

            };

            partition@3fc0000 {

                label = "ospi.phypattern";

                reg = <0x3fc0000 0x40000>;

            };

        };

/\*

        partitions {

            compatible = "fixed-partitions";

            #address-cells = <1>;

            #size-cells = <1>;

            partition@0 {

                label = "ospi.tiboot3";

                reg = <0x0 0x100000>;

            };

            partition@100000 {

                label = "ospi.tispl";

                reg = <0x100000 0x200000>;

            };

            partition@300000 {

                label = "ospi.u-boot";

                reg = <0x300000 0x400000>;

            };

            partition@700000 {

                label = "ospi.env";

                reg = <0x700000 0x40000>;

            };

            partition@740000 {

                label = "ospi.env.backup";

                reg = <0x740000 0x40000>;

            };

            partition@800000 {

                label = "ospi.rootfs";

                reg = <0x800000 0x37c0000>;

            };

            partition@3fc0000 {

                label = "ospi.phypattern";

                reg = <0x3fc0000 0x40000>;

            };

        };\*/

    };

};

&mailbox0\_cluster2 {

    mbox\_main\_r5fss0\_core0: mbox-main-r5fss0-core0 {

        ti,mbox-rx = <0 0 2>;

        ti,mbox-tx = <1 0 2>;

    };

    /\*

    mbox\_main\_r5fss0\_core1: mbox-main-r5fss0-core1 {

        ti,mbox-rx = <2 0 2>;

        ti,mbox-tx = <3 0 2>;

    };

    \*/  //commented by user

};

&mailbox0\_cluster3 {

    status = "disabled";

};

&mailbox0\_cluster4 {

    mbox\_main\_r5fss1\_core0: mbox-main-r5fss1-core0 {

        ti,mbox-rx = <0 0 2>;

        ti,mbox-tx = <1 0 2>;

    };

    /\*

    mbox\_main\_r5fss1\_core1: mbox-main-r5fss1-core1 {

        ti,mbox-rx = <2 0 2>;

        ti,mbox-tx = <3 0 2>;

    };

    \*/  //commented by user

};

&mailbox0\_cluster5 {

    status = "disabled";

};

&mailbox0\_cluster6 {

    mbox\_m4\_0: mbox-m4-0 {

        ti,mbox-rx = <0 0 2>;

        ti,mbox-tx = <1 0 2>;

    };

};

&mailbox0\_cluster7 {

    status = "disabled";

};

//added by user

/\* set R5F subsystem to single-CPU mode \*/

&main\_r5fss0 {

    ti,cluster-mode = <2>;

};

//added by user

/\* set R5F subsystem to single-CPU mode \*/

&main\_r5fss1 {

    ti,cluster-mode = <2>;

};

/\*

//added by user

&oc\_sram {

    main\_r5fss0\_core0\_sram: r5f-sram@40000 {

        reg = <0x40000 0x40000>;

    };

    main\_r5fss0\_core1\_sram: r5f-sram@80000 {

        reg = <0x80000 0x40000>;

    };

    main\_r5fss1\_core0\_sram: r5f-sram@c0000 {

        reg = <0xc0000 0x40000>;

    };

    main\_r5fss1\_core1\_sram: r5f-sram@100000 {

        reg = <0x100000 0x40000>;

    };

};\*/

&main\_r5fss0\_core0 {

    mboxes = <&mailbox0\_cluster2 &mbox\_main\_r5fss0\_core0>;

    memory-region = <&main\_r5fss0\_core0\_dma\_memory\_region>,

            <&main\_r5fss0\_core0\_memory\_region>;

    //sram = <&main\_r5fss0\_core0\_sram>; //added by user

    status = "okay";            //added by user

};

&main\_r5fss0\_core1 {

    /\*

    mboxes = <&mailbox0\_cluster2 &mbox\_main\_r5fss0\_core1>;

    memory-region = <&main\_r5fss0\_core1\_dma\_memory\_region>,

            <&main\_r5fss0\_core1\_memory\_region>;

        //commented by user

    sram = <&main\_r5fss0\_core1\_sram>;   //added by user

    \*/

    //status = "disabled";          //added by user

};

&main\_r5fss1\_core0 {

    mboxes = <&mailbox0\_cluster4 &mbox\_main\_r5fss1\_core0>;

    memory-region = <&main\_r5fss1\_core0\_dma\_memory\_region>,

            <&main\_r5fss1\_core0\_memory\_region>;

    //sram = <&main\_r5fss1\_core0\_sram>; //added by user

    status = "okay";            //added by user

};

&main\_r5fss1\_core1 {

    /\*

    mboxes = <&mailbox0\_cluster4 &mbox\_main\_r5fss1\_core1>;

    memory-region = <&main\_r5fss1\_core1\_dma\_memory\_region>,

            <&main\_r5fss1\_core1\_memory\_region>;

        //commented by user

    //sram = <&main\_r5fss1\_core1\_sram>; //added by user

    \*/

    //status = "disabled";          //added by user

};

&mcu\_m4fss {

    mboxes = <&mailbox0\_cluster6 &mbox\_m4\_0>;

    memory-region = <&mcu\_m4fss\_dma\_memory\_region>,

            <&mcu\_m4fss\_memory\_region>;

    //status = "disabled";          //added by user

};

&serdes\_ln\_ctrl {

    idle-states = <AM64\_SERDES0\_LANE0\_PCIE0>;

};

&serdes0 {

    serdes0\_pcie\_link: phy@0 {

        reg = <0>;

        cdns,num-lanes = <1>;

        #phy-cells = <0>;

        cdns,phy-type = <PHY\_TYPE\_PCIE>;

        resets = <&serdes\_wiz0 1>;

    };

};

&pcie0\_rc {

    //status = "okay";  //commented by user

    status = "disabled";    //Added by user

    //reset-gpios = <&exp1 5 GPIO\_ACTIVE\_HIGH>;

    phys = <&serdes0\_pcie\_link>;

    phy-names = "pcie-phy";

    num-lanes = <1>;

};

&pcie0\_ep {

    phys = <&serdes0\_pcie\_link>;

    phy-names = "pcie-phy";

    num-lanes = <1>;

};

&ecap0 {

    status = "okay";

    /\* PWM is available on Pin 1 of header J12 \*/

    pinctrl-names = "default";

    pinctrl-0 = <&main\_ecap0\_pins\_default>;

};

&main\_mcan0 {

    //status = "okay";

    pinctrl-names = "default";

    //pinctrl-0 = <&main\_mcan0\_pins\_default>;

    phys = <&transceiver1>;

    status = "disabled";    //Added by user

};

&main\_mcan1 {

    //status = "okay";

    pinctrl-names = "default";

    //pinctrl-0 = <&main\_mcan1\_pins\_default>;

    phys = <&transceiver2>;

    status = "disabled";    //Added by user

};

/\*

&icssg1\_mdio {

    status = "okay";

    pinctrl-names = "default";

    pinctrl-0 = <&icssg1\_mdio1\_pins\_default>;

    icssg1\_phy1: ethernet-phy@0 {

        reg = <0xf>;

        tx-internal-delay-ps = <250>;

        rx-internal-delay-ps = <2000>;

    };

};\*/

#define TS\_OFFSET(pa, val)     (0x4+(pa)\*4) (0x10000 | val)

&timesync\_router {

    status = "okay";

    pinctrl-names = "default";

    pinctrl-0 = <&cpsw\_cpts\_pps>;

    /\*

     \* Use Time Sync Router to map GENF1 input to HW8\_TS\_PUSH output as well

     \* as the PRU ICSSG0 SYNC1 output.

     \*/

    cpsw\_cpts\_pps: cpsw-cpts-pps {

        pinctrl-single,pins = <

            /\* pps [cpts genf1] in22 -> out37 [cpts hw8\_push] \*/

            TS\_OFFSET(37, 22)

            /\* pps [cpts genf1] in22 -> out26 [SYNC1\_OUT pin] \*/

            TS\_OFFSET(26, 22)

            >;

    };

};

/\*

&icssg1\_iep0 {

    pinctrl-names = "default";

    pinctrl-0 = <&icssg1\_iep0\_pins\_default>;

};\*/