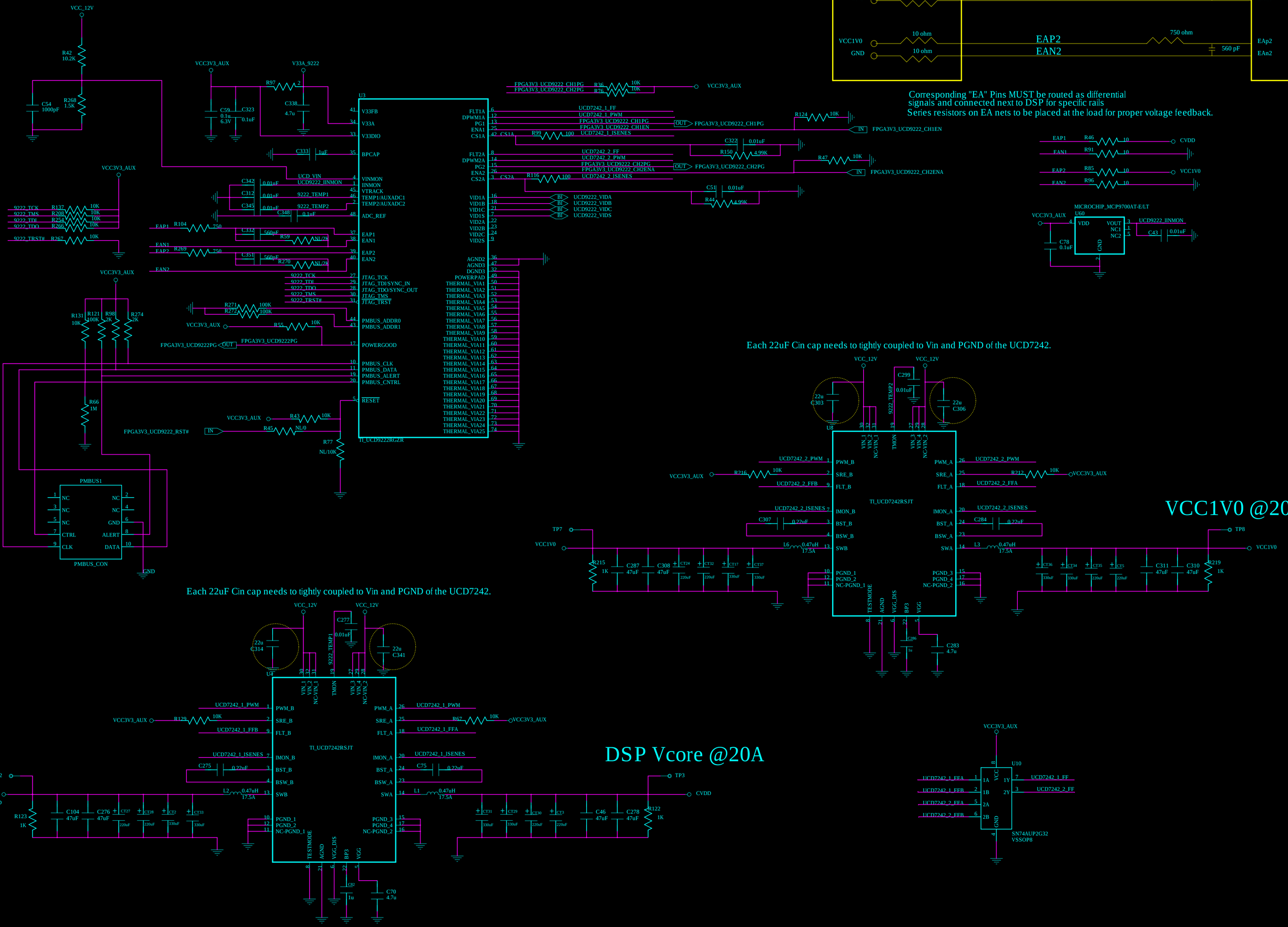
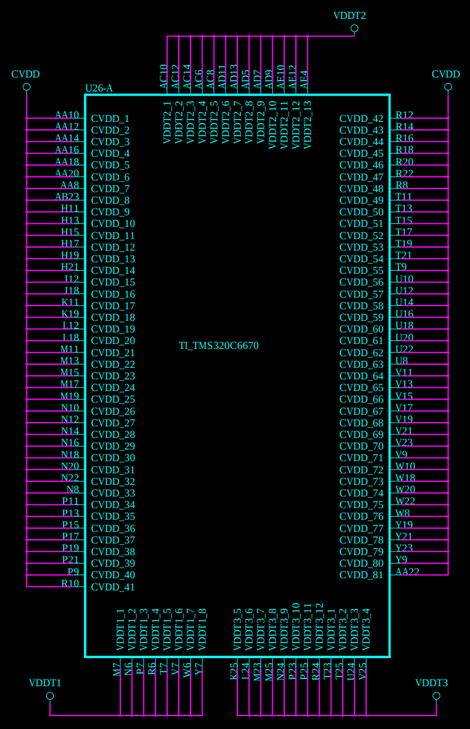
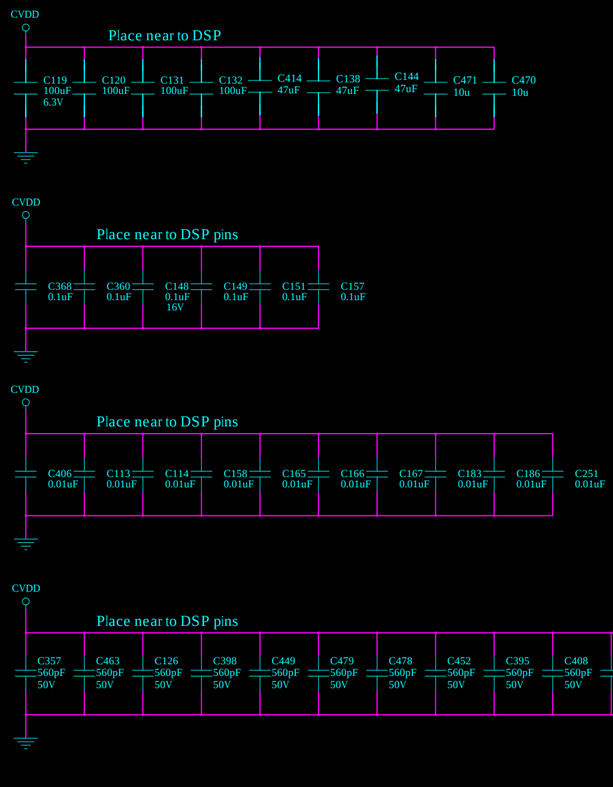
CVDD / VCC1V0

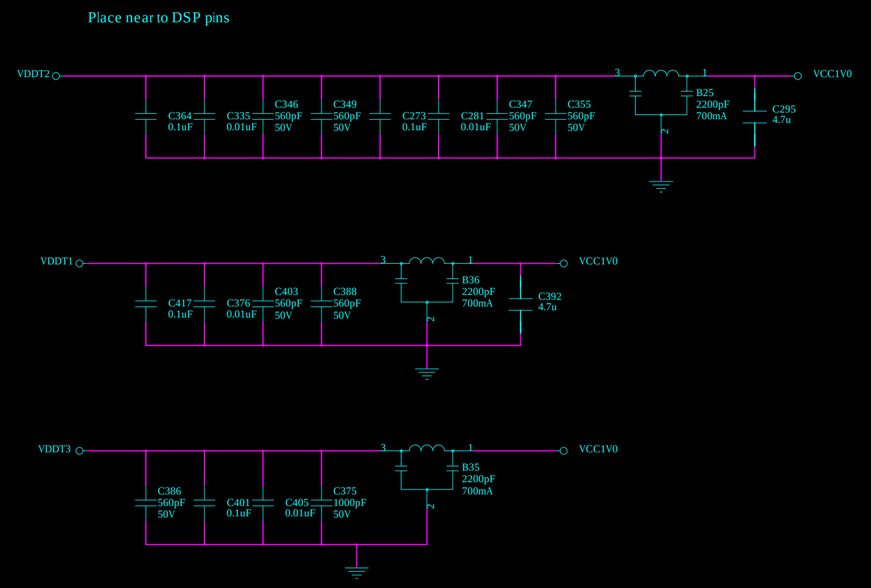

VCC_12V
R42 10.2K
R268 1.5K
C54 1000pF
VCC3V3_AUX
V33A_9222
R97 2
C59 0.1u 6.3V
C323 0.1uF
C338 4.7u
U3
V33FB
V33A
V33DIO
BPCAP
C333 1uF
UCD_VIN
VINMON
UCD9222_IINMON
IINMON
VTRACK
TEMP1/AUXADC1
TEMP2/AUXADC2
ADC_REF
C342 0.01uF
C312 0.01uF
C345 0.01uF
C348 0.1uF
9222_TEMP1
9222_TEMP2
EAP1
EAN1
EAP2
EAN2
R104 750
R269 750
C332 560pF
C351 560pF
R59 ANL/2R
R270 ANL/2R
9222_TCK
9222_TDI
9222_TDO
9222_TMS
9222_TRST#
JTAG_TCK
JTAG_TDI/SYNC_IN
JTAG_TDO/SYNC_OUT
JTAG_TMS
JTAG_TRST
R271 100K
R272 100K
PMBUS_ADDR0
PMBUS_ADDR1
R55 10K
POWERGOOD
FPGA3V3_UCD9222PG
PMBUS_CLK
PMBUS_DATA
PMBUS_ALERT
PMBUS_CNTRL
RESET
R66 1M
R43 10K
R45 NL/0
FPGA3V3_UCD9222_RST#
R77 NL/10K
TI_UCD9222RGZR
FPGA3V3_UCD9222_CH1PG
FPGA3V3_UCD9222_CH2PG
R36 10K
R76 10K
FLT1A
DPWM1A
PG1
ENA1
CS1A
FLT2A
DPWM2A
PG2
ENA2
CS2A
VID1A
VID1B
VID1C
VID1S
VID2A
VID2B
VID2C
VID2S
AGND2
AGND3
DGND3
POWERPAD
THERMAL_VIA1
THERMAL_VIA2
THERMAL_VIA3
THERMAL_VIA4
THERMAL_VIA5
THERMAL_VIA6
THERMAL_VIA7
THERMAL_VIA8
THERMAL_VIA9
THERMAL_VIA10
THERMAL_VIA11
THERMAL_VIA12
THERMAL_VIA13
THERMAL_VIA14
THERMAL_VIA15
THERMAL_VIA16
THERMAL_VIA17
THERMAL_VIA18
THERMAL_VIA19
THERMAL_VIA20
THERMAL_VIA21
THERMAL_VIA22
THERMAL_VIA23
THERMAL_VIA24
THERMAL_VIA25
UCD7242_1_FF
UCD7242_1_PWM
FPGA3V3_UCD9222_CH1PG
FPGA3V3_UCD9222_CH1EN
UCD7242_1_ISENES
UCD7242_2_FF
UCD7242_2_PWM
FPGA3V3_UCD9222_CH2PG
FPGA3V3_UCD9222_CH2ENA
UCD7242_2_ISENES
UCD9222_VIDA
UCD9222_VIDB
UCD9222_VIDC
UCD9222_VIDS
R99 100
R116 100
C322 0.01uF
R150 4.99K
C51 0.01uF
R44 4.99K
R124 10K
R47 10K
FPGA3V3_UCD9222_CH1EN
FPGA3V3_UCD9222_CH2ENA
DSP
CVDD
GND
VCC1V0
10 ohm
EAP1
EAN1
EAP2
EAN2
750 ohm
560 pF
UCD9222
EAp1
EAn1
EAp2
EAn2
Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails
Series resistors on EA nets to be placed at the load for proper voltage feedback.
R46 10
R91 10
R85 10
R96 10
MICROCHIP_MCP9700AT-E/LT
U60
VDD
VOUT
NC1
NC2
GND
C78 0.1uF
C43 0.01uF
R137 10K
R208 10K
R254 10K
R266 10K
R267 10K
R131 10K
R121 100K
R98 2K
R274 2K
PMBUS1
NC
CTRL
ALERT
CLK
DATA
PMBUS_CON
GND
Each 22uF Cin cap needs to tightly coupled to Vin and PGND of the UCD7242.
C277 0.01uF
C314 22u
C341 22u
U4
TI_UCD7242RSJT
PWM_B
SRE_B
FLT_B
IMON_B
BST_B
BSW_B
SWB
PGND_1
PGND_2
NC-PGND_1
PWM_A
SRE_A
FLT_A
IMON_A
BST_A
BSW_A
SWA
PGND_3
PGND_4
NC-PGND_2
TESTMODE
AGND
VGG_DIS
BP3
VGG
VIN_1
VIN_2
NC-VIN_1
TMON
VIN_3
VIN_4
NC-VIN_2
R129 10K
R67 10K
C275 0.22uF
C75 0.22uF
L2 0.47uH 17.5A
L1 0.47uH 17.5A
C82 1u
C70 4.7u
C280 1u
C283 4.7u
TP2
TP3
CVDD
R123 1K
R122 1K
C104 47uF
C276 47uF
C46 47uF
C278 47uF
DSP Vcore @20A
Each 22uF Cin cap needs to tightly coupled to Vin and PGND of the UCD7242.
C299 0.01uF
C303 22u
C306 22u
U8
R216 10K
R212 10K
C307 0.22uF
C284 0.22uF
L6 0.47uH 17.5A
L3 0.47uH 17.5A
R215 1K
R219 1K
C287 47uF
C308 47uF
C311 47uF
C310 47uF
TP7
TP8
VCC1V0
VCC1V0 @20A
U10
SN74AUP2G32
VSSOP8
1A
1B
2A
2B
1Y
2Y
VCC
GND
UCD7242_1_FFA
UCD7242_1_FFB
UCD7242_2_FFA
UCD7242_2_FFB

0.9V - 1.1V (CVDD) (Smart Reflex)

Fix_1.0V(VCC1V0)







1.0V Serdes