HINDUJA HYPER CAR HEAD MPU

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BOARD REVISION	ET-001
SCHEMATIC VERSION	1.0

Note:
Verify the DNI components configuration with respect to the SK schematics (Use PDF) after completion of design before board assembly

Link to Design Collaterals : https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am62x-am62ax-custom-board-hardware-design---collaterals-for-reference-during-schematic-design-and-schematics-review

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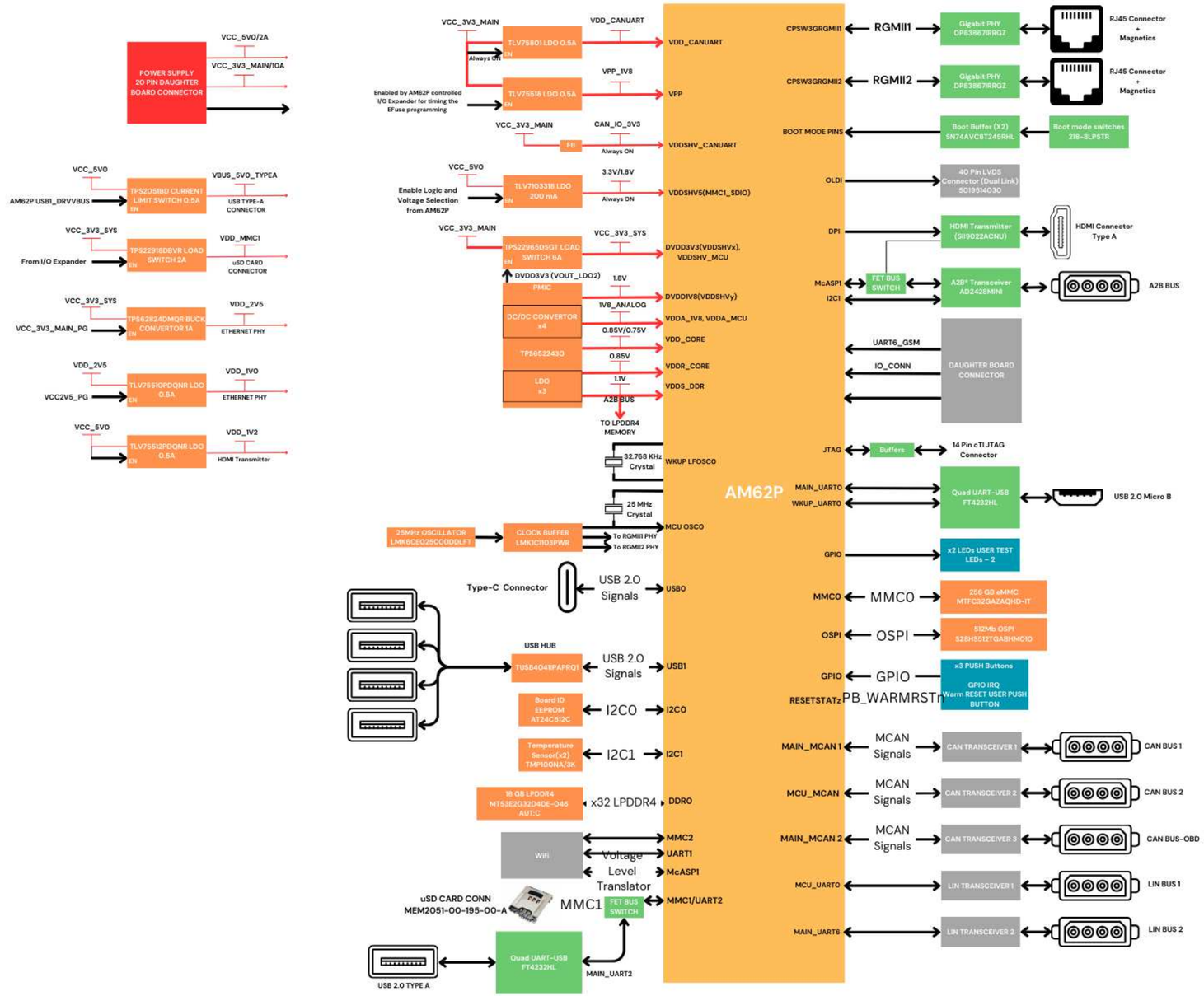
BLOCK DIAGRAM OF VIRTUAL COCKPIT MAIN_BRD



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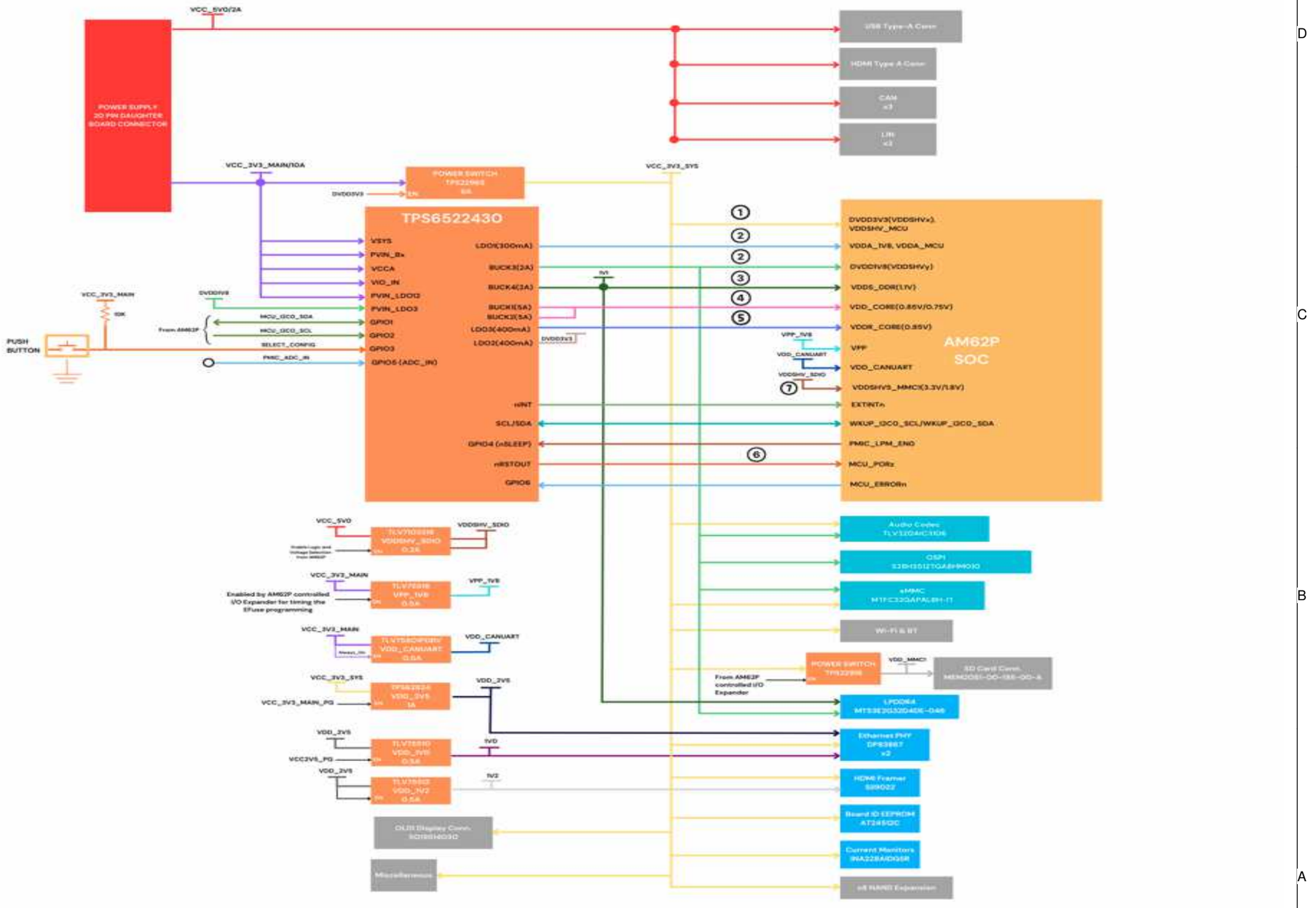
POWER ARCHITECTURE BLOCK DIAGRAM



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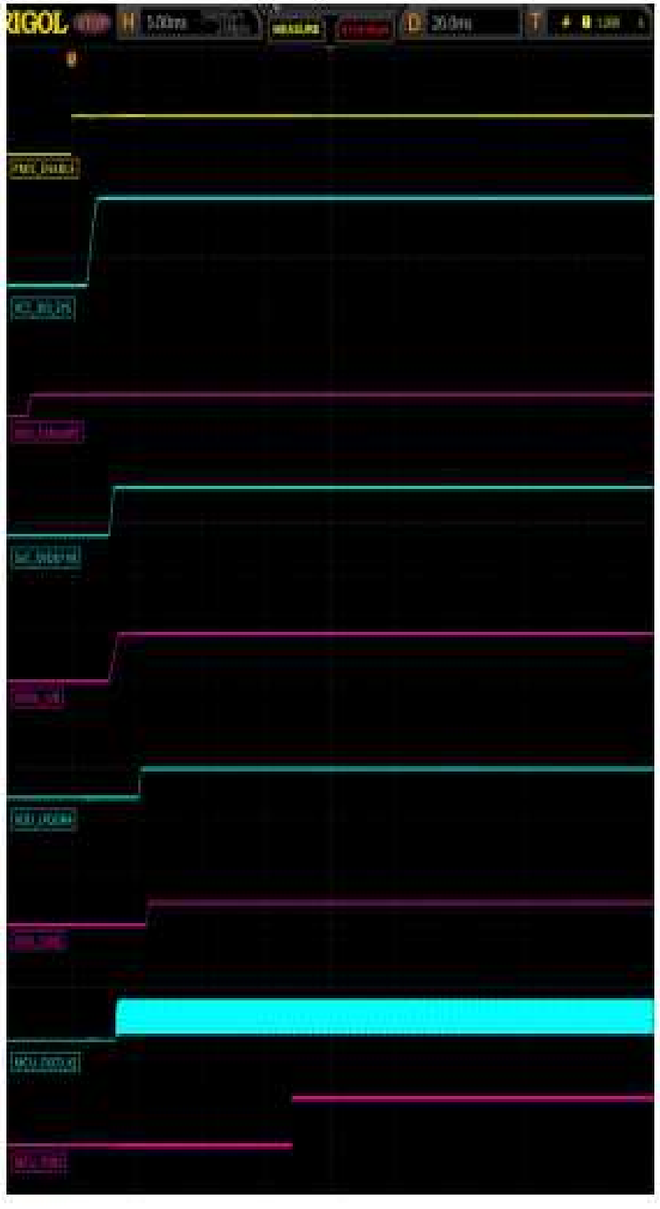
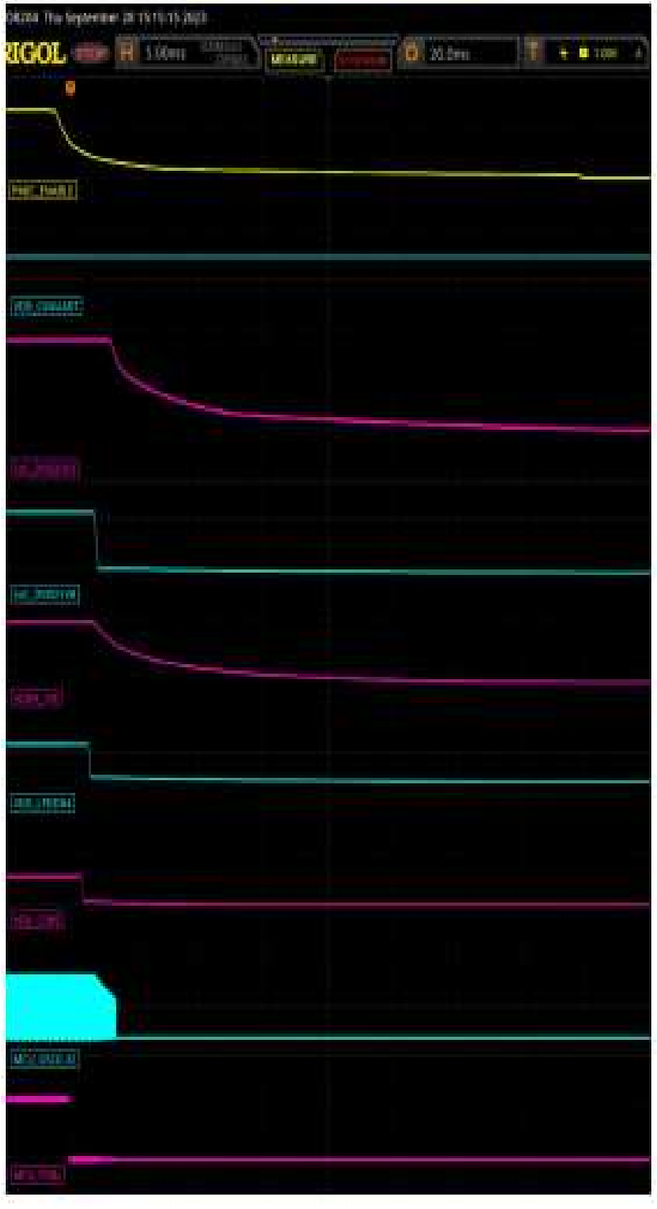
POWER UP SEQUENCE



POWER DOWN SEQUENCE



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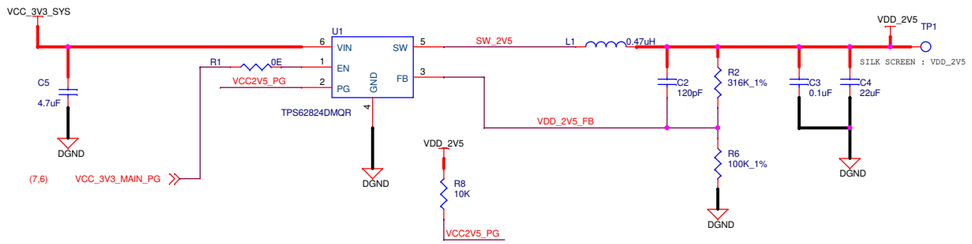
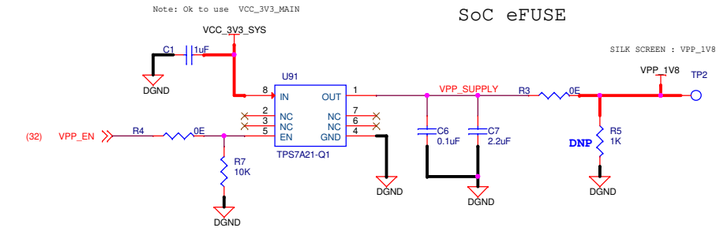
PERIPHERAL POWER SUPPLY-1

2.5V (ETHERNET PHY), 1.0AMPS SUPPLY

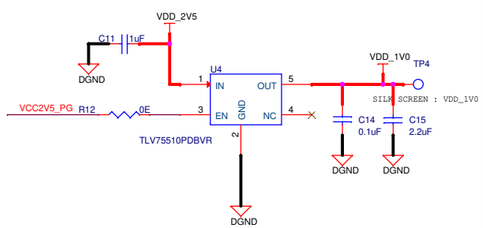


1.8V VPP (eFUSE), 0.5AMPS SUPPLY



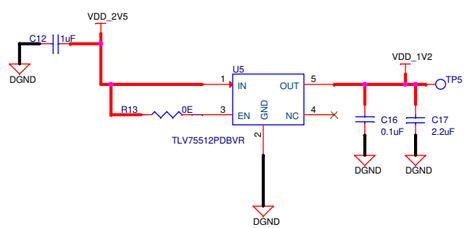
Package changed

1.0V (ETHERNET PHY), 0.5AMPS SUPPLY



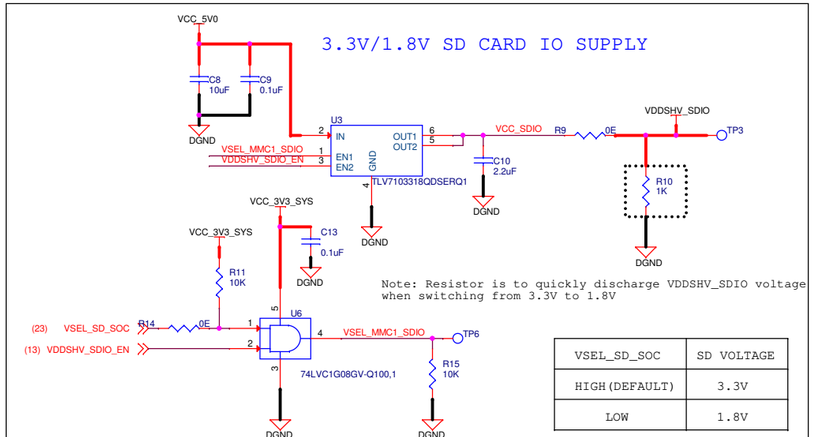
Package changed

1.2V (HDMI), 0.5AMPS SUPPLY



Package changed

3.3V/1.8V SD CARD IO SUPPLY



Note: Resistor is to quickly discharge VDDSHV_SDIO voltage when switching from 3.3V to 1.8V

VSEL_SD_SOC	SD VOLTAGE
HIGH(DEFAULT)	3.3V
LOW	1.8V

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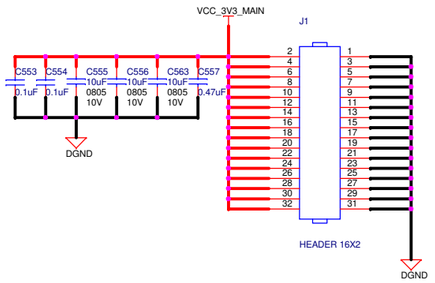
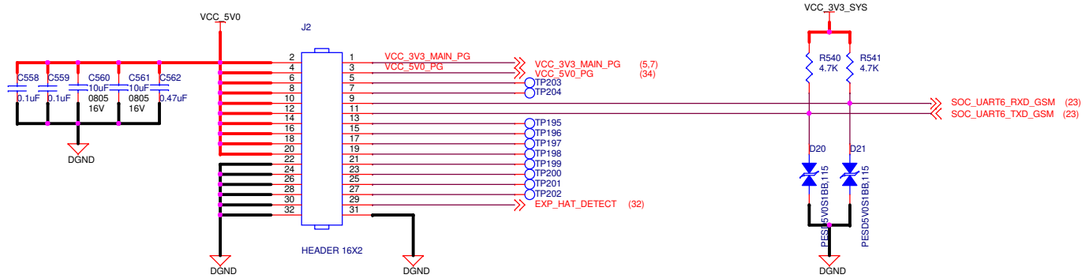
PERIPHERAL POWER SUPPLY-2





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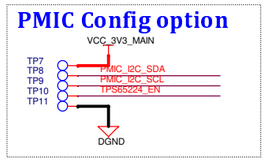
SOC POWER SUPPLY PMIC

PMIC Config option



Silk: PMIC_PROG

CAD Note :-
Follow Kelvin connection for Current
Sensing when using 2 terminal resistors

Route as Pseudo differential pair trace
from Load (Remote Sense)
(See "PCB Notes")

Silk: PMIC

PMIC uses default I2C1 ADDR: 0x48,0x49, 0x4A, 0x4B

Silk: PMIC_LPM_SEL

PMIC PUSH BUTTON LOGIC

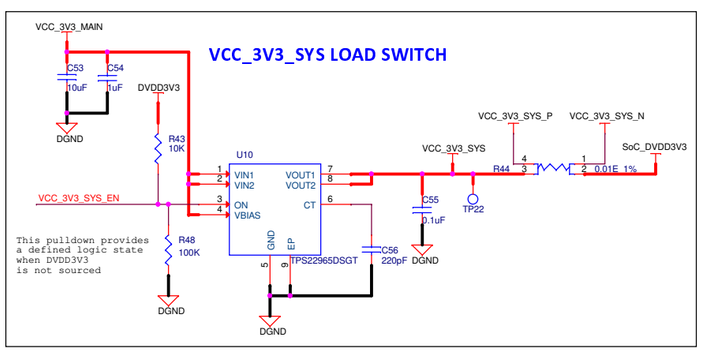
R41	VDD_CORE VOLTAGE
Mounted	0.85 V (DEFAULT)
Not Mounted	0.75 V

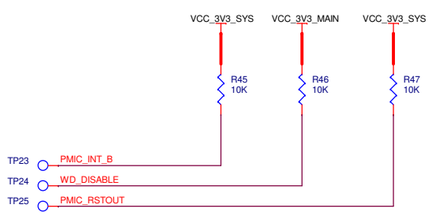
Silk: PMIC_CORE_CONFIG

Note: When R157 is DNI, Push Button (SW2) becomes operational through internal pullup on PMIC GPIO3

PMIC POWER INDICATION LED

VCC_3V3_SYS LOAD SWITCH





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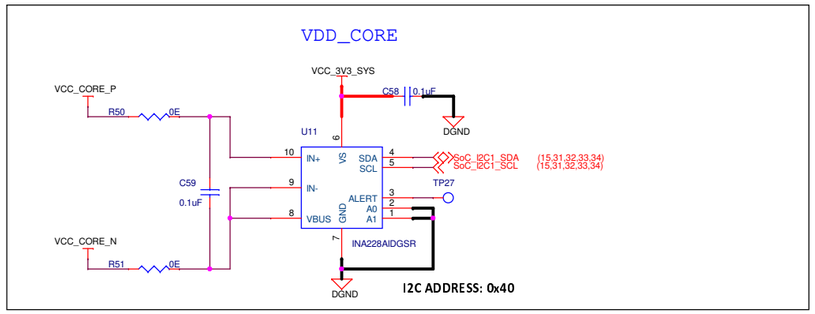
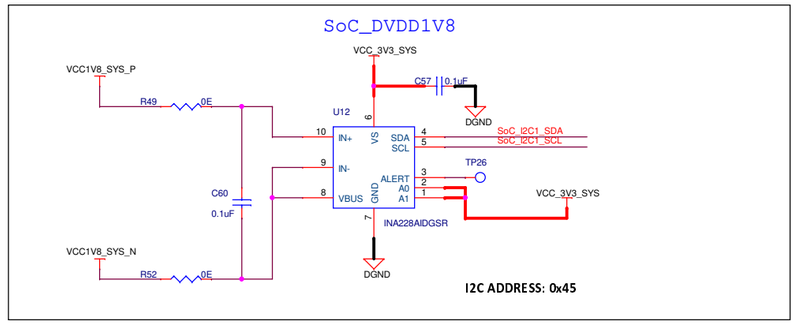
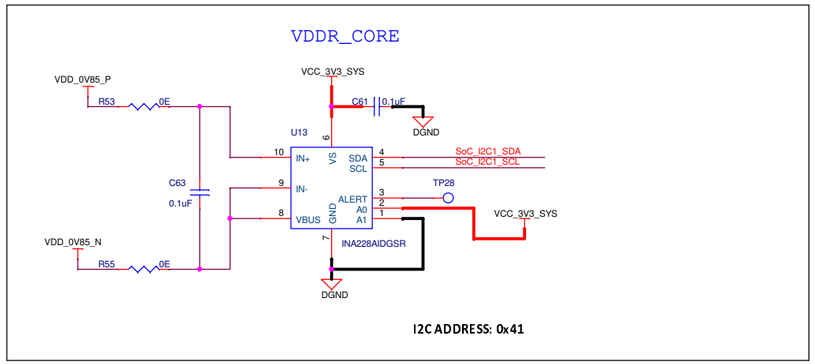
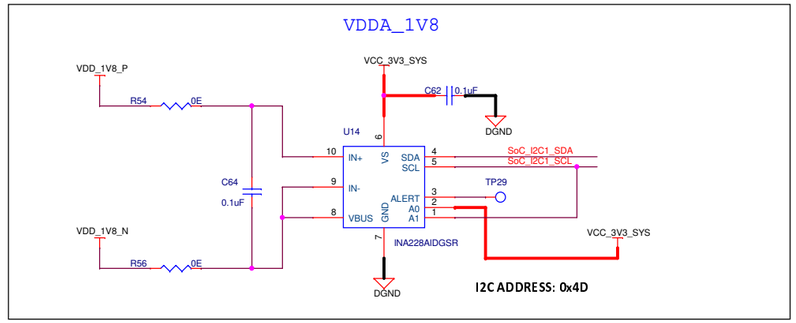
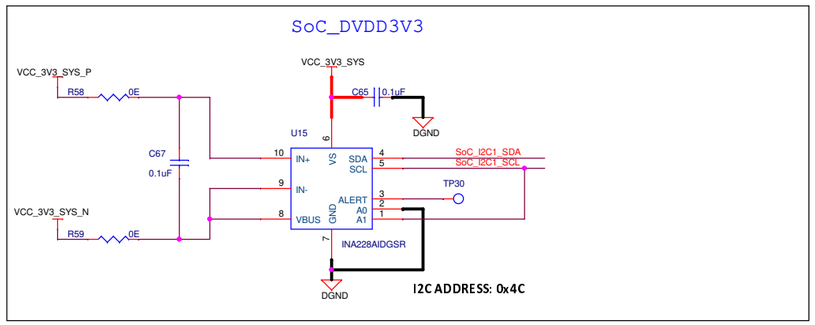
CURRENT MONITORING DEVICES - 2

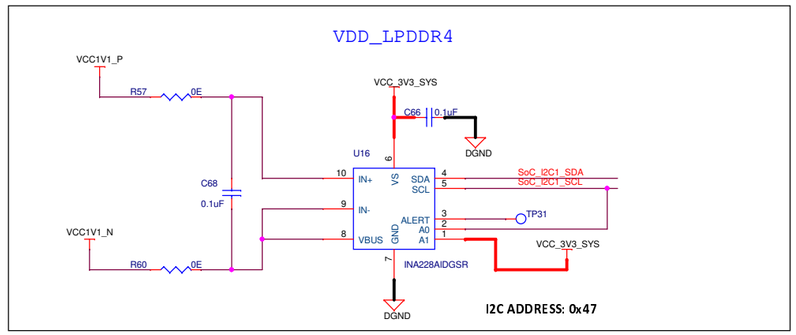












Note: The design supports current/voltage measurements using either INA228 or INA231. INA228 will be populated on the the SK (Implemented via stacked PCB footprint).

INA I2C SLAVE ADDRESS

POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

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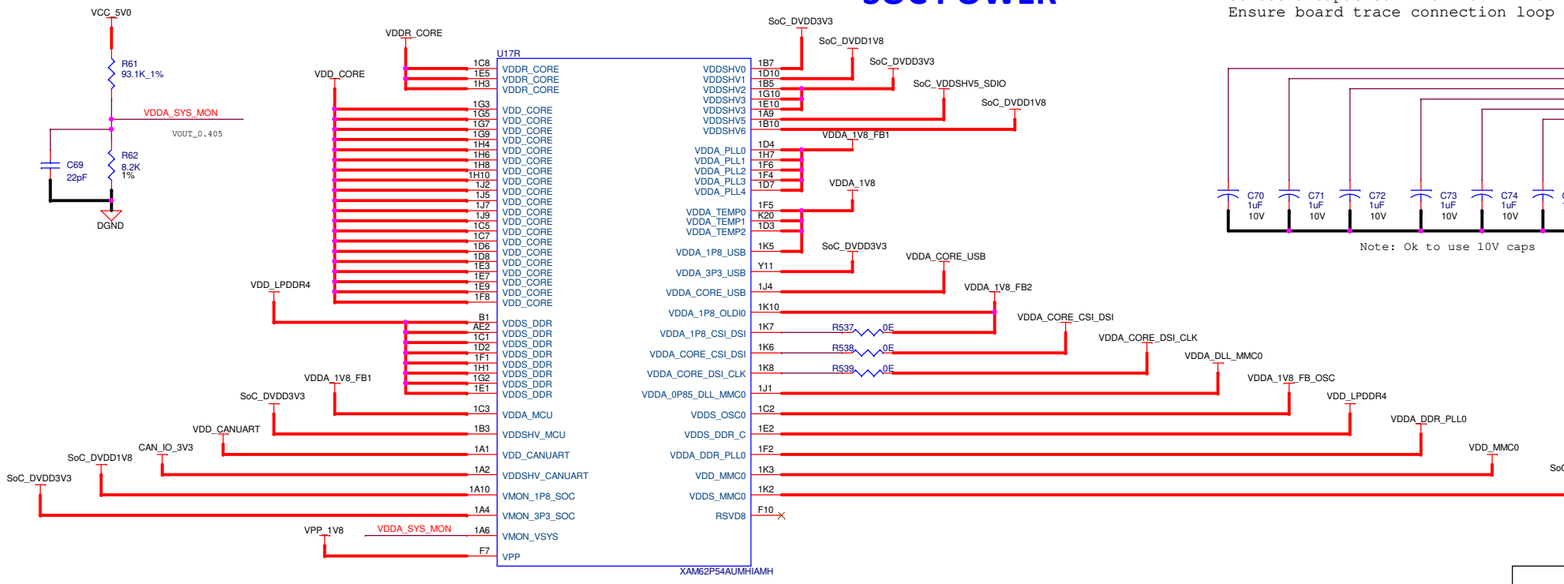
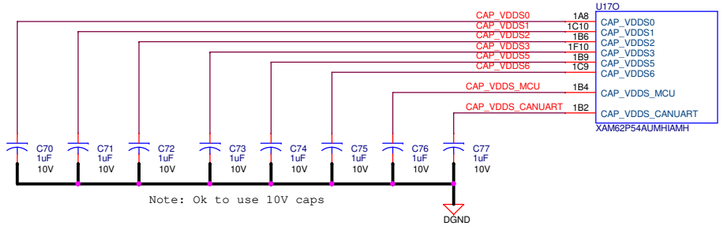
SOC POWER

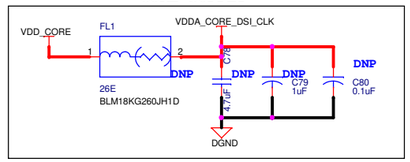


Select a capacitor with ESR < 1 O
Ensure board trace connection loop inductance is < 2.5-nH

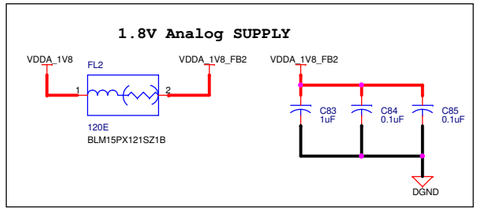


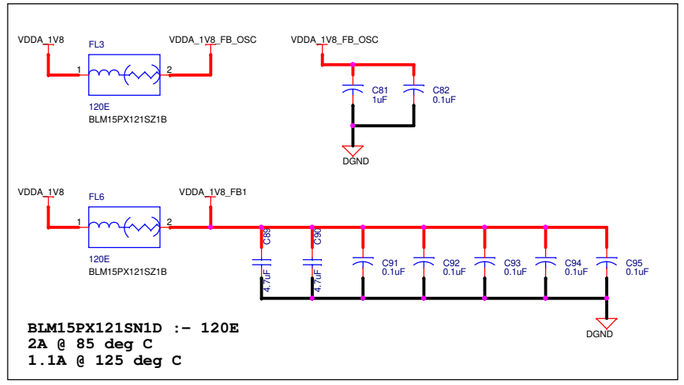
Note: Ok to use 10V caps

CORE SUPPLY

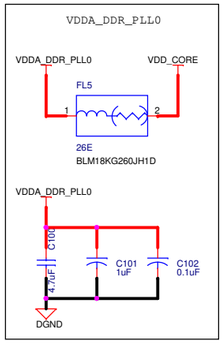


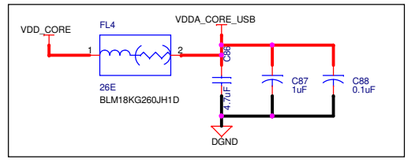
1.8V Analog SUPPLY

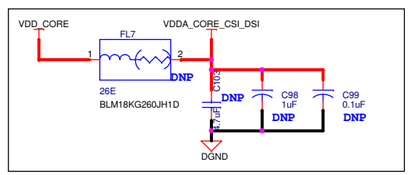


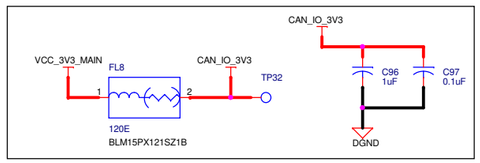


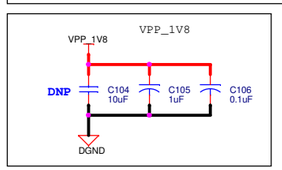
BLM15PX121SN1D :- 120E
2A @ 85 deg C
1.1A @ 125 deg C



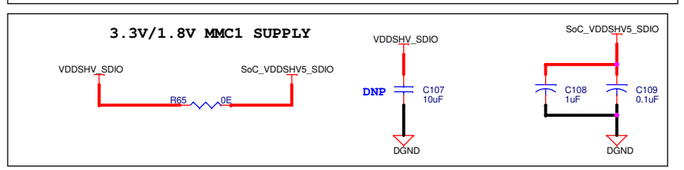


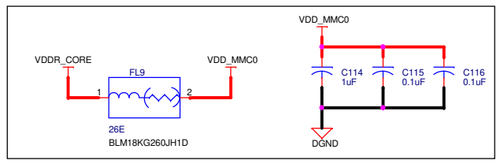


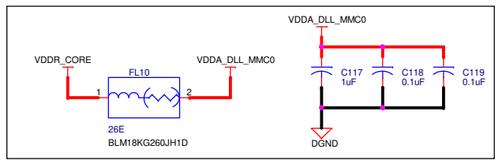


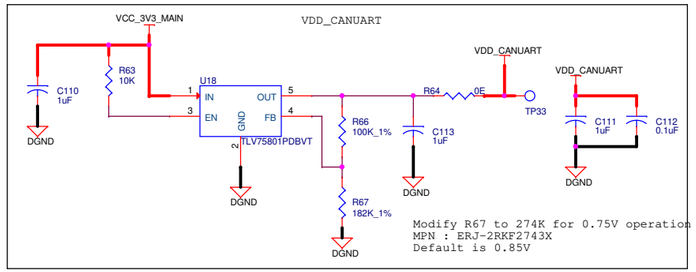


3.3V/1.8V MMC1 SUPPLY









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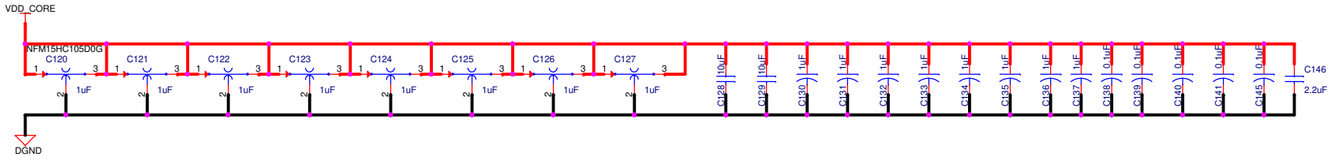
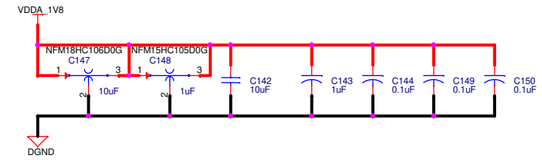
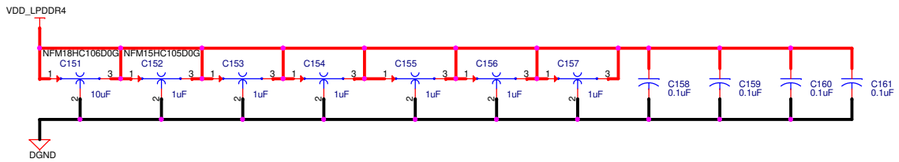
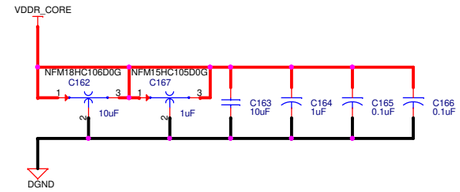
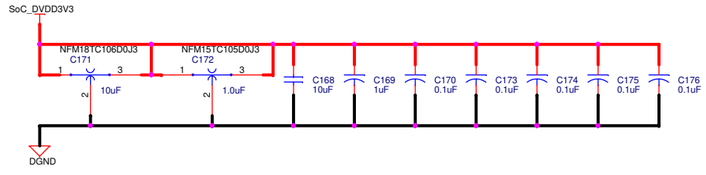
SOC POWER DECAPS

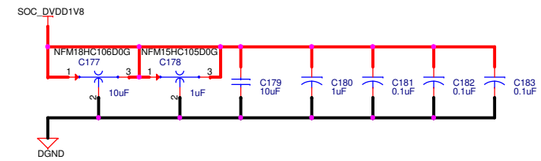




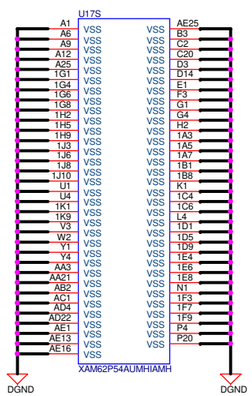








SOC VSS



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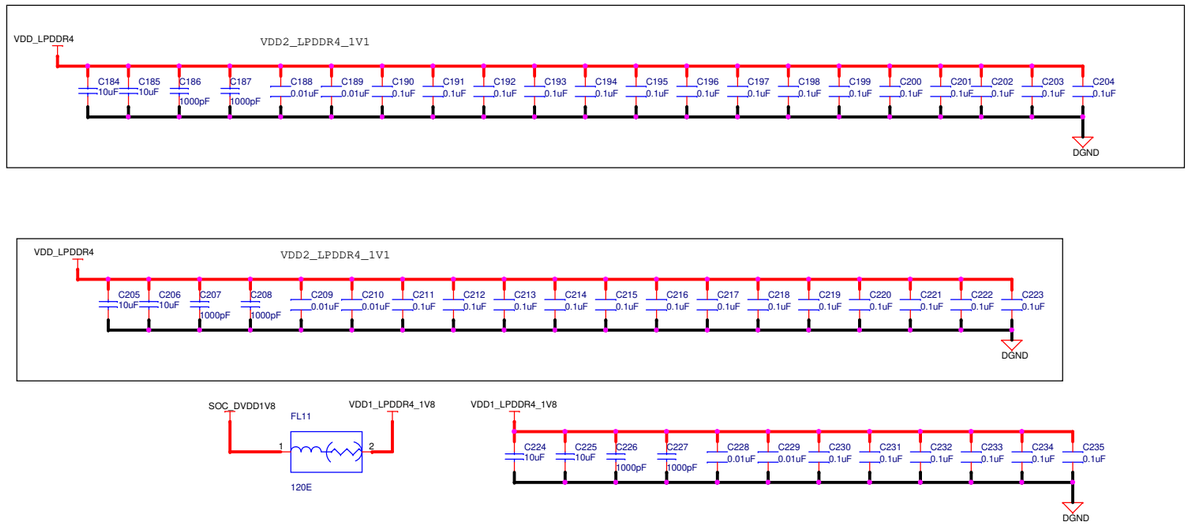
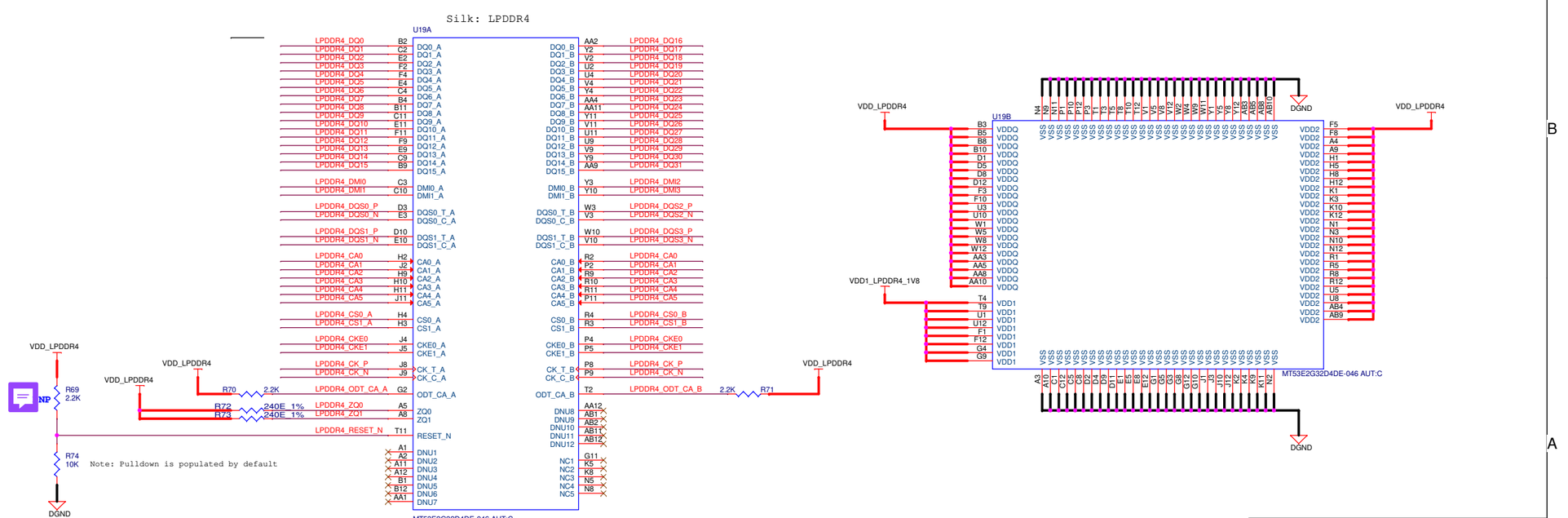
SOC LPDDR4 INTERFACE

LPDDR4 POWER DECAPS



LPDDR4 DEVICE



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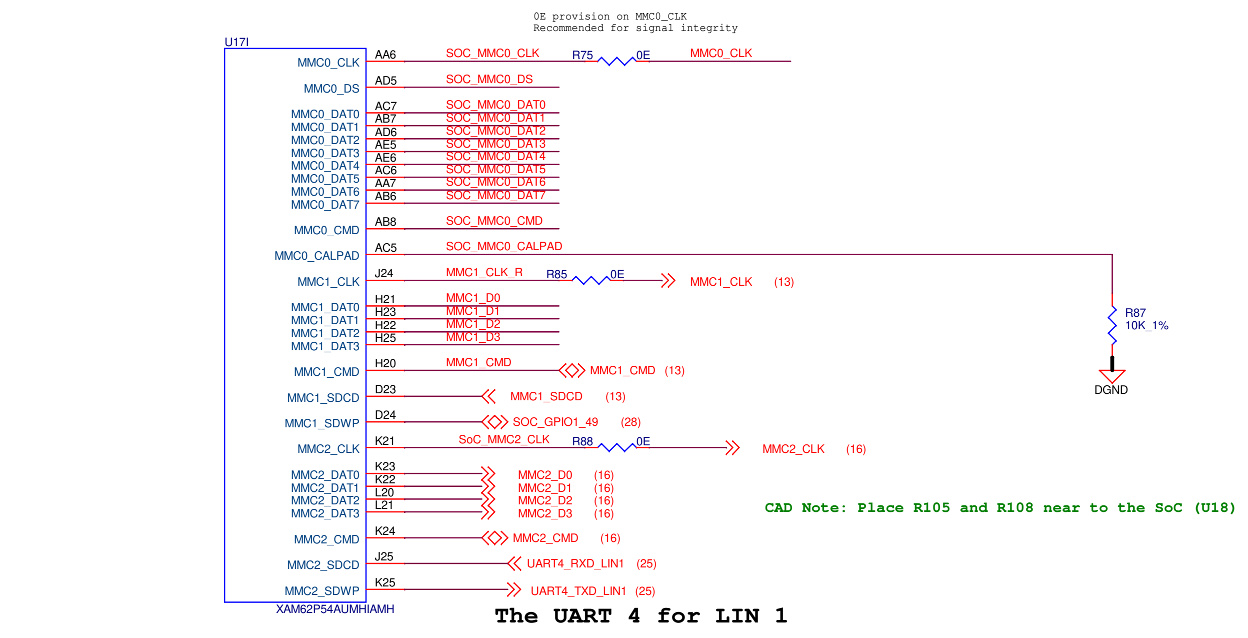
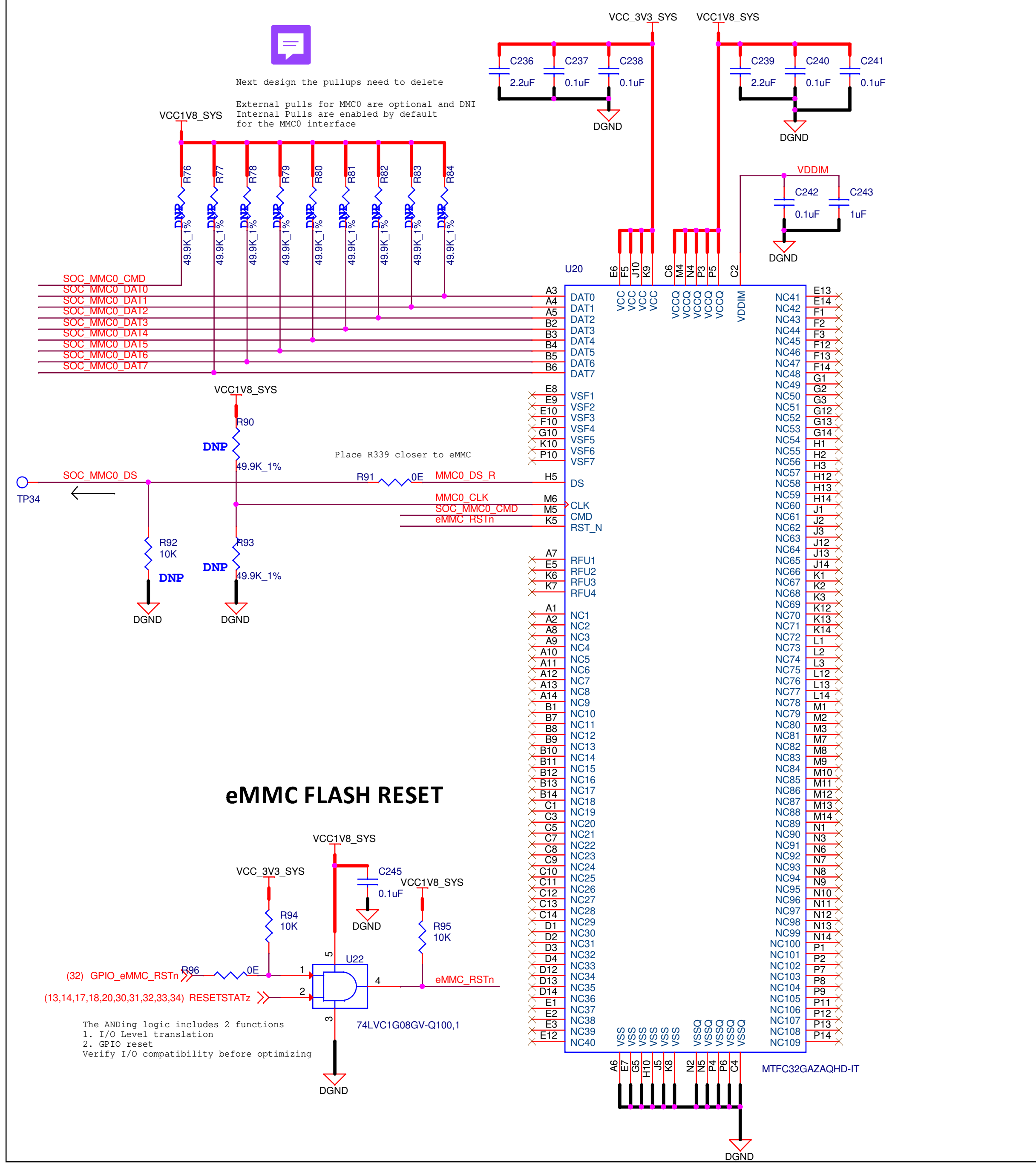
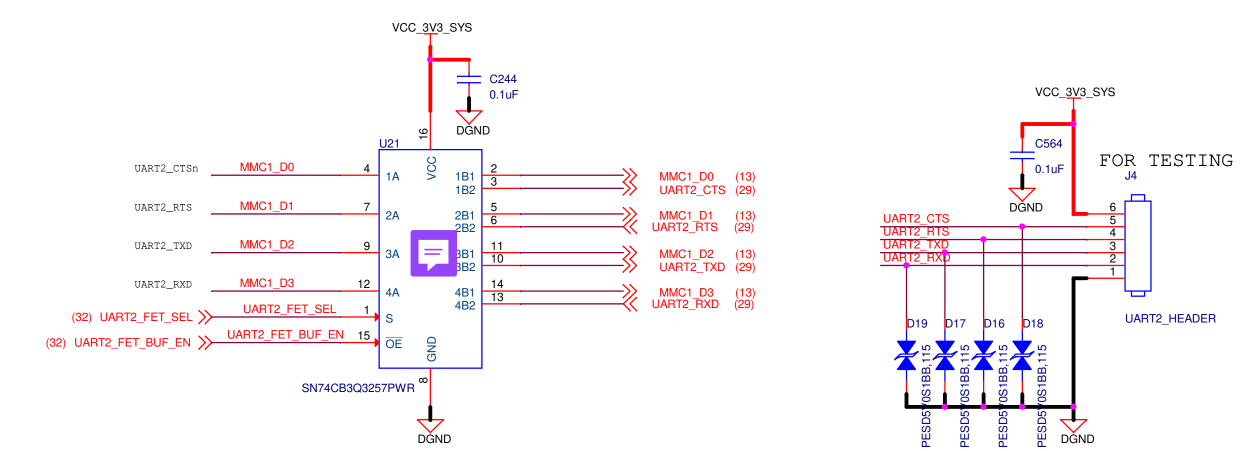
SOC - MMC Interface



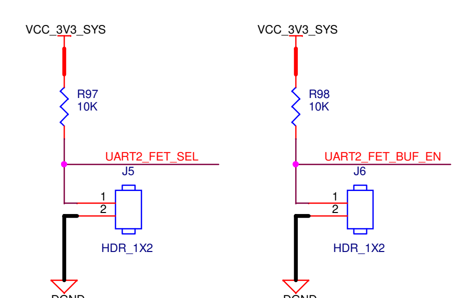
eMMC FLASH



UART FET SW FOR LIN,USB BRIDGE & SD CARD



OEn	SEL	INPUT/OUTPUT An	
L	L	An=nB1	SOC - SD-CARD
L	H(DEFAULT)	An=nB2	SOC - UART2_USB



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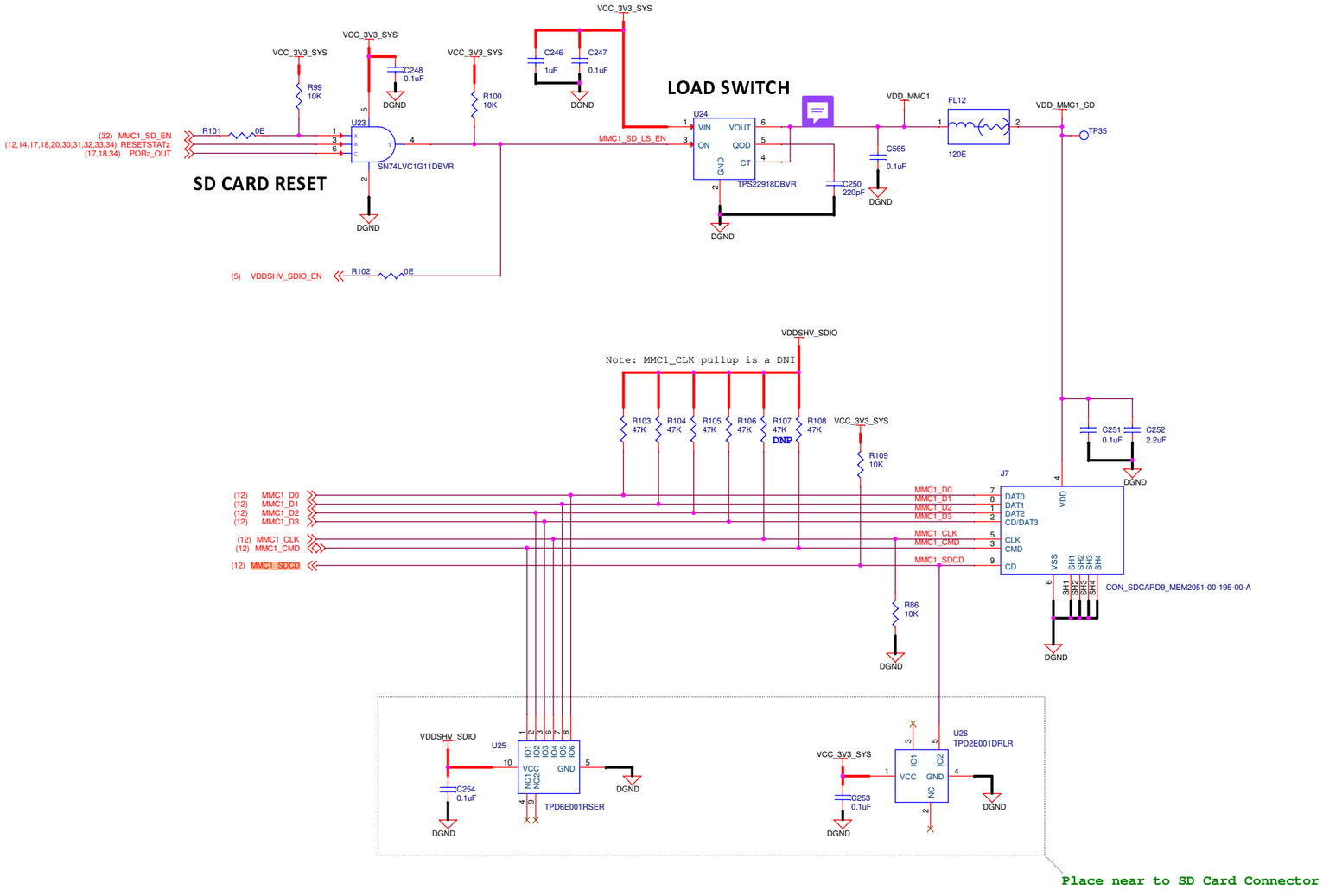
SD CARD INTERFACE



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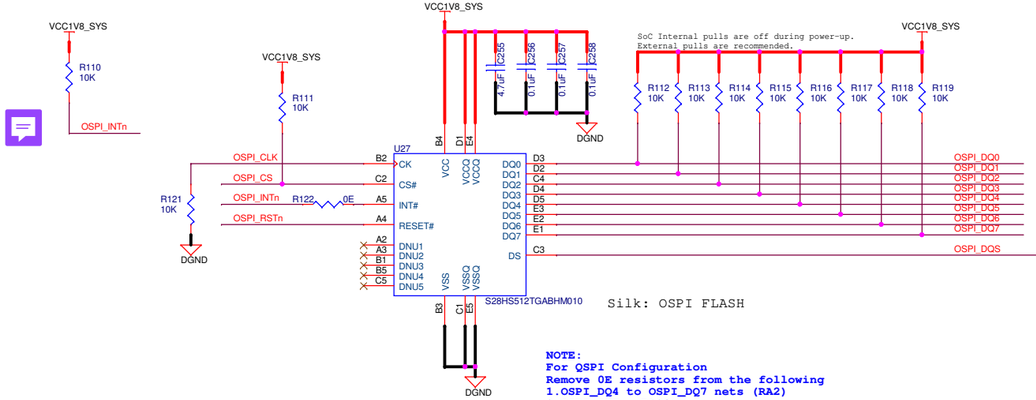
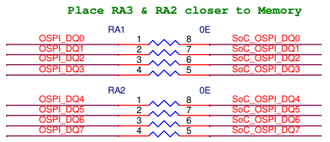
OSPI FLASH



NOTE:
For QSPI Configuration
Remove 0E resistors from the following
1.OSPI_DQ4 to OSPI_DQ7 nets (RA2)
2.OSPI_INTn (R129)
OSPI NOR Flash can be replaced with the Footprint compatible OCTAL NAND Flash (Mfr Part# W35N01JWTBAG)

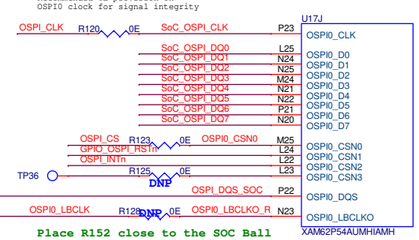
Place RA3 & RA2 closer to Memory



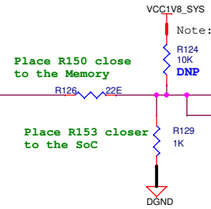
These series resistors are for enabling OSPI and QSPI
These are specific to SK and optional if the interface is fixed

SOC OSPI INTERFACE

Recommended 0E provision on
OSPI0 clock for signal integrity



OSPI0_LBCLK series resistors(R151 and R152) are DNI



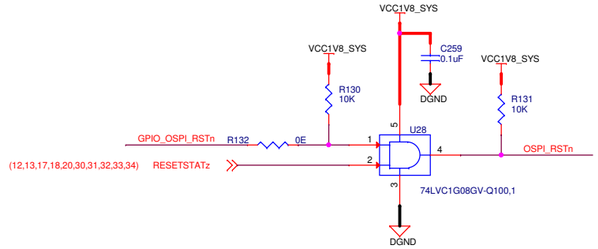
Place R150 close to the Memory

Place R153 closer to the SoC

Tripad R150 & R151 to avoid stubs

Place R152 close to the SOC Ball with as little trace as possible

OSPI FLASH RESET



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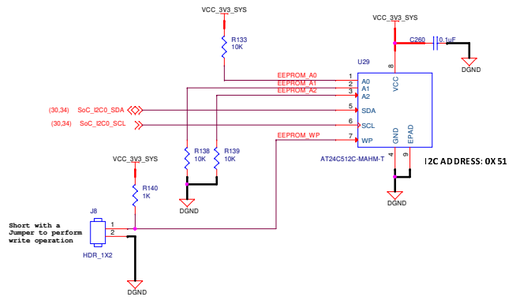
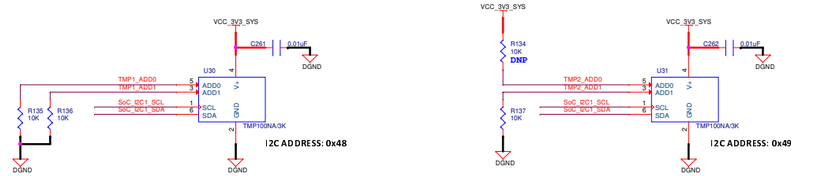
BOARD ID EEPROM

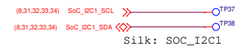


TEMPERATURE SENSORS



CAD NOTE: PLACE TEMP SENSOR U16 CLOSE TO SoC

CAD NOTE: PLACE TEMP SENSOR U10 CLOSE TO LPDDR4



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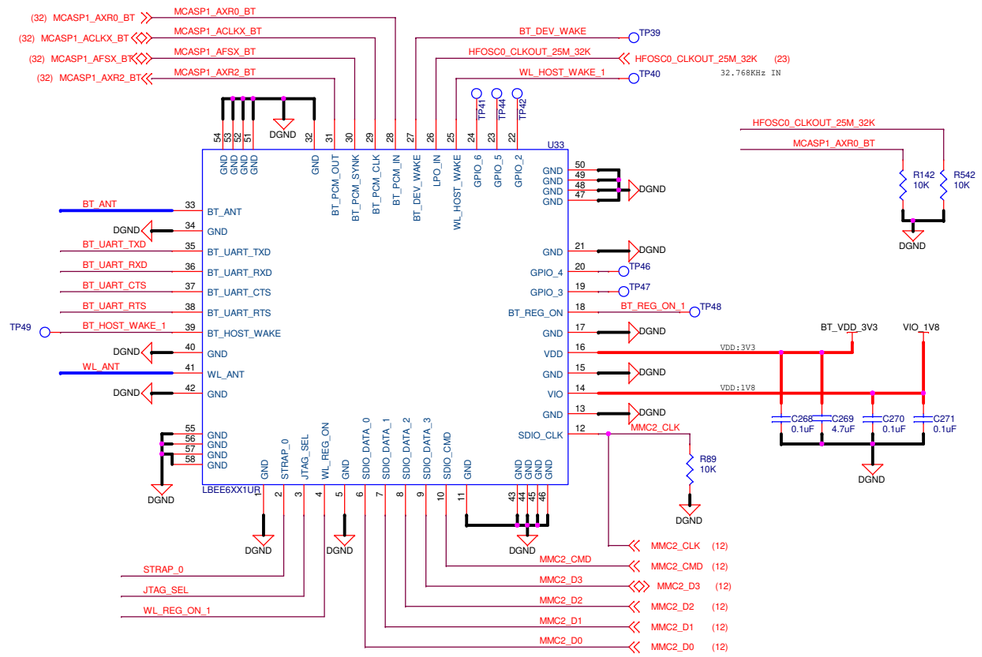
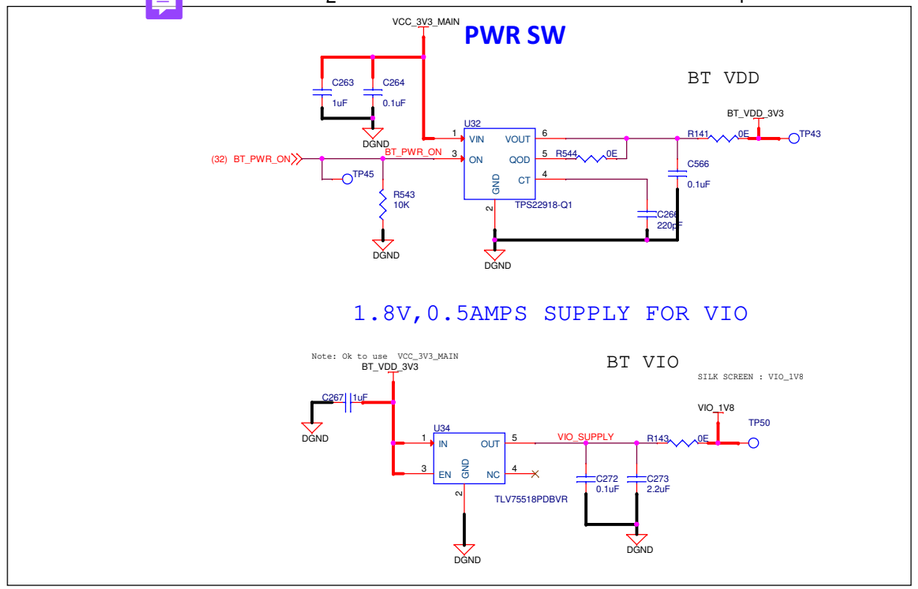
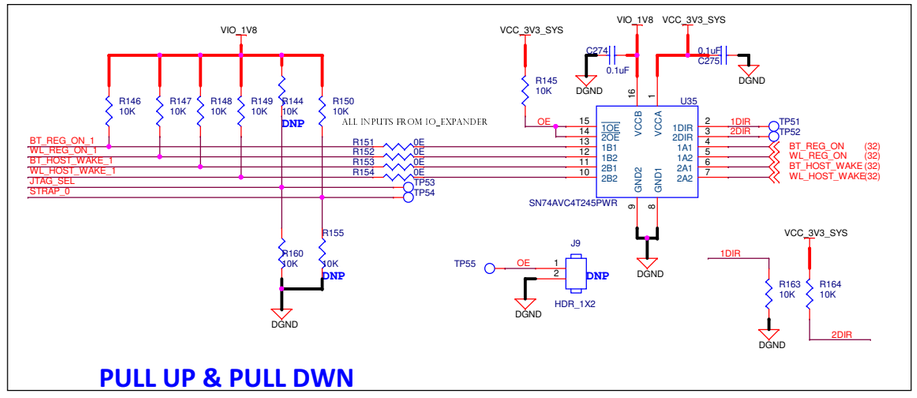
SOC_WIFI&BT/BLE MODULE

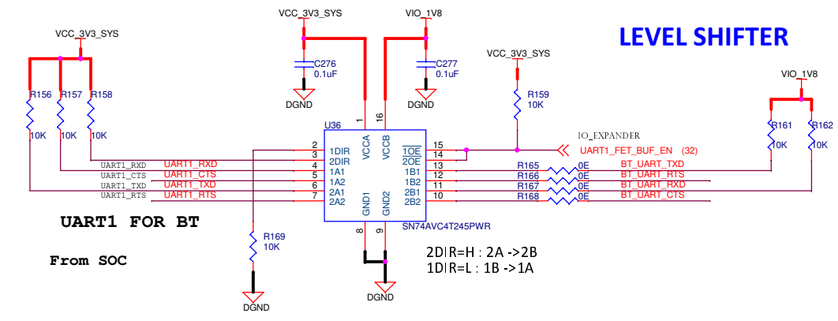


PWR SW

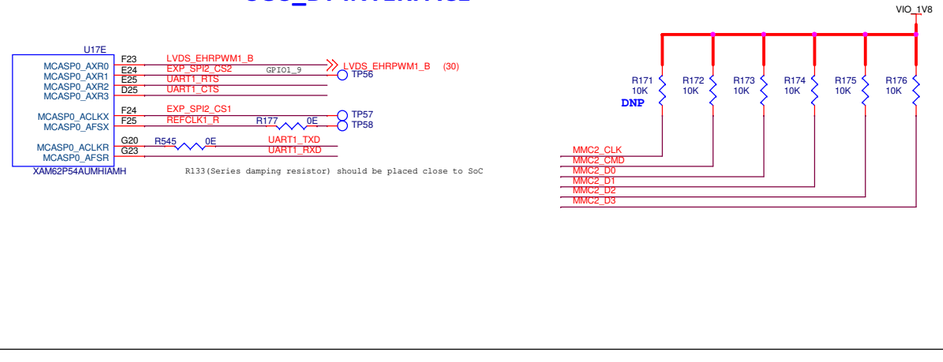




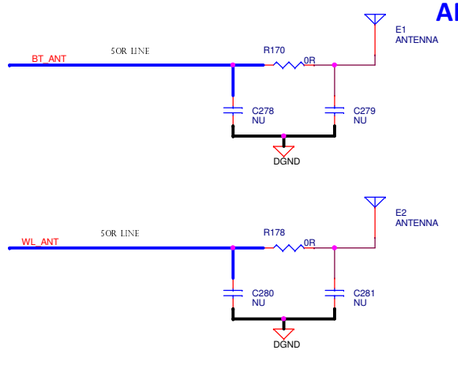
LEVEL SHIFTER



SOS_BT INTERFACE



ANTENNAS



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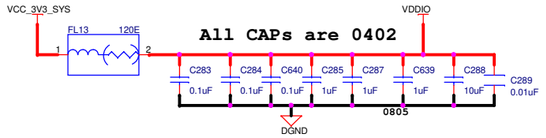
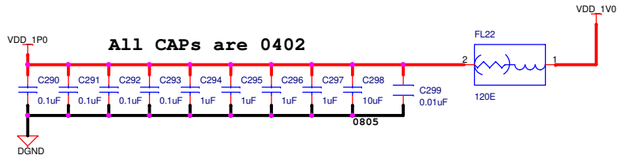
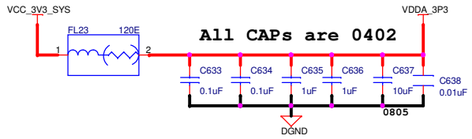
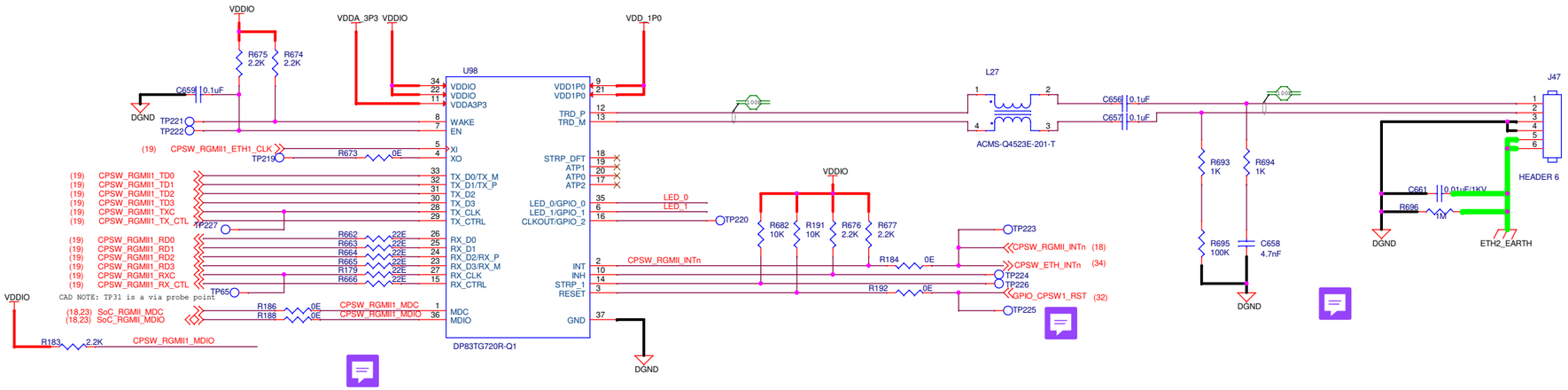
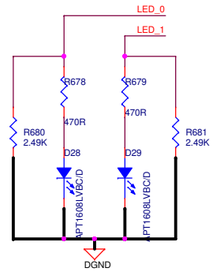
CPSW3G RGMII 1 - PHY











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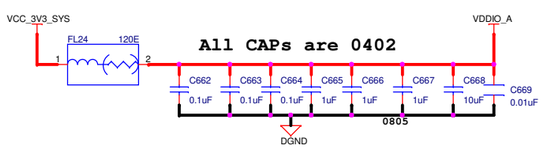
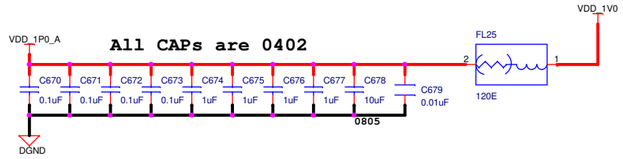
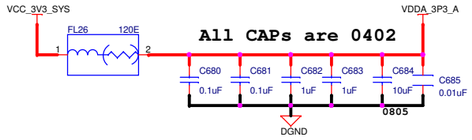
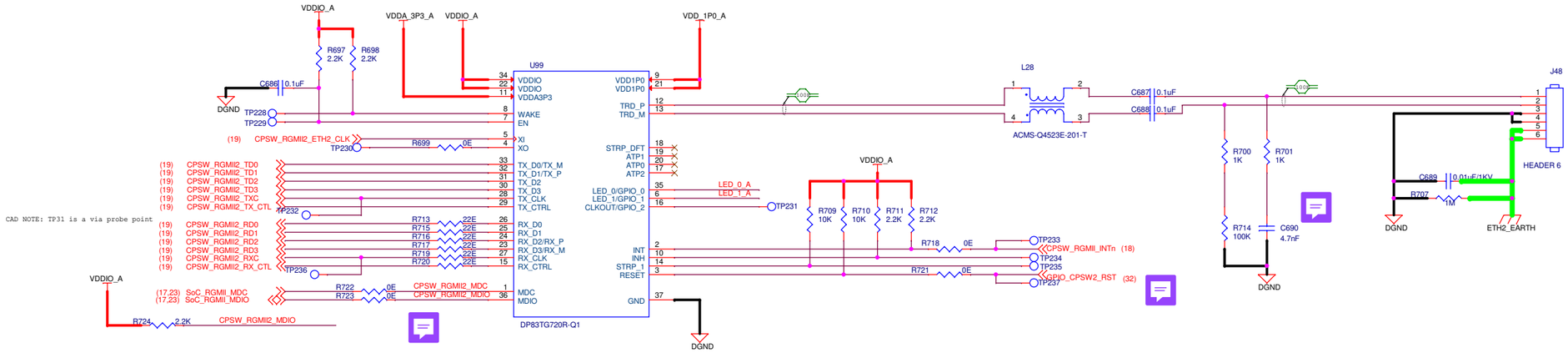
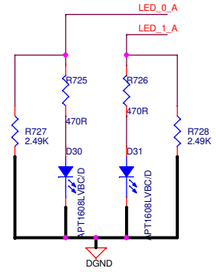
CPSW3G RGMII 2 - PHY











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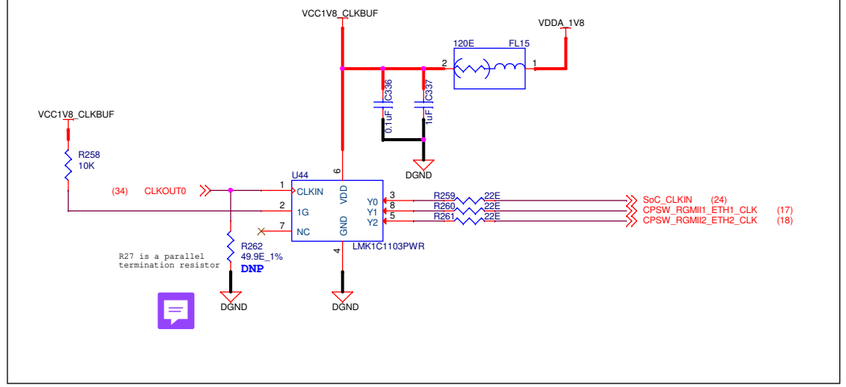
SOC CPSW3G ETHERNET INTERFACE

SOC & ETHERNET PHY CLOCK BUFFER



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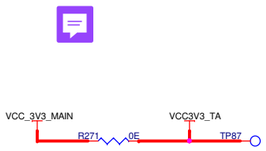
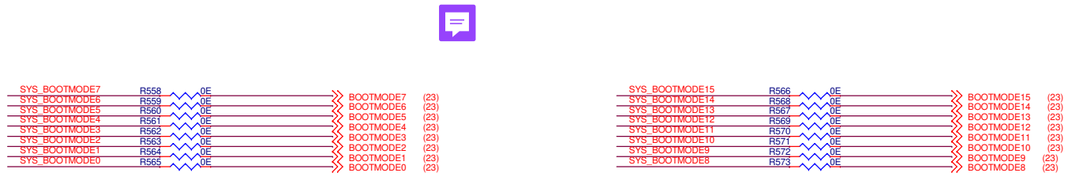
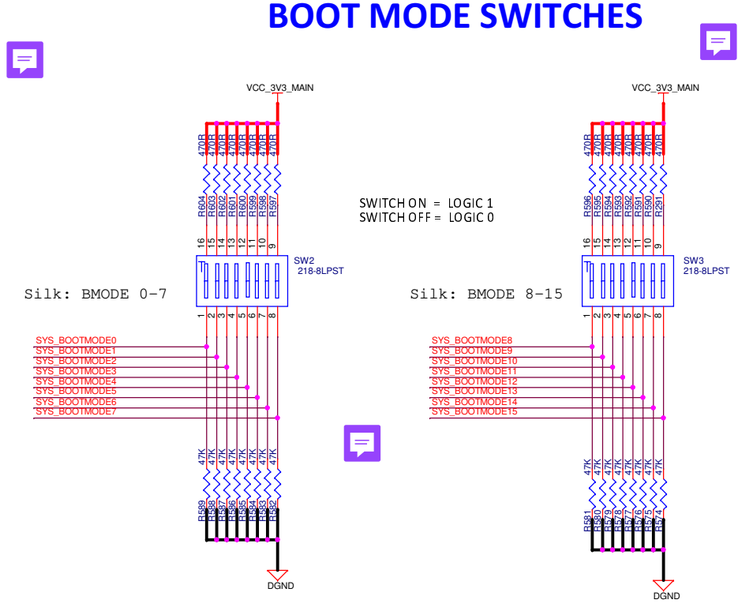


BOOT MODE BUFFERS



BOOT MODE SWITCHES



BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. ETHERNET
6. USB0 DFU
7. USB0 MS

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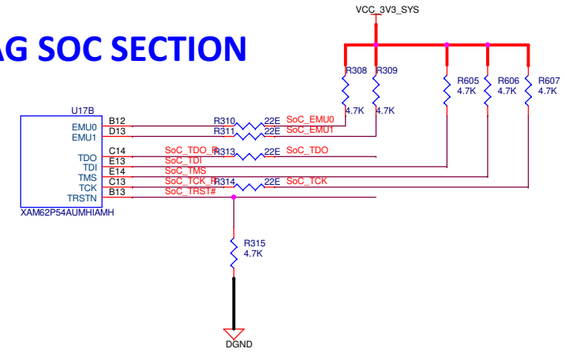
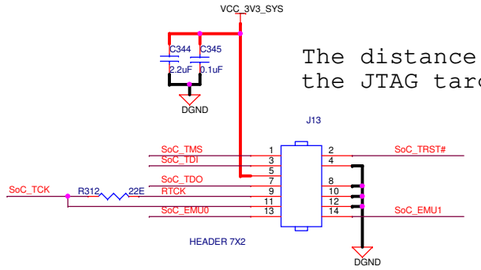
The EMU and TDO series termination values should be placed within 0.5" of the device with total routing length not to exceed 3"

JTAG SOC SECTION



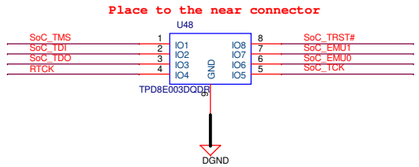
JTAG 14 PIN CONNECTOR



The distance between the header and the JTAG target device should be no more than 6 inches.

Table 1. 14-Pin Header Signal Descriptions
1.TMS Test mode select
2.TDI Test data input
3.TDO Test data output
4.TCK Test clock
TCK is a 10.368-MHz clock source from the emulation cable pod.
This signal can be used to drive the system test clock
5.TRST† Test reset
6.EMU0 Emulation pin
7.EMU1 Emulation pin
8.PD(VCC) Presence detect. Indicates that the emulation cable is connected and that the target is powered up.
PD should be tied to VCC in the target system.
9.TCK_RET Test clock return.
Test clock input to the emulator.
May be a buffered or unbuffered version of TCK.
10.GND Ground

ESD Diode



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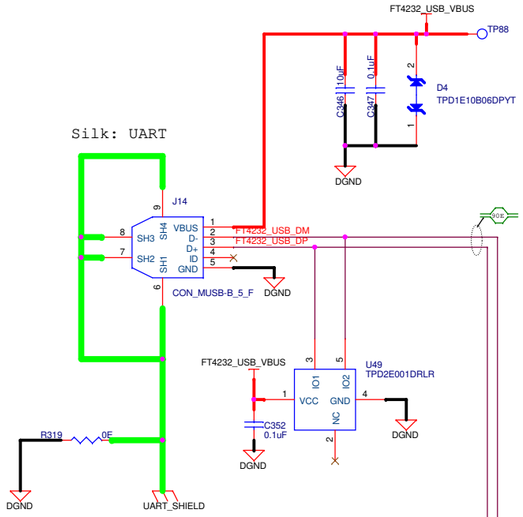
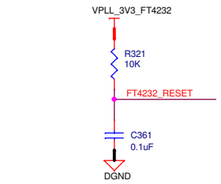
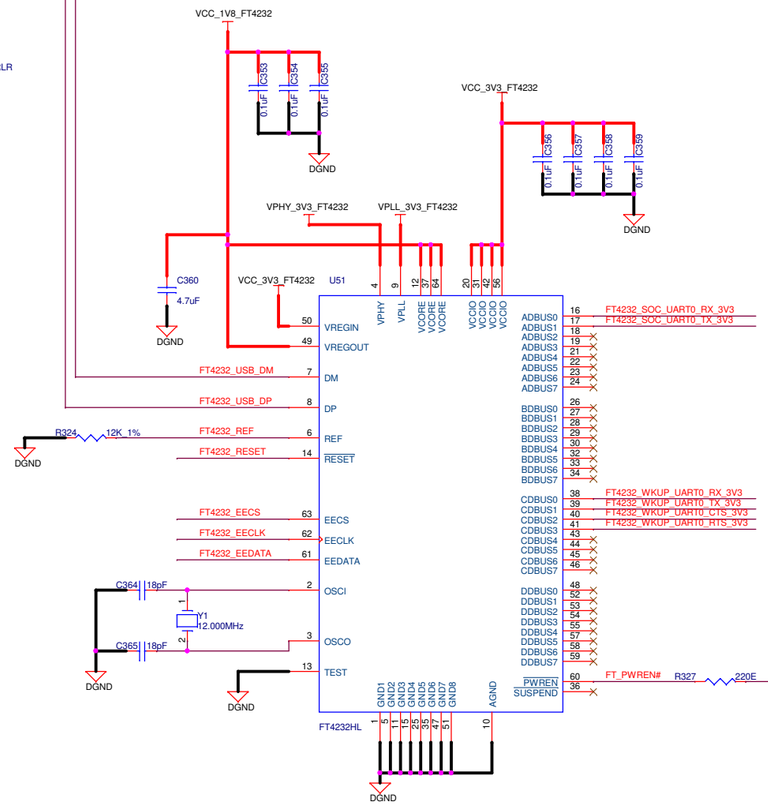
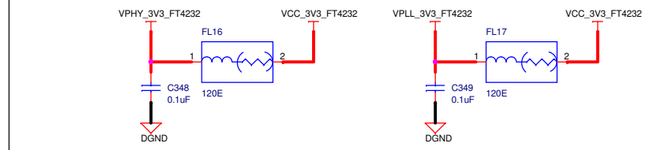
FT4232 UART

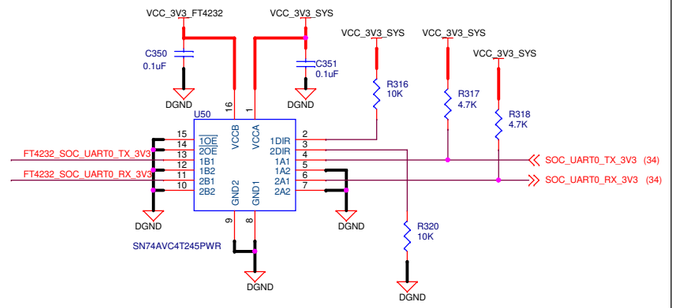
Silk: UART

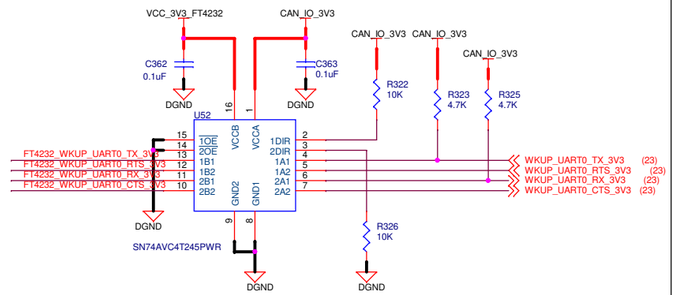




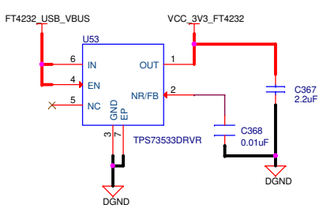




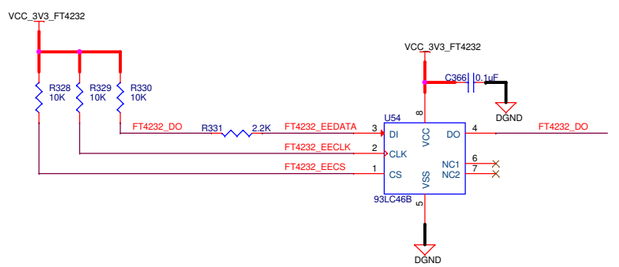




FT4232: 5V to 3.3V@500mA LDO



EEPROM



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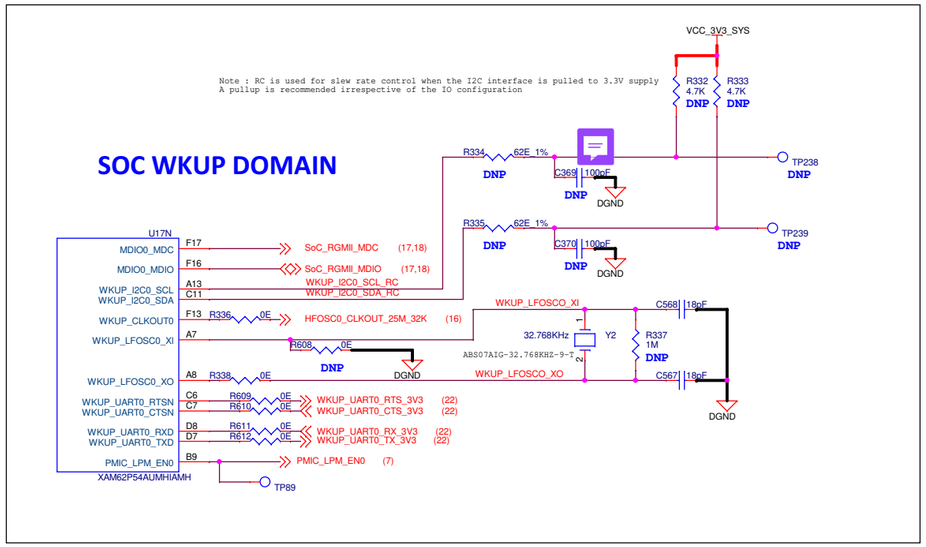
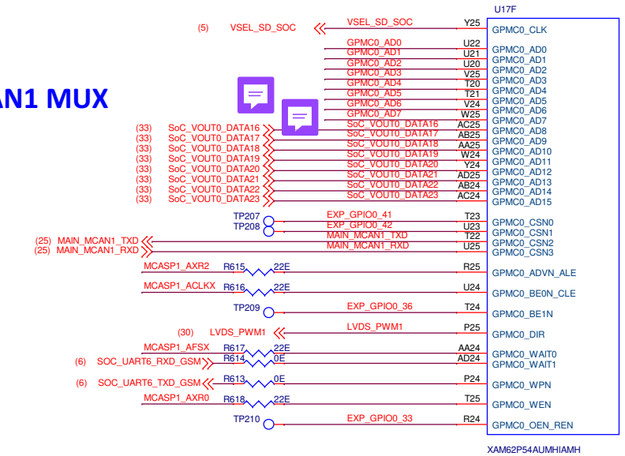
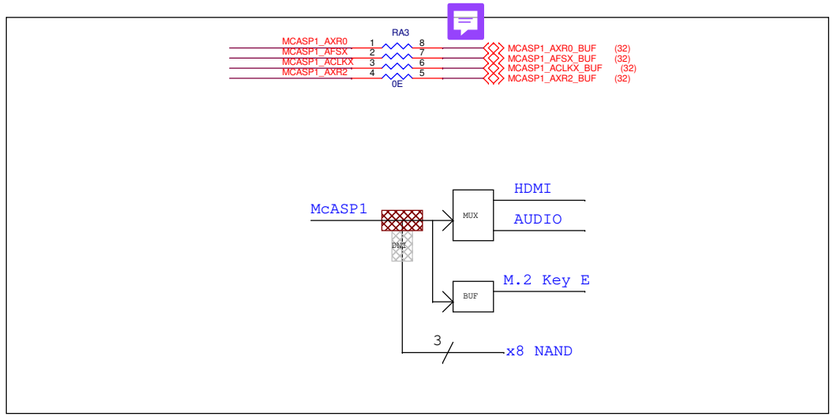
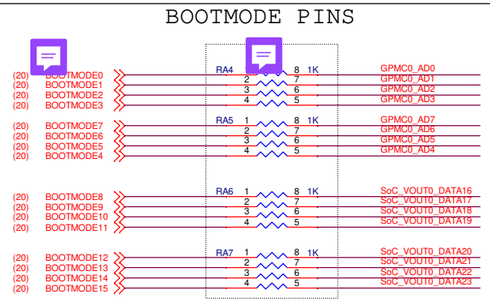
SOC WKUP DOMAIN



SOC I2C2/MCAN1 MUX







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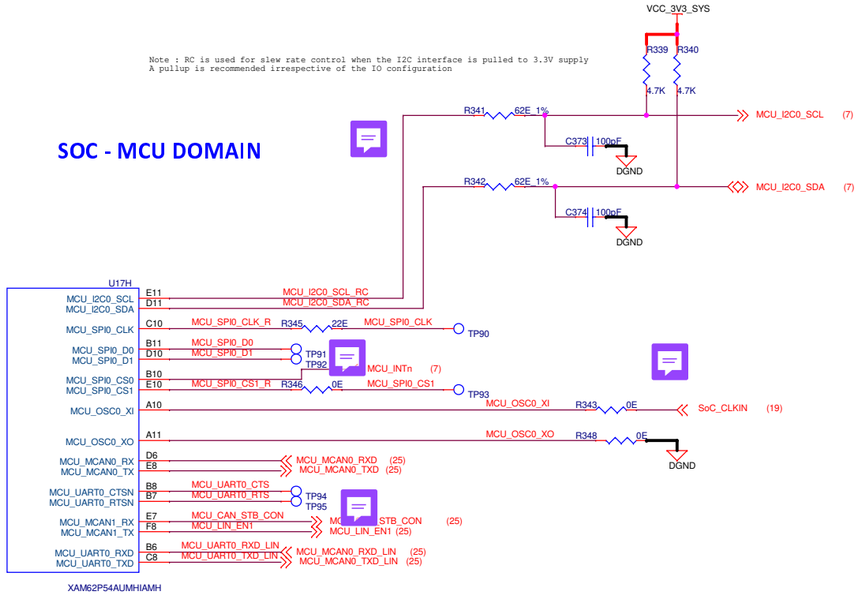
SOC - MCU DOMAIN

Note : RC is used for slew rate control when the I2C interface is pulled to 3.3V supply
A pullup is recommended irrespective of the IO configuration



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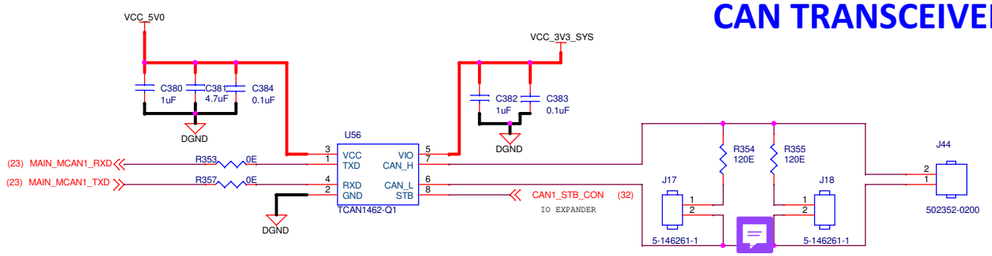
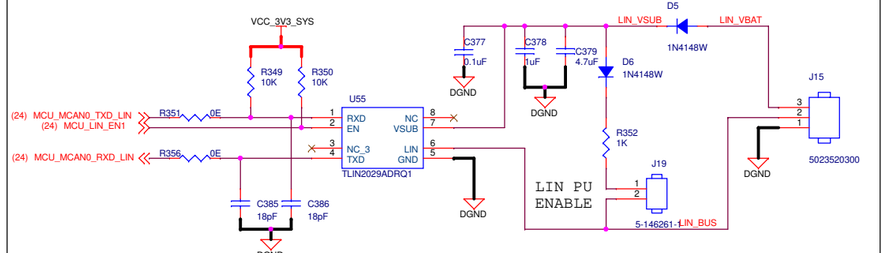
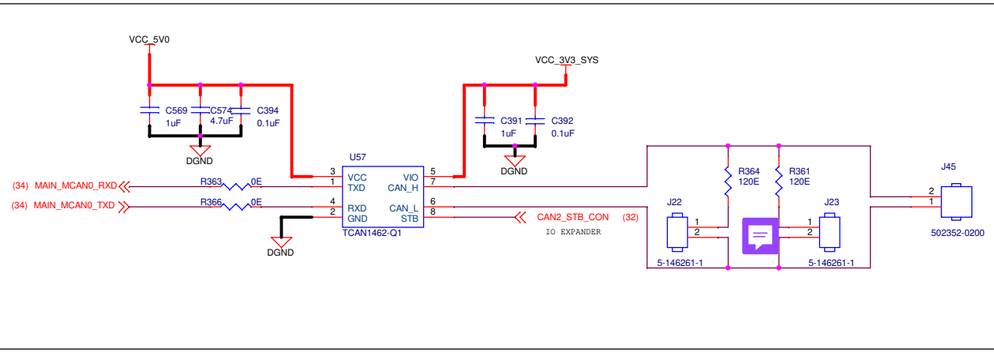
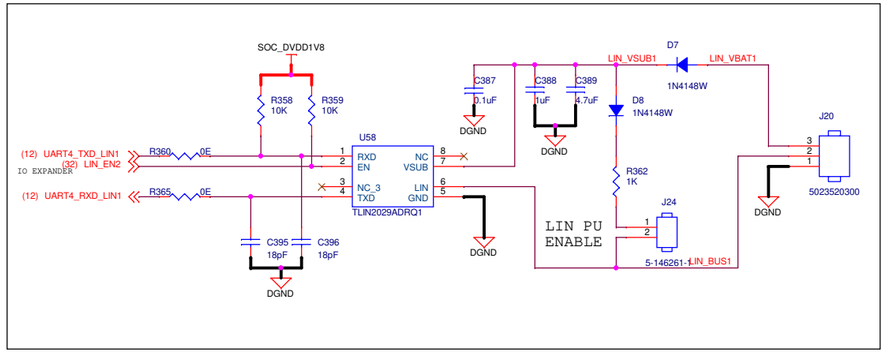
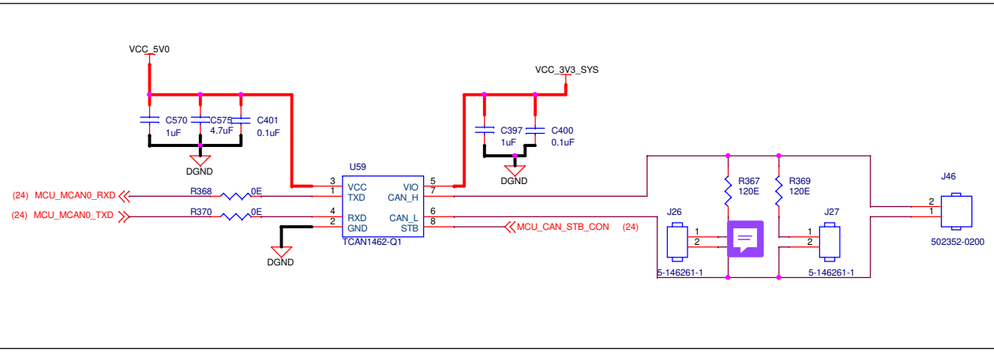
CAN TRANSCEIVER











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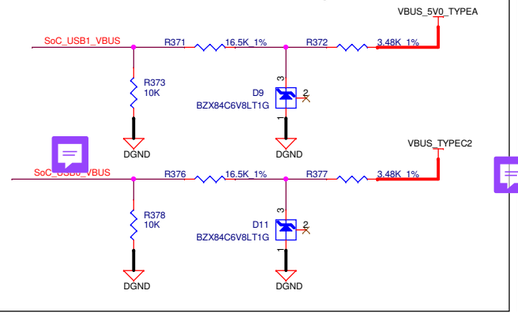
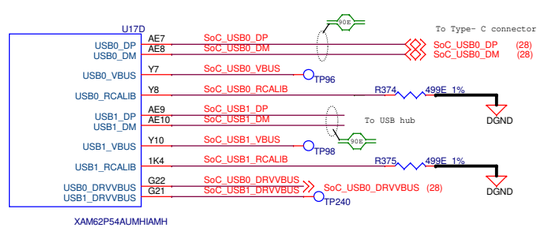
VBUS SENSE

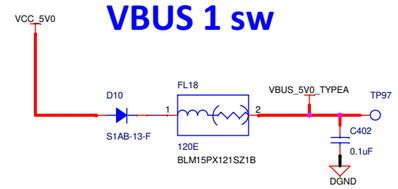
Note: Refer data sheet USB VBUS Design Guidelines section.



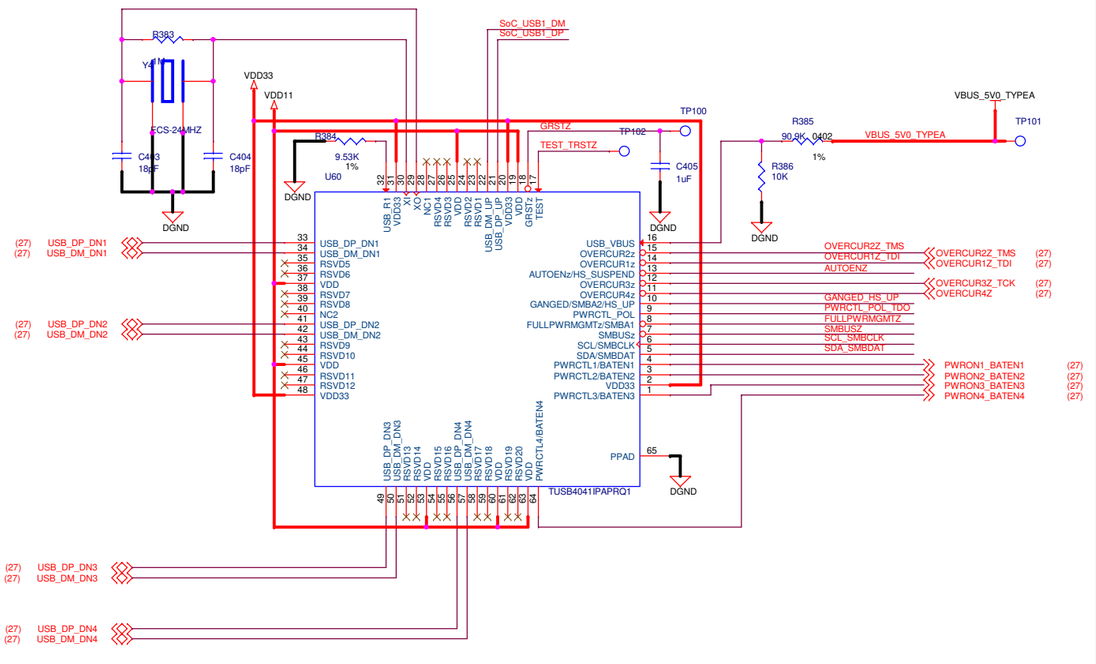
SoC_USB



VBUS 1 sw

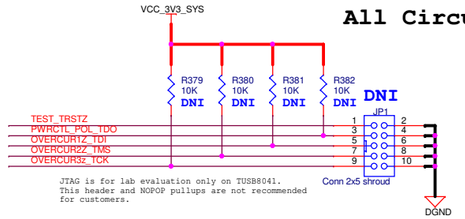


USB1 HUB

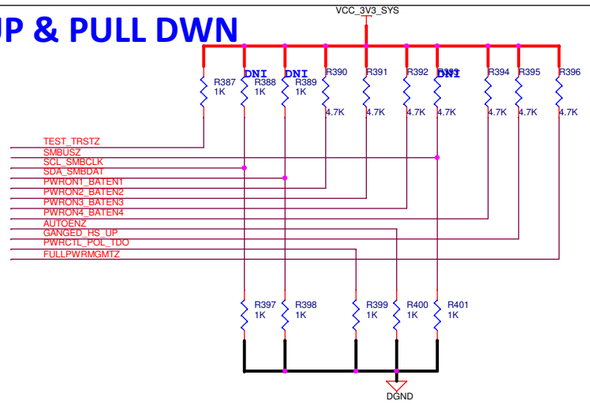


JTAG

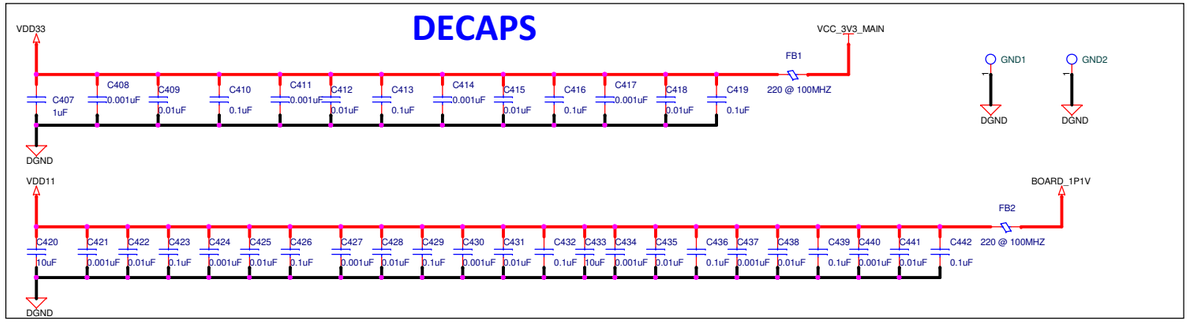
All Circuits are DNP



PULL-UP & PULL DWN

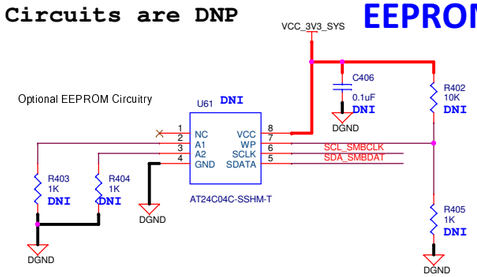


DECAPS



All Circuits are DNP

EEPROM



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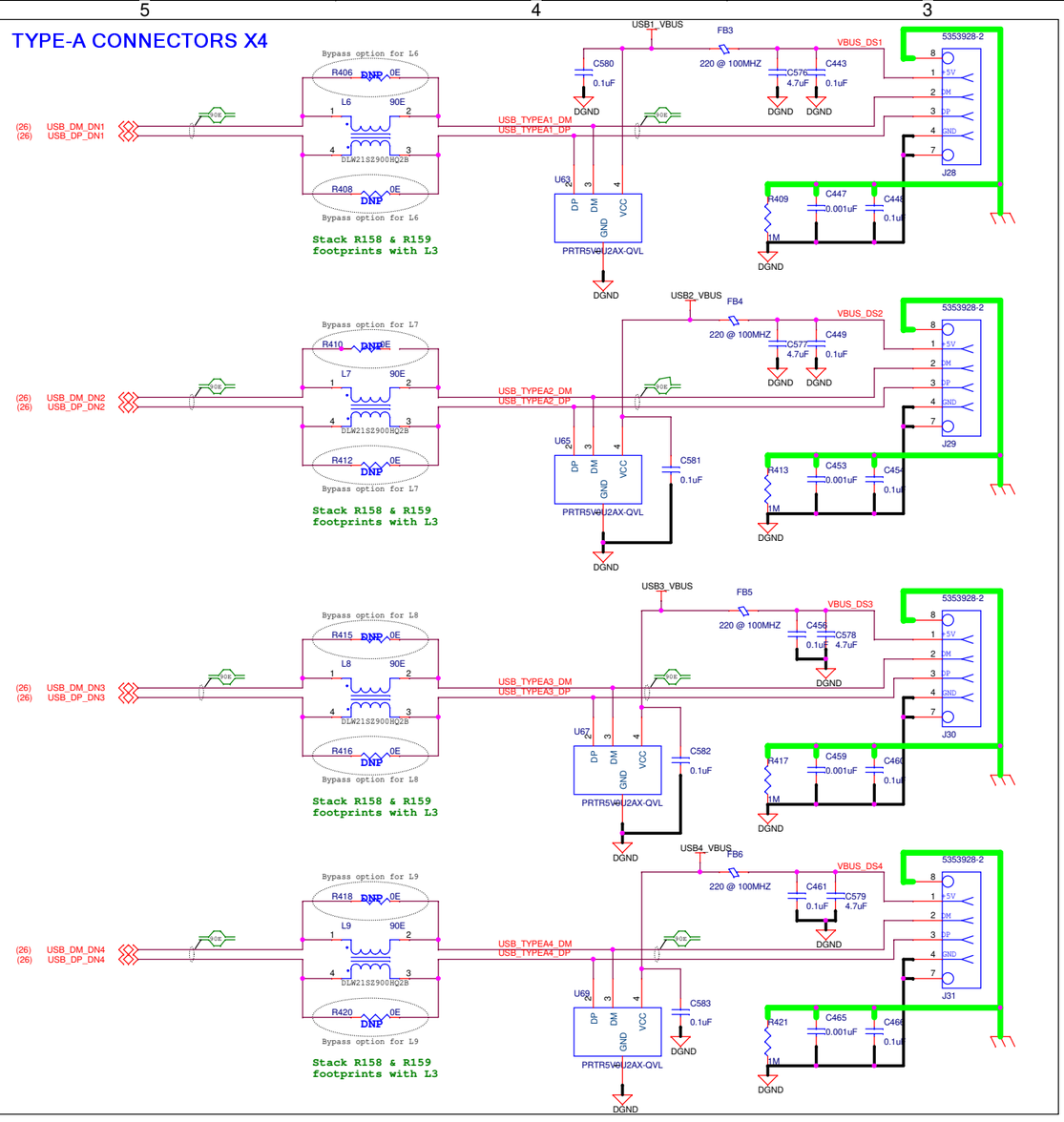
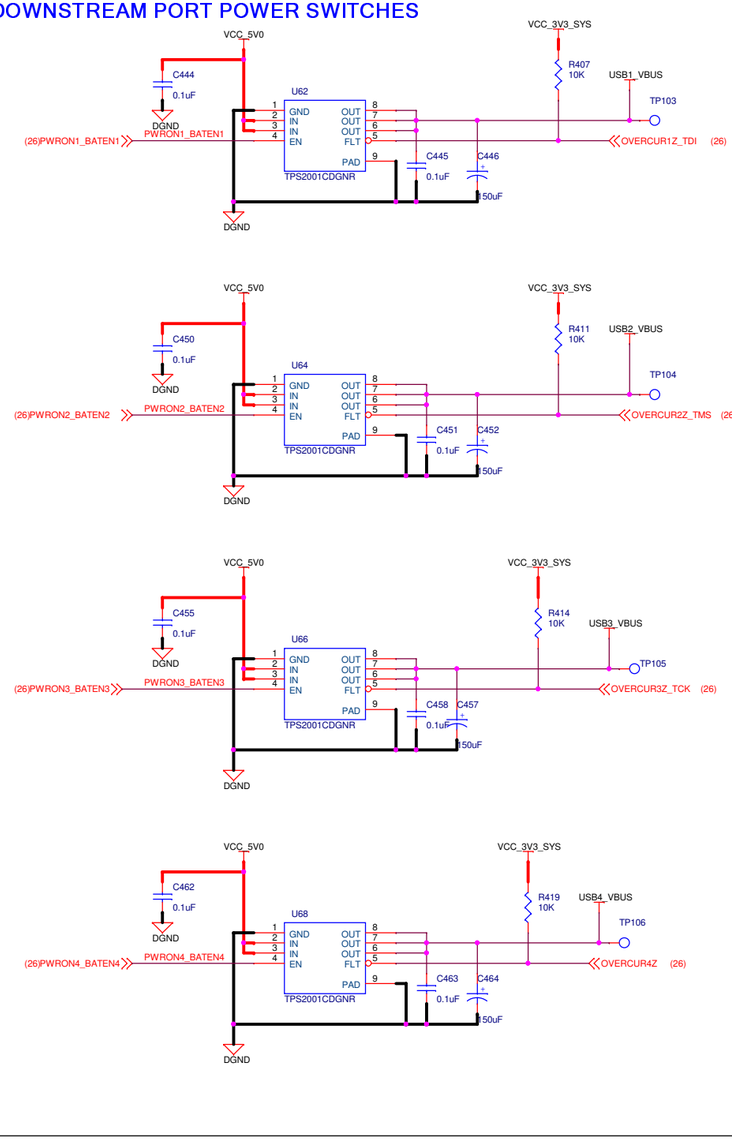
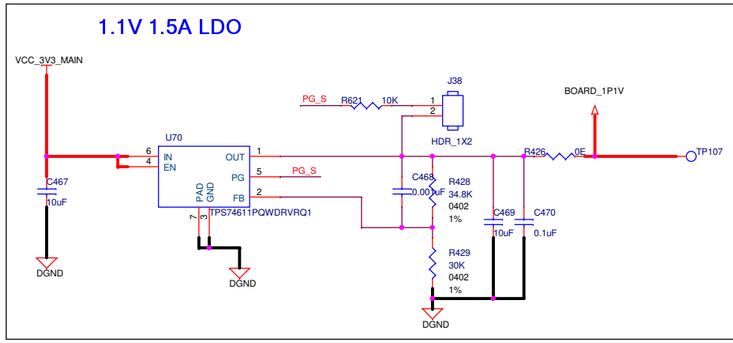
TYPE-A CONNECTORS X4

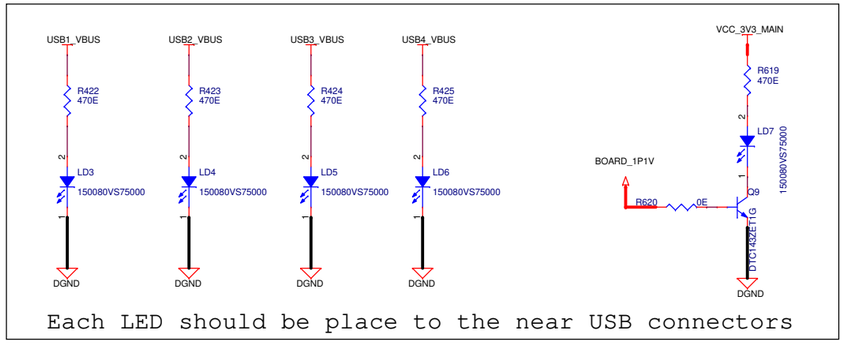


DOWNSTREAM PORT POWER SWITCHES



1.1V 1.5A LDO





Each LED should be place to the near USB connectors

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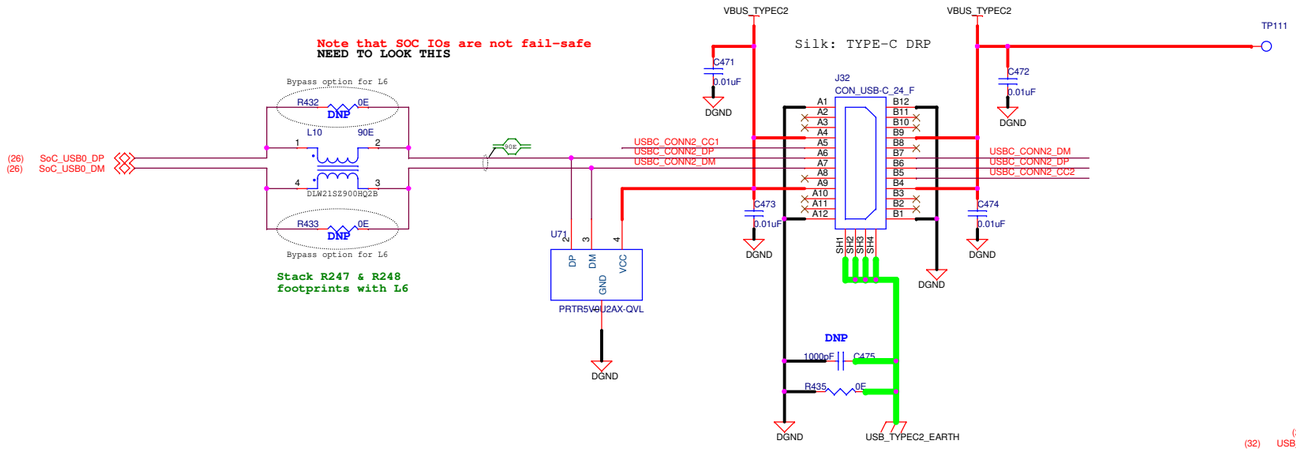
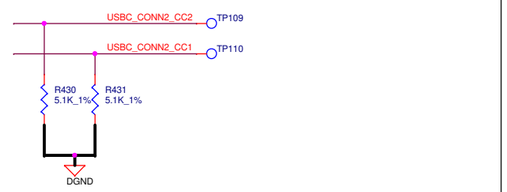
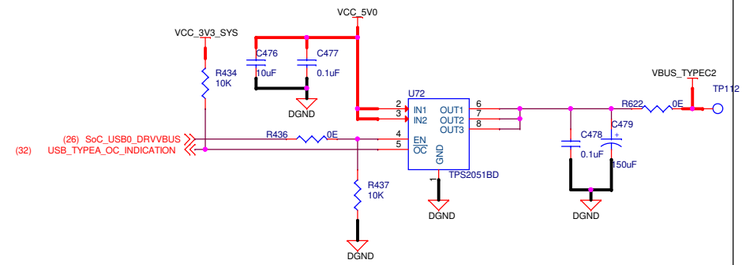
USB0 TYPE-C DRP

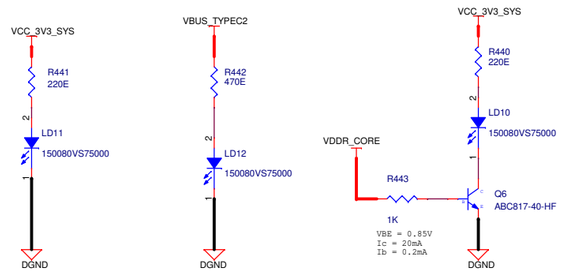




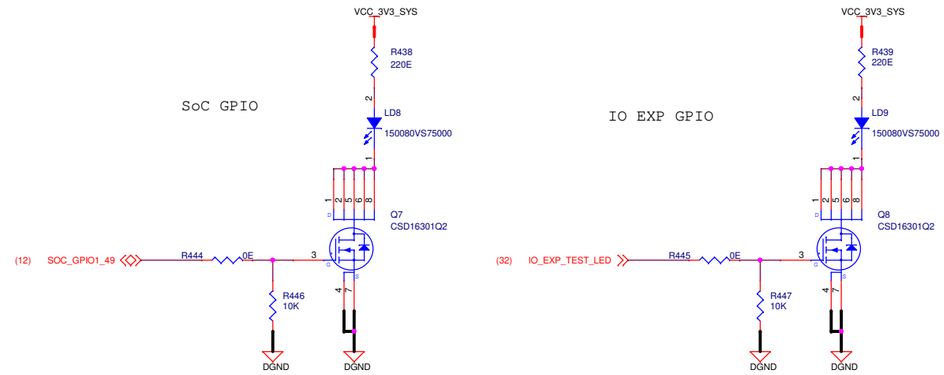


POWER RAIL LEDS

POWER INDICATION LED: VBUS_TYPEC2



USER TEST LEDS



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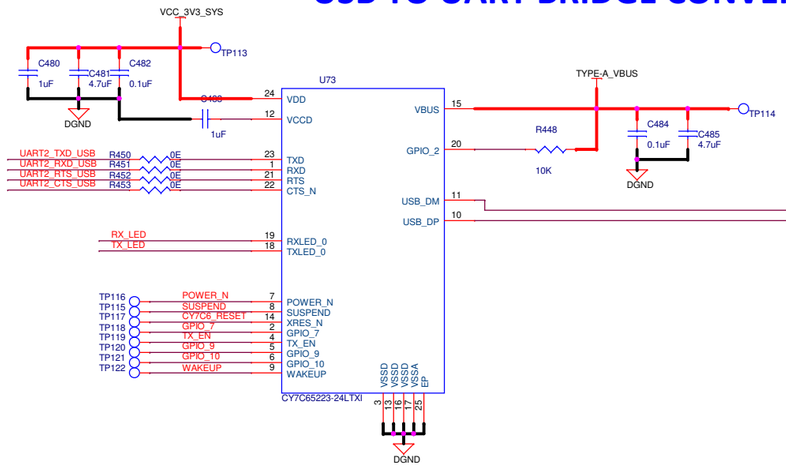
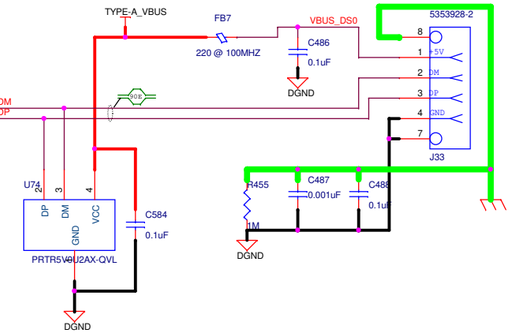
USB TO UART BRIDGE CONVERTER

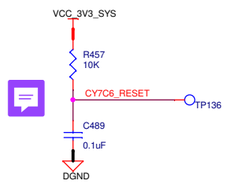


Stack R158 & R159 footprints with L3

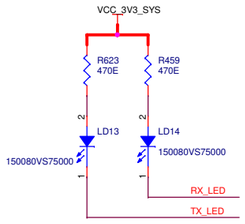
TYPE-A CONNECTOR



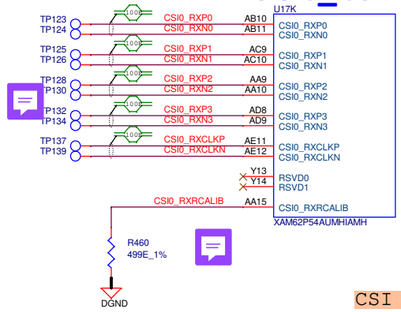
RESET



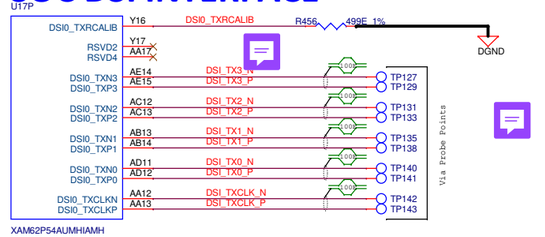
LED INDICATOR



SOC_CSI

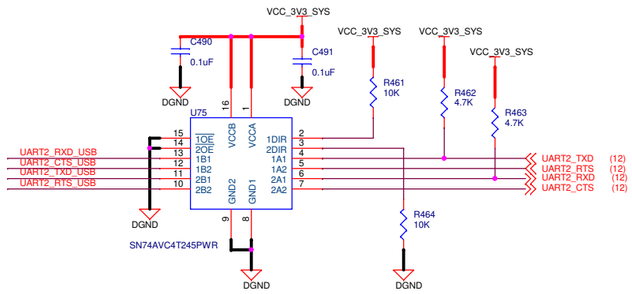


SOC DSI INTERFACE



CSI SND DSI IS NOT USED IN THIS DESIGN

UART BUFFER



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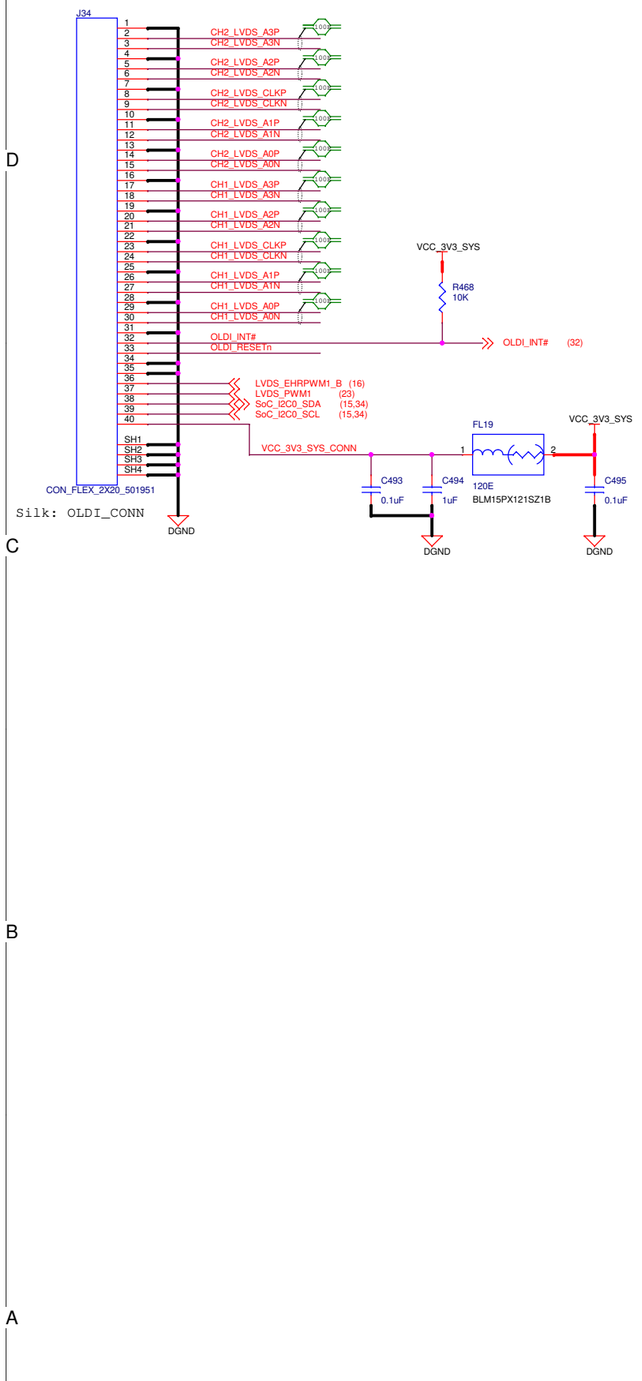
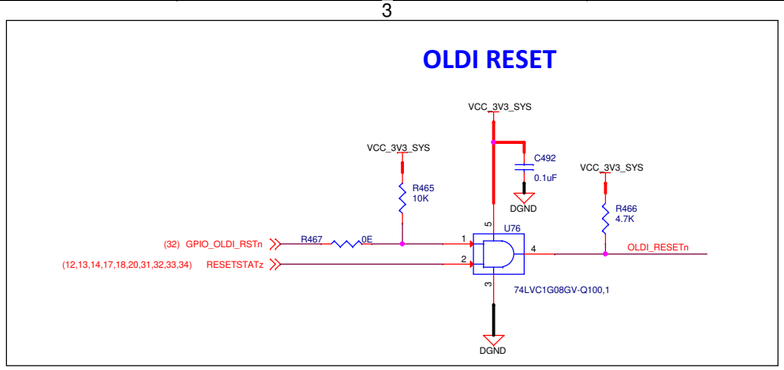
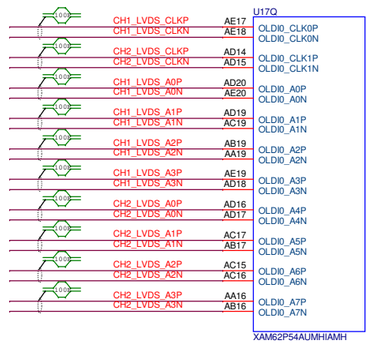


OLDI RESET



SOC OLDI INTERFACE



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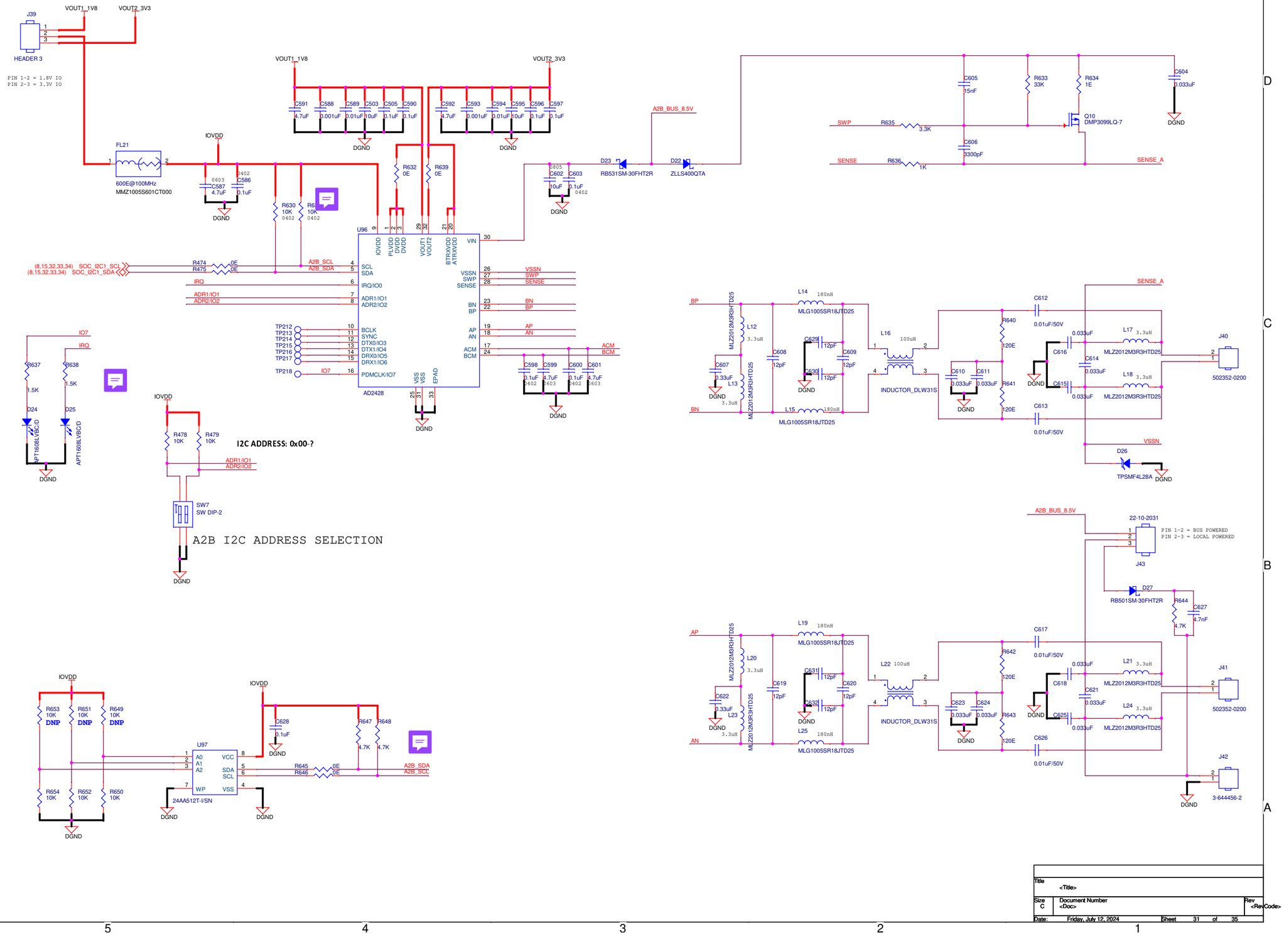
MIC/MEMS INTERFACE(A2B)



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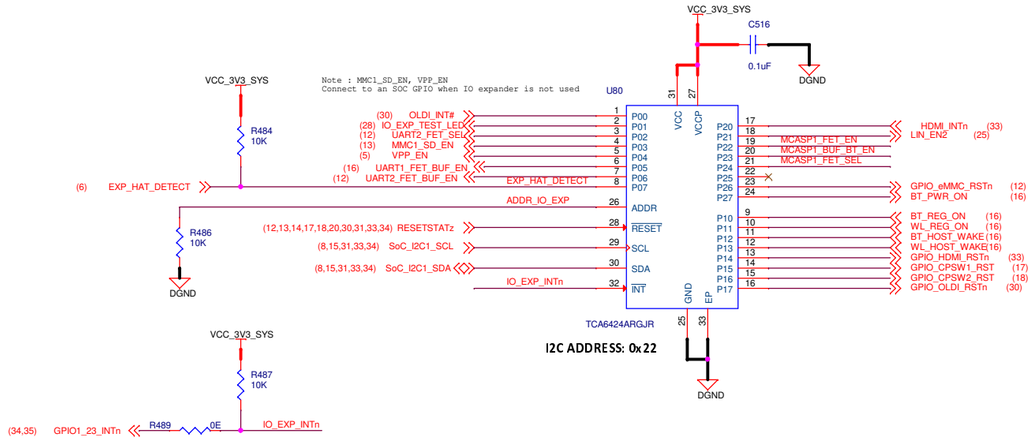
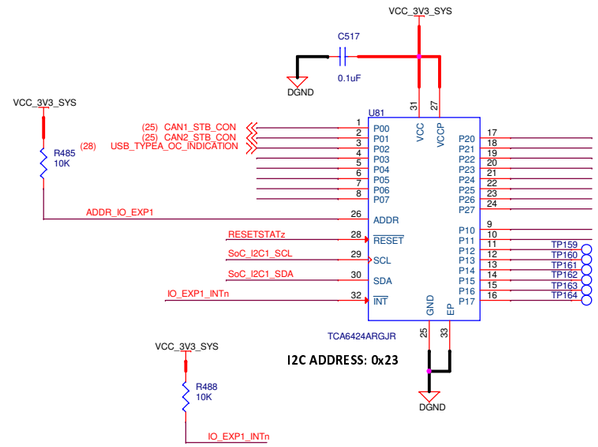
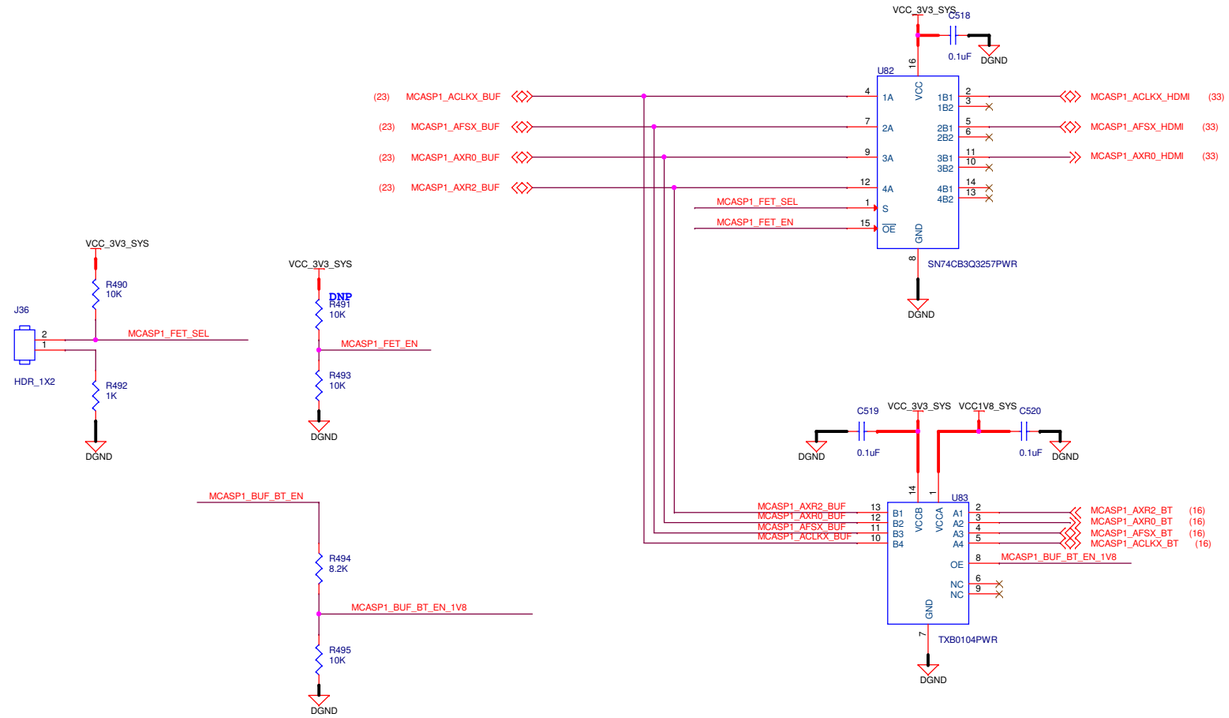
IO EXPANDER





SOC MAIN McASP1 FET BUS SWITCH & VOLTAGE LEVEL TRANSLATOR



OEn	SEL	INPUT/OUTPUT An	
L	H(DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

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HDMI INTERFACE

U17M

VOUT0_DATA0	AE24	SoC_VOUT0_DATA0
VOUT0_DATA1	W23	SoC_VOUT0_DATA1
VOUT0_DATA2	AA23	SoC_VOUT0_DATA2
VOUT0_DATA3	Y23	SoC_VOUT0_DATA3
VOUT0_DATA4	AB23	SoC_VOUT0_DATA4
VOUT0_DATA5	AD23	SoC_VOUT0_DATA5
VOUT0_DATA6	AC23	SoC_VOUT0_DATA6
VOUT0_DATA7	AE23	SoC_VOUT0_DATA7
VOUT0_DATA8	AE22	SoC_VOUT0_DATA8
VOUT0_DATA9	AC22	SoC_VOUT0_DATA9
VOUT0_DATA10	W22	SoC_VOUT0_DATA10
VOUT0_DATA11	AE21	SoC_VOUT0_DATA11
VOUT0_DATA12	AD21	SoC_VOUT0_DATA12
VOUT0_DATA13	AC21	SoC_VOUT0_DATA13
VOUT0_DATA14	AA20	SoC_VOUT0_DATA14
VOUT0_DATA15	Y20	SoC_VOUT0_DATA15
VOUT0_PCLK	Y21	SoC_VOUT0_PCLK — R497 0E — HDMI_PCLK
VOUT0_DE	W21	R624 0E — SoC_VOUT0_DE
VOUT0_HSYNC	AC20	R625 0E — SoC_VOUT0_HSYNC
VOUT0_VSYNC	W20	R626 0E — SoC_VOUT0_VSYNC

XAM62P54AUMHAMH

VDD_1V2 — FB9 300E — VHDMI_AVCC_1V2
C532 4.7uF, C533 10uF, C534 0.1uF, C535 0.1uF — DGND

VHDMI_CVCC_1V2 — FB8 300E — VDD_1V2
C521 0.1uF, C522 0.1uF, C523 0.1uF, C524 0.1uF, C525 0.1uF, C526 0.1uF — DGND
C527 10uF — DGND

VHDMI_IOVCC_3V3 — FB10 300E — VCC_3V3_SYS
C538 0.1uF, C539 0.1uF, C540 0.1uF, C541 0.1uF — DGND
C542 10uF — DGND

VHDMI_IOVCC_3V3 — R501 4.7K

U85

(8,15,31,32,34) SoC_I2C1_SCL	1	CSCL	
(8,15,31,32,34) SoC_I2C1_SDA	2	CSDA	
	72	CECA	
HDMI_RSTn	51	RESET#	
HDMI_PCLK	22	IDCK	
SoC_VOUT0_DATA0	32	D0	
SoC_VOUT0_DATA1	31	D1	
SoC_VOUT0_DATA2	30	D2	
SoC_VOUT0_DATA3	29	D3	
SoC_VOUT0_DATA4	28	D4	
SoC_VOUT0_DATA5	27	D5	
SoC_VOUT0_DATA6	25	D6	
SoC_VOUT0_DATA7	24	D7	
SoC_VOUT0_DATA8	23	D8	
SoC_VOUT0_DATA9	20	D9	
SoC_VOUT0_DATA10	19	D10	
SoC_VOUT0_DATA11	18	D11	
SoC_VOUT0_DATA12	17	D12	
SoC_VOUT0_DATA13	16	D13	
SoC_VOUT0_DATA14	15	D14	
SoC_VOUT0_DATA15	14	D15	
(23) SoC_VOUT0_DATA16	13	D16	
(23) SoC_VOUT0_DATA17	11	D17	
(23) SoC_VOUT0_DATA18	10	D18	
(23) SoC_VOUT0_DATA19	9	D19	
(23) SoC_VOUT0_DATA20	8	D20	
(23) SoC_VOUT0_DATA21	7	D21	
(23) SoC_VOUT0_DATA22	6	D22	
(23) SoC_VOUT0_DATA23	4	D23	
SoC_VOUT0_HSYNC	34	HSYNC	
SoC_VOUT0_VSYNC	35	VSYNC	
SoC_VOUT0_DE	33	DE	
	36	SPDIF	
HDMI_MSTRCLK	38	MCLK	
(32) MCASP1_ACLKX_HDMI	45	SCK	
(32) MCASP1_AFSX_HDMI	44	WS	
	60, 66	AVCC12_1, AVCC12_2	
	5	CVCC12_1	
	12	CVCC12_2	
	26	CVCC12_3	
	42	CVCC12_4	
	47	CVCC12_5	
	53	CVCC12_6	
	3	IOVCC1	
	21	IOVCC2	
	46	IOVCC3	
	48	DSDA — HDMI_I2C_SDA	
	49	DSCL — HDMI_I2C_SCL	
	52	INT — HDMI_INTn (32)	
	54	HPD — HDMI_HPD	
	56	EXT_SWING — HDMI_EXTSWING	
	59	TXC+ — HDMI_CLK+	
	58	TXC- — HDMI_CLK-	
	62	TX0+ — HDMI_TX0+	
	61	TX0- — HDMI_TX0-	
	65	TX1+ — HDMI_TX1+	
	64	TX1- — HDMI_TX1-	
	68	TX2+ — HDMI_TX2+	
	67	TX2- — HDMI_TX2-	
	71	CEC_A — HDMI_CEC	
	50	CEC_D — HDMI_CEC_D — TP172	
	55	RSVDL	
	69	IO_SEL — R504 0E — DGND	
	70	VDDQ	
	41	SD0 — HDMI_AUDD1 — TP174	
	40	SD1 — HDMI_AUDD2 — TP175	
	39	SD2 — HDMI_AUDD3 — TP176	
	37	SD3 — MCASP1_AXR0_HDMI (32)	
	57	IOGND	
	43	CGND	
	63	AGND	
	73	PAD	

SII9022ACNU

VHDMI_IOVCC_3V3 — R498 2.2K DNP, R499 2.2K DNP, R500 10K

R502 5.1K 1%, R503 10K DNP — DGND

REXT_SWING modified to 5.1K_5% Value changed for internal testing (Radiated Emission) Refer device data sheet for the recommended value

I2C ADDRESS: 0x3B, 0x3F, 0x62

VCC_3V3_SYS — C543 0.1uF, C544 1uF — DGND

R505 10K

U94 MC2520Z12.2880C19XSH: OE/NC, VCC, OUT, GND — 12.288MHz — R506 0E — HDMI_MSTRCLK

$:TRI-PAD WITH R140

R507 0E — DGND

TP166 HDMI_PCLK, TP167 SoC_VOUT0_DATA0, TP168 SoC_VOUT0_DATA8, TP169 SoC_VOUT0_DATA9, TP170 SoC_VOUT0_DATA10, TP171 SoC_VOUT0_DATA11, TP173 SoC_VOUT0_DATA23

HDMI ESD DEVICE

VCC_3V3_SYS — C528 10uF, C530 0.1uF — DGND
VCC_5V0 — C529 10uF, C531 0.1uF — DGND
VCC_3V3_SYS — R496 0E
VCC_5V0_HDMICONN — C536 0.1uF, C537 10uF — DGND — TP165

U84 TPD12S016PWR

HDMI_TX0+	18	D0+	
HDMI_TX0-	17	D0-	
HDMI_TX1+	21	D1+	
HDMI_TX1-	20	D1-	
HDMI_TX2+	23	D2+	
HDMI_TX2-	22	D2-	
HDMI_CLK+	16	CLK+	
HDMI_CLK-	15	CLK-	
HDMI_CONN_I2CSCL	8	SCL_B	
HDMI_CONN_I2CSDA	9	SDA_B	
HDMICONN_HPD	10	HPD_B	
HDMICONN_CECC	7	CEC_B	
	24	VCCA	
	11	VCC5V	
	13	5V_OUT	
	12	CT_HPD	
	5	LS_OE	
	2	SCL_A — HDMI_I2C_SCL	
	3	SDA_A — HDMI_I2C_SDA	
	4	HPD_A — HDMI_HPD	
	1	CEC_A — HDMI_CEC	
	6, 14, 19	GND1, GND2, GND3	

NOTE:
TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.

HDMI CONNECTOR

J37 CON_HDMI_19_F

HDMI_TX2+	1	
HDMI_TX2-	3	
HDMI_TX1+	4	
HDMI_TX1-	6	
HDMI_TX0+	7	
HDMI_TX0-	9	
HDMI_CLK+	10	
HDMI_CLK-	12	
HDMI_CONNCEC	13	
HDMI_CONN_I2CSCL	15	
HDMI_CONN_I2CSDA	16	
VCC_5V0_HDMICONN	18	
HDMICONN_HPD	19	
	2, 5, 8, 11, 14, 17	
	SH1, SH2, SH3, SH4	

Silk: HDMI

FL20 120E BLM15PX121SZ1B — DGND — HDMI_EARTH

HDMI RESET

VCC_3V3_SYS — R508 10K
VCC_3V3_SYS — C545 0.1uF — DGND

U87 74LVC1G08GV-Q100,1

(32) GPIO_HDMI_RSTn — R509 0E — HDMI_RSTn
(12,13,14,17,18,20,30,31,32,34) RESETSTATz

R510 10K — DGND

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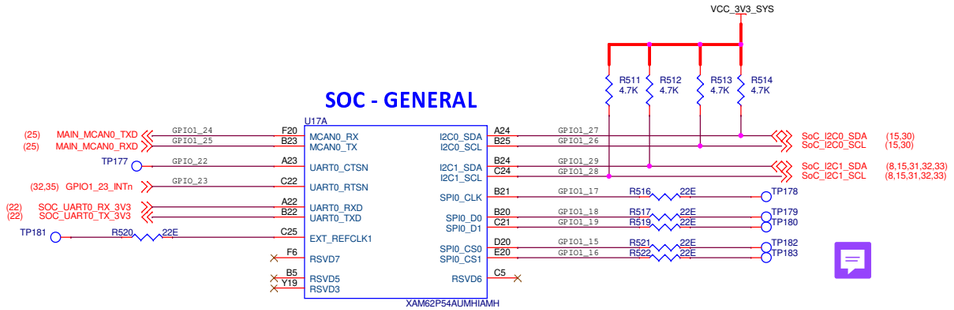
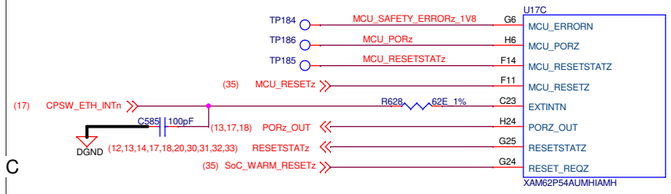
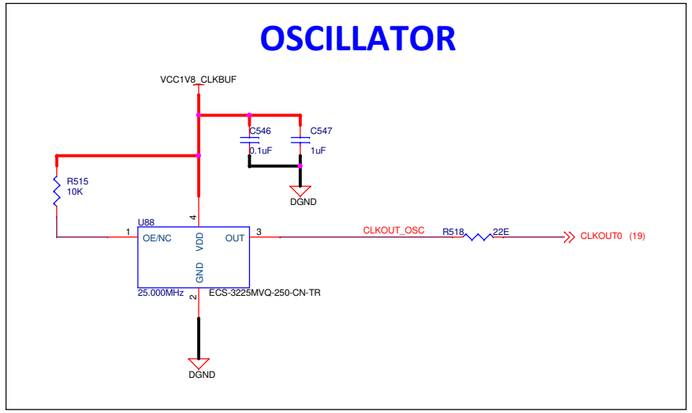
SOC - GENERAL

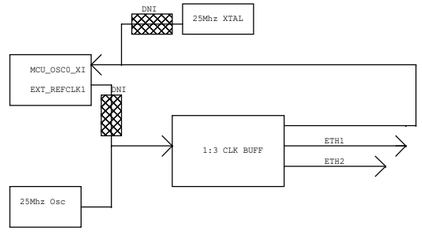


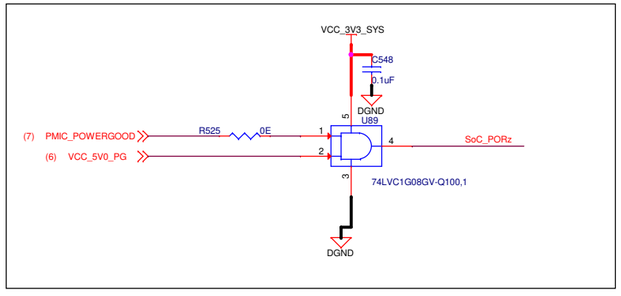
SOC - RESET

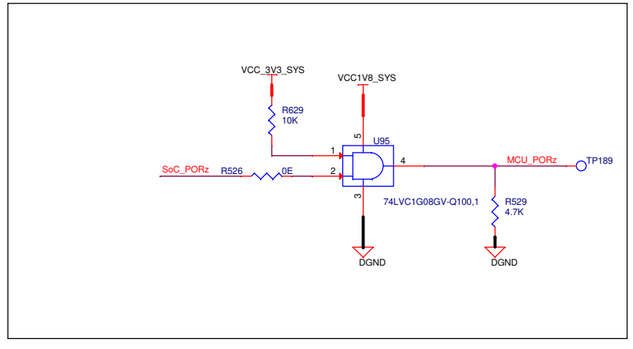


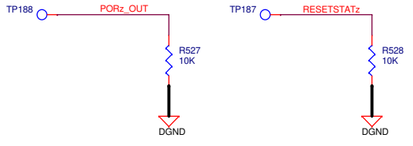
OSCILLATOR



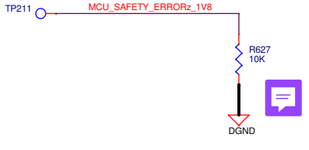








Pull-down resistor on PORz_OUT is provided to keep the signal low until the processor is released from reset during the power-up seqence



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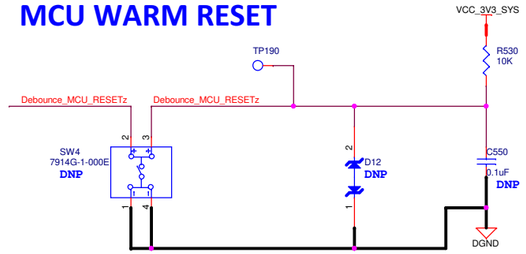
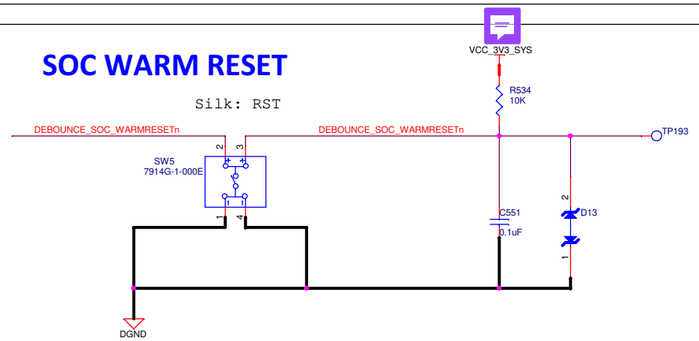
SOC RESET

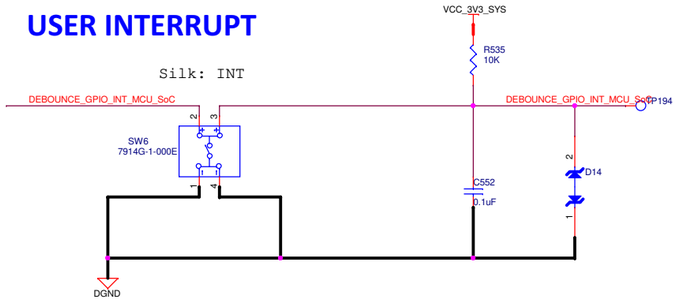
MCU WARM RESET



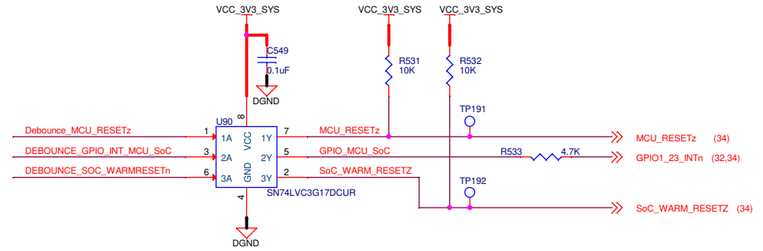
SOC WARM RESET



USER INTERRUPT



RESET & INT DEBOUNCE CIRCUIT



CAN-FD FAST WAKE UP SW

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