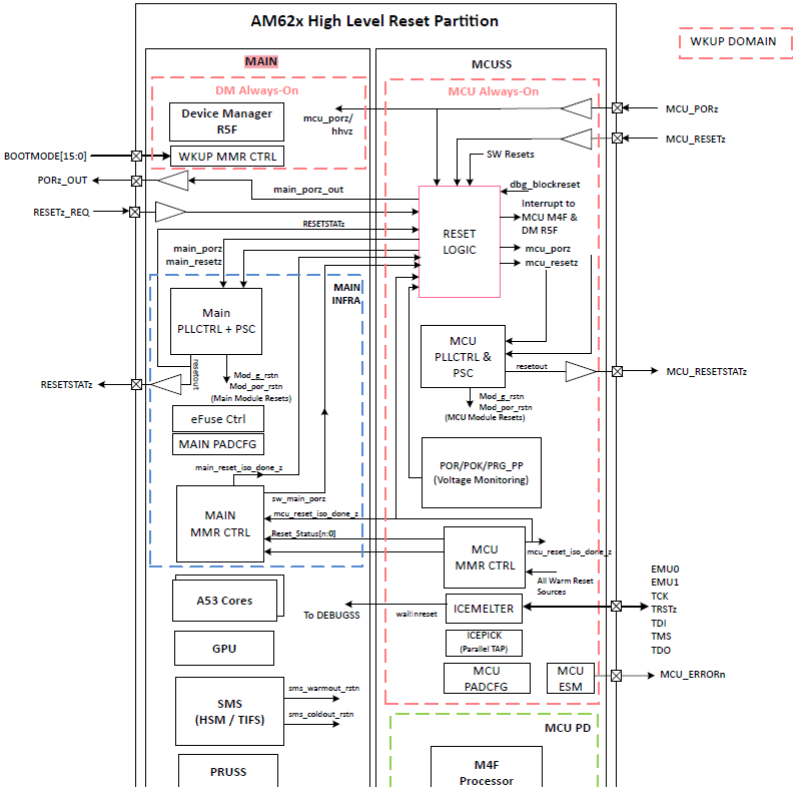
AM62 Deep Sleep IO Considerations

Summary

- During Deepsleep IOs are configured to Isolation state. During IO isolation, Receiver is kept ON for wake-up event propagation. Transmitter is turned OFF. IO can hold a value of ‘1’ or ‘0’ through an internal pull (~20K). Before entering into deeplseep mode, IO must be configured by programming the PADCFG MMRs to hold the value during deepsleep (bits 24, 27, 28). **System designers must ensure that there is no opposing pulls or driver values on these pins on the board. Failure to do so will lead to indeterminate IO level.**
- **Behavior of IOs on Main domain**: Based on few SOC architecture considerations for key modules that exist in main domain, **main domain is put in PORz state during deepsleep**. Since the Main PADCFG is also located in Main domain, it is put into PORz state causing MMR context to be lost. **Hence the only option for Main domain IOs is IO isolation as described above (IO holds the pre-programmed state).**
- **Behavior of IOs in MCU/WKUP domain**: MCU PADCFG is located in always ON WKUP domain. PADCFG MMR context is still preserved during deeplseep. Hence, MCU/WKUP domain IOs can have more options during deeplseep. For example, desired IOs can be removed from IO Isolation (ISO bypass – bit23). The Transmitter can be kept ON and can drive a value of ‘1’ or ‘0’ (bits 23-26).

6.3.1.5.1 Reset Architecture Block Diagram

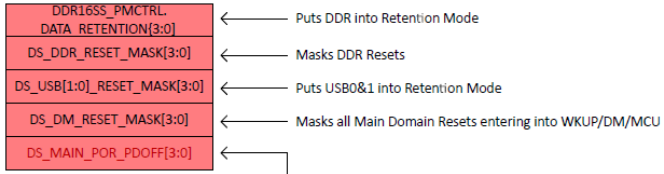
Reset Architecture Block Diagram shows the device reset architecture block diagram. It describes the device reset sub-modules and critical internal signal interconnections.



https://www.ti.com/lit/ug/spruiv7b/spruiv7b.pdf (Pg 577)

WKUP MMR DEEP SLEEP CONTROLS

These bits are multi-bit encoded fields (ideally 4 bits) to prevent single bit flip/error from causing a reset. When this 4bit MMR filed is programmed with a value of 4'b0110, the decode logic must make that signal active ('1'). For all other values, the decode logic makes reset inactive. The default value must be 4'b1111, which is reset inactive. These MMRs are key-lock protected and firewall protected. Reset control for these MMRs is MCU PLLCTRL CHIP_1_RST_n

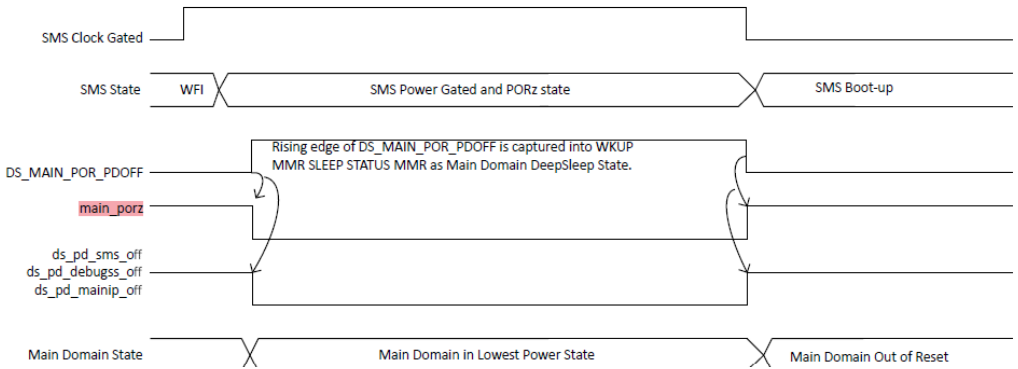


When DS_MAIN_POR_PDOFF is programmed high (towards the end of Deepsleep sequence), this signal is used to assert main_porz (=Low) and also force ds_pd_sms_off, ds_pd_debugss_off, ds_pd_mainip_off to off state (= '0'). This MMR is programmed only during Deepsleep mode.

Rising edge of DS_MAIN_POR_PDOFF is captured into WKUP MMR SLEEP STATUS MMR as Main Domain DeepSleep State. When Main domain resumes from Deepsleep, TIFS can read this MMR to detect that it is resuming from deeplseep state. TIFS can clear this bit or can request DM to clear this bit.

Since DS_MAIN_POR_PDOFF is also causing a Main Domain Porz during deeplseep mode, inverted version of DS_MAIN_POR_PDOFF should be captured as ds_main_porz in Reset Status MMR in MCU CTRL MMR.

High Level Sequence



https://www.ti.com/lit/ug/spruiv7b/spruiv7b.pdf (Pg 612, Figure 6-30)

Table 6-5. Low Power Modes

Low Power Modes	Wakeup Sources	Application State and Use Case
Partial I/O	CANUART I/O Bank pins	The entire SoC is OFF except I/O pins in CANUART I/O Bank to maintain I/O wakeup capability from CANUART I/O Bank I/O pins.
DeepSleep	GP Timers, RTC Timer, UART, I2C, WKUP GPIO, I/O Daisy Chain	Core domain register information will be lost. On-chip peripheral register (context) information of core domain needs to be saved by application to DDR before entering this mode. DDR is in self-refresh. Boot ROM executes and branches to peripheral context restore for wakeup, followed by system resume. This mode is primarily used for Suspend to RAM for battery lifetime or backup operation.
MCU Only	DeepSleep wakeup events, Interrupt events supported in MCU channel	The MCU subsystem runs at the MCU PLL clock. The rest of the SoC status is the same as DeepSleep. DDR is in self-refresh. MCU can run applications with MCU domain peripherals while in this low power mode.
Standby	Any SoC interrupt event	On-chip contents are fully preserved. Any SoC interrupt event can cause a wakeup event from this low power mode. A53 and MCU M4F are in WFI or Power Down. DDR memory is in self-refresh. The device can run low-level processing with non-Wakeup/MCU domain peripherals and support wakeup from those peripherals.

Table 6-6. Voltage, Power and Clock Domain Status

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6.2.4.11 I/O Power Management and Daisy Chaining

I/O power management is useful when the main oscillator is clock gated and the power domains for the peripherals connected to LVCMOS I/Os are OFF (power-gated state) in DeepSleep or MCU-Only. Since the I/Os are controlled by modules in power-gated state, I/O power management is required to have flexibility when interfacing with external devices. During DeepSleep or MCU-Only, the wakeup feature is active, described in **Wakeup** below. Isolation is required to be activated and deactivated during sleep and wakeup sequencing, respectively (see following description of **Isolation**).

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Three aspects comprise I/O cell power management:

- **Isolation** - Isolation from power state transitions.
  - When ISOLATED, the I/Os will hold their previous state (0,1, tristate) until the ISOLATION is released. The controls for the ISOLATION travel through the chain. Isolation is controlled during sleep and wakeup sequencing.

Note

The Device Manager must have the optional feature to remove isolation from DDR I/Os while allowing rest of the I/O isolation to be removed later. This allows for software to restore any critical peripherals from DDR and ensure the peripheral is in a required or valid state (like GPIO) before the remaining I/Os are removed from Isolation.

During IO Isolation, **Driver is disabled**. Output state can be held at ‘1’ or ‘0’ through a weak internal pull-up/down (~20K).

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Table 14-6172. Description Of The Pad Configuration Register Bits (continued)

Bit	Field	Type	Reset	Description
30	WKUP_EVT	R/W	(1)	Wakeup event status 0 - No wake event on pin 1 - Wake event occurred on pin
29	WKUP_EN	R/W	(1)	Wakeup enable 0 - Wakeup operation disabled 1 - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	(1)	Deep Sleep pull-up/down selection 0 - Offmode pulldown selected 1 - Offmode pullup selected
27	DS_PULLUD_EN	R/W	(1)	Deep Sleep pull-up/down enable (active low) 0 - Pullup / pulldown is enabled 1 - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	(1)	Deep Sleep output value 0 - Output value is 0 1 - Output value is 1
25	DSOUT_DIS	R/W	(1)	Deep Sleep output disable 0 - Output enabled 1 - Output disabled
24	DS_EN	R/W	(1)	Deep Sleep override control 0 - IO keeps its previous state when Deep Sleep mode is active 1 - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	(1)	Isolation Bypass 0 - IO isolation is preserved 1 - IO isolation is bypassed
22	ISO_OVR	R/W	(1)	Isolation Override 0 - IO isolation is preserved 1 - IO isolation is overridden

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