AM62P EVM with Burton PMIC

VCC_5V0

USB Domain

This is the input supply if no USB connector is used as input supply

Not needed if no USB connector is used as input supply

Dual port USB Type-C™ and USB PD controller
TPS65988

CC1/CC2 — C1_CC1 / C1_CC2 — VBUS_TYPEC1 — VBUS1 — PP_HV1
CC1/CC2 — C2_CC1 / C2_CC2 — VBUS_TYPEC2 — VBUS2 — PP_HV1

VMAIN

VBUS_TYPEC1 / VBUS_TYPEC2

For systems without USB connector as input supply:

- Automotive systems with CAN transceiver: use CAN_INH for power-up/down, connect this point to the CAN_INH pin. (CAN transceiver pulls CAN_INH to VBAT for wake-up, hence the resistive divider from CAN_INH to ground measures whether the VBAT is high enough to allow system start-up)
- Alternative solution: connect this point to input supply of the Prereg Buck

Buck-Boost USB Supply

BUCK-BOOST REG (5V)
TPS630702RNMR
2V < Vin < 16V
Buck-Boost (2A)
EN (VIH > 1.05V) — (OD) PG
VCC_5V0_EN

VCC_5V0 — VCC_5V0_PG

Prereg Buck

Step-Dn Controller
LM5141QRGYRQ1
3.5 < Vin < 42V
Buck1
Alternative:
Step-Dn Converter
LM63635DQDRRRQ1
EN (VIH > 1.05V) — (OD) PG
EN_LM5141_ON
VCC_3V3_MAIN_PG

VCC_3V3_MAIN

Discrete LDO – A

Not needed if Partial IO mode is not used

Low V_{DO}, 300mA LDO
TLV75801PDBVT
VIN (2 - 5.5V) — VOUT (0.75V / 0.85V) max @ 300mA, Vo = 0.75V
EN (VIH > 0.9V; VIL < 0.4V) — FB

NOTE: for 0.85V option, this output voltage needs to be 0.85V as well! Modify LDO voltage by changing feedback resistive divider

GND

Discrete LDO – C

Low V_{DO}, 200mA LDO
TLV70033QDDCRQ1
VIN (2 - 5.5V) — VOUT (3.3V) max @ 200mA, Vo = 3.3V
EN (VIH > 0.9V; VIL < 0.4V)

Not needed if Partial IO mode is not used, or if the Prereg BUCK is providing 3.3V and is kept enabled in Partial IO mode

VDD_CANUART

CAN_IO_3V3

Single Load Switch
TPS22965D5GT
Vin — Vout
ON (Vih > 1.2V)

VDD_3V3_SYS

Burton PMIC

Processor PMIC – Power Rscs
TPS6522**430**

3 < Vin < 5.5V	**Buck1**	1-Phase: Vo = 0.5-3.3V (5/10/20mV), 5A **Dual-Ph**: 3.0<Vin<5.5; Vo = 0.5-1.2V, 5A/Ph
3 < Vin < 5.5V	**Buck2**	1-Phase: Vo = 0.5-3.3V (25/50mV), 5A **Dual-Ph**: 3.0<Vin<5.5; Vo = 0.5-1.2V, 5A/Ph
3 < Vin < 5.5V	**Buck3**	1-Phase: Vo = 0.5-3.3V (25/50mV), 2A
3 < Vin < 5.5V	**Buck4**	1-Phase: Vo = 0.5-3.3V (25/50mV), 2A
2.2 < Vin < VCCA or 5V	**LDO1**	Vo = 1.2 – 3.3V, (50mV steps), Low Noise, **LDO mode**, 300mA
1.5 < Vin < VCCA or 5V	**LDO2**	Vo = 0.4 – 3.3V (50mV), **Bypass mode**, 400mA
1.5 < Vin < VCCA or 5V	**LDO3**	Vo = 0.4 – 3.3V (50mV steps), **LDO mode**, 400mA
Vin =VCCA	**LDOVINT**	Vo = 1.8V (internal LDO)

4.4MHz High Perf Use-Case — ①
4.4MHz Normal Perf Use-Case — VDD_1V8
4.4MHz Normal Perf Use-Case — VDD_DDR_1V1 ①
VDDA_1V8
VCC_3V3_SYS_EN
VDDR_CORE

VDD_1V8

Burton PMIC

Processor PMIC – Digital & Cntl IO & Analog VMON
TPS6522**430**

VSENSE >1.32V needed for startup
VMAIN_SENSE — EN/PB/**VSENSE**
H_SOC_I2C0 — ③ — I2C1 (VIO_IN; Default Addr) ADDR = 0x48, 49, 4A & 4B
VCCA
VIO_IN
INTn (OD) / EN_DRV (10k PU to VIO)
nRSTOUT (OD)

VCC_3V3_SYS — H_MCU_INTn_3V3
0 Ohm + TP, needed to allow debugging backdoor
H_MCU_PORz_1V8

VCC_3V3_MAIN — ④ TRIG_WDOG *From AM62P GPIO* — H_MCU_I2C0
SW — SW_SEL_VCORE — ① — GND
SELECT_CONFIG

GPIO1 (VIO): **OUT** = GPO, nINT, SDO_SPI (OD/PP) **IN/OUT = SDA_I2C2 (HiZ) =>ADDR = 0x12** IN = GPI, NSLEEP2 (400k PU/PD or HiZ)
GPIO2 (VIO): OUT = GPO (OD/PP) **IN** = GPI, **SCL_I2C2**/CS_SPI_TRIG_WDOG (400k PU/PD or **HiZ**)
GPIO3 (VIO): OUT = GPO (OD/PP) IN = **GPI => PB**, VMON1_mI, NSLEEP1 (**400k PU**/PD or HiZ)
PMIC_LPM_EN0 — ⑤ — GPIO4 (VIO): OUT = GPO (OD/PP) IN = **GPI**, VMON 2, ADC_IN, **NSLEEP1** (400k PU/**PD** or HiZ)
GPIO5 (VINT): OUT = GPO (OD/PP) IN = GPI, WKUP_SYNCCLKIN, **ADC_IN** (400k PU/PD or **HiZ**)
H_MCU_SAFETY_ERRn — Jumper between WD_DISABLE and VCC_3V3_MAIN to disable watchdog at startup — WD_DISABLE — ② — GPIO6 (VINT): OUT = GPO (OD/PP) IN = NSLEEP2, **nERR_MCU**, WKUP (**400k** PD/**PD** or HiZ)
VCC_3V3_SYS
VMON1 (**Single-Ended w.r.t AGND**, or Differential w.r.t VMON1_m) VMON1_PGSET = 3.3V

Discrete LDO – B

Dual Low V_{DO} LDO
TLV7103318QDSERQ1
VIN (1.45 - 5.5V) — VOUT1 (3.3V) max @ 200mA, Vo = 3.3V
EN1 (VIH > 0.9V; VIL < 0.4V)
VIN (1.45 - 5.5V) — VOUT2 (1.8V) max @ 200mA, Vo = 1.8V
EN2 (VIH > 0.9V; VIL < 0.4V)

VCC_3V3_SYS — From AM62P GPIO or through IO expander — VSEL_SD_SOC
VCC_3V3_SYS — VSEL_MMC1_SDIO
VDDSHV_SDIO_EN — From AM62P GPIO or through IO expander
VDDSHV_SDIO

VCC_3V3_SYS — From AM62P GPIO or through IO expander — MMC1_SD_EN
VCC_3V3_SYS — MMC1_SD_LS_EN
H_MCU_RESETSTATz
PORz_OUT
MMC1_SDCARD_EN
Same as AM62A EVM

VCC_3V3_SYS — **Single Load Switch** TPS22918DBVR — Vin / ON (Vih > 1.2V) — Vout — VDD_MMC1_SD

SD Card IO Domain

VCC_3V3_MAIN — **Analog 8-channel MUX** TMUX1308
VMAIN_SENSE — SW — D — From AM62x processor
ON AM62P EVM, use at least a jumper pin to allow connecting external voltages to ADC_IN

Discrete LDO – C

Low V_{DO}, 500mA LDO
TLV75518PDQNR
VIN (1.45 - 5.5V) — VOUT (1.8V) max @ 500mA, Vo = 1.8V
EN (VIH > 0.9V; VIL < 0.4V)
VCC_3V3_MAIN
VPP_EN — From AM62P GPIO or through IO expander
This LDO is not needed when the customer does a one-time eFUse programming in factory
Need an LDO with good transient load-step spec

Efuse_VPP_1V8

VCC_3V3_MAIN — VDD_CORE

AM62P Processor

Power Management Control Signaling

H_SOC_I2C0	SOC_I2C0_SCL/SDA (vddshv0)	PORz_OUT (vddshv0_mcu)	PORz_OUT
H_MCU_I2C0	MCU_I2C0_SCL/SDA (vddshv_mcu)	MCU_ERRORn (vddshv_mcu)	H_MCU_SAFETY_ERRn
H_MCU_PORz_1V8	MCU_PORz [Cold Rst] (vdds_osc0 [1V8])	MCU_RESETSTATz (vddshv_mcu)	H_MCU_RESETSTATz
H_MCU_RESETz	MCU_RESETz [Wrm Rst] (vddshv_mcu)	RESETSTATz (vddshv0)	**H_RESETSTATz**
H_SOC_RESET_REQz	RESET_REQz [Wrm Rst] (vddshv0)	POK VMON_VSYS	VMON1_VSYS
		POK VMON_1P8_SOC	VMON2_1V8
		POK VMON_3P3_SOC	VMON3_3V3

H_MCU_RESETz and H_SOC_RESET_REQz are external signals/n, n'ot from PMIC

VCC_3V3_MAIN — VDD_1V8 — VDD_3V3

Core Domain
vdd_core — Core Logic

0.85V Analog CLK & PLL Domains
vdda_0P85_dll_mmc0
vdd_mmc0

DSI Domain
VDDA_CORE_CSI_DSI
VDDA_CORE_DSI_CLK
VDDA_1P8_CSI_DSI
VDDA_1P8_FB2 — ③

RAM Domains

Vddr_core	Core Logic RAM
vdds_ddr	EMIF Core & IO
vdds_ddr_c	EMIF Clock

Analog PHY Domains
VDDA_CORE_USB
VDD_CANUART
vdda_CORE_CSIRX

1.8V Analog CLK & PLL Domains
VDDA_PLLGRP_1V8 — vdda_mcu
vdda_pll4..0
VDDS_OSC1_1V8 — vdds_osc0
VDDA_TEMP_1V8 — vdda_temp2..0

1.8V Analog PHY Domains
VDDA_1P8_USB — vdda_1p8_usb
VDDA_1P8_FB2 — vdda_1p8_oldi0

3.3V Analog PHY Power Domains
vdda_3p3_usb

Dual Voltage (1.8/3.3V) Digital I/O Domains
vddshv0
vddshv1
vddshv2
vddshv3 — EXTINTn (GPIO0_32, VDDSHV3 domain) — H_MCU_INTn_3V3
vdds_mmc0
vddshv5
vddshv6
vddshv_CANUART
vddshv_MCU — PMIC_LPM_EN0(MCU_GPIO_22, vddshv_CANUART domain) — PMIC_LPM_EN0

1.8V EFUSE Domains
vpp — Efuse_VPP_1V8

VDDSHV_SDIO

LPDDR4

vdd1	Core 1
vdd2	Core 2 & Input Buffer
vddq	I/O Buffer

VDD_DDR_1V1

Legend:

Power Rails
PDN base (black, purple, amber, blue, light-blue)
Partial IO mode (green, light-green)
DDR_Retention (aka S2R)
Peripheral supply (e.g. SD Card)
End Product option

Control Signals: < Signals >
General cntrl & logic
PDN base cntrl
Func Safety
End Product option
Debug/Development option

Test Point
(#) Note items
POK On-Chip "Pwr OK" Monitors (OV & UV)
POK-UV On-Chip "Pwr OK" Monitors (UV only)
Provisioned In-Line Supply Filter =

Notes:

1) SELECT_CONFIG: TPS65224 PMIC initially at start-up checks the level of GPIO3.
a) if SW_SEL_VCORE is open -> GPIO3 open-connect (default config for AM62P EVM):
- normal core speed VDD_CORE=0.75V (BUCK1/2 VOUT=0.75V)
b) if SW_SEL_VCORE is closed -> GPIO3 is pulled-up with 10k to VCCA:
- high core speed VDD_CORE = 0.85V (BUCK1/2 VOUT=0.85V)
=> any level change on GPIO3 after power-up (before start of power-up sequence) is ignored by the PMIC
=> after start-up, PMIC re-configures GPIO3 into PB ***with internal pull-up***

Notes:

2) DISABLE_WDOG: TPS65224 PMIC reads the level at the GPIO6 pin during the power-up sequence.
a) If the level at the GPIO6 pin is high after start-up of VCC_3V3_MAIN (jumper between WD_DISABLE and VCC_3V3_MAIN closed), the PMIC sets the WD_PWRHOLD bit to disable the long-window time-out of the watchdog.
b) If the level at the GPIO6 pin is low after start-up of VCC_3V3_MAIN (jumper between WD_DISABLE and VCC_3V3_MAIN open, hence GPIO6 is low through internal PD), the PMIC does not set the WD_PWRHOLD bit and hence the long-window time-out of the watchdog is activated

3) For single I2C usage: use I2C from MCU, or use both SoC&MCU I2C as multi-master

4) GPIO2 can be re-configured into TRIG_WDOG after startup. In order to use GPIO2 as TRIG_WDOG, configuration bits GPIO2_SEL need to be set to 0x3

5) GPIO4 (NSLEEP): select LPDDR4/DDR4 use-case. (**AM62P EVM only supports LPDDR4, so GPIO4 has no pull-down and is connected to PMIC_LPM_EN0 signal from AM62P if RETENTION mode is used)**
a) no pull-down: LPDDR4 use-case
b) 10k pull-down: DDR4 use-case (not supported on AM62P EVM)
=> for case a): after start-up, PMIC PFSM re-configures GPIO4 into NSLEEP1 with internal pull-up. AM62P EVM use-case with LPDDR4: signal PMIC_LPM_EN0 from AM62P is used at PMIC GPIO4 to:
- put PMIC into RETENTION if PMIC_LPM_EN0=0
- wake-up from RETENTION if PMIC_LPM_EN0=1

=> in case of 10k pull-down at GPIO4 (DDR4 use-case), either use GPIO3 as PB for wake-up&power-down, or, if GPIO3 has no ext pull-up, use GPIO3 as NSLEEP1 (SW reconfigures GPIO3 into NSLEEP1)
=> in case of 10k pull-down at GPIO4 (DDR4 use-case) and 10k pull-up at GPIO3, customer can, if I2C2 is not used, re-configure GPIO1 into NSLEEP2 to put PMIC into RETENTION with PMIC_LPM_EN0 signal

7.9.2.2.1 Power-Up Sequencing

Figure 7-5 describes the device power-up sequencing.

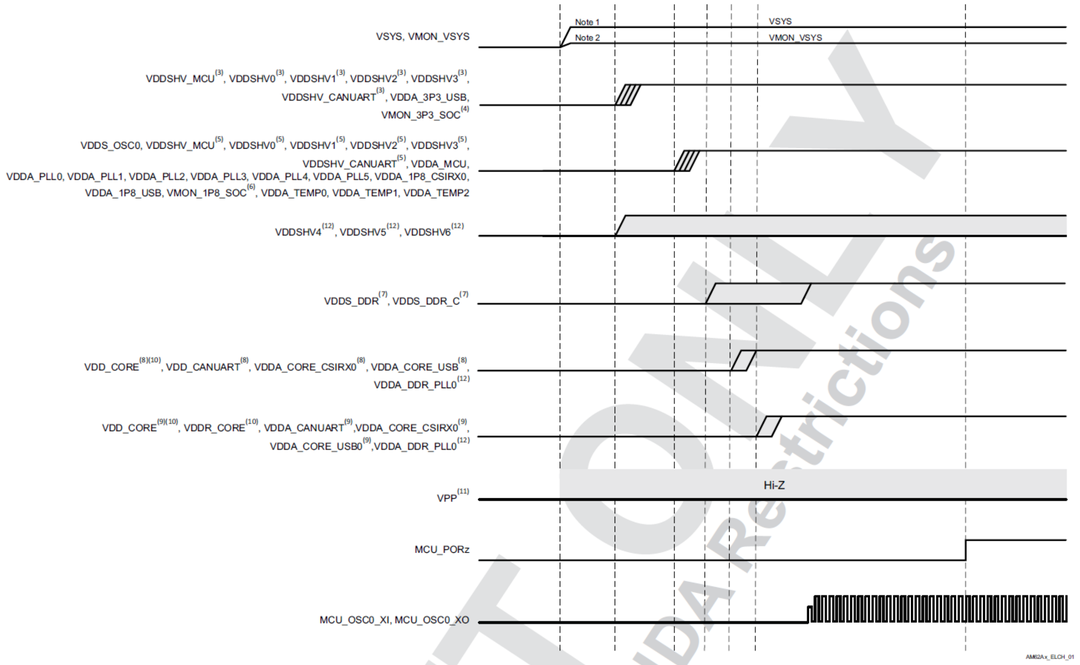


Figure 7-5. Power-Up Sequencing

1. VSYS represents the name of a supply which sources power to the entire system. This supply is expected to be a pre-regulated supply that sources power management devices which source all other supplies.
2. VMON_VSYS input is used to monitor VSYS via an external resistor divider circuit. For more information, see the *System Power Supply Monitor Design Guidelines*.
3. VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-6] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements. VDDSHV_CANUART shall be connected to an always-on power source when using Partial IO low power mode, or conencted to any valid IO power source when not using Partial IO low power mode. When VDDSHV_CANUART is not connected to an always-on power source and is operating at 3.3V, it shall be ramped up with other 3.3V supplies during the 3.3V ramp period defined by this waveform. When any of the VDDSHV_MCU and VDDSHVx [x=0-6] IO supplies are operating at 3.3V, they shall be ramped up with other 3.3V supplies during the 3.3V ramp period defined by this waveform.
4. The VMON_3P3_SOC input is used to monitor supply voltage and shall be connected to the respective 3.3V supply source.
5. VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-6] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements. VDDSHV_CANUART shall be connected to an always-on power source when using Partial IO low power mode, or conencted to any valid IO power source when not using Partial IO low power mode. When VDDSHV_CANUART is not connected to an always-on power source and is operating at 1.8V, it shall be ramped up with other 1.8V supplies during the 1.8V ramp period defined by this waveform. When any of the VDDSHV_MCU and VDDSHVx [x=0-6] IO supplies are operating at 1.8V, they shall be ramped up with other 1.8V supplies during the 1.8V ramp period defined by this waveform.
6. The VMON_1P8_SOC input is used to monitor supply voltage and shall be connected to the respective 1.8V supply source.
7. VDDS_DDR and VDDS_DDR_C are expected to be powered by the same source such that they ramp together.
8. VDD_CANUART shall be connected to an always-on power source when using Partial IO low power mode, or connected to the same power source as VDD_CORE when not using Partial IO low power mode. VDD_CORE, VDDA_CORE_CSIRX0, VDDA_CORE_USB, and VDDA_DDR_PLL0 shall always be sourced from the same power source and can be operated at 0.75V or 0.85V. When these supplies are operating at 0.75V, they shall be ramped up prior to all 0.85V supplies as shown in this waveform.
9. VDD_CANUART shall be connected to an always-on power source when using Partial IO low power mode, or connected to the same power source as VDD_CORE when not using Partial IO low power mode. VDD_CORE, VDDA_CORE_CSIRX0, VDDA_CORE_USB, and VDDA_DDR_PLL0 shall be sourced from the same power source and can be operated at 0.75V or 0.85V. When these supplies are operating at 0.85V, they shall be ramped up with other 0.85V supplies during the 0.85V ramp period defined by this waveform.
10. The potential applied to VDDR_CORE must never be greater than the potential applied to VDD_CORE + 0.18V during power-up or power-down. This requires VDD_CORE to ramp up before and ramp down after VDDR_CORE when VDD_CORE is operating at 0.75V. VDD_CORE does not have any ramp requirements beyond the one defined for VDDR_CORE. VDD_CORE and VDDR_CORE are expected to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85V.
11. VPP is the 1.8V eFuse programming supply, which shall be left floating (HiZ) or grounded during power-up/down sequences and during normal device operation. This supply shall only be sourced while programming eFuse.
12. VDDSHV4, VDDSHV5, and VDDSHV6 were designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.

7.9.2.2.2 Power-Down Sequencing

Figure 7-6 describes the device power-down sequencing.

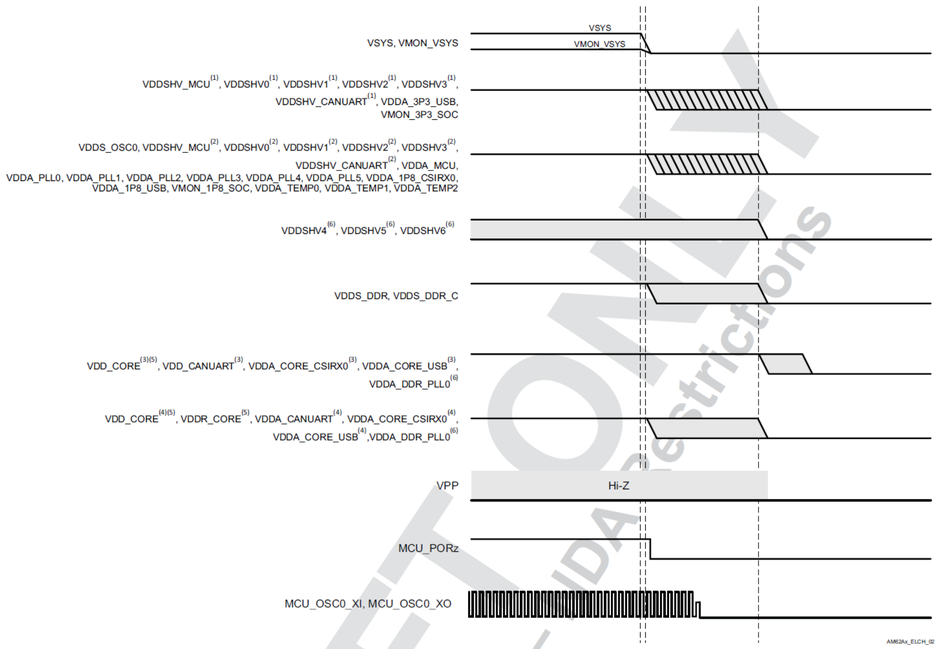


Figure 7-6. Power-Down Sequencing

1. VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-6] when operating at 3.3V.
2. VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-6] when operating at 1.8V.
3. VDD_CORE, VDD_CANUART, VDDA_CORE_CSIRX0, VDDA_CORE_USB, and VDDA_DDR_PLL0 when operating at 0.75V.
4. VDD_CORE, VDD_CANUART, VDDA_CORE_CSIRX0, VDDA_CORE_USB, and VDDA_DDR_PLL0 when operating at 0.85V.
5. The potential applied to VDDR_CORE must never be greater than the potential applied to VDD_CORE + 0.18V during power-up or power-down. This requires VDD_CORE to ramp up before and ramp down after VDDR_CORE when VDD_CORE is operating at 0.75V. VDD_CORE does not have any ramp requirements beyond the one defined for VDDR_CORE. VDD_CORE and VDDR_CORE are expected to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85V.
6. VDDSHV4, VDDSHV5, and VDDSHV6 were designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.

7.9.2.1 Power Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate of supplies to be less than 18 mV/µs. For instance, as shown in Figure 7-2, TI recommends having the supply ramp slew for a 1.8-V supply of more than 100 µs.

Figure 7-2 describes the Power Supply Slew Rate Requirement in the device.

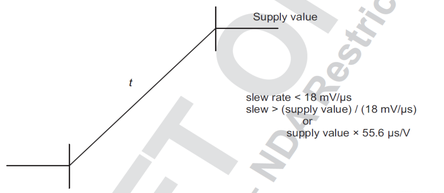
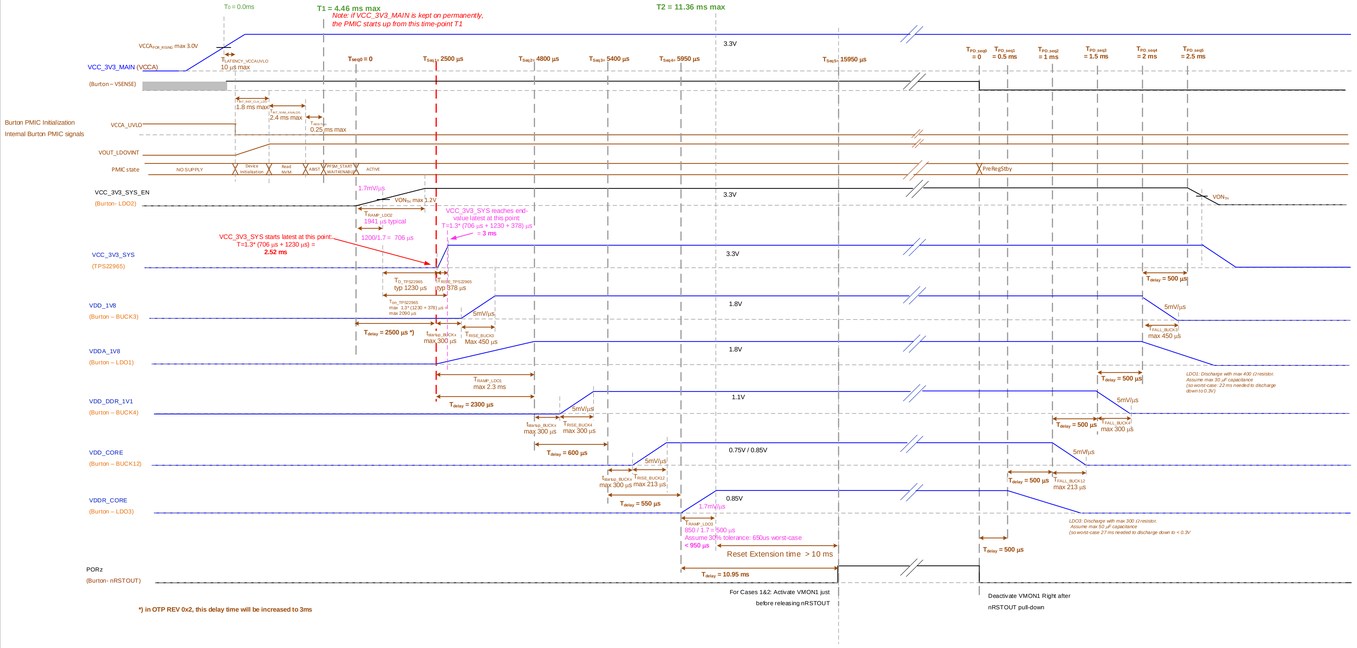


Figure 7-2. Power Supply Slew and Slew Rate

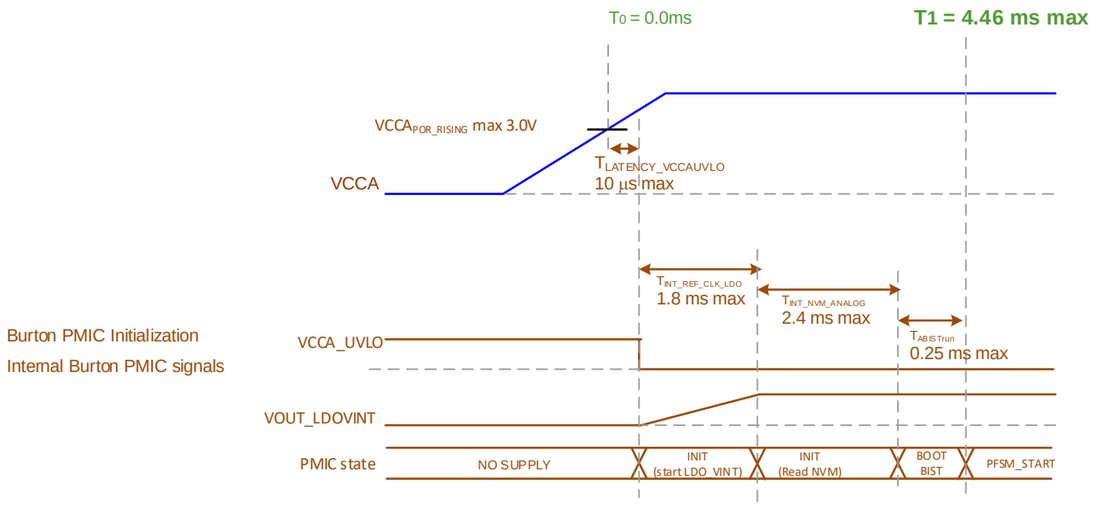
Power Up Sequence Burton PMIC

Legend:
System Time
Device Time
Board Nets Board Control Signals
Power Resource
OTP Set Values: (Resource, Current Capacity, Boot Voltage, Delay After Enable [us], Slew Rate [mV/us])



**) In OTP REV 0x2, this delay time will be increased to 3ms*

Legend:
System Time
Device Time
Board Nets Board Control Signals
Power Resource
OTP Set Values: (Resource, Current Capacity, Boot Voltage, Delay After Enable [us], Slew Rate [mV/us])



Change Log

V1.0	11/30/2022	1. Initial Creation and Mapping
V1.1	01/24/2023	Updated PDN diagram (GPIO mapping), GPIO select pin
V1.2	02/01/2023	Corrected LDO2 and LDO3 minimum input voltage, added recommended component number for the NMOS at the VMAIN_SENSE resistive divider
V1.3	02/09/23	Review with Sirara apps team. - Put additional notes in red (high-current LDO for VPP, VDD_CANUART voltage from LDO needs to be the same as VDD_CORE, even of 0.85V option) - Added 3-input AND gate for enabling the SD_CARD (processor power-on reset connected to the first input, the processor warm reset connected to the second input, and a GPIO connected to the third input) - Modified **Note 6**: SD-CARD voltage from LDO2 can only be changed from 3.3V to 1.8V by setting the TRIGGER_I2C_5 bit through I2C. Clearing bit TRIGGER_I2C_5 bit through I2C5 does not set the LDO2 voltage back to 3.3V. => Only after a re-enable of the SD_CARD, so when the signal at PMIC GPIO2 (MMC_SDCARD_EN signal) has a new rising edge, the LDO2 is re-enabled with 3.3V. - Modified **Note 3**: level of WD_DISABLE at GPIO6 is read after VCC_3V3_SYS comes up (not right at startup before the processor supply is enabled).
V1.4	03/13/23	Changed GPIO4 into VSEL_SD_SOC, and added footnote 7)
V1.5	03/16/23	Removed SD-Card support from Burton PMIC – SD_IO voltage created with external dual-output LDO. Burton LDO2 used for VSYS_3V3 – removed external Load-Switch Updated GPIO assignment of Burton PMIC Removed mux for PMIC_LPM_EN signal Removed power-fet from VMAIN resistive divider
V1.6	03/23/2023	Connected VIO and nINT pull-up resistor to VCC_3V3_SYS
V1.7	03/27/2023	Corrected schematic note 1), added schematic note 5)
V1.8	04/27/2023	Updated schematic note 1) by mentioning the internal pull-up at GPIO3 when configured as Push-Button, and updated proposed circuit at GPIO3. Connected VIO_IN to VCCA
V1.9	05/08/2023	Added control logic for the VDD_SDIO discrete dual-output LDO Added 6A load-switch for VSYS_3V3 (controlled with LDO2 from PMIC) Updated pin/domain names in AM62P symbol, and added the DSI domain
V2.0	05/09/2023	Changed part number for VDD_CANUART LDO into TLV75801PDBVT
V2.1	05/15/2023	Added resistive divider connection from VCC_SYS_3V3 to PMIC VMON1 Added PowerUpSequence_Burton waveforms
V2.2	05/23/2023	Removed resistive divider connection from VCC_SYS_3V3 to PMIC VMON1 (reduce quiescent current in DDR-retention) Updated note 5 for GPIO4 in schematics (Note 5 is not relevant for the AM62P EVM, but is relevant if customers want to use the AM62P with DDR4 instead of LPDDR4)
V2.3	07/26/2023	Updated timing diagram for Power-Up Sequence
V2.4	11/02/2023	Added USB-connectors to schematics, and corrected connection for the resistive divider connected to the VSENSE pin of the PMIC. Updated timing diagram for Power-Up Sequence