

2.5.16.1 EVM DIP Switches

AM62x SKEVM has two 8 - position DIP Switch to set the SoC Boot mode and related parameters.

2.5.16.2 Boot Modes

The boot mode for the SK EVM board is defined by two banks of switches SW1 and SW2 or by the I2C buffer connected to the Test automation connector. This allows for AM62x SoC Boot mode control by either the user (DIP Switch Control) or by the Test Automation connector.

All the bits of switch (SW1 and SW2) have week pull down resistor and a strong pull up resistor as shown in below picture. Note that OFF setting provides a low logic level ('0') and an ON setting provides a high logic level ('1').

Note The boot mode orientation has changed between E1 and E2. Please follow board silkscreen.



uSD Boot (MMC1) – 25 Mhz PLL

Note: Actual Board Silkscreen May Appear Inverted in this Orientation. Follow Physical Switch Text

Figure 2-7. Bootmode Switch Configuration for SD Boot (E1)

The boot mode pins of the SoC have associated alternate functions during normal operation. Hence isolation is provided using Buffer IC's to cater for alternate pin functionality. The output of the buffer is connected to the bootmode pins on the AM62x and the output is enabled when the bootmode is needed during a reset cycle. The input to the buffer is connected to the DIP switch circuit and to the output of an I2C buffer set by the test automation circuit. If the test automation circuit is going to control the bootmode, all the switches will manually be set to the OFF position. The bootmode buffer should be powered by an always ON power supply to ensure that the bootmode remains present even if the SoC power is cycled.

Switch SW1 and SW2 bits [15:0] are used to set the SoC Boot mode.

The switch map to the boot mode functions is provided in the tables below.

	Table 2-17. BOOT-MODE Pin Mapping														
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserv ed	Reserv ed	Backup Boot Mode Config uration	Backup	Boot Mo	de	Primary Configu	Boot Mo ration	ode	Primary	Boot Mo	de		PLL Co	nfiguratio	n

BOOT-MODE [0:2] – Denote system clock frequency for PLL configuration. By default, this bits are set for 25 MHz.

Table 2-18 gives details ON PLL reference clock selection.

Bit 2	Bit 1	Bit 0	PLL REF CLK (MHz)			
OFF	OFF	OFF	RSVD			
OFF	OFF	ON	RSVD			
OFF	ON	OFF	24			
OFF	ON	ON	25			
ON	OFF	OFF	26			
ON	OFF	ON	RSVD			
ON	ON	OFF	RSVD			
ON	ON	ON	RSVD			

Table 2-18. PLL Reference Clock Selection BOOTMODE [2:0]

• BOOT-MODE [3:6] – This provides primary boot mode configuration to select the requested boot mode after POR, that is, the peripheral/memory to boot from. Table 2-19 provides primary boot device selection details.

Bit 6	Bit 5	Bit 4	Bit 3	Primary Boot Device Selected
OFF	OFF	OFF	OFF	Serial NAND
OFF	OFF	OFF	ON	OSPI
OFF	OFF	ON	OFF	QSPI
OFF	OFF	ON	ON	SPI
OFF	ON	OFF	OFF	Ethernet RGMII1
OFF	ON	OFF	ON	Ethernet RMII1
OFF	ON	ON	OFF	I2C
OFF	ON	ON	ON	UART
ON	OFF	OFF	OFF	MMC/SD card
ON	OFF	OFF	ON	eMMC
ON	OFF	ON	OFF	USB0
ON	OFF	ON	ON	GPMC NAND
ON	ON	OFF	OFF	GPMC NOR
ON	ON	OFF	ON	Rsvd
ON	ON	ON	OFF	xSPI
ON	ON	ON	ON	No boot/Dev Boot

Table 2-19. Boot Device Selection BOOT-MODE [6:3]

• BOOT-MODE [10:12] – Select the backup boot mode, that is, the peripheral/memory to boot from, if primary boot device failed.

Table 2-20 provides backup boot mode selection details.

Table 2-20. Backup Boot Mode Selection BOOT-MODE [12:10]

Bit 12	Bit 11	Bit 10	Backup Boot Device Selected
OFF	OFF	OFF	None (No backup mode)



Table 2-20. Backup Boot Mode Selection BOOT-MODE [12:10] (continued)						
Bit 12	Bit 11	Bit 10	Backup Boot Device Selected			
OFF	OFF	ON	USB			
OFF	ON	OFF	Reserved			
OFF	ON	ON	UART			
ON	OFF	OFF	Ethernet			
ON	OFF	ON	MMC/SD			
ON	ON	OFF	SPI			
ON	ON	ON	12C			

 BOOT-MODE [9:7] – These pins provide optional settings and are used in conjunction with the primary boot device selected.

Table 2-21 gives primary boot media configuration details.

Table 2-21. Primary Boo	t Media Configuration	BOOT-MODE [9:7	1
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Bit 9	Bit 8	Bit 7	Boot Device
Reserved	Read Mode 2	Read Mode 1	Serial NAND
Speed	lclk	Csel	OSPI
Reserved	lclk	Csel	QSPI
Reserved	Mode	Csel	SPI
Clkout	Delay	Link stat	Ethernet RGMII
Clkout	Clk src	Reserved	Ethernet RMII
Bus Reset	Reserved	Addr	I2C
Rese	erved	Reserved	UART
Port	Reserved	Fs/raw	MMC/ SD card
Rese	erved	voltage	eMMC
Reserved	Mode	Lane swap	USB0
	Reserved		GPMC NAND
	Reserved		GPMC NOR
	Reserved		Reserved
SFDP	Read Cmd	Mode	xSPI
Rese	erved	No/Dev No boot/Dev Boot	

- BOOT-MODE [13] These pins provide optional settings and are used in conjunction with the backup boot device devices. Switch SW2.6 when ON sets 1 and sets 0 if OFF, see the device-specific TRM.
- BOOT-MODE [14:15] Reserved.

Table 2-22 provides backup boot media configuration options.

Table 2-22. Backup Boot Media Configuration BOOT-MODE [13]

Bit 13	Boot Device
Reserved	None
Mode	USB
Reserved	Reserved
Reserved	UART
IF	Ethernet
Port	MMC/SD
Reserved	SPI
Reserved	12C

2.5.16.3 User Test LEDs

The AM62x SKEVM board contains two LEDs for user defined functions.