1 Interrupts

This chapter describes the details related to device interrupts.

1.1 Interrupt Architecture

AM62 Interrupt Architecture includes information on how to utilize various interrupts and events in the system and relationships between interrupts and events.

An interrupt is defined as a physical signal which can be routed to the interrupt controller of various processors, which can cause the Interrupt Service Routing (ISR). This physical signal can be either a pulse or level and the polarity can be either negative or positive. And an interrupt is correspondent to an individual wire.

An event is defined as information transported by the event bus or PSI_L bus. Events are coded using an event index. The same event bus or PSI_L bus is used to transport multiple events. An event can also be routed and multiplexed to different locations. Events can't trigger a processor's ISR directly. It has to go through the Interrupt Aggregator (IA) to convert the event into an interrupt line. For more information, see Interrupt Aggregator (INTAGGR) , *Interrupt Aggregator (INTAGGR)*

The DMA transfer using BCDMA and PktDMA in AM62 can only be triggered using an event. The SoC level interrupt could be used as a BCDMA trigger using L2G logic. Interrupts in the SoC level can't be used to trigger a pktDMA transfer.

Each type of the processor has its unique interrupt controller. All A53 cores share a single Generic Interrupt Controller (GIC). Each M4F micro controller has its own dedicated interrupt controller, called Nested Vector Interrupt Controller (NVIC). Each R5 micro controller has its own dedicated interrupt controller, called Vectored Interrupt Manager (VIM). ICSSM uses an embedded local interrupt controller called INTC to manage its interrupts, refer to Table 1-1. Please refer to the following sections for the detailed usage of GICSS, VIM, INTC and MCUSS NVIC.

Table 1-1. Interrupt Controllers

Processors	Interrupt Controllers
A53 core 0	All four A53 cores share the same GICSS
A53 core 1	
A53 core 2	
A53 core 3	
R5 core inside R5FSS	Dedicated VIM inside R5FSS
M4F core inside MCUSS	Dedicated NVIC inside MCUSS
TIFS	Dedicated NVIC for TIFS
HSM	Dedicated NVIC for HSM. HSM receives the same sets of interrupt as TIFS
ICSSM	INTC embedded inside ICSSM

AM62 also contains multiple SoC level interrupt routers. The main function of those SoC level interrupt routers is to provide flexibility to select interrupt sources from a large group of interrupt sources. There are multiple places which utilize this feature, such as GPIO interrupts and some time synchronization related interrupts.

AM62 contains two ESM modules. ESM is used to consolidate/monitor the error events in the device. In this document, ESM may also be referred to as ESM0.

AM62 also has some chip level glue logic to convert some miscellaneous signals used as interrupt sources. Those miscellaneous signals are normally self-clear signals and do not need to clear after the Interrupt Service Routing (ISP) like the normal interrupts generated by the peripherals.

Figure 1-1 shows the high level interrupt architecture in AM62.

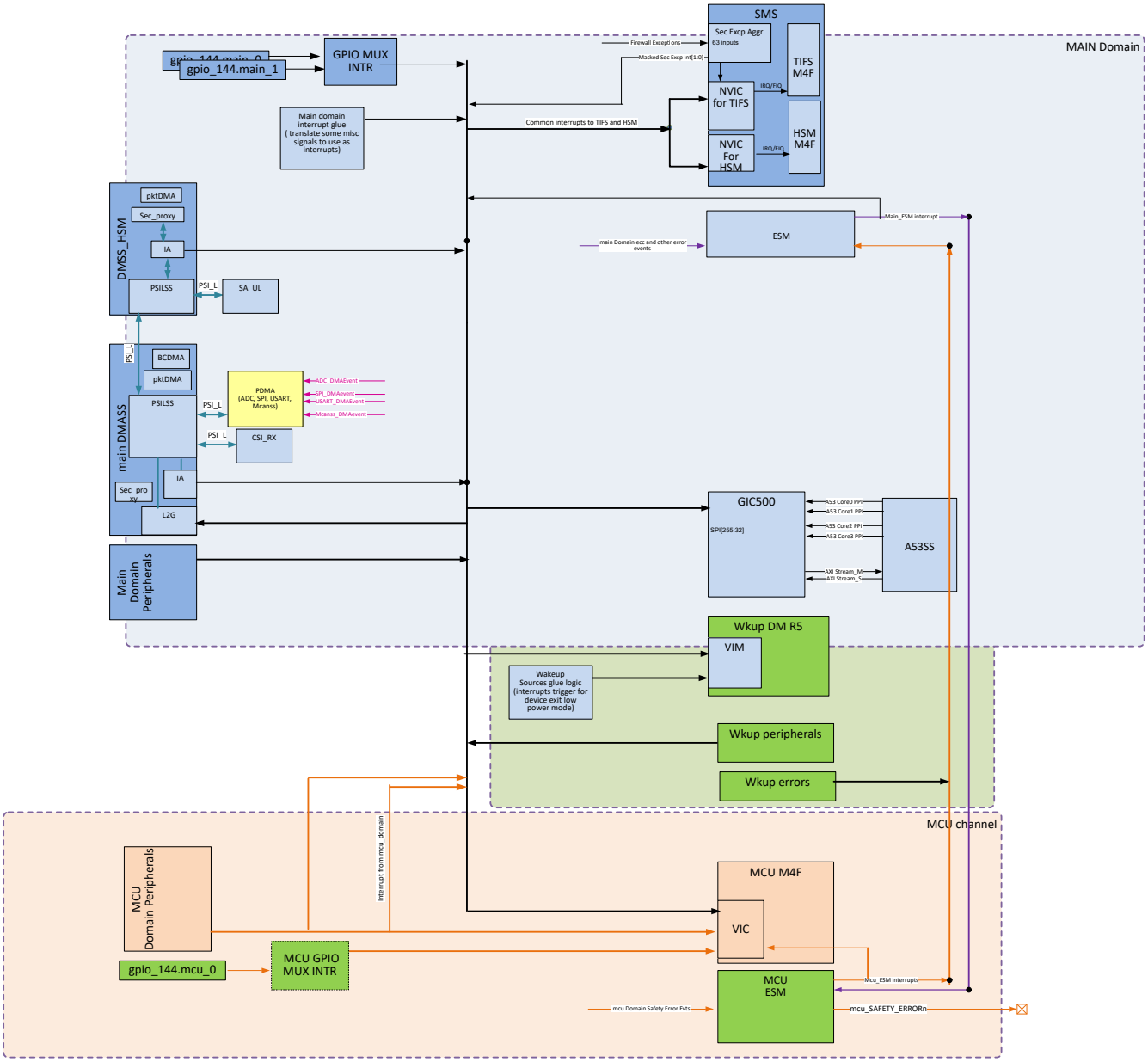

Figure 1-1. AM62 Interrupt Architecture

1.1.1 ESM Connectivity

AM62 contains two ESM modules to consolidate the error interrupts in SoC. One is in the Main domain and one is in the MCU domain. Figure 1-2 shows how error interrupts are connected to these two ESM.

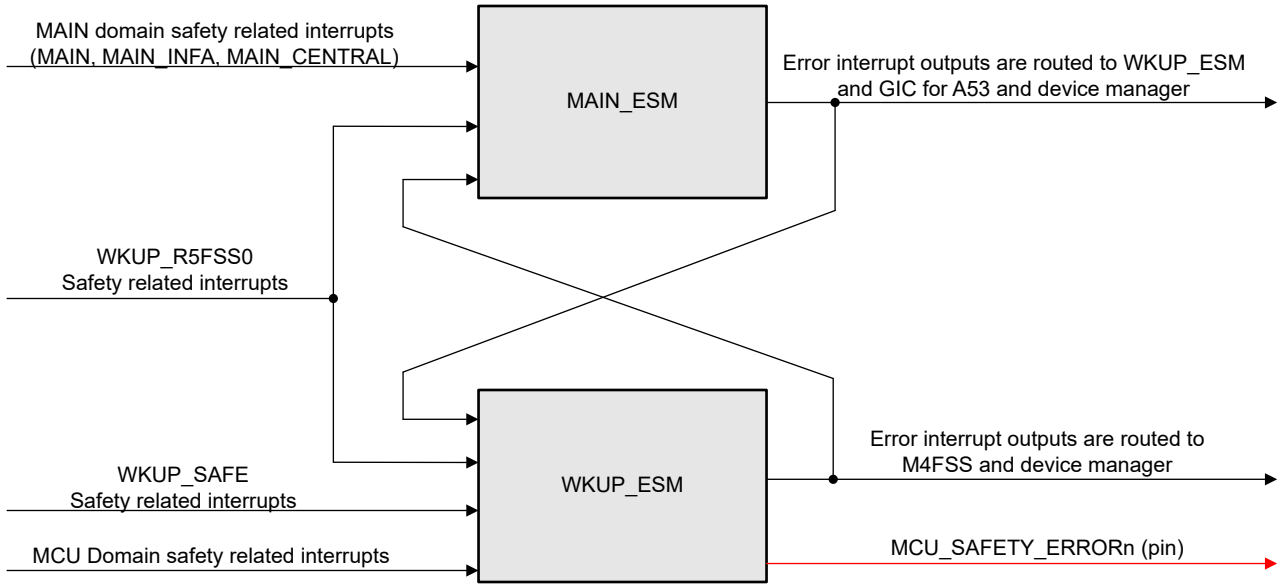

Figure 1-2. ESM Connection

The error interrupts from the Wkup_DM domain are routed to both Main ESM and MCU ESM. Users can configure ESM to cause ESM generating interrupt output from the interrupt inputs. The interrupt outputs of the Main ESM are routed as interrupt inputs to the MCU ESM. The interrupt outputs of the MCU ESM are routed as the interrupt inputs to the Main ESM. This means that user can configure the device to use one ESM to monitor the error interrupts for the whole device. AM62 supports the following three use cases.

1.1.1.1 Using MCU ESM to Monitor All Error Events in SoC

In this use case, the Main ESM is used to consolidate all the error interrupts in the Main domain and Wkup_DM domain as main ESM's interrupt outputs, which are routed as interrupt inputs to the MCU ESM.

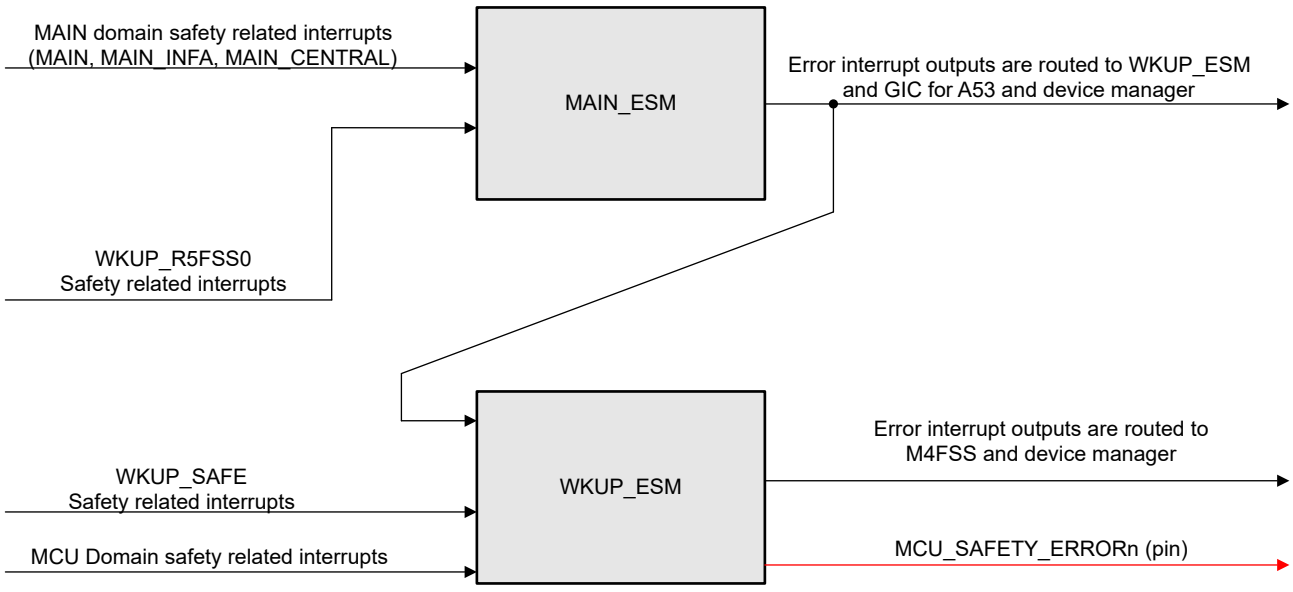

Figure 1-3. Using MCU ESM for All Error Interrupts in SoC

In this use case, the Main ESM should be configured to disable the interrupt inputs coming from the MCU ESM interrupts. If those interrupt inputs are not disabled by the Main ESM, the dependence loop will be formed as following:

1. Error interrupts in the Main domain are routed to Main ESM triggers interrupt outputs generated by the Main ESM

2. The error interrupt outputs from the Main ESM are routed to the MCU ESM as interrupt inputs
3. Those error interrupt inputs triggers the MCU ESM generating its error interrupts outputs
4. Those interrupt outputs from the MCU ESM are routed back to the Main ESM as interrupt inputs. If those interrupts are not disabled at the Main ESM, it will trigger Main ESM generating interrupt outputs in the Main ESM again. Going back to step 1 again.

In addition, since Wkup_DM error events are already routed to the Main ESM, so the input events in the MCU ESM connecting to those error events from the Wkup_DM domain shall be disabled, otherwise those events can trigger the interrupt in both the Main ESM as well as the MCU ESM

1.1.1.2 Using MAIN ESM to Monitor All Error Interrupts in SoC

In this configuration, the MCU ESM is used to consolidate all the error interrupts from the MCU domain and the Wkup_safe domain as interrupt outputs, and those interrupt outputs from the MCU ESM are routed as interrupt inputs to the Main ESM. In order to avoid the interrupt dependence loop, the MCU ESM shall disable the interrupt inputs from ESM0.

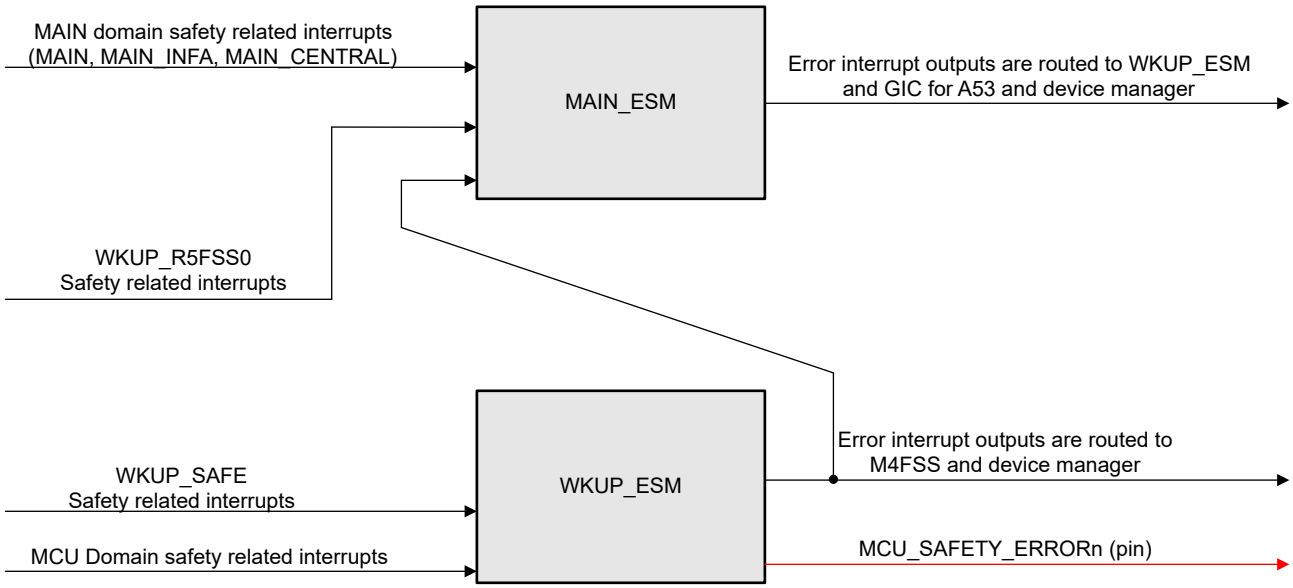

Figure 1-4. Using MAIN ESM to Monitor All Error Interrupts in SoC

1.1.1.3 ESM Configuration During Deep Sleep Mode

When device is in deep sleep mode, only the components in the Wkup_DM domain and the Wkup_safe are available. The Main domain is powered off, so the Main ESM is no longer available. Since MCU ESM is located in the Wkup_safe domain, the MCU ESM is monitoring all of the error events during the deep sleep mode and informs the device manager.

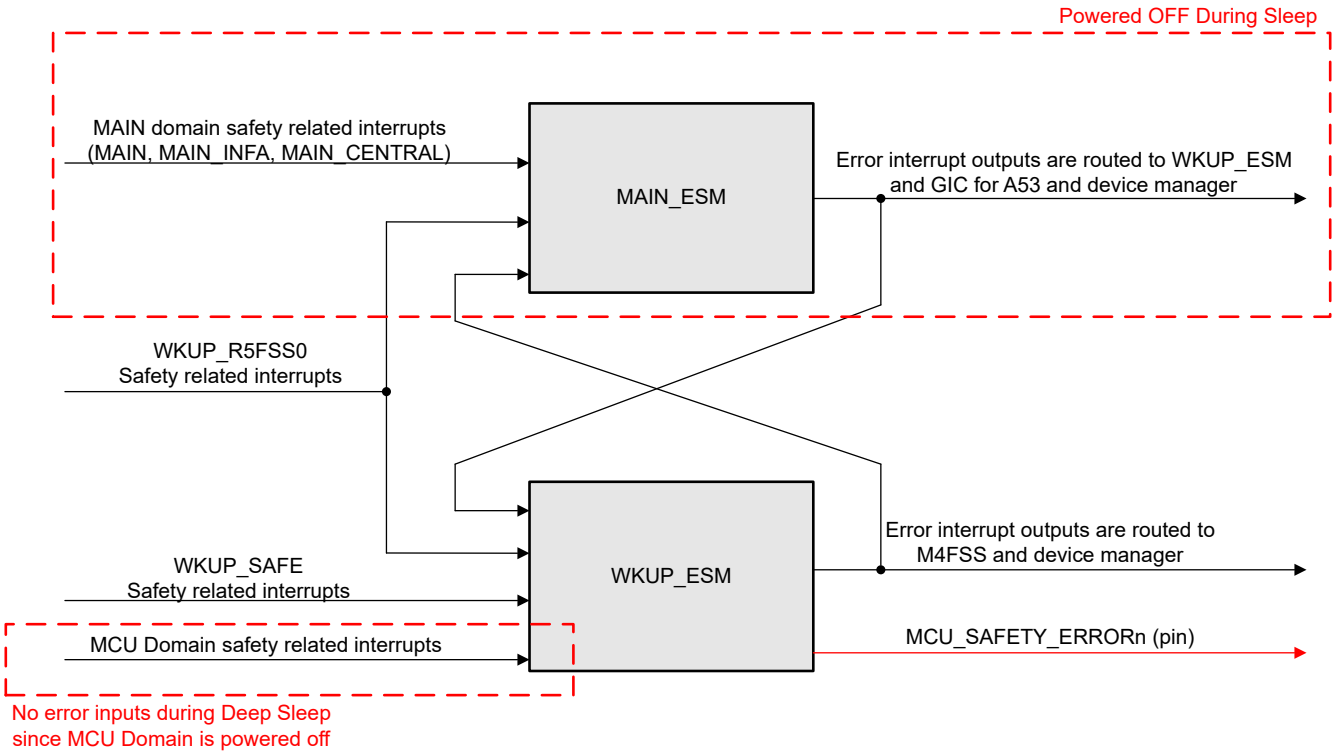

Figure 1-5. Deep Sleep Use Case

1.1.1.4 ESM0_INTERRUPT_MAP

Table 1-2. ESM0_INTERRUPT_MAP Memory Map

Interrupt Input Line	Interrupt ID	Source Interrupt
ESM0_ESM_LVL_EVENT_IN_0	0	CSI_RX_IF0_CSI_ERR_IRQ_0
ESM0_ESM_LVL_EVENT_IN_1	1	ECC_AGGR0_UNCORR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_2	2	ECC_AGGR0_CORR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_3	3	CPSW0_ECC_SEC_PEND_0
ESM0_ESM_LVL_EVENT_IN_4	4	SMS0_RAT_0_EXP_INTR_0
ESM0_ESM_LVL_EVENT_IN_6	6	DDR16SS0_DDRSS_DRAM_ECC_CORR_ERR_LVL_0
ESM0_ESM_LVL_EVENT_IN_7	7	PLLFRACF_SSMOD17_LOCKLOSS_IPCFG_0
ESM0_ESM_LVL_EVENT_IN_8	8	PLLFRACF_SSMOD16_LOCKLOSS_IPCFG_0
ESM0_ESM_LVL_EVENT_IN_9	9	DMASS0_ECC_AGGR_0_ECC_CORRECTED_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_10	10	DMASS0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_11	11	FSS0_OSPI_0_OSPI_ECC_CORR_LVL_INTR_0
ESM0_ESM_LVL_EVENT_IN_12	12	GICSS0_ECC_AGGR_CORR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_13	13	ICSSM0_PR1_ECC_SEC_ERR_PEND_0
ESM0_ESM_LVL_EVENT_IN_14	14	SMS0_RAT_1_EXP_INTR_0
ESM0_ESM_LVL_EVENT_IN_15	15	PDMA0_ECC_SEC_PEND_0
ESM0_ESM_LVL_EVENT_IN_16	16	MCAN0_MCANSS_MSGMEM_WRAP_ECC_AGGR_MCANSS_ECC_CORR_LVL_INT_0
ESM0_ESM_LVL_EVENT_IN_18	18	PSRAMECC_16K0_ECC_CORR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_20	20	WKUP_ECC_AGGR0_CORR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_21	21	WKUP_ECC_AGGR0_UNCORR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_22	22	PSC0_ECC_AGGR_0_FW_CH_BR_ECC_AGGR_CORR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_23	23	PSC0_ECC_AGGR_0_FW_CH_BR_ECC_AGGR_UNCORR_LEVEL_0

Table 1-2. ESM0_INTERRUPT_MAP Memory Map (continued)

Interrupt Input Line	Interrupt ID	Source Interrupt
ESM0_ESM_LVL_EVENT_IN_24	24	COMPUTE_CLUSTER0_ECC_ECCAGGR0_CORRECTED_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_25	25	COMPUTE_CLUSTER0_ECC_ECCAGGR1_CORRECTED_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_26	26	COMPUTE_CLUSTER0_ECC_ECCAGGR_COREPAC_CORRECTED_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_28	28	PDMA1_ECC_SEC_PEND_0
ESM0_ESM_LVL_EVENT_IN_29	29	PSRAMECC0_ECC_CORR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_30	30	R5FSS0_CORE0_ECC_CORRECTED_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_32	32	USB0_HOST_SYSTEM_ERROR_0
ESM0_ESM_LVL_EVENT_IN_33	33	USB1_HOST_SYSTEM_ERROR_0
ESM0_ESM_LVL_EVENT_IN_34	34	MMCSD2_EMMCSD4SS_ECC_AGGR_RXMEM_EMMCSDSS_RXMEM_CORR_ERR_LVL_0
ESM0_ESM_LVL_EVENT_IN_35	35	USB0_A_ECC_AGGR_CORRECTED_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_36	36	MMCSD2_EMMCSD4SS_ECC_AGGR_RXMEM_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_0
ESM0_ESM_LVL_EVENT_IN_37	37	WKUP_ESM0_ESM_INT_CFG_LVL_0
ESM0_ESM_LVL_EVENT_IN_38	38	WKUP_ESM0_ESM_INT_HI_LVL_0
ESM0_ESM_LVL_EVENT_IN_39	39	WKUP_ESM0_ESM_INT_LOW_LVL_0
ESM0_ESM_LVL_EVENT_IN_40	40	R5FSS0_COMMON0_ECC_DE_TO_ESM_0_0
ESM0_ESM_LVL_EVENT_IN_42	42	R5FSS0_COMMON0_ECC_SE_TO_ESM_0_0
ESM0_ESM_LVL_EVENT_IN_44	44	COMPUTE_CLUSTER0_DFT_PBIST_SAFETY_ERROR_0
ESM0_ESM_LVL_EVENT_IN_45	45	COMPUTE_CLUSTER0_ECC_ECCAGGR2_CORRECTED_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_46	46	COMPUTE_CLUSTER0_ECC_ECCAGGR2_UNCORRECTED_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_47	47	COMPUTE_CLUSTER0_ECC_ECCAGGR3_CORRECTED_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_48	48	COMPUTE_CLUSTER0_ECC_ECCAGGR3_UNCORRECTED_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_49	49	MMCSD2_EMMCSD4SS_ECC_AGGR_TXMEM_EMMCSDSS_TXMEM_CORR_ERR_LVL_0
ESM0_ESM_LVL_EVENT_IN_50	50	SMS0_TIMER_0_INTR_PEND_0
ESM0_ESM_LVL_EVENT_IN_51	51	SMS0_TIMER_1_INTR_PEND_0
ESM0_ESM_LVL_EVENT_IN_52	52	SMS0_TIMER_2_INTR_PEND_0
ESM0_ESM_LVL_EVENT_IN_53	53	SMS0_TIMER_3_INTR_PEND_0
ESM0_ESM_LVL_EVENT_IN_54	54	MMCSD0_EMMCSDSS_RXMEM_CORR_ERR_LVL_0
ESM0_ESM_LVL_EVENT_IN_55	55	MMCSD0_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_0
ESM0_ESM_LVL_EVENT_IN_56	56	MMCSD0_EMMCSDSS_TXMEM_CORR_ERR_LVL_0
ESM0_ESM_LVL_EVENT_IN_57	57	MMCSD0_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_0
ESM0_ESM_LVL_EVENT_IN_58	58	MMCSD1_EMMCSD4SS_ECC_AGGR_RXMEM_EMMCSDSS_RXMEM_CORR_ERR_LVL_0
ESM0_ESM_LVL_EVENT_IN_59	59	MMCSD1_EMMCSD4SS_ECC_AGGR_RXMEM_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_0
ESM0_ESM_LVL_EVENT_IN_60	60	MMCSD1_EMMCSD4SS_ECC_AGGR_TXMEM_EMMCSDSS_TXMEM_CORR_ERR_LVL_0
ESM0_ESM_LVL_EVENT_IN_61	61	MMCSD1_EMMCSD4SS_ECC_AGGR_TXMEM_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_0
ESM0_ESM_LVL_EVENT_IN_65	65	MMCSD2_EMMCSD4SS_ECC_AGGR_TXMEM_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_0
ESM0_ESM_LVL_EVENT_IN_66	66	CSI_RX_IF0_CORR_LEVEL_0

Table 1-2. ESM0_INTERRUPT_MAP Memory Map (continued)

Interrupt Input Line	Interrupt ID	Source Interrupt
ESM0_ESM_LVL_EVENT_IN_67	67	CPSW0_ECC_DED_PEND_0
ESM0_ESM_LVL_EVENT_IN_68	68	ICSSM0_PR1_EDIO0_WD_TRIIG_0
ESM0_ESM_LVL_EVENT_IN_69	69	DDR16SS0_DDRSS_DRAM_ECC_UNCORR_ERR_LVL_0
ESM0_ESM_LVL_EVENT_IN_70	70	CSI_RX_IF0_CSI_FATAL_0
ESM0_ESM_LVL_EVENT_IN_71	71	CSI_RX_IF0_CSI_NONFATAL_0
ESM0_ESM_LVL_EVENT_IN_72	72	CSI_RX_IF0_CSI_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_74	74	FSS0_OSPI_0_OSPI_ECC_UNCORR_LVL_INTR_0
ESM0_ESM_LVL_EVENT_IN_75	75	GICSS0_ECC_AGGR_UNCORR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_76	76	ICSSM0_PR1_ECC_DED_ERR_PEND_0
ESM0_ESM_LVL_EVENT_IN_77	77	CSI_RX_IF0_UNCORR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_78	78	MCAN0_MCANSS_MSGMEM_WRAP_ECC_AGGR_MCANSS_ECC_UNCORR_LVL_INT_0
ESM0_ESM_LVL_EVENT_IN_79	79	DCC6_INTR_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_80	80	PSRAMECC_16K0_ECC_UNCORR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_81	81	SMS0_RTI_1_WDG_INTR_0
ESM0_ESM_LVL_EVENT_IN_82	82	SMS0_RTI_1_WDG_INTR_1
ESM0_ESM_LVL_EVENT_IN_83	83	SMS0_RTI_1_WDG_INTR_2
ESM0_ESM_LVL_EVENT_IN_84	84	SMS0_RTI_1_WDG_INTR_3
ESM0_ESM_LVL_EVENT_IN_85	85	SMS0_RTI_1_WDG_INTR_4
ESM0_ESM_LVL_EVENT_IN_87	87	SMS0_RTI_0_WDG_INTR_0
ESM0_ESM_LVL_EVENT_IN_88	88	PDMA0_ECC_DED_PEND_0
ESM0_ESM_LVL_EVENT_IN_89	89	PDMA1_ECC_DED_PEND_0
ESM0_ESM_LVL_EVENT_IN_90	90	PSRAMECC0_ECC_UNCORR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_91	91	R5FSS0_CORE0_ECC_UNCORRECTED_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_92	92	SMS0_RTI_0_WDG_INTR_1
ESM0_ESM_LVL_EVENT_IN_93	93	COMPUTE_CLUSTER0_ECC_ECCAGGR1_UNCORRECTED_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_94	94	COMPUTE_CLUSTER0_ECC_ECCAGGR0_UNCORRECTED_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_95	95	COMPUTE_CLUSTER0_ECC_ECCAGGR_COREPAC_UNCORRECTED_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_96	96	SMS0_RTI_0_WDG_INTR_2
ESM0_ESM_LVL_EVENT_IN_97	97	SMS0_RTI_0_WDG_INTR_3
ESM0_ESM_LVL_EVENT_IN_98	98	DFTSS0_DFT_SAFETY_123_0
ESM0_ESM_LVL_EVENT_IN_99	99	DFTSS0_DFT_SAFETY_MULTI_0
ESM0_ESM_LVL_EVENT_IN_100	100	DFTSS0_DFT_SAFETY_ONE_0
ESM0_ESM_LVL_EVENT_IN_101	101	MCU_MCU0_VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG_IPCFG_0
ESM0_ESM_LVL_EVENT_IN_102	102	MCU_MCU0_VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG_IPCFG_0
ESM0_ESM_LVL_EVENT_IN_103	103	SMS0_RTI_0_WDG_INTR_4
ESM0_ESM_LVL_EVENT_IN_110	110	DDR16SS0_DDRSS_V2A_OTHER_ERR_LVL_0
ESM0_ESM_LVL_EVENT_IN_111	111	USB0_A_ECC_AGGR_UNCORRECTED_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_112	112	DCC0_INTR_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_113	113	DCC1_INTR_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_114	114	DCC2_INTR_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_115	115	DCC3_INTR_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_116	116	DCC4_INTR_ERR_LEVEL_0

Table 1-2. ESM0_INTERRUPT_MAP Memory Map (continued)

Interrupt Input Line	Interrupt ID	Source Interrupt
ESM0_ESM_LVL_EVENT_IN_117	117	DCC5_INTR_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_118	118	SA3_SS0_DMSS_ECCAGGR_0_DMSS_ECC_DED_PEND_0
ESM0_ESM_LVL_EVENT_IN_119	119	SA3_SS0_DMSS_ECCAGGR_0_DMSS_ECC_SEC_PEND_0
ESM0_ESM_LVL_EVENT_IN_120	120	SA3_SS0_SA_UL_0_SA_UL_ECC_CORR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_121	121	SA3_SS0_SA_UL_0_SA_UL_ECC_UNCORR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_124	124	R5FSS0_CORE0_EXP_INTR_0
ESM0_ESM_LVL_EVENT_IN_128	128	PLLFRACF_SSMOD0_LOCKLOSS_IPCFG_0
ESM0_ESM_LVL_EVENT_IN_129	129	PLLFRACF_SSMOD1_LOCKLOSS_IPCFG_0
ESM0_ESM_LVL_EVENT_IN_130	130	PLLFRACF_SSMOD2_LOCKLOSS_IPCFG_0
ESM0_ESM_LVL_EVENT_IN_131	131	PLLFRACF_SSMOD8_LOCKLOSS_IPCFG_0
ESM0_ESM_LVL_EVENT_IN_132	132	PLLFRACF_SSMOD12_LOCKLOSS_IPCFG_0
ESM0_ESM_LVL_EVENT_IN_133	133	PLLFRACF_SSMOD15_LOCKLOSS_IPCFG_0
ESM0_ESM_LVL_EVENT_IN_134	134	MCU_PLLFRACF_SSMOD0_LOCKLOSS_IPCFG_0
ESM0_ESM_LVL_EVENT_IN_135	135	HFOSC0_CLKLOSS_GLUE_REF_CLK_LOSS_DETECT_OUT_0
ESM0_ESM_LVL_EVENT_IN_136	136	WKUP_VTM0_COMMON_0_THERM_LVL_LT_TH0_INTR_0
ESM0_ESM_LVL_EVENT_IN_137	137	WKUP_VTM0_COMMON_0_THERM_LVL_GT_TH1_INTR_0
ESM0_ESM_LVL_EVENT_IN_138	138	WKUP_VTM0_COMMON_0_THERM_LVL_GT_TH2_INTR_0
ESM0_ESM_LVL_EVENT_IN_139	139	WKUP_VTM0_K3VTM_NC_ECCAGGR_CORR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_140	140	WKUP_VTM0_K3VTM_NC_ECCAGGR_UNCORR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_141	141	FSS0_FSAS_0_ECC_INTR_ERR_PEND_0
ESM0_ESM_LVL_EVENT_IN_144	144	COMPUTE_CLUSTER0_EXTERRIRQ_0
ESM0_ESM_LVL_EVENT_IN_145	145	COMPUTE_CLUSTER0_INTERRIRQ_0
ESM0_ESM_LVL_EVENT_IN_146	146	USB1_A_ECC_AGGR_CORRECTED_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_147	147	USB1_A_ECC_AGGR_UNCORRECTED_ERR_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_150	150	SMS0_ECC_AGGR_1_ECC_CORRECTED_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_151	151	SMS0_ECC_AGGR_1_ECC_UNCORRECTED_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_153	153	SMS0_ECC_AGGR_0_ECC_CORRECTED_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_154	154	SMS0_ECC_AGGR_0_ECC_UNCORRECTED_LEVEL_0
ESM0_ESM_LVL_EVENT_IN_156	156	PBIST1_DFT_PBIST_SAFETY_ERROR_0
ESM0_ESM_LVL_EVENT_IN_157	157	PBIST0_DFT_PBIST_SAFETY_ERROR_0
ESM0_ESM_LVL_EVENT_IN_158	158	WKUP_PBIST0_DFT_PBIST_SAFETY_ERROR_0
ESM0_ESM_PLS_EVENT0_IN_160	160	RTI0_INTR_WWD_0
ESM0_ESM_PLS_EVENT1_IN_160	160	RTI0_INTR_WWD_0
ESM0_ESM_PLS_EVENT2_IN_160	160	RTI0_INTR_WWD_0
ESM0_ESM_PLS_EVENT0_IN_161	161	RTI1_INTR_WWD_0
ESM0_ESM_PLS_EVENT1_IN_161	161	RTI1_INTR_WWD_0
ESM0_ESM_PLS_EVENT2_IN_161	161	RTI1_INTR_WWD_0
ESM0_ESM_PLS_EVENT0_IN_162	162	RTI15_INTR_WWD_0
ESM0_ESM_PLS_EVENT1_IN_162	162	RTI15_INTR_WWD_0
ESM0_ESM_PLS_EVENT2_IN_162	162	RTI15_INTR_WWD_0
ESM0_ESM_PLS_EVENT0_IN_163	163	WKUP_RTI0_INTR_WWD_0
ESM0_ESM_PLS_EVENT1_IN_163	163	WKUP_RTI0_INTR_WWD_0
ESM0_ESM_PLS_EVENT2_IN_163	163	WKUP_RTI0_INTR_WWD_0
ESM0_ESM_PLS_EVENT0_IN_164	164	PBIST0_DFT_PBIST_CPU_0
ESM0_ESM_PLS_EVENT1_IN_164	164	PBIST0_DFT_PBIST_CPU_0
ESM0_ESM_PLS_EVENT2_IN_164	164	PBIST0_DFT_PBIST_CPU_0
ESM0_ESM_PLS_EVENT0_IN_165	165	PBIST1_DFT_PBIST_CPU_0

Table 1-2. ESM0_INTERRUPT_MAP Memory Map (continued)

Interrupt Input Line	Interrupt ID	Source Interrupt
ESM0_ESM_PLS_EVENT1_IN_165	165	PBIST1_DFT_PBIST_CPU_0
ESM0_ESM_PLS_EVENT2_IN_165	165	PBIST1_DFT_PBIST_CPU_0
ESM0_ESM_PLS_EVENT0_IN_166	166	GICSS0_AXIM_ERR_0
ESM0_ESM_PLS_EVENT1_IN_166	166	GICSS0_AXIM_ERR_0
ESM0_ESM_PLS_EVENT2_IN_166	166	GICSS0_AXIM_ERR_0
ESM0_ESM_PLS_EVENT0_IN_167	167	GICSS0_ECC_FATAL_0
ESM0_ESM_PLS_EVENT1_IN_167	167	GICSS0_ECC_FATAL_0
ESM0_ESM_PLS_EVENT2_IN_167	167	GICSS0_ECC_FATAL_0
ESM0_ESM_PLS_EVENT0_IN_170	170	WKUP_PBIST0_DFT_PBIST_CPU_0
ESM0_ESM_PLS_EVENT1_IN_170	170	WKUP_PBIST0_DFT_PBIST_CPU_0
ESM0_ESM_PLS_EVENT2_IN_170	170	WKUP_PBIST0_DFT_PBIST_CPU_0
ESM0_ESM_PLS_EVENT0_IN_176	176	COMPUTE_CLUSTER0_DFT_PBIST_CPU_0
ESM0_ESM_PLS_EVENT1_IN_176	176	COMPUTE_CLUSTER0_DFT_PBIST_CPU_0
ESM0_ESM_PLS_EVENT2_IN_176	176	COMPUTE_CLUSTER0_DFT_PBIST_CPU_0
ESM0_ESM_PLS_EVENT0_IN_177	177	RTI2_INTR_WWD_0
ESM0_ESM_PLS_EVENT1_IN_177	177	RTI2_INTR_WWD_0
ESM0_ESM_PLS_EVENT2_IN_177	177	RTI2_INTR_WWD_0
ESM0_ESM_PLS_EVENT0_IN_178	178	RTI3_INTR_WWD_0
ESM0_ESM_PLS_EVENT1_IN_178	178	RTI3_INTR_WWD_0
ESM0_ESM_PLS_EVENT2_IN_178	178	RTI3_INTR_WWD_0

1.1.1.5 WKUP_ESM0_INTERRUPT_MAP

Table 1-3. WKUP_ESM0_INTERRUPT_MAP Memory Map

Interrupt Input Line	Interrupt ID	Source Interrupt
WKUP_ESM0_ESM_LVL_EVENT_IN_0	0	ESM0_ESM_INT_CFG_LVL_0
WKUP_ESM0_ESM_LVL_EVENT_IN_1	1	ESM0_ESM_INT_HI_LVL_0
WKUP_ESM0_ESM_LVL_EVENT_IN_2	2	ESM0_ESM_INT_LOW_LVL_0
WKUP_ESM0_ESM_LVL_EVENT_IN_3	3	MCU_M4FSS0_RAT_EXP_0
WKUP_ESM0_ESM_LVL_EVENT_IN_4	4	MCU_M4FSS0_ECC_AGGR_LVL_CORRECTED_ERR_0
WKUP_ESM0_ESM_LVL_EVENT_IN_5	5	MCU_M4FSS0_ECC_AGGR_LVL_UNCORRECTED_ERR_0
WKUP_ESM0_ESM_LVL_EVENT_IN_6	6	EFUSE_SCAN_GLUE_CRC_ERR_0
WKUP_ESM0_ESM_LVL_EVENT_IN_7	7	PLLFRACF_SSMOD16_LOCKLOSS_IPCFG_0
WKUP_ESM0_ESM_LVL_EVENT_IN_8	8	WKUP_VTM0_COMMON_0_THERM_LVL_GT_TH1_INTR_0
WKUP_ESM0_ESM_LVL_EVENT_IN_9	9	WKUP_VTM0_COMMON_0_THERM_LVL_LT_TH0_INTR_0
WKUP_ESM0_ESM_LVL_EVENT_IN_10	10	WKUP_VTM0_COMMON_0_THERM_LVL_GT_TH2_INTR_0
WKUP_ESM0_ESM_LVL_EVENT_IN_11	11	WKUP_VTM0_K3VTM_NC_ECCAGGR_CORR_LEVEL_0
WKUP_ESM0_ESM_LVL_EVENT_IN_12	12	WKUP_VTM0_K3VTM_NC_ECCAGGR_UNCORR_LEVEL_0
WKUP_ESM0_ESM_LVL_EVENT_IN_13	13	HFOSC0_CLKLOSS_GLUE_REF_CLK_LOSS_DETECT_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_14	14	MCU_ECC_AGGR0_CORR_LEVEL_0
WKUP_ESM0_ESM_LVL_EVENT_IN_15	15	MCU_ECC_AGGR0_UNCORR_LEVEL_0
WKUP_ESM0_ESM_LVL_EVENT_IN_16	16	MCU_MCAN0_MCANSS_MSGMEM_WRAP_ECC_AGGR_MCANSS_ECC_CORR_LVL_INT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_17	17	MCU_MCAN0_MCANSS_MSGMEM_WRAP_ECC_AGGR_MCANSS_ECC_UNCORR_LVL_INT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_18	18	MCU_MCAN1_MCANSS_MSGMEM_WRAP_ECC_AGGR_MCANSS_ECC_CORR_LVL_INT_0

Table 1-3. WKUP_ESM0_INTERRUPT_MAP Memory Map (continued)

Interrupt Input Line	Interrupt ID	Source Interrupt
WKUP_ESM0_ESM_LVL_EVENT_IN_19	19	MCU_MCAN1_MCANSS_MSGMEM_WRAP_ECC_AGGR_MCANSS_ECC_UNCORR_LVL_INT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_20	20	WKUP_SAFE_ECC_AGGR0_CORR_LEVEL_0
WKUP_ESM0_ESM_LVL_EVENT_IN_21	21	WKUP_SAFE_ECC_AGGR0_UNCORR_LEVEL_0
WKUP_ESM0_ESM_LVL_EVENT_IN_22	22	PLLFRACF_SSMOD17_LOCKLOSS_IPCFG_0
WKUP_ESM0_ESM_LVL_EVENT_IN_23	23	WKUP_ECC_AGGR0_CORR_LEVEL_0
WKUP_ESM0_ESM_LVL_EVENT_IN_24	24	WKUP_ECC_AGGR0_UNCORR_LEVEL_0
WKUP_ESM0_ESM_LVL_EVENT_IN_25	25	GLUE_EFC_ERROR_AGGREGATED_ERR_0
WKUP_ESM0_ESM_LVL_EVENT_IN_26	26	MGASKET_INTR_GLUE_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_27	27	SGASKET_INTR_GLUE_OUT_0
WKUP_ESM0_ESM_LVL_EVENT_IN_37	37	MCU_DCC0_INTR_ERR_LEVEL_0
WKUP_ESM0_ESM_LVL_EVENT_IN_47	47	MCU_PLLFRACF_SSMOD0_LOCKLOSS_IPCFG_0
WKUP_ESM0_ESM_LVL_EVENT_IN_54	54	PLLFRACF_SSMOD0_LOCKLOSS_IPCFG_0
WKUP_ESM0_ESM_LVL_EVENT_IN_55	55	PLLFRACF_SSMOD1_LOCKLOSS_IPCFG_0
WKUP_ESM0_ESM_LVL_EVENT_IN_56	56	PLLFRACF_SSMOD2_LOCKLOSS_IPCFG_0
WKUP_ESM0_ESM_LVL_EVENT_IN_57	57	PLLFRACF_SSMOD8_LOCKLOSS_IPCFG_0
WKUP_ESM0_ESM_LVL_EVENT_IN_58	58	PLLFRACF_SSMOD12_LOCKLOSS_IPCFG_0
WKUP_ESM0_ESM_LVL_EVENT_IN_59	59	PLLFRACF_SSMOD15_LOCKLOSS_IPCFG_0
WKUP_ESM0_ESM_PLS_EVENT0_IN_64	64	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_0
WKUP_ESM0_ESM_PLS_EVENT1_IN_64	64	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_0
WKUP_ESM0_ESM_PLS_EVENT2_IN_64	64	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_0
WKUP_ESM0_ESM_PLS_EVENT0_IN_65	65	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_1
WKUP_ESM0_ESM_PLS_EVENT1_IN_65	65	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_1
WKUP_ESM0_ESM_PLS_EVENT2_IN_65	65	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_1
WKUP_ESM0_ESM_PLS_EVENT0_IN_66	66	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_2
WKUP_ESM0_ESM_PLS_EVENT1_IN_66	66	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_2
WKUP_ESM0_ESM_PLS_EVENT2_IN_66	66	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_2
WKUP_ESM0_ESM_PLS_EVENT0_IN_69	69	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_3
WKUP_ESM0_ESM_PLS_EVENT1_IN_69	69	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_3
WKUP_ESM0_ESM_PLS_EVENT2_IN_69	69	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_3
WKUP_ESM0_ESM_PLS_EVENT0_IN_70	70	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_4
WKUP_ESM0_ESM_PLS_EVENT1_IN_70	70	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_4
WKUP_ESM0_ESM_PLS_EVENT2_IN_70	70	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_4
WKUP_ESM0_ESM_PLS_EVENT0_IN_71	71	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_0
WKUP_ESM0_ESM_PLS_EVENT1_IN_71	71	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_0
WKUP_ESM0_ESM_PLS_EVENT2_IN_71	71	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_0
WKUP_ESM0_ESM_PLS_EVENT0_IN_72	72	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_1
WKUP_ESM0_ESM_PLS_EVENT1_IN_72	72	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_1
WKUP_ESM0_ESM_PLS_EVENT2_IN_72	72	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_1
WKUP_ESM0_ESM_PLS_EVENT0_IN_73	73	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_2
WKUP_ESM0_ESM_PLS_EVENT1_IN_73	73	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_2
WKUP_ESM0_ESM_PLS_EVENT2_IN_73	73	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_2
WKUP_ESM0_ESM_PLS_EVENT0_IN_76	76	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_3
WKUP_ESM0_ESM_PLS_EVENT1_IN_76	76	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_3
WKUP_ESM0_ESM_PLS_EVENT2_IN_76	76	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_3
WKUP_ESM0_ESM_PLS_EVENT0_IN_77	77	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_4
WKUP_ESM0_ESM_PLS_EVENT1_IN_77	77	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_4

Table 1-3. WKUP_ESM0_INTERRUPT_MAP Memory Map (continued)

Interrupt Input Line	Interrupt ID	Source Interrupt
WKUP_ESM0_ESM_PLS_EVENT2_IN_77	77	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_4
WKUP_ESM0_ESM_PLS_EVENT0_IN_78	78	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_0
WKUP_ESM0_ESM_PLS_EVENT1_IN_78	78	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_0
WKUP_ESM0_ESM_PLS_EVENT2_IN_78	78	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_0
WKUP_ESM0_ESM_PLS_EVENT0_IN_79	79	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_1
WKUP_ESM0_ESM_PLS_EVENT1_IN_79	79	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_1
WKUP_ESM0_ESM_PLS_EVENT2_IN_79	79	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_1
WKUP_ESM0_ESM_PLS_EVENT0_IN_80	80	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_2
WKUP_ESM0_ESM_PLS_EVENT1_IN_80	80	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_2
WKUP_ESM0_ESM_PLS_EVENT2_IN_80	80	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_2
WKUP_ESM0_ESM_PLS_EVENT0_IN_81	81	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_3
WKUP_ESM0_ESM_PLS_EVENT1_IN_81	81	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_3
WKUP_ESM0_ESM_PLS_EVENT2_IN_81	81	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_3
WKUP_ESM0_ESM_PLS_EVENT0_IN_82	82	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_4
WKUP_ESM0_ESM_PLS_EVENT1_IN_82	82	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_4
WKUP_ESM0_ESM_PLS_EVENT2_IN_82	82	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_4
WKUP_ESM0_ESM_PLS_EVENT0_IN_85	85	MCU_RTI0_INTR_WWD_0
WKUP_ESM0_ESM_PLS_EVENT1_IN_85	85	MCU_RTI0_INTR_WWD_0
WKUP_ESM0_ESM_PLS_EVENT2_IN_85	85	MCU_RTI0_INTR_WWD_0
WKUP_ESM0_ESM_PLS_EVENT0_IN_88	88	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_8
WKUP_ESM0_ESM_PLS_EVENT1_IN_88	88	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_8
WKUP_ESM0_ESM_PLS_EVENT2_IN_88	88	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_8
WKUP_ESM0_ESM_PLS_EVENT0_IN_89	89	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_9
WKUP_ESM0_ESM_PLS_EVENT1_IN_89	89	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_9
WKUP_ESM0_ESM_PLS_EVENT2_IN_89	89	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_9
WKUP_ESM0_ESM_PLS_EVENT0_IN_90	90	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_10
WKUP_ESM0_ESM_PLS_EVENT1_IN_90	90	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_10
WKUP_ESM0_ESM_PLS_EVENT2_IN_90	90	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_10
WKUP_ESM0_ESM_PLS_EVENT0_IN_91	91	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_11
WKUP_ESM0_ESM_PLS_EVENT1_IN_91	91	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_11
WKUP_ESM0_ESM_PLS_EVENT2_IN_91	91	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_11

1.1.2 Events

Events are mainly generated by the BCDMA and the pktDMA. In addition, the sec_proxy IPC module also generates event outputs. Events can be directly utilized by the BCDMA and the pktDMA. If those events need to be processed by processor, the events need to be converted to interrupts through the Interrupt Aggregator (IA) Module. Refer to for information on how IA is used. Figure 1-6 shows which modules generates events and how the events are converted to the interrupt.

BCDMA transfer can only be triggered through an event or by software. There are 32 SoC level interrupt signals that can be used to trigger a BCDMA transfer. Figure 1-7 shows all of the possible interrupts and signals that can be used to trigger BCDMA transfer autonomously.

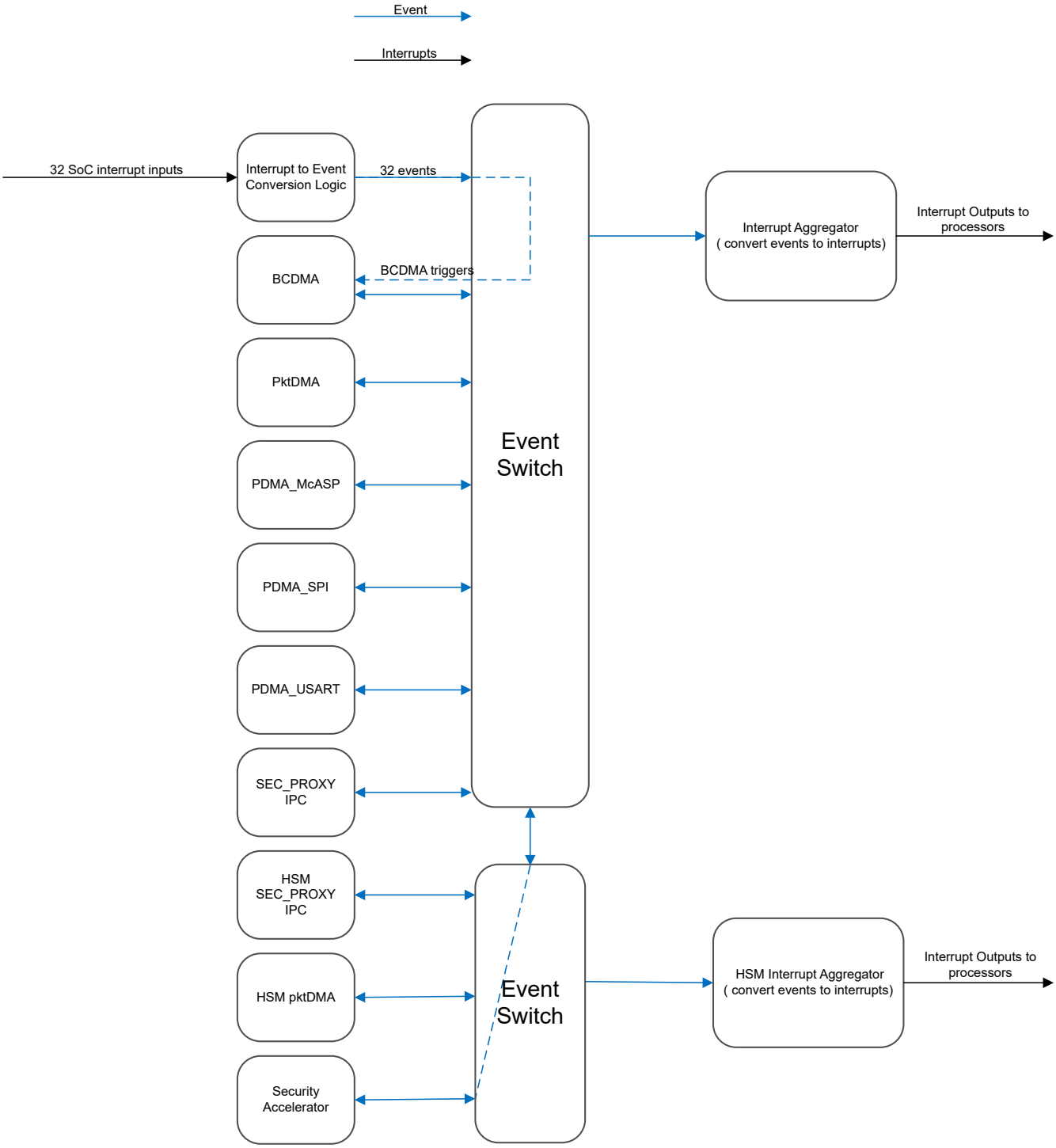

Figure 1-6. Event Handling

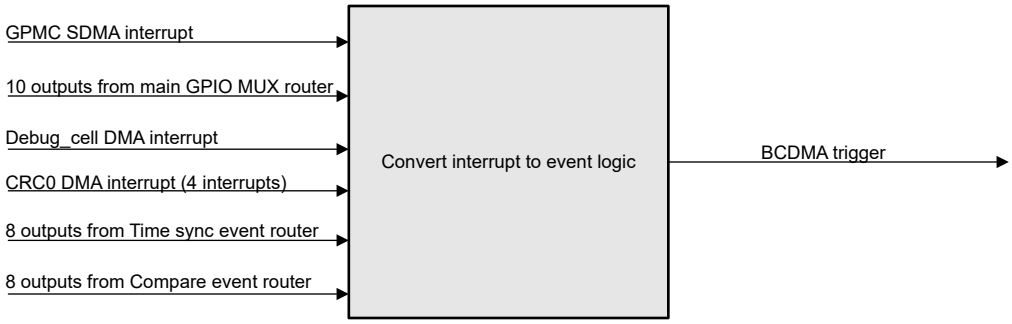

Figure 1-7. SoC Level Interrupt Could be Used for BCDMA Trigger

Table 1-4shows all the possible interrupt sources which can be used as BCDMA triggers.

Table 1-4. Interrupts Can Be Used as BCDMA Triggers

Input Index	Interrupt Sources
0	cmp_event_introuter.0.outp.24
1	cmp_event_introuter.0.outp.25
2	cmp_event_introuter.0.outp.26
3	cmp_event_introuter.0.outp.27
4	cmp_event_introuter.0.outp.28
5	cmp_event_introuter.0.outp.29
6	cmp_event_introuter.0.outp.30
7	cmp_event_introuter.0.outp.31
8	timesync_event_introuter0.outl.0
9	timesync_event_introuter0.outl.1
10	timesync_event_introuter0.outl.2
11	timesync_event_introuter0.outl.3
12	timesync_event_introuter0.outl.4
13	timesync_event_introuter0.outl.5
14	timesync_event_introuter0.outl.6
15	timesync_event_introuter0.outl.7
16	gpiomux_introuter.outp.24
17	gpiomux_introuter.outp.25
18	gpiomux_introuter.outp.26
19	gpiomux_introuter.outp.27
20	gpiomux_introuter.outp.28
21	gpiomux_introuter.outp.29
22	gpiomux_introuter.outp.30
23	gpiomux_introuter.outp.31
24	gpiomux_introuter.outp.22
25	gpiomux_introuter.outp.23
26	gpmc.0.gpmc_sdmareq.0
27	debugssdavdma_level.0
28	mcrc64.0.dma_event.0
29	mcrc64.0.dma_event.1
30	mcrc64.0.dma_event.2
31	mcrc64.0.dma_event.3

1.1.3 Interrupt Router (INTROUTER)

1.1.3.1 INTROUTER Integration

See the Interrupts section of the Module Integration Chapter for details on clocks, resets and hardware requests.

1.1.4 Time Synchronization Support

Time sync event router enables the flexibility to choose any time synchronization source, whether it is the time synchronization source coming from the external pin or the synchronization pulse generated by the internal peripheral or from the ARM system time counter. Time sync event router also enables the system to utilize time synchronized signal as block copy DMA trigger or as periodical control of EPWM.

The compare event router allows the processor to be interrupted by any of the compared events periodically or use a compared event to generate periodical control on EPWM or triggering block copy DMA transfer. Figure 1-8 shows all the synchronization sources and compare events in the device.

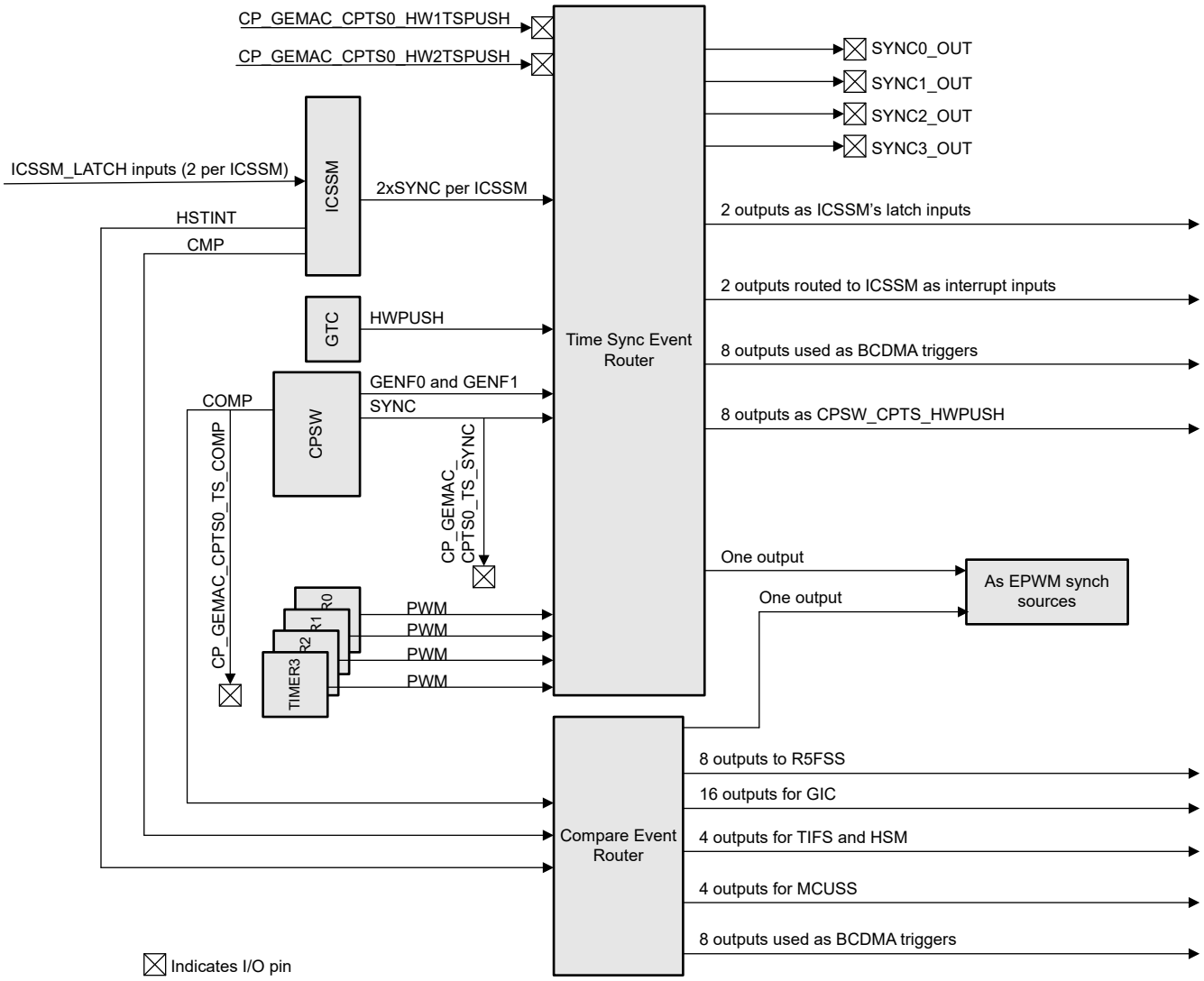

Figure 1-8. Time Synchronization Support

1.1.5 GPIO Interrupt Handling

There are three GPIO modules in the device, which could generate almost 200 interrupts. Those GPIO interrupt outputs are routed to the GPIO interrupt router first before they are routed to the final interrupt destination. The GPIO interrupt router allows each output to select each GPIO interrupt independently.

Two of the GPIO modules in the Main domain use one GPIO interrupt router while the GPIO module in MCU domain has its own dedicated GPIO router. See Figure 1-9.

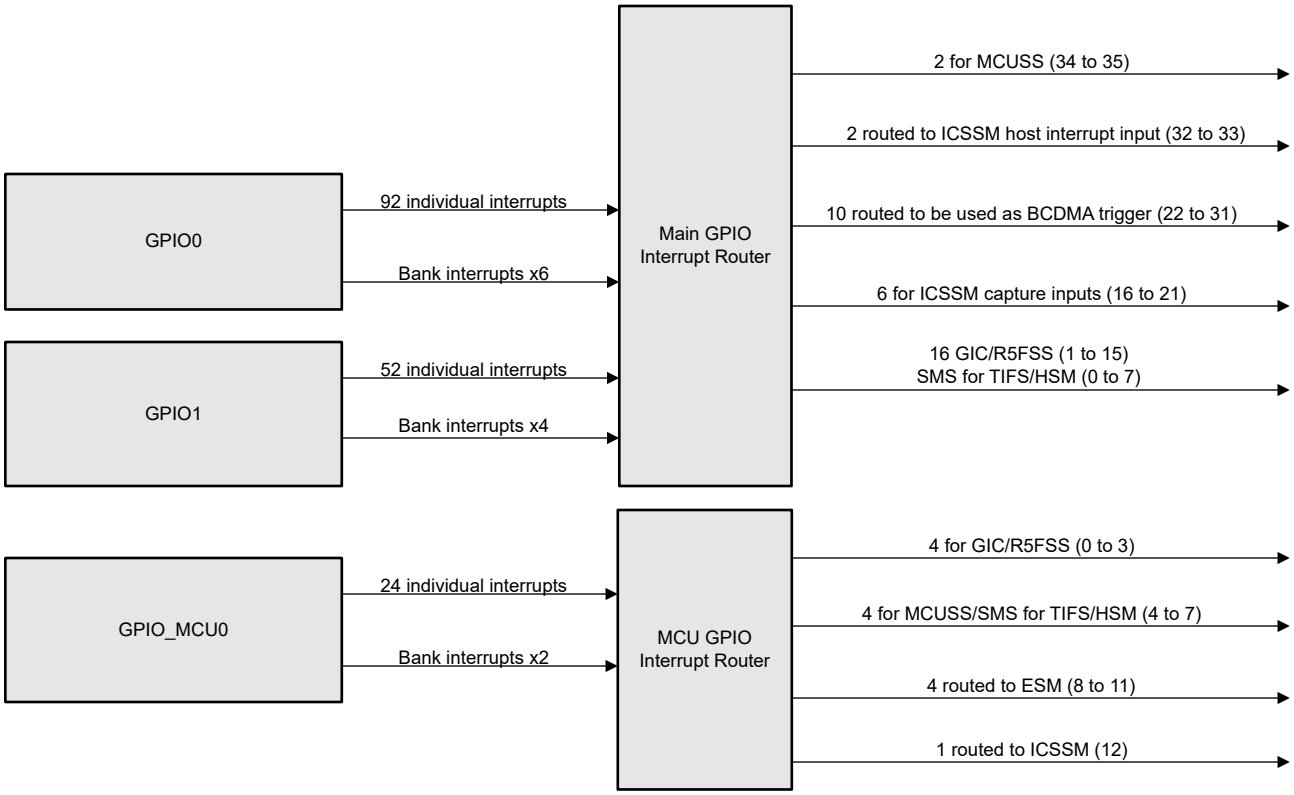

Figure 1-9. GPIO Interrupt Routing

Table 1-5. GPIO_mux_introuter Connection

Input index	Interrupt Source
0	GPIO0.gpio.0
1	GPIO0.gpio.1
2	GPIO0.gpio.2
3	GPIO0.gpio.3
4	GPIO0.gpio.4
5	GPIO0.gpio.5
6	GPIO0.gpio.6
7	GPIO0.gpio.7
8	GPIO0.gpio.8
9	GPIO0.gpio.9
10	GPIO0.gpio.10
11	GPIO0.gpio.11
12	GPIO0.gpio.12
13	GPIO0.gpio.13
14	GPIO0.gpio.14
15	GPIO0.gpio.15
16	GPIO0.gpio.16
17	GPIO0.gpio.17
18	GPIO0.gpio.18
19	GPIO0.gpio.19
20	GPIO0.gpio.20
21	GPIO0.gpio.21
22	GPIO0.gpio.22

Table 1-5. GPIO_mux_introuter Connection (continued)

Input index	Interrupt Source
23	GPIO0.gpio.23
24	GPIO0.gpio.24
25	GPIO0.gpio.25
26	GPIO0.gpio.26
27	GPIO0.gpio.27
28	GPIO0.gpio.28
29	GPIO0.gpio.29
30	GPIO0.gpio.30
31	GPIO0.gpio.31
32	GPIO0.gpio.32
33	GPIO0.gpio.33
34	GPIO0.gpio.34
35	GPIO0.gpio.35
36	GPIO0.gpio.36
37	GPIO0.gpio.37
38	GPIO0.gpio.38
39	GPIO0.gpio.39
40	GPIO0.gpio.40
41	GPIO0.gpio.41
42	GPIO0.gpio.42
43	GPIO0.gpio.43
44	GPIO0.gpio.44
45	GPIO0.gpio.45
46	GPIO0.gpio.46
47	GPIO0.gpio.47
48	GPIO0.gpio.48
49	GPIO0.gpio.49
50	GPIO0.gpio.50
51	GPIO0.gpio.51
52	GPIO0.gpio.52
53	GPIO0.gpio.53
54	GPIO0.gpio.54
55	GPIO0.gpio.55
56	GPIO0.gpio.56
57	GPIO0.gpio.57
58	GPIO0.gpio.58
59	GPIO0.gpio.59
60	GPIO0.gpio.60
61	GPIO0.gpio.61
62	GPIO0.gpio.62
63	GPIO0.gpio.63
64	GPIO0.gpio.64
65	GPIO0.gpio.65
66	GPIO0.gpio.66
67	GPIO0.gpio.67
68	GPIO0.gpio.68
69	GPIO0.gpio.69

Table 1-5. GPIO_mux_introuter Connection (continued)

Input index	Interrupt Source
70	GPIO0.gpio.70
71	GPIO0.gpio.71
72	GPIO0.gpio.72
73	GPIO0.gpio.73
74	GPIO0.gpio.74
75	GPIO0.gpio.75
76	GPIO0.gpio.76
77	GPIO0.gpio.77
78	GPIO0.gpio.78
79	GPIO0.gpio.79
80	GPIO0.gpio.80
81	GPIO0.gpio.81
82	GPIO0.gpio.82
83	GPIO0.gpio.83
84	GPIO0.gpio.84
85	GPIO0.gpio.85
86	GPIO0.gpio.86
87	GPIO0.gpio.87
88	GPIO0.gpio.88
89	GPIO0.gpio.89
90	GPIO1.gpio.0
91	GPIO1.gpio.1
92	GPIO1.gpio.2
93	GPIO1.gpio.3
94	GPIO1.gpio.4
95	GPIO1.gpio.5
96	GPIO1.gpio.6
97	GPIO1.gpio.7
98	GPIO1.gpio.8
99	GPIO1.gpio.9
100	GPIO1.gpio.10
101	GPIO1.gpio.11
102	GPIO1.gpio.12
103	GPIO1.gpio.13
104	GPIO1.gpio.14
105	GPIO1.gpio.15
106	GPIO1.gpio.16
107	GPIO1.gpio.17
108	GPIO1.gpio.18
109	GPIO1.gpio.19
110	GPIO1.gpio.20
111	GPIO1.gpio.21
112	GPIO1.gpio.22
113	GPIO1.gpio.23
114	GPIO1.gpio.24
115	GPIO1.gpio.25
116	GPIO1.gpio.26

Table 1-5. GPIO_mux_introuter Connection (continued)

Input index	Interrupt Source
117	GPIO1.gpio.27
118	GPIO1.gpio.28
119	GPIO1.gpio.29
120	GPIO1.gpio.30
121	GPIO1.gpio.31
122	GPIO1.gpio.32
123	GPIO1.gpio.33
124	GPIO1.gpio.34
125	GPIO1.gpio.35
126	GPIO1.gpio.36
127	GPIO1.gpio.37
128	GPIO1.gpio.38
129	GPIO1.gpio.39
130	GPIO1.gpio.40
131	GPIO1.gpio.41
132	GPIO1.gpio.42
133	GPIO1.gpio.43
134	GPIO1.gpio.44
135	GPIO1.gpio.45
136	GPIO1.gpio.46
137	GPIO1.gpio.47
138	GPIO1.gpio.48
139	GPIO1.gpio.49
140	GPIO1.gpio.50
141	GPIO1.gpio.51
142	GPIO1.gpio.52
143	GPIO1.gpio.53
144	GPIO1.gpio.54
145	GPIO1.gpio.55
146	GPIO1.gpio.56
147	GPIO1.gpio.57
148	GPIO1.gpio.58
149	GPIO1.gpio.59
150	GPIO1.gpio.60
151	GPIO1.gpio.61
152	GPIO1.gpio.62
153	GPIO1.gpio.63
154	GPIO1.gpio.64
155	GPIO1.gpio.65
156	GPIO1.gpio.66
157	GPIO1.gpio.67
158	GPIO1.gpio.68
159	GPIO1.gpio.69
160	GPIO1.gpio.70
161	GPIO1.gpio.71
162	
163	

Table 1-5. GPIO_mux_introuter Connection (continued)

Input index	Interrupt Source
164	
165	
166	
167	
168	
169	
170	
171	
172	
173	
174	
175	
176	GPIO0.gpio.90
177	GPIO0.gpio.91
178	
179	
180	GPIO1.gpio_bank.0
181	GPIO1.gpio_bank.1
182	GPIO1.gpio_bank.2
183	GPIO1.gpio_bank.3
184	GPIO1.gpio_bank.4
185	
186	
187	
188	
189	
190	GPIO0.gpio_bank.0
191	GPIO0.gpio_bank.1
192	GPIO0.gpio_bank.2
193	GPIO0.gpio_bank.3
194	GPIO0.gpio_bank.4
195	GPIO0.gpio_bank.5
196	
197	
198	
199	

Table 1-6. MCU GPIO MUX Introuter Connections

Input Index	Interrupt Source
0	GPIO0_mcu.gpio.0
1	GPIO0_mcu.gpio.1
2	GPIO0_mcu.gpio.2
3	GPIO0_mcu.gpio.3
4	GPIO0_mcu.gpio.4
5	GPIO0_mcu.gpio.5
6	GPIO0_mcu.gpio.6
7	GPIO0_mcu.gpio.7

Table 1-6. MCU GPIO MUX Introuter Connections (continued)

Input Index	Interrupt Source
8	GPIO0_mcu.gpio.8
9	GPIO0_mcu.gpio.9
10	GPIO0_mcu.gpio.10
11	GPIO0_mcu.gpio.11
12	GPIO0_mcu.gpio.12
13	GPIO0_mcu.gpio.13
14	GPIO0_mcu.gpio.14
15	GPIO0_mcu.gpio.15
16	GPIO0_mcu.gpio.16
17	GPIO0_mcu.gpio.17
18	GPIO0_mcu.gpio.18
19	GPIO0_mcu.gpio.19
20	GPIO0_mcu.gpio.20
21	GPIO0_mcu.gpio.21
22	GPIO0_mcu.gpio.22
23	GPIO0_mcu.gpio.23
24	
25	
26	
27	
28	
29	
30	GPIO0_mcu.gpio_bank.0
31	GPIO0_mcu.gpio_bank.1

1.1.6 Utilizing Miscellaneous Signals as Interrupt

Some of the signals are aggregated through glue logic and need to be handled separately.

1.1.6.1 Aggregated Interrupt from Timeout Gasket

There are multiple timeout gaskets in SoC, some of them are inserted at the initiator side and the others are inserted at the target interface side. Each timeout gasket module generates its own interrupt. Instead of routing the interrupt from each timeout gasket individually to the processor, the interrupts from all the timeout gasket inserted at the target sides are aggregated together (ORed), and all the interrupts from all the timeout gasket inserted at the initiator sides are aggregated together (ORed). The status of each interrupt status is captured by the TOG_STAT registers in both wkup_ctrl_mmr and mcu_ctrl_mmr. Refer to Figure 1-10.

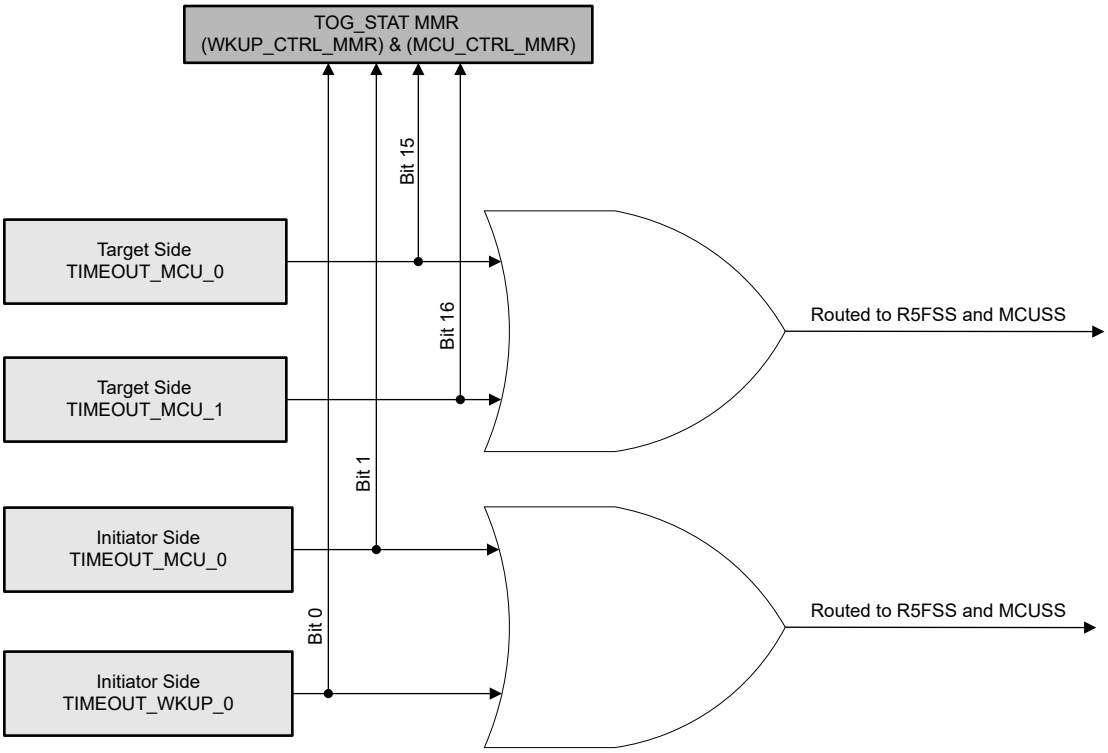

Figure 1-10. Interrupt from Timeout Gaskets

1.1.6.2 Aggregated DCC Interrupt

There are multiple DCC modules in the main domain and each DCC module generates its own DCC_done interrupt. The DCC_done interrupt from all the DCC modules in the main domain are aggregated (ORed) together before it is routed to all the processors, refer to Figure 1-11.

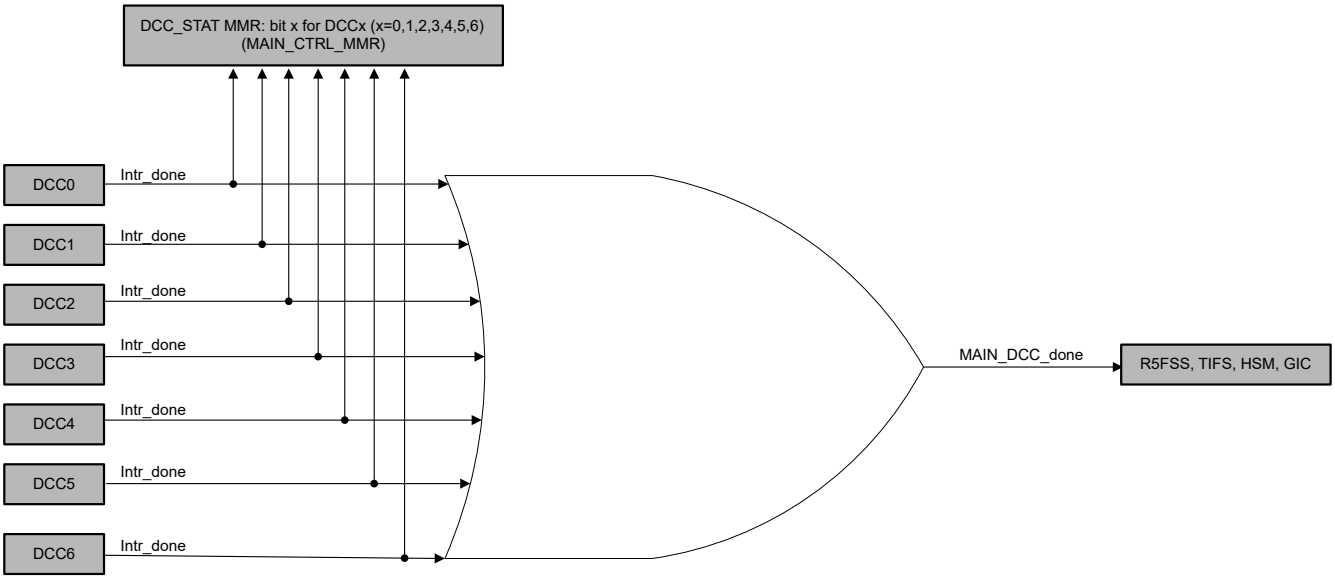

Figure 1-11. DCC Intr_done Interrupt Aggregation

1.1.6.3 Aggregated Access Error Interrupt from CBASS

CBASS modules are the interconnection blocks on the SoC level to provide access path between initiators and targets. When the transaction is not completed successfully, an interrupt is generated by the CBASS and the error transaction is logged by the CBASS module.

There are multiple CBASS modules on the SoC level to provide three layers of interconnect: the data plane, security configuration plane and debug configuration plane. The CBASS access error from the security configuration plane is only routed to TIFS and HSM, and the other CBASS access errors are aggregated before routing it to the processors, refer to Figure 1-12.

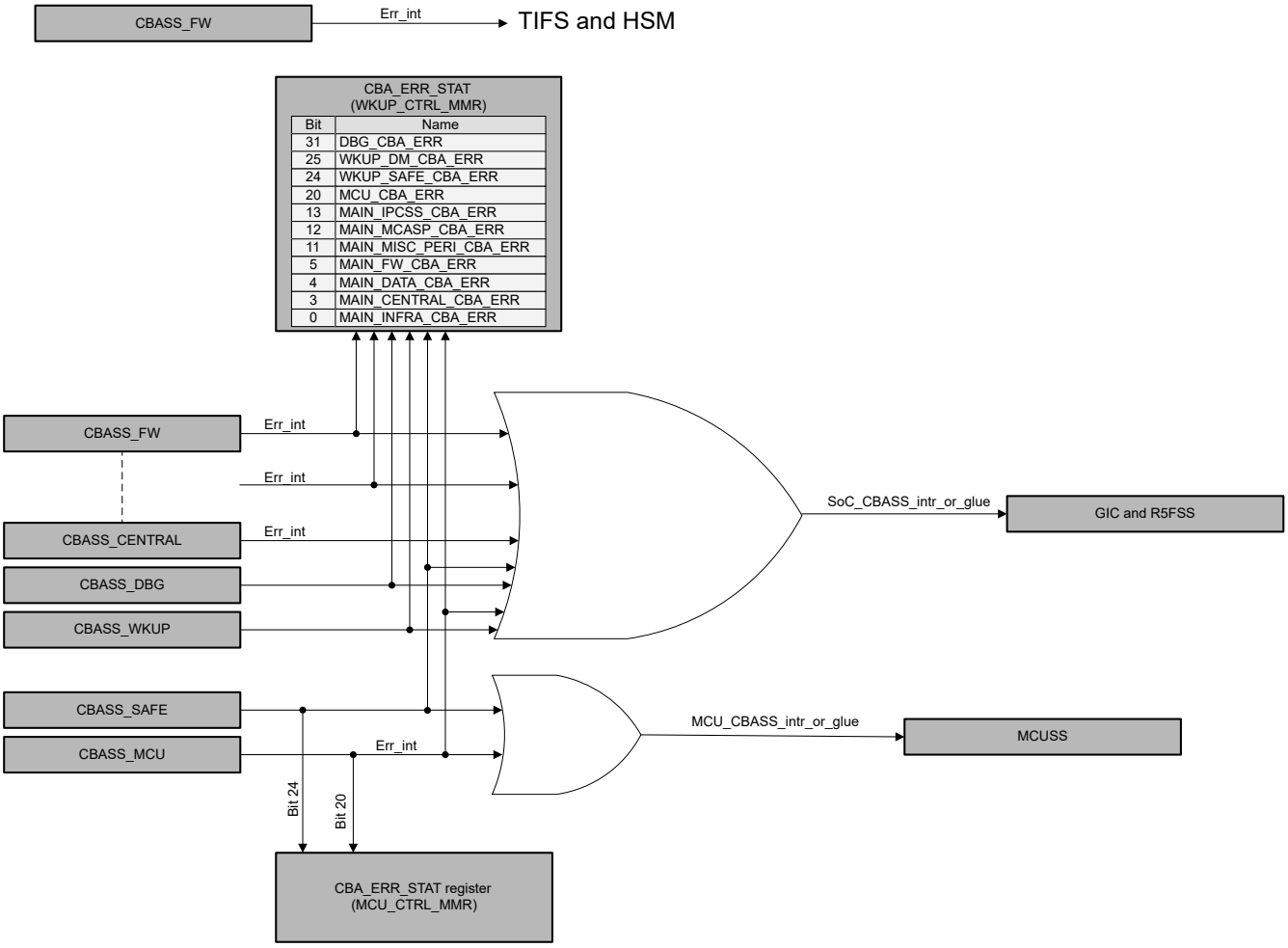

Figure 1-12. Aggregated CBASS Access Error

1.1.6.4 Access Error to Control Register Block Interrupt Aggregation

There are multiple register blocks on the SoC level, and each register block generates an error interrupt when there is an access error. Those access error interrupts are aggregated together before they are routed to processor, refer to Figure 1-13.

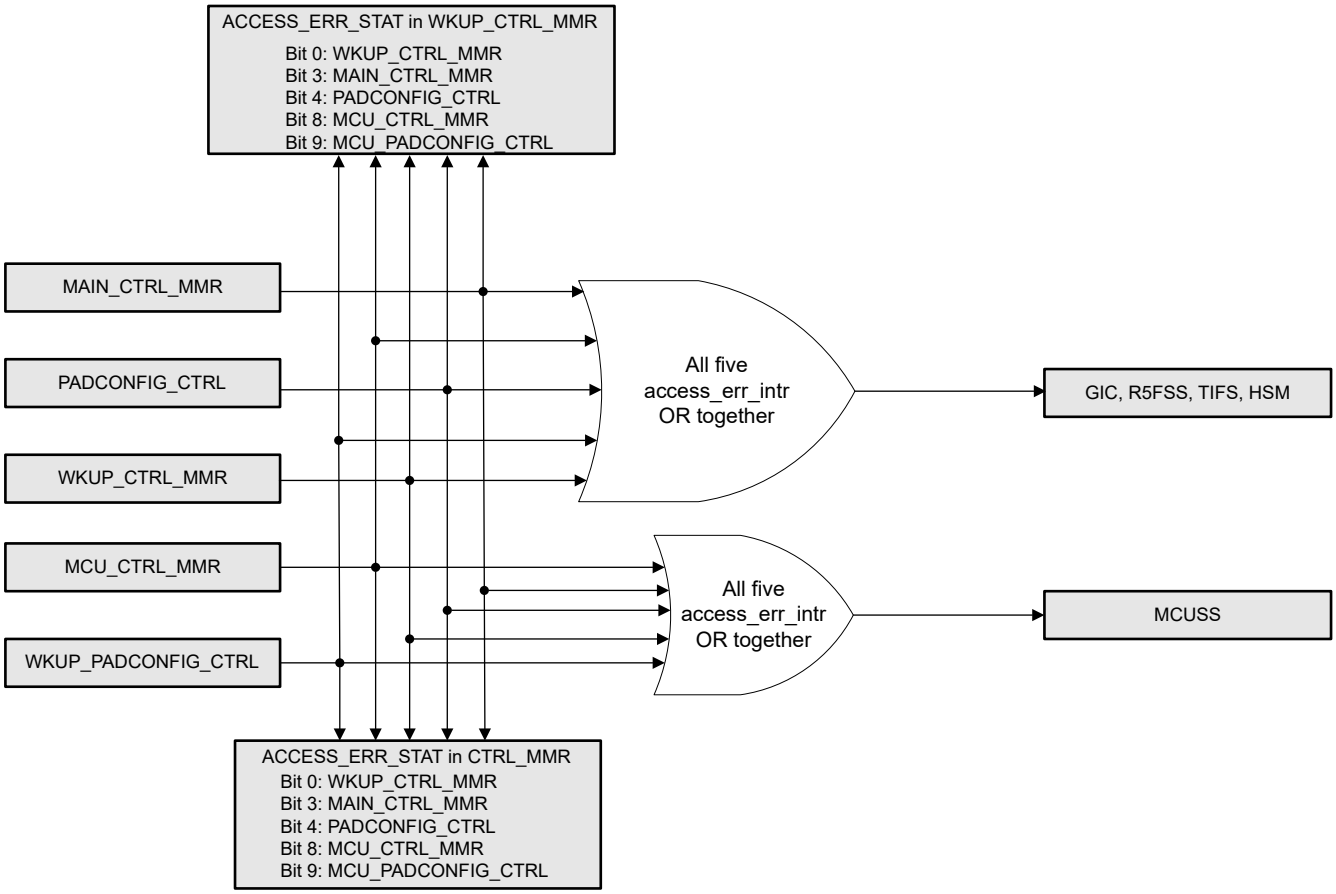

Figure 1-13. Access Error Aggregation

1.1.6.4.1 EPWM Trip Signal Aggregation

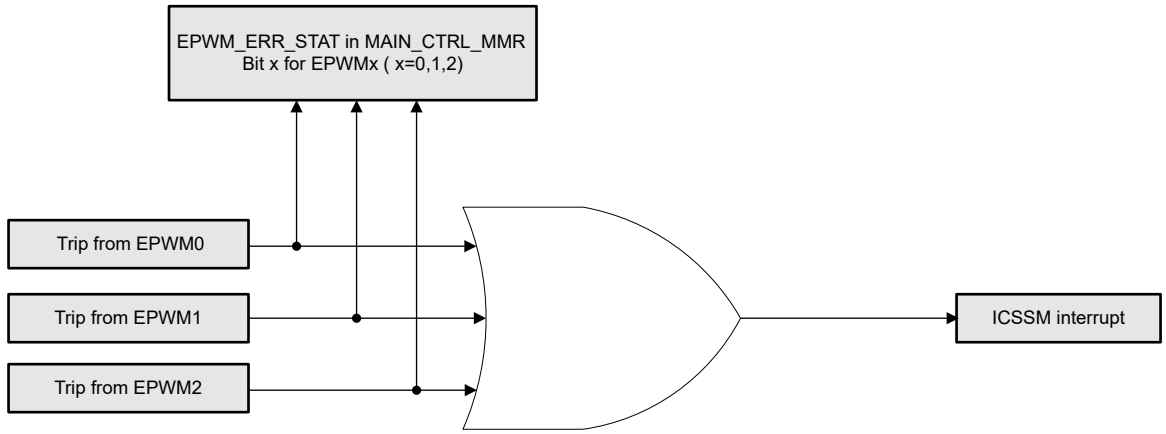

Figure 1-14. EPWM Trip Signal Aggregation as Interrupt

1.1.7 Interrupt Connections Summary

Table 1-7. Interrupt Connections Summary

	GIC	R5FSS	MCUSS	TIFS/HSM	ICSSM
SPI: MAIN domain	Y	Y	N	Y	Y
SPI: MCU domain	Y	Y	Y	Y	N

Table 1-7. Interrupt Connections Summary (continued)

	GIC	R5FSS	MCUSS	TIFS/HSM	ICSSM
USART: MAIN domain	Y	Y	N	Y	Y
UART: WKUP domain	Y	Y	N	N	N
UART:MCU domain	Y	Y	Y	Y	N
I2C: MAIN domain	Y	Y	N	Y	Y
I2C: WKUP domain	Y	Y	N	N	N
I2C: MCU	Y	Y	Y	Y	N
TIMER: MAIN	Y	N	N	N	N
TIMER: WKUP	N	Y	N	N	N
TIMER:MCU	N	N	Y	N	N
MCAN: MAIN	Y	Y	N	Y	N
MCAN: MCU	N	N	Y	Y	N
ECAP	Y	N	N	Y	Y
EQEP	Y	N	N	Y	Y
PWM	Y	N	Y	Y	Y
McASP	Y	N	N	Y	Y
USB	Y	Y	N	N	N
EMMC4b	Y	Y	N	N	N
EMMC8b	Y	Y	N	N	N
GPMC	Y	Y	N	N	N
ELM	Y	Y	N	N	N
MCRC: MAIN	Y	Y	N	Y	N
MCRC:MCU	Y	Y	Y	N	N
debug_cell	Y	Y	N	N	N
wakeup signals from peripherals	N	Y	N	N	N
GIC wake up	N	Y	N	Y	N
DDR frequency scaling	Y	Y	N	Y	N
Other DDR interrupt	Y	Y	N	N	N
FSS	Y	Y	N	Y	Y
CPSW	Y	Y	N	N	N
DSS	Y	Y	Y	N	N
CSI_RX	Y	Y	N	N	N
MAIN DMSS	Y	Y	Y	Y	Y
DMSS_HSM	Y	Y	Y	Y	N
DDPA	Y	Y	Y	Y	N
VTM	Y	Y	Y	Y	N
RTC	Y	Y	N	N	N
ESM: MAIN	Y	Y	Y	Y	N
ESM:MCU	Y	Y	Y	Y	N

Table 1-7. Interrupt Connections Summary (continued)

	GIC	R5FSS	MCUSS	TIFS/HSM	ICSSM
sa3_UL	Y	Y	N	Y	N
GPIO: MAIN	Y	Y	Y	Y	Both as Capture inputs and interrupts
GPIO: MCU	Y	Y	Y	Y	Only as interrupts
PBIST:MAIN	N	Y	N	Y	N
PBIST: WKUP	N	Y	N	Y	N
PBIST:MCU	N	Y	N	Y	N
DCC: MAIN	Y	Y	N	Y	N
DCC:MCU	N	Y	Y	Y	N
ICSSM			Y		n/a
PSC MAIN	Y	Y	N	Y	N
PSC:MCU	N	Y	Y	Y	N
SMS	Y	Y	Y	N/A	N
Timeout gasket	N	Y	Y	N	N
CMP_event_introute output	Y	Y	N	Y	N
timesynch Intrrouter output	Y	Y	N	Y	Y
MAILBOX	Y	Y	Y	Y	Y

1.1.8 Interrupts (Inputs)

Table 1-8. Interrupts (Inputs)

Instance	Interrupt Input Line	Source Interrupt
PINFUNCTION_CP_GEMAC_CPTS0_TS_COMPout	PINFUNCTION_CP_GEMAC_CPTS0_TS_COMPOUT_CP_GEMAC_CPTS0_TS_COMP_IN_0	CPSW0_CPTS_COMP_OUT_0
PINFUNCTION_CP_GEMAC_CPTS0_TS_SYNCout	PINFUNCTION_CP_GEMAC_CPTS0_TS_SYNCOUT_CP_GEMAC_CPTS0_TS_SYNC_IN_0	CPSW0_CPTS_SYNC_OUT_0
PINFUNCTION_SYNC0_OUTout	PINFUNCTION_SYNC0_OUTOUT_SYNC0_OUT_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_20
PINFUNCTION_SYNC1_OUTout	PINFUNCTION_SYNC1_OUTOUT_SYNC1_OUT_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_21
PINFUNCTION_SYNC2_OUTout	PINFUNCTION_SYNC2_OUTOUT_SYNC2_OUT_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_22
PINFUNCTION_SYNC3_OUTout	PINFUNCTION_SYNC3_OUTOUT_SYNC3_OUT_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_23
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_IN_IN_0	ICSSM0_PR1_HOST_INTR_REQ_OUT_0
	CMP_EVENT_INTROUTER0_IN_IN_1	ICSSM0_PR1_HOST_INTR_REQ_OUT_1
	CMP_EVENT_INTROUTER0_IN_IN_2	ICSSM0_PR1_HOST_INTR_REQ_OUT_2
	CMP_EVENT_INTROUTER0_IN_IN_3	ICSSM0_PR1_HOST_INTR_REQ_OUT_3
	CMP_EVENT_INTROUTER0_IN_IN_4	ICSSM0_PR1_HOST_INTR_REQ_OUT_4
	CMP_EVENT_INTROUTER0_IN_IN_5	ICSSM0_PR1_HOST_INTR_REQ_OUT_5
	CMP_EVENT_INTROUTER0_IN_IN_6	ICSSM0_PR1_HOST_INTR_REQ_OUT_6
	CMP_EVENT_INTROUTER0_IN_IN_7	ICSSM0_PR1_HOST_INTR_REQ_OUT_7
	CMP_EVENT_INTROUTER0_IN_IN_8	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_0
	CMP_EVENT_INTROUTER0_IN_IN_9	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_1
	CMP_EVENT_INTROUTER0_IN_IN_10	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_2
	CMP_EVENT_INTROUTER0_IN_IN_11	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_3
	CMP_EVENT_INTROUTER0_IN_IN_12	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_4
	CMP_EVENT_INTROUTER0_IN_IN_13	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_5
	CMP_EVENT_INTROUTER0_IN_IN_14	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_6
	CMP_EVENT_INTROUTER0_IN_IN_15	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_7
	CMP_EVENT_INTROUTER0_IN_IN_16	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_8
	CMP_EVENT_INTROUTER0_IN_IN_17	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_9
	CMP_EVENT_INTROUTER0_IN_IN_18	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_10
	CMP_EVENT_INTROUTER0_IN_IN_19	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_11
	CMP_EVENT_INTROUTER0_IN_IN_20	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_12
	CMP_EVENT_INTROUTER0_IN_IN_21	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_13
	CMP_EVENT_INTROUTER0_IN_IN_22	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_14
	CMP_EVENT_INTROUTER0_IN_IN_23	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_15
	CMP_EVENT_INTROUTER0_IN_IN_24	CPSW0_CPTS_COMP_OUT_0
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_0	GPIO0_GPIO_OUT_0
	MAIN_GPIOMUX_INTROUTER0_IN_IN_1	GPIO0_GPIO_OUT_1
	MAIN_GPIOMUX_INTROUTER0_IN_IN_2	GPIO0_GPIO_OUT_2

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_3	GPIO0_GPIO_OUT_3
	MAIN_GPIOMUX_INTROUTER0_IN_IN_4	GPIO0_GPIO_OUT_4
	MAIN_GPIOMUX_INTROUTER0_IN_IN_5	GPIO0_GPIO_OUT_5
	MAIN_GPIOMUX_INTROUTER0_IN_IN_6	GPIO0_GPIO_OUT_6
	MAIN_GPIOMUX_INTROUTER0_IN_IN_7	GPIO0_GPIO_OUT_7
	MAIN_GPIOMUX_INTROUTER0_IN_IN_8	GPIO0_GPIO_OUT_8
	MAIN_GPIOMUX_INTROUTER0_IN_IN_9	GPIO0_GPIO_OUT_9
	MAIN_GPIOMUX_INTROUTER0_IN_IN_10	GPIO0_GPIO_OUT_10
	MAIN_GPIOMUX_INTROUTER0_IN_IN_11	GPIO0_GPIO_OUT_11
	MAIN_GPIOMUX_INTROUTER0_IN_IN_12	GPIO0_GPIO_OUT_12
	MAIN_GPIOMUX_INTROUTER0_IN_IN_13	GPIO0_GPIO_OUT_13
	MAIN_GPIOMUX_INTROUTER0_IN_IN_14	GPIO0_GPIO_OUT_14
	MAIN_GPIOMUX_INTROUTER0_IN_IN_15	GPIO0_GPIO_OUT_15
	MAIN_GPIOMUX_INTROUTER0_IN_IN_16	GPIO0_GPIO_OUT_16
	MAIN_GPIOMUX_INTROUTER0_IN_IN_17	GPIO0_GPIO_OUT_17
	MAIN_GPIOMUX_INTROUTER0_IN_IN_18	GPIO0_GPIO_OUT_18
	MAIN_GPIOMUX_INTROUTER0_IN_IN_19	GPIO0_GPIO_OUT_19
	MAIN_GPIOMUX_INTROUTER0_IN_IN_20	GPIO0_GPIO_OUT_20
	MAIN_GPIOMUX_INTROUTER0_IN_IN_21	GPIO0_GPIO_OUT_21
	MAIN_GPIOMUX_INTROUTER0_IN_IN_22	GPIO0_GPIO_OUT_22
	MAIN_GPIOMUX_INTROUTER0_IN_IN_23	GPIO0_GPIO_OUT_23
	MAIN_GPIOMUX_INTROUTER0_IN_IN_24	GPIO0_GPIO_OUT_24
	MAIN_GPIOMUX_INTROUTER0_IN_IN_25	GPIO0_GPIO_OUT_25
	MAIN_GPIOMUX_INTROUTER0_IN_IN_26	GPIO0_GPIO_OUT_26
	MAIN_GPIOMUX_INTROUTER0_IN_IN_27	GPIO0_GPIO_OUT_27
	MAIN_GPIOMUX_INTROUTER0_IN_IN_28	GPIO0_GPIO_OUT_28
	MAIN_GPIOMUX_INTROUTER0_IN_IN_29	GPIO0_GPIO_OUT_29
	MAIN_GPIOMUX_INTROUTER0_IN_IN_30	GPIO0_GPIO_OUT_30
	MAIN_GPIOMUX_INTROUTER0_IN_IN_31	GPIO0_GPIO_OUT_31
	MAIN_GPIOMUX_INTROUTER0_IN_IN_32	GPIO0_GPIO_OUT_32
	MAIN_GPIOMUX_INTROUTER0_IN_IN_33	GPIO0_GPIO_OUT_33
	MAIN_GPIOMUX_INTROUTER0_IN_IN_34	GPIO0_GPIO_OUT_34
	MAIN_GPIOMUX_INTROUTER0_IN_IN_35	GPIO0_GPIO_OUT_35
	MAIN_GPIOMUX_INTROUTER0_IN_IN_36	GPIO0_GPIO_OUT_36

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_37	GPIO0_GPIO_OUT_37
	MAIN_GPIOMUX_INTROUTER0_IN_IN_38	GPIO0_GPIO_OUT_38
	MAIN_GPIOMUX_INTROUTER0_IN_IN_39	GPIO0_GPIO_OUT_39
	MAIN_GPIOMUX_INTROUTER0_IN_IN_40	GPIO0_GPIO_OUT_40
	MAIN_GPIOMUX_INTROUTER0_IN_IN_41	GPIO0_GPIO_OUT_41
	MAIN_GPIOMUX_INTROUTER0_IN_IN_42	GPIO0_GPIO_OUT_42
	MAIN_GPIOMUX_INTROUTER0_IN_IN_43	GPIO0_GPIO_OUT_43
	MAIN_GPIOMUX_INTROUTER0_IN_IN_44	GPIO0_GPIO_OUT_44
	MAIN_GPIOMUX_INTROUTER0_IN_IN_45	GPIO0_GPIO_OUT_45
	MAIN_GPIOMUX_INTROUTER0_IN_IN_46	GPIO0_GPIO_OUT_46
	MAIN_GPIOMUX_INTROUTER0_IN_IN_47	GPIO0_GPIO_OUT_47
	MAIN_GPIOMUX_INTROUTER0_IN_IN_48	GPIO0_GPIO_OUT_48
	MAIN_GPIOMUX_INTROUTER0_IN_IN_49	GPIO0_GPIO_OUT_49
	MAIN_GPIOMUX_INTROUTER0_IN_IN_50	GPIO0_GPIO_OUT_50
	MAIN_GPIOMUX_INTROUTER0_IN_IN_51	GPIO0_GPIO_OUT_51
	MAIN_GPIOMUX_INTROUTER0_IN_IN_52	GPIO0_GPIO_OUT_52
	MAIN_GPIOMUX_INTROUTER0_IN_IN_53	GPIO0_GPIO_OUT_53
	MAIN_GPIOMUX_INTROUTER0_IN_IN_54	GPIO0_GPIO_OUT_54
	MAIN_GPIOMUX_INTROUTER0_IN_IN_55	GPIO0_GPIO_OUT_55
	MAIN_GPIOMUX_INTROUTER0_IN_IN_56	GPIO0_GPIO_OUT_56
	MAIN_GPIOMUX_INTROUTER0_IN_IN_57	GPIO0_GPIO_OUT_57
	MAIN_GPIOMUX_INTROUTER0_IN_IN_58	GPIO0_GPIO_OUT_58
	MAIN_GPIOMUX_INTROUTER0_IN_IN_59	GPIO0_GPIO_OUT_59
	MAIN_GPIOMUX_INTROUTER0_IN_IN_60	GPIO0_GPIO_OUT_60
	MAIN_GPIOMUX_INTROUTER0_IN_IN_61	GPIO0_GPIO_OUT_61
	MAIN_GPIOMUX_INTROUTER0_IN_IN_62	GPIO0_GPIO_OUT_62
	MAIN_GPIOMUX_INTROUTER0_IN_IN_63	GPIO0_GPIO_OUT_63
	MAIN_GPIOMUX_INTROUTER0_IN_IN_64	GPIO0_GPIO_OUT_64
	MAIN_GPIOMUX_INTROUTER0_IN_IN_65	GPIO0_GPIO_OUT_65
	MAIN_GPIOMUX_INTROUTER0_IN_IN_66	GPIO0_GPIO_OUT_66
	MAIN_GPIOMUX_INTROUTER0_IN_IN_67	GPIO0_GPIO_OUT_67
	MAIN_GPIOMUX_INTROUTER0_IN_IN_68	GPIO0_GPIO_OUT_68
	MAIN_GPIOMUX_INTROUTER0_IN_IN_69	GPIO0_GPIO_OUT_69
	MAIN_GPIOMUX_INTROUTER0_IN_IN_70	GPIO0_GPIO_OUT_70

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_71	GPIO0_GPIO_OUT_71
	MAIN_GPIOMUX_INTROUTER0_IN_IN_72	GPIO0_GPIO_OUT_72
	MAIN_GPIOMUX_INTROUTER0_IN_IN_73	GPIO0_GPIO_OUT_73
	MAIN_GPIOMUX_INTROUTER0_IN_IN_74	GPIO0_GPIO_OUT_74
	MAIN_GPIOMUX_INTROUTER0_IN_IN_75	GPIO0_GPIO_OUT_75
	MAIN_GPIOMUX_INTROUTER0_IN_IN_76	GPIO0_GPIO_OUT_76
	MAIN_GPIOMUX_INTROUTER0_IN_IN_77	GPIO0_GPIO_OUT_77
	MAIN_GPIOMUX_INTROUTER0_IN_IN_78	GPIO0_GPIO_OUT_78
	MAIN_GPIOMUX_INTROUTER0_IN_IN_79	GPIO0_GPIO_OUT_79
	MAIN_GPIOMUX_INTROUTER0_IN_IN_80	GPIO0_GPIO_OUT_80
	MAIN_GPIOMUX_INTROUTER0_IN_IN_81	GPIO0_GPIO_OUT_81
	MAIN_GPIOMUX_INTROUTER0_IN_IN_82	GPIO0_GPIO_OUT_82
	MAIN_GPIOMUX_INTROUTER0_IN_IN_83	GPIO0_GPIO_OUT_83
	MAIN_GPIOMUX_INTROUTER0_IN_IN_84	GPIO0_GPIO_OUT_84
	MAIN_GPIOMUX_INTROUTER0_IN_IN_85	GPIO0_GPIO_OUT_85
	MAIN_GPIOMUX_INTROUTER0_IN_IN_86	GPIO0_GPIO_OUT_86
	MAIN_GPIOMUX_INTROUTER0_IN_IN_87	GPIO0_GPIO_OUT_87
	MAIN_GPIOMUX_INTROUTER0_IN_IN_88	GPIO0_GPIO_OUT_88
	MAIN_GPIOMUX_INTROUTER0_IN_IN_89	GPIO0_GPIO_OUT_89
	MAIN_GPIOMUX_INTROUTER0_IN_IN_90	GPIO1_GPIO_OUT_0
	MAIN_GPIOMUX_INTROUTER0_IN_IN_91	GPIO1_GPIO_OUT_1
	MAIN_GPIOMUX_INTROUTER0_IN_IN_92	GPIO1_GPIO_OUT_2
	MAIN_GPIOMUX_INTROUTER0_IN_IN_93	GPIO1_GPIO_OUT_3
	MAIN_GPIOMUX_INTROUTER0_IN_IN_94	GPIO1_GPIO_OUT_4
	MAIN_GPIOMUX_INTROUTER0_IN_IN_95	GPIO1_GPIO_OUT_5
	MAIN_GPIOMUX_INTROUTER0_IN_IN_96	GPIO1_GPIO_OUT_6
	MAIN_GPIOMUX_INTROUTER0_IN_IN_97	GPIO1_GPIO_OUT_7
	MAIN_GPIOMUX_INTROUTER0_IN_IN_98	GPIO1_GPIO_OUT_8
	MAIN_GPIOMUX_INTROUTER0_IN_IN_99	GPIO1_GPIO_OUT_9
	MAIN_GPIOMUX_INTROUTER0_IN_IN_100	GPIO1_GPIO_OUT_10
	MAIN_GPIOMUX_INTROUTER0_IN_IN_101	GPIO1_GPIO_OUT_11
	MAIN_GPIOMUX_INTROUTER0_IN_IN_102	GPIO1_GPIO_OUT_12
	MAIN_GPIOMUX_INTROUTER0_IN_IN_103	GPIO1_GPIO_OUT_13
	MAIN_GPIOMUX_INTROUTER0_IN_IN_104	GPIO1_GPIO_OUT_14

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_105	GPIO1_GPIO_OUT_15
	MAIN_GPIOMUX_INTROUTER0_IN_IN_106	GPIO1_GPIO_OUT_16
	MAIN_GPIOMUX_INTROUTER0_IN_IN_107	GPIO1_GPIO_OUT_17
	MAIN_GPIOMUX_INTROUTER0_IN_IN_108	GPIO1_GPIO_OUT_18
	MAIN_GPIOMUX_INTROUTER0_IN_IN_109	GPIO1_GPIO_OUT_19
	MAIN_GPIOMUX_INTROUTER0_IN_IN_110	GPIO1_GPIO_OUT_20
	MAIN_GPIOMUX_INTROUTER0_IN_IN_111	GPIO1_GPIO_OUT_21
	MAIN_GPIOMUX_INTROUTER0_IN_IN_112	GPIO1_GPIO_OUT_22
	MAIN_GPIOMUX_INTROUTER0_IN_IN_113	GPIO1_GPIO_OUT_23
	MAIN_GPIOMUX_INTROUTER0_IN_IN_114	GPIO1_GPIO_OUT_24
	MAIN_GPIOMUX_INTROUTER0_IN_IN_115	GPIO1_GPIO_OUT_25
	MAIN_GPIOMUX_INTROUTER0_IN_IN_116	GPIO1_GPIO_OUT_26
	MAIN_GPIOMUX_INTROUTER0_IN_IN_117	GPIO1_GPIO_OUT_27
	MAIN_GPIOMUX_INTROUTER0_IN_IN_118	GPIO1_GPIO_OUT_28
	MAIN_GPIOMUX_INTROUTER0_IN_IN_119	GPIO1_GPIO_OUT_29
	MAIN_GPIOMUX_INTROUTER0_IN_IN_120	GPIO1_GPIO_OUT_30
	MAIN_GPIOMUX_INTROUTER0_IN_IN_121	GPIO1_GPIO_OUT_31
	MAIN_GPIOMUX_INTROUTER0_IN_IN_122	GPIO1_GPIO_OUT_32
	MAIN_GPIOMUX_INTROUTER0_IN_IN_123	GPIO1_GPIO_OUT_33
	MAIN_GPIOMUX_INTROUTER0_IN_IN_124	GPIO1_GPIO_OUT_34
	MAIN_GPIOMUX_INTROUTER0_IN_IN_125	GPIO1_GPIO_OUT_35
	MAIN_GPIOMUX_INTROUTER0_IN_IN_126	GPIO1_GPIO_OUT_36
	MAIN_GPIOMUX_INTROUTER0_IN_IN_127	GPIO1_GPIO_OUT_37
	MAIN_GPIOMUX_INTROUTER0_IN_IN_128	GPIO1_GPIO_OUT_38
	MAIN_GPIOMUX_INTROUTER0_IN_IN_129	GPIO1_GPIO_OUT_39
	MAIN_GPIOMUX_INTROUTER0_IN_IN_130	GPIO1_GPIO_OUT_40
	MAIN_GPIOMUX_INTROUTER0_IN_IN_131	GPIO1_GPIO_OUT_41
	MAIN_GPIOMUX_INTROUTER0_IN_IN_132	GPIO1_GPIO_OUT_42
	MAIN_GPIOMUX_INTROUTER0_IN_IN_133	GPIO1_GPIO_OUT_43
	MAIN_GPIOMUX_INTROUTER0_IN_IN_134	GPIO1_GPIO_OUT_44
	MAIN_GPIOMUX_INTROUTER0_IN_IN_135	GPIO1_GPIO_OUT_45
	MAIN_GPIOMUX_INTROUTER0_IN_IN_136	GPIO1_GPIO_OUT_46
	MAIN_GPIOMUX_INTROUTER0_IN_IN_137	GPIO1_GPIO_OUT_47
	MAIN_GPIOMUX_INTROUTER0_IN_IN_138	GPIO1_GPIO_OUT_48

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_139	GPIO1_GPIO_OUT_49
	MAIN_GPIOMUX_INTROUTER0_IN_IN_140	GPIO1_GPIO_OUT_50
	MAIN_GPIOMUX_INTROUTER0_IN_IN_141	GPIO1_GPIO_OUT_51
	MAIN_GPIOMUX_INTROUTER0_IN_IN_142	GPIO1_GPIO_OUT_52
	MAIN_GPIOMUX_INTROUTER0_IN_IN_143	GPIO1_GPIO_OUT_53
	MAIN_GPIOMUX_INTROUTER0_IN_IN_144	GPIO1_GPIO_OUT_54
	MAIN_GPIOMUX_INTROUTER0_IN_IN_145	GPIO1_GPIO_OUT_55
	MAIN_GPIOMUX_INTROUTER0_IN_IN_146	GPIO1_GPIO_OUT_56
	MAIN_GPIOMUX_INTROUTER0_IN_IN_147	GPIO1_GPIO_OUT_57
	MAIN_GPIOMUX_INTROUTER0_IN_IN_148	GPIO1_GPIO_OUT_58
	MAIN_GPIOMUX_INTROUTER0_IN_IN_149	GPIO1_GPIO_OUT_59
	MAIN_GPIOMUX_INTROUTER0_IN_IN_150	GPIO1_GPIO_OUT_60
	MAIN_GPIOMUX_INTROUTER0_IN_IN_151	GPIO1_GPIO_OUT_61
	MAIN_GPIOMUX_INTROUTER0_IN_IN_152	GPIO1_GPIO_OUT_62
	MAIN_GPIOMUX_INTROUTER0_IN_IN_153	GPIO1_GPIO_OUT_63
	MAIN_GPIOMUX_INTROUTER0_IN_IN_154	GPIO1_GPIO_OUT_64
	MAIN_GPIOMUX_INTROUTER0_IN_IN_155	GPIO1_GPIO_OUT_65
	MAIN_GPIOMUX_INTROUTER0_IN_IN_156	GPIO1_GPIO_OUT_66
	MAIN_GPIOMUX_INTROUTER0_IN_IN_157	GPIO1_GPIO_OUT_67
	MAIN_GPIOMUX_INTROUTER0_IN_IN_158	GPIO1_GPIO_OUT_68
	MAIN_GPIOMUX_INTROUTER0_IN_IN_159	GPIO1_GPIO_OUT_69
	MAIN_GPIOMUX_INTROUTER0_IN_IN_160	GPIO1_GPIO_OUT_70
	MAIN_GPIOMUX_INTROUTER0_IN_IN_161	GPIO1_GPIO_OUT_71
	MAIN_GPIOMUX_INTROUTER0_IN_IN_176	GPIO0_GPIO_OUT_90
	MAIN_GPIOMUX_INTROUTER0_IN_IN_177	GPIO0_GPIO_OUT_91
	MAIN_GPIOMUX_INTROUTER0_IN_IN_180	GPIO1_GPIO_BANK_OUT_0
	MAIN_GPIOMUX_INTROUTER0_IN_IN_181	GPIO1_GPIO_BANK_OUT_1
	MAIN_GPIOMUX_INTROUTER0_IN_IN_182	GPIO1_GPIO_BANK_OUT_2
	MAIN_GPIOMUX_INTROUTER0_IN_IN_183	GPIO1_GPIO_BANK_OUT_3
	MAIN_GPIOMUX_INTROUTER0_IN_IN_184	GPIO1_GPIO_BANK_OUT_4
	MAIN_GPIOMUX_INTROUTER0_IN_IN_190	GPIO0_GPIO_BANK_OUT_0
	MAIN_GPIOMUX_INTROUTER0_IN_IN_191	GPIO0_GPIO_BANK_OUT_1
	MAIN_GPIOMUX_INTROUTER0_IN_IN_192	GPIO0_GPIO_BANK_OUT_2
	MAIN_GPIOMUX_INTROUTER0_IN_IN_193	GPIO0_GPIO_BANK_OUT_3

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_IN_IN_194	GPIO0_GPIO_BANK_OUT_4
	MAIN_GPIOMUX_INTROUTER0_IN_IN_195	GPIO0_GPIO_BANK_OUT_5
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_0	MCU_GPIO0_GPIO_OUT_0
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_1	MCU_GPIO0_GPIO_OUT_1
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_2	MCU_GPIO0_GPIO_OUT_2
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_3	MCU_GPIO0_GPIO_OUT_3
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_4	MCU_GPIO0_GPIO_OUT_4
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_5	MCU_GPIO0_GPIO_OUT_5
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_6	MCU_GPIO0_GPIO_OUT_6
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_7	MCU_GPIO0_GPIO_OUT_7
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_8	MCU_GPIO0_GPIO_OUT_8
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_9	MCU_GPIO0_GPIO_OUT_9
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_10	MCU_GPIO0_GPIO_OUT_10
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_11	MCU_GPIO0_GPIO_OUT_11
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_12	MCU_GPIO0_GPIO_OUT_12
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_13	MCU_GPIO0_GPIO_OUT_13
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_14	MCU_GPIO0_GPIO_OUT_14
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_15	MCU_GPIO0_GPIO_OUT_15
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_16	MCU_GPIO0_GPIO_OUT_16
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_17	MCU_GPIO0_GPIO_OUT_17
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_18	MCU_GPIO0_GPIO_OUT_18
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_19	MCU_GPIO0_GPIO_OUT_19
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_20	MCU_GPIO0_GPIO_OUT_20
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_21	MCU_GPIO0_GPIO_OUT_21
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_22	MCU_GPIO0_GPIO_OUT_22
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_23	MCU_GPIO0_GPIO_OUT_23
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_30	MCU_GPIO0_GPIO_BANK_OUT_0
	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_31	MCU_GPIO0_GPIO_BANK_OUT_1
TIMESYNC_EVENT_ROUTER0	TIMESYNC_EVENT_ROUTER0_IN_IN_0	TIMER0_TIMER_PWM_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_1	TIMER1_TIMER_PWM_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_2	TIMER2_TIMER_PWM_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_3	TIMER3_TIMER_PWM_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_8	EPWM0_EPWM_SYNCO_O_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_9	ICSSM0_PR1_EDC0_SYNC1_OUT_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
TIMESYNC_EVENT_ROUTER0	TIMESYNC_EVENT_ROUTER0_IN_IN_10	ICSSM0_PR1_EDC0_SYNC0_OUT_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_11	WKUP_GTC0_GTC_PUSH_EVENT_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_12	PINFUNCTION_CP_GEMAC_CPTS0_HW1TSPUSHIN_CP_GEMAC_CPTS0_HW1TSPUSH_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_13	PINFUNCTION_CP_GEMAC_CPTS0_HW2TSPUSHIN_CP_GEMAC_CPTS0_HW2TSPUSH_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_16	CPSW0_CPTS_GENF0_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_17	CPSW0_CPTS_GENF1_OUT_0
	TIMESYNC_EVENT_ROUTER0_IN_IN_18	CPSW0_CPTS_SYNC_OUT_0
MCU_M4FSS0_CORE0	MCU_M4FSS0_CORE0_NVIC_IN_0	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_4
	MCU_M4FSS0_CORE0_NVIC_IN_1	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_5
	MCU_M4FSS0_CORE0_NVIC_IN_2	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_6
	MCU_M4FSS0_CORE0_NVIC_IN_3	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_7
	MCU_M4FSS0_CORE0_NVIC_IN_4	MCU_TIMER0_INTR_PEND_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_5	MCU_TIMER1_INTR_PEND_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_6	MCU_TIMER2_INTR_PEND_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_7	MCU_TIMER3_INTR_PEND_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_8	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_7
	MCU_M4FSS0_CORE0_NVIC_IN_11	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_12	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_13	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_14	MCU_M4FSS0_RAT_0_EXP_INTR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_15	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_34
	MCU_M4FSS0_CORE0_NVIC_IN_16	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_35
	MCU_M4FSS0_CORE0_NVIC_IN_17	MCU_I2C0_POINTRPEND_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_18	DDPA0_DDPA_INTR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_19	MCU_RTI0_INTR_WWD_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_20	WKUP_PSC0_PSC_ALLINT_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_21	MCU_DCC0_INTR_DONE_LEVEL_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_22	MCU_MCSPI0_INTR_SPI_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_23	MCU_MCSPI1_INTR_SPI_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_24	MCU_UART0_USART_IRQ_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_25	MCU_MCRC64_0_INT_MCRC_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_28	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_29	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_30	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MCU_M4FSS0_CORE0	MCU_M4FSS0_CORE0_NVIC_IN_31	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_31	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_32	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_168
	MCU_M4FSS0_CORE0_NVIC_IN_33	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_169
	MCU_M4FSS0_CORE0_NVIC_IN_34	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_170
	MCU_M4FSS0_CORE0_NVIC_IN_35	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_171
	MCU_M4FSS0_CORE0_NVIC_IN_36	EPWM0_EPWM_ETINT_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_37	EPWM1_EPWM_ETINT_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_38	EPWM2_EPWM_ETINT_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_39	CTRL_MMR0_ACCESS_ERR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_39	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_39	PADCFG_CTRL0_ACCESS_ERR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_39	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_39	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_40	DSS0_DISPC_INTR_REQ_0_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_41	DSS0_DISPC_INTR_REQ_1_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_42	MCU_MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_43	MCU_MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_44	MCU_MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
	MCU_M4FSS0_CORE0_NVIC_IN_45	MCU_MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_46	MCU_MCAN1_MCANSS_MCAN_LVL_INT_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_47	MCU_MCAN1_MCANSS_MCAN_LVL_INT_OUT_1
	MCU_M4FSS0_CORE0_NVIC_IN_50	MAILBOX0_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_2
	MCU_M4FSS0_CORE0_NVIC_IN_51	ICSSM0_PR1_HOST_INTR_PEND_OUT_6
	MCU_M4FSS0_CORE0_NVIC_IN_52	ICSSM0_PR1_HOST_INTR_PEND_OUT_7
	MCU_M4FSS0_CORE0_NVIC_IN_53	ICSSM0_ISO_RESET_PROTCOL_ACK_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_54	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_172
	MCU_M4FSS0_CORE0_NVIC_IN_55	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_173
	MCU_M4FSS0_CORE0_NVIC_IN_56	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_174
	MCU_M4FSS0_CORE0_NVIC_IN_57	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_175
	MCU_M4FSS0_CORE0_NVIC_IN_58	CMP_EVENT_INTROUTER0_OUTP_OUT_34
	MCU_M4FSS0_CORE0_NVIC_IN_59	CMP_EVENT_INTROUTER0_OUTP_OUT_35
	MCU_M4FSS0_CORE0_NVIC_IN_60	CMP_EVENT_INTROUTER0_OUTP_OUT_36
	MCU_M4FSS0_CORE0_NVIC_IN_61	CMP_EVENT_INTROUTER0_OUTP_OUT_37

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
MCU_M4FSS0_CORE0	MCU_M4FSS0_CORE0_NVIC_IN_62	MCU_TIMEOUT1_TRANS_ERR_LVL_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_62	MCU_TIMEOUT0_TRANS_ERR_LVL_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_63	TIMEOUT0_TIMED_OUT_OUT_0
	MCU_M4FSS0_CORE0_NVIC_IN_63	WKUP_TIMEOUT0_TIMED_OUT_OUT_0
CPSW0	CPSW0_CPTS_HW1_PUSH_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_10
	CPSW0_CPTS_HW2_PUSH_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_11
	CPSW0_CPTS_HW3_PUSH_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_12
	CPSW0_CPTS_HW4_PUSH_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_13
	CPSW0_CPTS_HW5_PUSH_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_14
	CPSW0_CPTS_HW6_PUSH_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_15
	CPSW0_CPTS_HW7_PUSH_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_16
	CPSW0_CPTS_HW8_PUSH_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_17
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_0	CMP_EVENT_INTROUTER0_OUTP_OUT_24
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_1	CMP_EVENT_INTROUTER0_OUTP_OUT_25
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_2	CMP_EVENT_INTROUTER0_OUTP_OUT_26
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_3	CMP_EVENT_INTROUTER0_OUTP_OUT_27
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_4	CMP_EVENT_INTROUTER0_OUTP_OUT_28
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_5	CMP_EVENT_INTROUTER0_OUTP_OUT_29
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_6	CMP_EVENT_INTROUTER0_OUTP_OUT_30
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_7	CMP_EVENT_INTROUTER0_OUTP_OUT_31
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_8	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_0
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_9	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_1
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_10	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_2
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_11	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_3
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_12	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_4
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_13	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_5
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_14	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_6
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_15	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_7
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_16	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_24
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_17	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_25
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_18	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_26
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_19	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_27
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_20	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_28
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_21	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_29

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_22	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_30
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_23	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_31
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_24	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_22
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_25	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_23
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_26	GPMC0_GPMC_SDMAREQ_OUT_0
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_27	DEBUGSS0_DAVDMA_LEVEL_OUT_0
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_28	MCRC64_0_DMA_EVENT_OUT_0
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_29	MCRC64_0_DMA_EVENT_OUT_1
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_30	MCRC64_0_DMA_EVENT_OUT_2
	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_31	MCRC64_0_DMA_EVENT_OUT_3
ESM0	ESM0_ESM_LVL_EVENT_IN_0	CSI_RX_IF0_CSI_ERR_IRQ_OUT_0
	ESM0_ESM_LVL_EVENT_IN_1	ECC_AGGR0_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_2	ECC_AGGR0_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_3	CPSW0_ECC_SEC_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_6	DDR16SS0_DDRSS_DRAM_ECC_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_7	PLLFRACF2_SSMOD_16FFT17_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_8	PLLFRACF2_SSMOD_16FFT16_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_9	DMASS0_ECC_AGGR_0_ECC_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_10	DMASS0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_11	FSS0_OSPI_0_OSPI_ECC_CORR_LVL_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_12	GICSS0_ECC_AGGR_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_13	ICSSM0_PR1_ECC_SEC_ERR_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_15	PDMA0_ECC_SEC_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_16	MCAN0_MCANSS_ECC_CORR_LVL_INT_OUT_0
	ESM0_ESM_LVL_EVENT_IN_18	PSRAMECC_16K0_ECC_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_20	WKUP_ECC_AGGR0_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_21	WKUP_ECC_AGGR0_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_22	PSC0_ECC_AGGR_0_FW_CH_BR_ECC_AGGR_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_23	PSC0_ECC_AGGR_0_FW_CH_BR_ECC_AGGR_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_24	A53SS0_ECC_ECCAGGR0_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_25	A53SS0_ECC_ECCAGGR1_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_26	A53SS0_ECC_ECCAGGR_COREPAC_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_28	PDMA1_ECC_SEC_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_29	PSRAMECC0_ECC_CORR_LEVEL_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
ESM0	ESM0_ESM_LVL_EVENT_IN_30	WKUP_R5FSS0_CORE0_ECC_CORRECTED_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_32	USB0_HOST_SYSTEM_ERROR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_33	USB1_HOST_SYSTEM_ERROR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_34	MMCSD2_EMMCSDSS_RXMEM_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_35	USB0_A_ECC_AGGR_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_36	MMCSD2_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_37	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_38	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_39	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_40	WKUP_R5FSS0_COMMON0_ECC_DE_TO_ESM_0_OUT_0
	ESM0_ESM_LVL_EVENT_IN_42	WKUP_R5FSS0_COMMON0_ECC_SE_TO_ESM_0_OUT_0
	ESM0_ESM_LVL_EVENT_IN_44	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_SAFETY_ERROR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_45	A53SS0_ECC_ECCAGGR2_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_46	A53SS0_ECC_ECCAGGR2_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_47	A53SS0_ECC_ECCAGGR3_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_48	A53SS0_ECC_ECCAGGR3_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_49	MMCSD2_EMMCSDSS_TXMEM_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_54	MMCSD0_EMMCSDSS_RXMEM_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_55	MMCSD0_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_56	MMCSD0_EMMCSDSS_TXMEM_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_57	MMCSD0_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_58	MMCSD1_EMMCSDSS_RXMEM_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_59	MMCSD1_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_60	MMCSD1_EMMCSDSS_TXMEM_CORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_61	MMCSD1_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_65	MMCSD2_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_66	CSI_RX_IF0_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_67	CPSW0_ECC_DED_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_68	ICSSM0_PR1_EDIO0_WD_TRIIG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_69	DDR16SS0_DDRSS_DRAM_ECC_UNCORR_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_70	CSI_RX_IF0_CSI_FATAL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_71	CSI_RX_IF0_CSI_NONFATAL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_72	CSI_RX_IF0_CSI_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_74	FSS0_OSPI_0_OSPI_ECC_UNCORR_LVL_INTR_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
ESM0	ESM0_ESM_LVL_EVENT_IN_75	GICSS0_ECC_AGGR_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_76	ICSSM0_PR1_ECC_DED_ERR_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_77	CSI_RX_IF0_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_78	MCAN0_MCANSS_ECC_UNCORR_LVL_INT_OUT_0
	ESM0_ESM_LVL_EVENT_IN_79	DCC6_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_80	PSRAMECC_16K0_ECC_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_88	PDMA0_ECC_DED_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_89	PDMA1_ECC_DED_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_90	PSRAMECC0_ECC_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_91	WKUP_R5FSS0_CORE0_ECC_UNCORRECTED_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_93	A53SS0_ECC_ECCAGGR1_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_94	A53SS0_ECC_ECCAGGR0_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_95	A53SS0_ECC_ECCAGGR_COREPAC_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_98	DFTSS0_DFT_SAFETY_123_OUT_0
	ESM0_ESM_LVL_EVENT_IN_99	DFTSS0_DFT_SAFETY_MULTI_OUT_0
	ESM0_ESM_LVL_EVENT_IN_100	DFTSS0_DFT_SAFETY_ONE_OUT_0
	ESM0_ESM_LVL_EVENT_IN_101	MCU_MCU_16FF0_VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_102	MCU_MCU_16FF0_VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_110	DDR16SS0_DDRSS_V2A_OTHER_ERR_LVL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_111	USB0_A_ECC_AGGR_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_112	DCC0_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_113	DCC1_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_114	DCC2_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_115	DCC3_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_116	DCC4_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_117	DCC5_INTR_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_118	SA3_SS0_DMSS_ECCAGGR_0_DMSS_ECC_DED_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_119	SA3_SS0_DMSS_ECCAGGR_0_DMSS_ECC_SEC_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_120	SA3_SS0_SA_UL_0_SA_UL_ECC_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_121	SA3_SS0_SA_UL_0_SA_UL_ECC_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_124	WKUP_R5FSS0_CORE0_EXP_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_128	PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_129	PLLFRACF2_SSMOD_16FFT1_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_130	PLLFRACF2_SSMOD_16FFT2_LOCKLOSS_IPCFG_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
ESM0	ESM0_ESM_LVL_EVENT_IN_131	PLLFRACF2_SSMOD_16FFT8_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_132	PLLFRACF2_SSMOD_16FFT12_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_133	PLLFRACF2_SSMOD_16FFT15_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_134	MCU_PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0
	ESM0_ESM_LVL_EVENT_IN_136	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_137	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_138	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_139	WKUP_VTM0_CORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_140	WKUP_VTM0_UNCORR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_141	FSS0_FSAS_0_ECC_INTR_ERR_PEND_OUT_0
	ESM0_ESM_LVL_EVENT_IN_144	A53SS0_EXTERRIRQ_OUT_0
	ESM0_ESM_LVL_EVENT_IN_145	A53SS0_INTERRIRQ_OUT_0
	ESM0_ESM_LVL_EVENT_IN_146	USB1_A_ECC_AGGR_CORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_147	USB1_A_ECC_AGGR_UNCORRECTED_ERR_LEVEL_OUT_0
	ESM0_ESM_LVL_EVENT_IN_156	PBIST1_DFT_PBIST_SAFETY_ERROR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_157	PBIST0_DFT_PBIST_SAFETY_ERROR_OUT_0
	ESM0_ESM_LVL_EVENT_IN_158	WKUP_PBIST0_DFT_PBIST_SAFETY_ERROR_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_160	RTI0_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_161	RTI1_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_162	RTI15_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_163	WKUP_RTI0_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_164	PBIST0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_165	PBIST1_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_166	GICSS0_AXIM_ERR_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_167	GICSS0_ECC_FATAL_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_170	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_176	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_177	RTI2_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT0_IN_178	RTI3_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_160	RTI0_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_161	RTI1_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_162	RTI15_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_163	WKUP_RTI0_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_164	PBIST0_DFT_PBIST_CPU_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
ESM0	ESM0_ESM_PLS_EVENT1_IN_165	PBIST1_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_166	GICSS0_AXIM_ERR_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_167	GICSS0_ECC_FATAL_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_170	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_176	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_177	RTI2_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT1_IN_178	RTI3_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_160	RTI0_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_161	RTI1_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_162	RTI15_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_163	WKUP_RTI0_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_164	PBIST0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_165	PBIST1_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_166	GICSS0_AXIM_ERR_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_167	GICSS0_ECC_FATAL_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_170	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_176	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_177	RTI2_INTR_WWD_OUT_0
	ESM0_ESM_PLS_EVENT2_IN_178	RTI3_INTR_WWD_OUT_0
WKUP_ESM0	WKUP_ESM0_ESM_LVL_EVENT_IN_0	ESM0_ESM_INT_CFG_LVL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_1	ESM0_ESM_INT_HI_LVL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_2	ESM0_ESM_INT_LOW_LVL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_3	MCU_M4FSS0_RAT_0_EXP_INTR_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_4	MCU_M4FSS0_ECC_AGGR_0_ECC_CORRECTED_ERR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_5	MCU_M4FSS0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_7	PLLFRACF2_SSMOD_16FFT16_LOCKLOSS_IPCFG_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_8	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_9	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_10	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_11	WKUP_VTM0_CORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_12	WKUP_VTM0_UNCORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_14	MCU_ECC_AGGR0_CORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_15	MCU_ECC_AGGR0_UNCORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_16	MCU_MCAN0_MCANSS_ECC_CORR_LVL_INT_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_ESM0	WKUP_ESM0_ESM_LVL_EVENT_IN_17	MCU_MCAN0_MCANSS_ECC_UNCORR_LVL_INT_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_18	MCU_MCAN1_MCANSS_ECC_CORR_LVL_INT_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_19	MCU_MCAN1_MCANSS_ECC_UNCORR_LVL_INT_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_20	WKUP_SAFE_ECC_AGGR0_CORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_21	WKUP_SAFE_ECC_AGGR0_UNCORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_22	PLLFRACF2_SSMOD_16FFT17_LOCKLOSS_IPCFG_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_23	WKUP_ECC_AGGR0_CORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_24	WKUP_ECC_AGGR0_UNCORR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_26	TIMEOUT0_TIMED_OUT_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_26	WKUP_TIMEOUT0_TIMED_OUT_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_27	MCU_TIMEOUT1_TRANS_ERR_LVL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_27	MCU_TIMEOUT0_TRANS_ERR_LVL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_37	MCU_DCC0_INTR_ERR_LEVEL_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_47	MCU_PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_54	PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_55	PLLFRACF2_SSMOD_16FFT1_LOCKLOSS_IPCFG_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_56	PLLFRACF2_SSMOD_16FFT2_LOCKLOSS_IPCFG_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_57	PLLFRACF2_SSMOD_16FFT8_LOCKLOSS_IPCFG_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_58	PLLFRACF2_SSMOD_16FFT12_LOCKLOSS_IPCFG_OUT_0
	WKUP_ESM0_ESM_LVL_EVENT_IN_59	PLLFRACF2_SSMOD_16FFT15_LOCKLOSS_IPCFG_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT0_IN_64	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT0_IN_65	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1
	WKUP_ESM0_ESM_PLS_EVENT0_IN_66	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2
	WKUP_ESM0_ESM_PLS_EVENT0_IN_69	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3
	WKUP_ESM0_ESM_PLS_EVENT0_IN_70	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT0_IN_71	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT0_IN_72	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
	WKUP_ESM0_ESM_PLS_EVENT0_IN_73	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
	WKUP_ESM0_ESM_PLS_EVENT0_IN_76	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
	WKUP_ESM0_ESM_PLS_EVENT0_IN_77	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT0_IN_78	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT0_IN_79	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
	WKUP_ESM0_ESM_PLS_EVENT0_IN_80	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
	WKUP_ESM0_ESM_PLS_EVENT0_IN_81	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_ESM0	WKUP_ESM0_ESM_PLS_EVENT0_IN_82	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT0_IN_85	MCU_RTI0_INTR_WWD_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT0_IN_88	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8
	WKUP_ESM0_ESM_PLS_EVENT0_IN_89	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9
	WKUP_ESM0_ESM_PLS_EVENT0_IN_90	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10
	WKUP_ESM0_ESM_PLS_EVENT0_IN_91	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11
	WKUP_ESM0_ESM_PLS_EVENT1_IN_64	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT1_IN_65	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1
	WKUP_ESM0_ESM_PLS_EVENT1_IN_66	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2
	WKUP_ESM0_ESM_PLS_EVENT1_IN_69	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3
	WKUP_ESM0_ESM_PLS_EVENT1_IN_70	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT1_IN_71	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT1_IN_72	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
	WKUP_ESM0_ESM_PLS_EVENT1_IN_73	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
	WKUP_ESM0_ESM_PLS_EVENT1_IN_76	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
	WKUP_ESM0_ESM_PLS_EVENT1_IN_77	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT1_IN_78	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT1_IN_79	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
	WKUP_ESM0_ESM_PLS_EVENT1_IN_80	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
	WKUP_ESM0_ESM_PLS_EVENT1_IN_81	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
	WKUP_ESM0_ESM_PLS_EVENT1_IN_82	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT1_IN_85	MCU_RTI0_INTR_WWD_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT1_IN_88	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8
	WKUP_ESM0_ESM_PLS_EVENT1_IN_89	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9
	WKUP_ESM0_ESM_PLS_EVENT1_IN_90	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10
	WKUP_ESM0_ESM_PLS_EVENT1_IN_91	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11
	WKUP_ESM0_ESM_PLS_EVENT2_IN_64	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT2_IN_65	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1
	WKUP_ESM0_ESM_PLS_EVENT2_IN_66	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2
	WKUP_ESM0_ESM_PLS_EVENT2_IN_69	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3
	WKUP_ESM0_ESM_PLS_EVENT2_IN_70	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT2_IN_71	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT2_IN_72	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
	WKUP_ESM0_ESM_PLS_EVENT2_IN_73	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_ESM0	WKUP_ESM0_ESM_PLS_EVENT2_IN_76	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
	WKUP_ESM0_ESM_PLS_EVENT2_IN_77	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT2_IN_78	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT2_IN_79	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1
	WKUP_ESM0_ESM_PLS_EVENT2_IN_80	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2
	WKUP_ESM0_ESM_PLS_EVENT2_IN_81	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3
	WKUP_ESM0_ESM_PLS_EVENT2_IN_82	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4
	WKUP_ESM0_ESM_PLS_EVENT2_IN_85	MCU_RTI0_INTR_WWD_OUT_0
	WKUP_ESM0_ESM_PLS_EVENT2_IN_88	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8
	WKUP_ESM0_ESM_PLS_EVENT2_IN_89	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9
	WKUP_ESM0_ESM_PLS_EVENT2_IN_90	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10
	WKUP_ESM0_ESM_PLS_EVENT2_IN_91	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11
GICSS0	GICSS0_PPI0_0_IN_18	A53SS0_CTIIRQ1_OUT_0
	GICSS0_PPI0_0_IN_19	A53SS0_CTIIRQ2_OUT_0
	GICSS0_PPI0_0_IN_20	A53SS0_CTIIRQ3_OUT_0
	GICSS0_PPI0_0_IN_22	A53SS0_COMMIRQ0_OUT_0
	GICSS0_PPI0_0_IN_23	A53SS0_PMUIRQ0_OUT_0
	GICSS0_PPI0_0_IN_24	A53SS0_CTIIRQ0_OUT_0
	GICSS0_PPI0_0_IN_25	A53SS0_VCPUMNTIRQ0_OUT_0
	GICSS0_PPI0_0_IN_26	A53SS0_CNTHPIRQ0_OUT_0
	GICSS0_PPI0_0_IN_27	A53SS0_CNTVIRQ0_OUT_0
	GICSS0_PPI0_0_IN_29	A53SS0_CNTPSIRQ0_OUT_0
	GICSS0_PPI0_0_IN_30	A53SS0_CNTPNSIRQ0_OUT_0
	GICSS0_PPI0_1_IN_17	A53SS0_CTIIRQ0_OUT_0
	GICSS0_PPI0_1_IN_19	A53SS0_CTIIRQ2_OUT_0
	GICSS0_PPI0_1_IN_20	A53SS0_CTIIRQ3_OUT_0
	GICSS0_PPI0_1_IN_22	A53SS0_COMMIRQ1_OUT_0
	GICSS0_PPI0_1_IN_23	A53SS0_PMUIRQ1_OUT_0
	GICSS0_PPI0_1_IN_24	A53SS0_CTIIRQ1_OUT_0
	GICSS0_PPI0_1_IN_25	A53SS0_VCPUMNTIRQ1_OUT_0
	GICSS0_PPI0_1_IN_26	A53SS0_CNTHPIRQ1_OUT_0
	GICSS0_PPI0_1_IN_27	A53SS0_CNTVIRQ1_OUT_0
	GICSS0_PPI0_1_IN_29	A53SS0_CNTPSIRQ1_OUT_0
	GICSS0_PPI0_1_IN_30	A53SS0_CNTPNSIRQ1_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_PPI0_2_IN_17	A53SS0_CTIIRQ0_OUT_0
	GICSS0_PPI0_2_IN_18	A53SS0_CTIIRQ1_OUT_0
	GICSS0_PPI0_2_IN_20	A53SS0_CTIIRQ3_OUT_0
	GICSS0_PPI0_2_IN_22	A53SS0_COMMIRQ2_OUT_0
	GICSS0_PPI0_2_IN_23	A53SS0_PMUIRQ2_OUT_0
	GICSS0_PPI0_2_IN_24	A53SS0_CTIIRQ2_OUT_0
	GICSS0_PPI0_2_IN_25	A53SS0_VCPUMNTIRQ2_OUT_0
	GICSS0_PPI0_2_IN_26	A53SS0_CNTHPIRQ2_OUT_0
	GICSS0_PPI0_2_IN_27	A53SS0_CNTVIRQ2_OUT_0
	GICSS0_PPI0_2_IN_29	A53SS0_CNTPSIRQ2_OUT_0
	GICSS0_PPI0_2_IN_30	A53SS0_CNTPNSIRQ2_OUT_0
	GICSS0_PPI0_3_IN_17	A53SS0_CTIIRQ0_OUT_0
	GICSS0_PPI0_3_IN_18	A53SS0_CTIIRQ1_OUT_0
	GICSS0_PPI0_3_IN_19	A53SS0_CTIIRQ2_OUT_0
	GICSS0_PPI0_3_IN_22	A53SS0_COMMIRQ3_OUT_0
	GICSS0_PPI0_3_IN_23	A53SS0_PMUIRQ3_OUT_0
	GICSS0_PPI0_3_IN_24	A53SS0_CTIIRQ3_OUT_0
	GICSS0_PPI0_3_IN_25	A53SS0_VCPUMNTIRQ3_OUT_0
	GICSS0_PPI0_3_IN_26	A53SS0_CNTHPIRQ3_OUT_0
	GICSS0_PPI0_3_IN_27	A53SS0_CNTVIRQ3_OUT_0
	GICSS0_PPI0_3_IN_29	A53SS0_CNTPSIRQ3_OUT_0
	GICSS0_PPI0_3_IN_30	A53SS0_CNTPNSIRQ3_OUT_0
	GICSS0_SPI_IN_32	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0
	GICSS0_SPI_IN_33	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1
	GICSS0_SPI_IN_34	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2
	GICSS0_SPI_IN_35	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3
	GICSS0_SPI_IN_36	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4
	GICSS0_SPI_IN_37	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5
	GICSS0_SPI_IN_38	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6
	GICSS0_SPI_IN_39	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7
	GICSS0_SPI_IN_40	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8
	GICSS0_SPI_IN_41	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9
	GICSS0_SPI_IN_42	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10
	GICSS0_SPI_IN_43	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_44	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12
	GICSS0_SPI_IN_45	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13
	GICSS0_SPI_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14
	GICSS0_SPI_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15
	GICSS0_SPI_IN_48	CMP_EVENT_INTROUTER0_OUTP_OUT_0
	GICSS0_SPI_IN_49	CMP_EVENT_INTROUTER0_OUTP_OUT_1
	GICSS0_SPI_IN_50	CMP_EVENT_INTROUTER0_OUTP_OUT_2
	GICSS0_SPI_IN_51	CMP_EVENT_INTROUTER0_OUTP_OUT_3
	GICSS0_SPI_IN_52	CMP_EVENT_INTROUTER0_OUTP_OUT_4
	GICSS0_SPI_IN_53	CMP_EVENT_INTROUTER0_OUTP_OUT_5
	GICSS0_SPI_IN_54	CMP_EVENT_INTROUTER0_OUTP_OUT_6
	GICSS0_SPI_IN_55	CMP_EVENT_INTROUTER0_OUTP_OUT_7
	GICSS0_SPI_IN_56	CMP_EVENT_INTROUTER0_OUTP_OUT_8
	GICSS0_SPI_IN_57	CMP_EVENT_INTROUTER0_OUTP_OUT_9
	GICSS0_SPI_IN_58	CMP_EVENT_INTROUTER0_OUTP_OUT_10
	GICSS0_SPI_IN_59	CMP_EVENT_INTROUTER0_OUTP_OUT_11
	GICSS0_SPI_IN_60	CMP_EVENT_INTROUTER0_OUTP_OUT_12
	GICSS0_SPI_IN_61	CMP_EVENT_INTROUTER0_OUTP_OUT_13
	GICSS0_SPI_IN_62	CMP_EVENT_INTROUTER0_OUTP_OUT_14
	GICSS0_SPI_IN_63	CMP_EVENT_INTROUTER0_OUTP_OUT_15
	GICSS0_SPI_IN_64	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_0
	GICSS0_SPI_IN_65	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_1
	GICSS0_SPI_IN_66	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_2
	GICSS0_SPI_IN_67	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_3
	GICSS0_SPI_IN_68	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_4
	GICSS0_SPI_IN_69	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_5
	GICSS0_SPI_IN_70	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_6
	GICSS0_SPI_IN_71	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_7
	GICSS0_SPI_IN_72	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_8
	GICSS0_SPI_IN_73	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_9
	GICSS0_SPI_IN_74	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_10
	GICSS0_SPI_IN_75	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_11
	GICSS0_SPI_IN_76	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_12
	GICSS0_SPI_IN_77	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_13

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_78	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_14
	GICSS0_SPI_IN_79	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_15
	GICSS0_SPI_IN_80	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_16
	GICSS0_SPI_IN_81	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_17
	GICSS0_SPI_IN_82	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_18
	GICSS0_SPI_IN_83	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_19
	GICSS0_SPI_IN_84	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_20
	GICSS0_SPI_IN_85	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_21
	GICSS0_SPI_IN_86	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_22
	GICSS0_SPI_IN_87	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_23
	GICSS0_SPI_IN_88	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_24
	GICSS0_SPI_IN_89	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_25
	GICSS0_SPI_IN_90	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_26
	GICSS0_SPI_IN_91	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_27
	GICSS0_SPI_IN_92	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_28
	GICSS0_SPI_IN_93	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_29
	GICSS0_SPI_IN_94	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_30
	GICSS0_SPI_IN_95	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_31
	GICSS0_SPI_IN_96	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_32
	GICSS0_SPI_IN_97	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_33
	GICSS0_SPI_IN_98	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_34
	GICSS0_SPI_IN_99	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_35
	GICSS0_SPI_IN_100	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_36
	GICSS0_SPI_IN_101	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_37
	GICSS0_SPI_IN_102	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_38
	GICSS0_SPI_IN_103	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_39
	GICSS0_SPI_IN_104	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0
	GICSS0_SPI_IN_105	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1
	GICSS0_SPI_IN_106	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2
	GICSS0_SPI_IN_107	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3
	GICSS0_SPI_IN_108	MAILBOX0_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_0
	GICSS0_SPI_IN_109	MAILBOX0_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_1
	GICSS0_SPI_IN_112	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_4
	GICSS0_SPI_IN_113	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_5

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_114	MMCSD2_EMMCSDSS_INTR_OUT_0
	GICSS0_SPI_IN_115	MMCSD1_EMMCSDSS_INTR_OUT_0
	GICSS0_SPI_IN_116	DSS0_DISPC_INTR_REQ_0_OUT_0
	GICSS0_SPI_IN_117	DSS0_DISPC_INTR_REQ_1_OUT_0
	GICSS0_SPI_IN_118	GPU0_GPU_OS_IRQ_OUT_0
	GICSS0_SPI_IN_119	GPU0_GPU_OS_IRQ_OUT_1
	GICSS0_SPI_IN_120	ICSSM0_PR1_HOST_INTR_PEND_OUT_0
	GICSS0_SPI_IN_121	ICSSM0_PR1_HOST_INTR_PEND_OUT_1
	GICSS0_SPI_IN_122	ICSSM0_PR1_HOST_INTR_PEND_OUT_2
	GICSS0_SPI_IN_123	ICSSM0_PR1_HOST_INTR_PEND_OUT_3
	GICSS0_SPI_IN_124	ICSSM0_PR1_HOST_INTR_PEND_OUT_4
	GICSS0_SPI_IN_125	ICSSM0_PR1_HOST_INTR_PEND_OUT_5
	GICSS0_SPI_IN_126	ICSSM0_PR1_HOST_INTR_PEND_OUT_6
	GICSS0_SPI_IN_127	ICSSM0_PR1_HOST_INTR_PEND_OUT_7
	GICSS0_SPI_IN_128	DCC0_INTR_DONE_LEVEL_OUT_0
	GICSS0_SPI_IN_128	DCC1_INTR_DONE_LEVEL_OUT_0
	GICSS0_SPI_IN_128	DCC2_INTR_DONE_LEVEL_OUT_0
	GICSS0_SPI_IN_128	DCC3_INTR_DONE_LEVEL_OUT_0
	GICSS0_SPI_IN_128	DCC4_INTR_DONE_LEVEL_OUT_0
	GICSS0_SPI_IN_128	DCC5_INTR_DONE_LEVEL_OUT_0
	GICSS0_SPI_IN_128	DCC6_INTR_DONE_LEVEL_OUT_0
	GICSS0_SPI_IN_129	CTRL_MMR0_ACCESS_ERR_OUT_0
	GICSS0_SPI_IN_129	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0
	GICSS0_SPI_IN_129	PADCFG_CTRL0_ACCESS_ERR_OUT_0
	GICSS0_SPI_IN_129	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0
	GICSS0_SPI_IN_129	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
	GICSS0_SPI_IN_132	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0
	GICSS0_SPI_IN_133	CBASS0_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	CBASS_IPCSS0_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_133	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_133	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0
	GICSS0_SPI_IN_134	CPSW0_EVNT_PEND_OUT_0
	GICSS0_SPI_IN_135	CPSW0_MDIO_PEND_OUT_0
	GICSS0_SPI_IN_136	CPSW0_STAT_PEND_OUT_0
	GICSS0_SPI_IN_138	GPMC0_GPMC_SINTERRUPT_OUT_0
	GICSS0_SPI_IN_139	MCU_I2C0_POINTRPEND_OUT_0
	GICSS0_SPI_IN_145	ECAP0_ECAP_INT_OUT_0
	GICSS0_SPI_IN_146	ECAP1_ECAP_INT_OUT_0
	GICSS0_SPI_IN_147	ECAP2_ECAP_INT_OUT_0
	GICSS0_SPI_IN_148	EQEP0_EQEP_INT_OUT_0
	GICSS0_SPI_IN_149	EQEP1_EQEP_INT_OUT_0
	GICSS0_SPI_IN_150	EQEP2_EQEP_INT_OUT_0
	GICSS0_SPI_IN_151	DDR16SS0_DDRSS_CONTROLLER_OUT_0
	GICSS0_SPI_IN_152	TIMER0_INTR_PEND_OUT_0
	GICSS0_SPI_IN_153	TIMER1_INTR_PEND_OUT_0
	GICSS0_SPI_IN_154	TIMER2_INTR_PEND_OUT_0
	GICSS0_SPI_IN_155	TIMER3_INTR_PEND_OUT_0
	GICSS0_SPI_IN_156	TIMER4_INTR_PEND_OUT_0
	GICSS0_SPI_IN_157	TIMER5_INTR_PEND_OUT_0
	GICSS0_SPI_IN_158	TIMER6_INTR_PEND_OUT_0
	GICSS0_SPI_IN_159	TIMER7_INTR_PEND_OUT_0
	GICSS0_SPI_IN_160	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0
	GICSS0_SPI_IN_161	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0
	GICSS0_SPI_IN_164	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0
	GICSS0_SPI_IN_165	MMCSD0_EMMCSDSS_INTR_OUT_0
	GICSS0_SPI_IN_166	MCRC64_0_INT_MCRC_OUT_0
	GICSS0_SPI_IN_167	ICSSM0_ISO_RESET_PROTCOL_ACK_OUT_0
	GICSS0_SPI_IN_171	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0
	GICSS0_SPI_IN_172	DDR16SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0
	GICSS0_SPI_IN_173	CSI_RX_IF0_CSI_IRQ_OUT_0
	GICSS0_SPI_IN_174	CSI_RX_IF0_CSI_LEVEL_OUT_0
	GICSS0_SPI_IN_175	CSI_RX_IF0_CSI_ERR_IRQ_OUT_0
	GICSS0_SPI_IN_177	DDPA0_DDPA_INTR_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_178	RTI15_INTR_WWD_OUT_0
	GICSS0_SPI_IN_180	ESM0_ESM_INT_CFG_LVL_OUT_0
	GICSS0_SPI_IN_181	ESM0_ESM_INT_HI_LVL_OUT_0
	GICSS0_SPI_IN_182	ESM0_ESM_INT_LOW_LVL_OUT_0
	GICSS0_SPI_IN_183	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	GICSS0_SPI_IN_184	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	GICSS0_SPI_IN_185	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	GICSS0_SPI_IN_186	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	GICSS0_SPI_IN_187	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
	GICSS0_SPI_IN_188	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
	GICSS0_SPI_IN_192	MCU_MCRC64_0_INT_MCRC_OUT_0
	GICSS0_SPI_IN_193	I2C0_POINTRPEND_OUT_0
	GICSS0_SPI_IN_194	I2C1_POINTRPEND_OUT_0
	GICSS0_SPI_IN_195	I2C2_POINTRPEND_OUT_0
	GICSS0_SPI_IN_196	I2C3_POINTRPEND_OUT_0
	GICSS0_SPI_IN_197	WKUP_I2C0_POINTRPEND_OUT_0
	GICSS0_SPI_IN_201	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
	GICSS0_SPI_IN_202	DEBUGSS0_CTM_LEVEL_OUT_0
	GICSS0_SPI_IN_203	PSC0_PSC_ALLINT_OUT_0
	GICSS0_SPI_IN_204	MCSPI0_INTR_SPI_OUT_0
	GICSS0_SPI_IN_205	MCSPI1_INTR_SPI_OUT_0
	GICSS0_SPI_IN_206	MCSPI2_INTR_SPI_OUT_0
	GICSS0_SPI_IN_208	MCU_MCSPI0_INTR_SPI_OUT_0
	GICSS0_SPI_IN_209	MCU_MCSPI1_INTR_SPI_OUT_0
	GICSS0_SPI_IN_210	UART0_USART_IRQ_OUT_0
	GICSS0_SPI_IN_211	UART1_USART_IRQ_OUT_0
	GICSS0_SPI_IN_212	UART2_USART_IRQ_OUT_0
	GICSS0_SPI_IN_213	UART3_USART_IRQ_OUT_0
	GICSS0_SPI_IN_214	UART4_USART_IRQ_OUT_0
	GICSS0_SPI_IN_215	UART5_USART_IRQ_OUT_0
	GICSS0_SPI_IN_216	UART6_USART_IRQ_OUT_0
	GICSS0_SPI_IN_217	MCU_UART0_USART_IRQ_OUT_0
	GICSS0_SPI_IN_218	WKUP_UART0_USART_IRQ_OUT_0
	GICSS0_SPI_IN_220	USB0_IRQ_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_221	USB0_IRQ_OUT_1
	GICSS0_SPI_IN_222	USB0_IRQ_OUT_2
	GICSS0_SPI_IN_223	USB0_IRQ_OUT_3
	GICSS0_SPI_IN_224	USB0_IRQ_OUT_4
	GICSS0_SPI_IN_225	USB0_IRQ_OUT_5
	GICSS0_SPI_IN_226	USB0_IRQ_OUT_6
	GICSS0_SPI_IN_227	USB0_IRQ_OUT_7
	GICSS0_SPI_IN_228	USB0_MISC_LEVEL_OUT_0
	GICSS0_SPI_IN_229	EPWM0_EPWM_ETINT_OUT_0
	GICSS0_SPI_IN_230	EPWM0_EPWM_TRIPZINT_OUT_0
	GICSS0_SPI_IN_231	EPWM1_EPWM_ETINT_OUT_0
	GICSS0_SPI_IN_233	EPWM1_EPWM_TRIPZINT_OUT_0
	GICSS0_SPI_IN_234	EPWM2_EPWM_ETINT_OUT_0
	GICSS0_SPI_IN_235	EPWM2_EPWM_TRIPZINT_OUT_0
	GICSS0_SPI_IN_244	ICSSM0_PR1_RX_SOF_INTR_REQ_OUT_0
	GICSS0_SPI_IN_245	ICSSM0_PR1_RX_SOF_INTR_REQ_OUT_1
	GICSS0_SPI_IN_246	ICSSM0_PR1_TX_SOF_INTR_REQ_OUT_0
	GICSS0_SPI_IN_247	ICSSM0_PR1_TX_SOF_INTR_REQ_OUT_1
	GICSS0_SPI_IN_252	RTI0_INTR_WWD_OUT_0
	GICSS0_SPI_IN_253	RTI1_INTR_WWD_OUT_0
	GICSS0_SPI_IN_254	RTI2_INTR_WWD_OUT_0
	GICSS0_SPI_IN_255	RTI3_INTR_WWD_OUT_0
	GICSS0_SPI_IN_256	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
	GICSS0_SPI_IN_258	USB1_IRQ_OUT_0
	GICSS0_SPI_IN_259	USB1_IRQ_OUT_1
	GICSS0_SPI_IN_260	USB1_IRQ_OUT_2
	GICSS0_SPI_IN_261	USB1_IRQ_OUT_3
	GICSS0_SPI_IN_262	USB1_IRQ_OUT_4
	GICSS0_SPI_IN_263	USB1_IRQ_OUT_5
	GICSS0_SPI_IN_264	USB1_IRQ_OUT_6
	GICSS0_SPI_IN_265	USB1_IRQ_OUT_7
	GICSS0_SPI_IN_266	USB1_MISC_LEVEL_OUT_0
	GICSS0_SPI_IN_267	MCASP0_REC_INTR_PEND_OUT_0
	GICSS0_SPI_IN_268	MCASP0_XMIT_INTR_PEND_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
GICSS0	GICSS0_SPI_IN_269	MCASP1_REC_INTR_PEND_OUT_0
	GICSS0_SPI_IN_270	MCASP1_XMIT_INTR_PEND_OUT_0
	GICSS0_SPI_IN_271	MCASP2_REC_INTR_PEND_OUT_0
	GICSS0_SPI_IN_272	MCASP2_XMIT_INTR_PEND_OUT_0
ICSSM0	ICSSM0_PR1_EDC0_LATCH0_IN_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_8
	ICSSM0_PR1_EDC0_LATCH1_IN_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_9
	ICSSM0_PR1_IEP0_CAP_INTR_REQ_IN_0	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_16
	ICSSM0_PR1_IEP0_CAP_INTR_REQ_IN_1	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_17
	ICSSM0_PR1_IEP0_CAP_INTR_REQ_IN_2	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_18
	ICSSM0_PR1_IEP0_CAP_INTR_REQ_IN_3	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_19
	ICSSM0_PR1_IEP0_CAP_INTR_REQ_IN_4	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_20
	ICSSM0_PR1_IEP0_CAP_INTR_REQ_IN_5	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_21
	ICSSM0_PR1_SLV_INTR_IN_0	UART1_USART_IRQ_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_1	MCASP1_XMIT_INTR_PEND_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_2	MCASP1_REC_INTR_PEND_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_3	ECAP1_ECAP_INT_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_4	ECAP2_ECAP_INT_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_5	EPWM2_EPWM_ETINT_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_6	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_12
	ICSSM0_PR1_SLV_INTR_IN_7	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_24
	ICSSM0_PR1_SLV_INTR_IN_8	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_25
	ICSSM0_PR1_SLV_INTR_IN_9	I2C0_POINTRPEND_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_10	ECAP0_ECAP_INT_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_11	EPWM0_EPWM_ETINT_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_12	MCSPI0_INTR_SPI_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_13	EQEP0_EQEP_INT_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_14	EPWM1_EPWM_ETINT_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_15	MCSPI1_INTR_SPI_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_16	EQEP1_EQEP_INT_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_17	EQEP2_EQEP_INT_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_18	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_32
	ICSSM0_PR1_SLV_INTR_IN_19	UART0_USART_IRQ_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_20	UART2_USART_IRQ_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_21	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_80

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
ICSSM0	ICSSM0_PR1_SLV_INTR_IN_22	MCASP0_REC_INTR_PEND_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_23	MCASP0_XMIT_INTR_PEND_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_24	EPWM0_EPWM_TRIPZINT_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_24	EPWM1_EPWM_TRIPZINT_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_24	EPWM2_EPWM_TRIPZINT_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_25	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_33
	ICSSM0_PR1_SLV_INTR_IN_26	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_27	MCASP2_XMIT_INTR_PEND_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_28	MCASP2_REC_INTR_PEND_OUT_0
	ICSSM0_PR1_SLV_INTR_IN_29	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_81
	ICSSM0_PR1_SLV_INTR_IN_30	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_82
	ICSSM0_PR1_SLV_INTR_IN_31	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_83
EPWM0	EPWM0_EPWM_SYNCIN_IN_0	PINFUNCTION_EHRPWM0_SYNCIIN_EHRPWM0_SYNCI_OUT_0
	EPWM0_EPWM_SYNCIN_IN_0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_19
	EPWM0_EPWM_SYNCIN_IN_0	CMP_EVENT_INTROUTER0_OUTP_OUT_32
	EPWM0_EPWM_SYNCIN_IN_0	ICSSM0_PR1_HOST_INTR_PEND_OUT_6
EPWM1	EPWM1_EPWM_SYNCIN_IN_0	EPWM0_EPWM_SYNCOUT_OUT_0
EPWM2	EPWM2_EPWM_SYNCIN_IN_0	EPWM1_EPWM_SYNCOUT_OUT_0
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_INTR_IN_0	MCU_CTRL_MMR0_IPC_SET0_IPC_SET_IPCFG_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_4	WKUP_R5FSS0_CORE0_EXP_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_5	WKUP_R5FSS0_COMMON0_COMMRX_LEVEL_0_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_6	WKUP_R5FSS0_COMMON0_COMMTX_LEVEL_0_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_7	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_6
	WKUP_R5FSS0_CORE0_INTR_IN_8	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_72
	WKUP_R5FSS0_CORE0_INTR_IN_9	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_73
	WKUP_R5FSS0_CORE0_INTR_IN_10	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_74
	WKUP_R5FSS0_CORE0_INTR_IN_11	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_75
	WKUP_R5FSS0_CORE0_INTR_IN_12	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_76
	WKUP_R5FSS0_CORE0_INTR_IN_13	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_77
	WKUP_R5FSS0_CORE0_INTR_IN_14	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_78
	WKUP_R5FSS0_CORE0_INTR_IN_15	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_79
	WKUP_R5FSS0_CORE0_INTR_IN_16	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_17	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_18	MCU_GPIO0_GPIO_LVL_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_INTR_IN_23	WKUP_ICEMELTER0_PSC_FORCE_POWER_ON_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_24	DSS0_DISPC_INTR_REQ_0_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_25	DSS0_DISPC_INTR_REQ_1_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_27	WKUP_DEEPSLEEP_SOURCES0_WAKEUP_EVENT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_28	WKUP_TIMER0_TIMER_CLKSTOP_WAKEUP_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_29	WKUP_TIMER1_TIMER_CLKSTOP_WAKEUP_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_30	WKUP_RTI0_INTR_WWD_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_32	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_33	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_34	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2
	WKUP_R5FSS0_CORE0_INTR_IN_35	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3
	WKUP_R5FSS0_CORE0_INTR_IN_36	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4
	WKUP_R5FSS0_CORE0_INTR_IN_37	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5
	WKUP_R5FSS0_CORE0_INTR_IN_38	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6
	WKUP_R5FSS0_CORE0_INTR_IN_39	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7
	WKUP_R5FSS0_CORE0_INTR_IN_40	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8
	WKUP_R5FSS0_CORE0_INTR_IN_41	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9
	WKUP_R5FSS0_CORE0_INTR_IN_42	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10
	WKUP_R5FSS0_CORE0_INTR_IN_43	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11
	WKUP_R5FSS0_CORE0_INTR_IN_44	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12
	WKUP_R5FSS0_CORE0_INTR_IN_45	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13
	WKUP_R5FSS0_CORE0_INTR_IN_46	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14
	WKUP_R5FSS0_CORE0_INTR_IN_47	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15
	WKUP_R5FSS0_CORE0_INTR_IN_48	CMP_EVENT_INTROUTER0_OUTP_OUT_16
	WKUP_R5FSS0_CORE0_INTR_IN_49	CMP_EVENT_INTROUTER0_OUTP_OUT_17
	WKUP_R5FSS0_CORE0_INTR_IN_50	CMP_EVENT_INTROUTER0_OUTP_OUT_18
	WKUP_R5FSS0_CORE0_INTR_IN_51	CMP_EVENT_INTROUTER0_OUTP_OUT_19
	WKUP_R5FSS0_CORE0_INTR_IN_52	CMP_EVENT_INTROUTER0_OUTP_OUT_20
	WKUP_R5FSS0_CORE0_INTR_IN_53	CMP_EVENT_INTROUTER0_OUTP_OUT_21
	WKUP_R5FSS0_CORE0_INTR_IN_54	CMP_EVENT_INTROUTER0_OUTP_OUT_22
	WKUP_R5FSS0_CORE0_INTR_IN_55	CMP_EVENT_INTROUTER0_OUTP_OUT_23
	WKUP_R5FSS0_CORE0_INTR_IN_56	GPIO0_GPIO_BANK_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_57	GPIO0_GPIO_BANK_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_58	WKUP_R5FSS0_CORE0_PMU_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_INTR_IN_59	WKUP_R5FSS0_CORE0_VALFIQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_60	WKUP_R5FSS0_CORE0_VALIRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_61	USB0_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_62	USB1_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_64	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_40
	WKUP_R5FSS0_CORE0_INTR_IN_65	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_41
	WKUP_R5FSS0_CORE0_INTR_IN_66	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_42
	WKUP_R5FSS0_CORE0_INTR_IN_67	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_43
	WKUP_R5FSS0_CORE0_INTR_IN_68	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_44
	WKUP_R5FSS0_CORE0_INTR_IN_69	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_45
	WKUP_R5FSS0_CORE0_INTR_IN_70	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_46
	WKUP_R5FSS0_CORE0_INTR_IN_71	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_47
	WKUP_R5FSS0_CORE0_INTR_IN_72	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_48
	WKUP_R5FSS0_CORE0_INTR_IN_73	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_49
	WKUP_R5FSS0_CORE0_INTR_IN_74	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_50
	WKUP_R5FSS0_CORE0_INTR_IN_75	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_51
	WKUP_R5FSS0_CORE0_INTR_IN_76	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_52
	WKUP_R5FSS0_CORE0_INTR_IN_77	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_53
	WKUP_R5FSS0_CORE0_INTR_IN_78	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_54
	WKUP_R5FSS0_CORE0_INTR_IN_79	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_55
	WKUP_R5FSS0_CORE0_INTR_IN_80	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_56
	WKUP_R5FSS0_CORE0_INTR_IN_81	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_57
	WKUP_R5FSS0_CORE0_INTR_IN_82	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_58
	WKUP_R5FSS0_CORE0_INTR_IN_83	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_59
	WKUP_R5FSS0_CORE0_INTR_IN_84	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_60
	WKUP_R5FSS0_CORE0_INTR_IN_85	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_61
	WKUP_R5FSS0_CORE0_INTR_IN_86	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_62
	WKUP_R5FSS0_CORE0_INTR_IN_87	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_63
	WKUP_R5FSS0_CORE0_INTR_IN_88	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_64
	WKUP_R5FSS0_CORE0_INTR_IN_89	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_65
	WKUP_R5FSS0_CORE0_INTR_IN_90	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_66
	WKUP_R5FSS0_CORE0_INTR_IN_91	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_67
	WKUP_R5FSS0_CORE0_INTR_IN_92	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_68
	WKUP_R5FSS0_CORE0_INTR_IN_93	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_69

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_INTR_IN_94	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_70
	WKUP_R5FSS0_CORE0_INTR_IN_95	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_71
	WKUP_R5FSS0_CORE0_INTR_IN_97	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_103	GPMC0_GPMC_SINTERRUPT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_104	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_105	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_106	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2
	WKUP_R5FSS0_CORE0_INTR_IN_107	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3
	WKUP_R5FSS0_CORE0_INTR_IN_108	MCU_DCC0_INTR_DONE_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_109	DCC0_INTR_DONE_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_109	DCC1_INTR_DONE_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_109	DCC2_INTR_DONE_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_109	DCC3_INTR_DONE_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_109	DCC4_INTR_DONE_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_109	DCC5_INTR_DONE_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_109	DCC6_INTR_DONE_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_110	MCU_M4FSS0_RAT_0_EXP_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_113	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_114	PBIST0_DFT_PBIST_CPU_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_115	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_116	PBIST1_DFT_PBIST_CPU_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_119	MCRC64_0_INT_MCRC_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_120	ICSSM0_PR1_HOST_INTR_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_121	ICSSM0_PR1_HOST_INTR_PEND_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_122	ICSSM0_PR1_HOST_INTR_PEND_OUT_2
	WKUP_R5FSS0_CORE0_INTR_IN_123	ICSSM0_PR1_HOST_INTR_PEND_OUT_3
	WKUP_R5FSS0_CORE0_INTR_IN_124	ICSSM0_PR1_HOST_INTR_PEND_OUT_4
	WKUP_R5FSS0_CORE0_INTR_IN_125	ICSSM0_PR1_HOST_INTR_PEND_OUT_5
	WKUP_R5FSS0_CORE0_INTR_IN_126	ICSSM0_PR1_HOST_INTR_PEND_OUT_6
	WKUP_R5FSS0_CORE0_INTR_IN_127	ICSSM0_PR1_HOST_INTR_PEND_OUT_7
	WKUP_R5FSS0_CORE0_INTR_IN_128	CTRL_MMR0_ACCESS_ERR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_128	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_128	PADCFG_CTRL0_ACCESS_ERR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_128	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_INTR_IN_128	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_134	CPSW0_EVNT_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_135	CPSW0_MDIO_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_136	CPSW0_STAT_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_138	WKUP_TIMER0_INTR_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_139	WKUP_TIMER1_INTR_PEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_140	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_141	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_142	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_143	WKUP_I2C0_CLKSTOP_WAKEUP_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_144	WKUP_UART0_CLKSTOP_WAKEUP_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_145	WKUP_PSC0_PSC_ALLINT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_146	PSC0_PSC_ALLINT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS0_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_147	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_IPCSS0_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_147	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_147	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_148	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_148	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_151	DDR16SS0_DDRSS_CONTROLLER_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_152	TIMEOUT0_TIMED_OUT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_152	WKUP_TIMEOUT0_TIMED_OUT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_153	MCU_TIMEOUT1_TRANS_ERR_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_153	MCU_TIMEOUT0_TRANS_ERR_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_154	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_155	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_156	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_2
	WKUP_R5FSS0_CORE0_INTR_IN_157	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_3
	WKUP_R5FSS0_CORE0_INTR_IN_161	MMCSD0_EMMCSDSS_INTR_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_INTR_IN_162	MMCSD1_EMMCSDSS_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_163	MMCSD2_EMMCSDSS_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_164	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_167	ESM0_ESM_INT_CFG_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_168	ESM0_ESM_INT_HI_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_169	ESM0_ESM_INT_LOW_LVL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_170	ICSSM0_ISO_RESET_PROTCOL_ACK_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_171	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_175	WKUP_R5FSS0_CORE0_CTI_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_177	DDPA0_DDPA_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_181	DDR16SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_183	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_184	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_185	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_186	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_187	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_188	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_190	WKUP_I2C0_POINTRPEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_192	MCU_MCRC64_0_INT_MCRC_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_193	I2C0_POINTRPEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_194	I2C1_POINTRPEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_195	I2C2_POINTRPEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_196	I2C3_POINTRPEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_197	MCU_I2C0_POINTRPEND_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_201	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_202	DEBUGSS0_CTM_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_203	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_204	MCSPI0_INTR_SPI_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_205	MCSPI1_INTR_SPI_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_206	MCSPI2_INTR_SPI_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_207	MCU_MCSPI0_INTR_SPI_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_208	MCU_MCSPI1_INTR_SPI_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_210	UART0_USART_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_211	UART1_USART_IRQ_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_INTR_IN_212	UART2_USART_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_213	UART3_USART_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_214	UART4_USART_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_215	UART5_USART_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_216	UART6_USART_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_217	MCU_UART0_USART_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_219	WKUP_UART0_USART_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_220	USB0_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_221	USB0_IRQ_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_222	USB0_IRQ_OUT_2
	WKUP_R5FSS0_CORE0_INTR_IN_223	USB0_IRQ_OUT_3
	WKUP_R5FSS0_CORE0_INTR_IN_224	USB0_IRQ_OUT_4
	WKUP_R5FSS0_CORE0_INTR_IN_225	USB0_IRQ_OUT_5
	WKUP_R5FSS0_CORE0_INTR_IN_226	USB0_IRQ_OUT_6
	WKUP_R5FSS0_CORE0_INTR_IN_227	USB0_IRQ_OUT_7
	WKUP_R5FSS0_CORE0_INTR_IN_228	USB0_MISC_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_230	USB1_IRQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_231	USB1_IRQ_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_232	USB1_IRQ_OUT_2
	WKUP_R5FSS0_CORE0_INTR_IN_233	USB1_IRQ_OUT_3
	WKUP_R5FSS0_CORE0_INTR_IN_234	USB1_IRQ_OUT_4
	WKUP_R5FSS0_CORE0_INTR_IN_235	USB1_IRQ_OUT_5
	WKUP_R5FSS0_CORE0_INTR_IN_236	USB1_IRQ_OUT_6
	WKUP_R5FSS0_CORE0_INTR_IN_237	USB1_IRQ_OUT_7
	WKUP_R5FSS0_CORE0_INTR_IN_238	USB1_MISC_LEVEL_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_244	ICSSM0_PR1_RX_SOF_INTR_REQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_245	ICSSM0_PR1_RX_SOF_INTR_REQ_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_246	ICSSM0_PR1_TX_SOF_INTR_REQ_OUT_0
	WKUP_R5FSS0_CORE0_INTR_IN_247	ICSSM0_PR1_TX_SOF_INTR_REQ_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_254	MAILBOX0_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_1
	WKUP_R5FSS0_CORE0_INTR_IN_255	MAILBOX0_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_3
WKUP_DEEPSLEEP_SOURCES0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_0	WKUP_I2C0_CLKSTOP_WAKEUP_OUT_0
	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_1	WKUP_UART0_CLKSTOP_WAKEUP_OUT_0
	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_2	MCU_GPIO0_GPIO_LVL_OUT_0

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
WKUP_DEEPSLEEP_SOURCES0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_3	WKUP_ICEMELTER0_PSC_FORCE_POWER_ON_OUT_0
	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_5	WKUP_TIMER0_TIMER_CLKSTOP_WAKEUP_OUT_0
	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_6	WKUP_TIMER1_TIMER_CLKSTOP_WAKEUP_OUT_0
	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_7	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0
	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_9	USB0_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0
	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_10	USB1_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0
PDMA2	PDMA2_MCASP_MAIN_0_RX_IN_0	MCASP0_REC_DMA_EVENT_REQ_OUT_0
	PDMA2_MCASP_MAIN_0_TX_IN_0	MCASP0_XMIT_DMA_EVENT_REQ_OUT_0
	PDMA2_MCASP_MAIN_1_RX_IN_0	MCASP1_REC_DMA_EVENT_REQ_OUT_0
	PDMA2_MCASP_MAIN_1_TX_IN_0	MCASP1_XMIT_DMA_EVENT_REQ_OUT_0
	PDMA2_MCASP_MAIN_2_RX_IN_0	MCASP2_REC_DMA_EVENT_REQ_OUT_0
	PDMA2_MCASP_MAIN_2_TX_IN_0	MCASP2_XMIT_DMA_EVENT_REQ_OUT_0
PDMA0	PDMA0_MCANSS_MAIN_0_FE_IN_0	MCAN0_MCANSS_FE_OUT_0
	PDMA0_MCANSS_MAIN_0_FE_IN_1	MCAN0_MCANSS_FE_OUT_1
	PDMA0_MCANSS_MAIN_0_FE_IN_2	MCAN0_MCANSS_FE_OUT_2
	PDMA0_MCANSS_MAIN_0_TX_IN_0	MCAN0_MCANSS_TX_DMA_OUT_0
	PDMA0_MCANSS_MAIN_0_TX_IN_1	MCAN0_MCANSS_TX_DMA_OUT_1
	PDMA0_MCANSS_MAIN_0_TX_IN_2	MCAN0_MCANSS_TX_DMA_OUT_2
	PDMA0_SPI_MAIN_0_RX_IN_0	MCSPI0_DMA_READ_EVENT_OUT_0
	PDMA0_SPI_MAIN_0_RX_IN_1	MCSPI0_DMA_READ_EVENT_OUT_1
	PDMA0_SPI_MAIN_0_RX_IN_2	MCSPI0_DMA_READ_EVENT_OUT_2
	PDMA0_SPI_MAIN_0_RX_IN_3	MCSPI0_DMA_READ_EVENT_OUT_3
	PDMA0_SPI_MAIN_0_TX_IN_0	MCSPI0_DMA_WRITE_EVENT_OUT_0
	PDMA0_SPI_MAIN_0_TX_IN_1	MCSPI0_DMA_WRITE_EVENT_OUT_1
	PDMA0_SPI_MAIN_0_TX_IN_2	MCSPI0_DMA_WRITE_EVENT_OUT_2
	PDMA0_SPI_MAIN_0_TX_IN_3	MCSPI0_DMA_WRITE_EVENT_OUT_3
	PDMA0_SPI_MAIN_1_RX_IN_0	MCSPI1_DMA_READ_EVENT_OUT_0
	PDMA0_SPI_MAIN_1_RX_IN_1	MCSPI1_DMA_READ_EVENT_OUT_1
	PDMA0_SPI_MAIN_1_RX_IN_2	MCSPI1_DMA_READ_EVENT_OUT_2
	PDMA0_SPI_MAIN_1_RX_IN_3	MCSPI1_DMA_READ_EVENT_OUT_3
	PDMA0_SPI_MAIN_1_TX_IN_0	MCSPI1_DMA_WRITE_EVENT_OUT_0
	PDMA0_SPI_MAIN_1_TX_IN_1	MCSPI1_DMA_WRITE_EVENT_OUT_1
	PDMA0_SPI_MAIN_1_TX_IN_2	MCSPI1_DMA_WRITE_EVENT_OUT_2
	PDMA0_SPI_MAIN_1_TX_IN_3	MCSPI1_DMA_WRITE_EVENT_OUT_3

Table 1-8. Interrupts (Inputs) (continued)

Instance	Interrupt Input Line	Source Interrupt
PDMA0	PDMA0_SPI_MAIN_2_RX_IN_0	MCSPI2_DMA_READ_EVENT_OUT_0
	PDMA0_SPI_MAIN_2_RX_IN_1	MCSPI2_DMA_READ_EVENT_OUT_1
	PDMA0_SPI_MAIN_2_RX_IN_2	MCSPI2_DMA_READ_EVENT_OUT_2
	PDMA0_SPI_MAIN_2_RX_IN_3	MCSPI2_DMA_READ_EVENT_OUT_3
	PDMA0_SPI_MAIN_2_TX_IN_0	MCSPI2_DMA_WRITE_EVENT_OUT_0
	PDMA0_SPI_MAIN_2_TX_IN_1	MCSPI2_DMA_WRITE_EVENT_OUT_1
	PDMA0_SPI_MAIN_2_TX_IN_2	MCSPI2_DMA_WRITE_EVENT_OUT_2
	PDMA0_SPI_MAIN_2_TX_IN_3	MCSPI2_DMA_WRITE_EVENT_OUT_3
PDMA1	PDMA1_USART_MAIN_0_RX_IN_0	UART0_USART_DMA_OUT_1
	PDMA1_USART_MAIN_0_TX_IN_0	UART0_USART_DMA_OUT_0
	PDMA1_USART_MAIN_1_RX_IN_0	UART1_USART_DMA_OUT_1
	PDMA1_USART_MAIN_1_TX_IN_0	UART1_USART_DMA_OUT_0
	PDMA1_USART_MAIN_2_RX_IN_0	UART2_USART_DMA_OUT_1
	PDMA1_USART_MAIN_2_TX_IN_0	UART2_USART_DMA_OUT_0
	PDMA1_USART_MAIN_3_RX_IN_0	UART3_USART_DMA_OUT_1
	PDMA1_USART_MAIN_3_TX_IN_0	UART3_USART_DMA_OUT_0
	PDMA1_USART_MAIN_4_RX_IN_0	UART4_USART_DMA_OUT_1
	PDMA1_USART_MAIN_4_TX_IN_0	UART4_USART_DMA_OUT_0
	PDMA1_USART_MAIN_5_RX_IN_0	UART5_USART_DMA_OUT_1
	PDMA1_USART_MAIN_5_TX_IN_0	UART5_USART_DMA_OUT_0
	PDMA1_USART_MAIN_6_RX_IN_0	UART6_USART_DMA_OUT_1
	PDMA1_USART_MAIN_6_TX_IN_0	UART6_USART_DMA_OUT_0
USB0	USB0_TRACE_INEP_PKT_BUFF_AVAIL_IN_0	DEBUGSS0_DAVDMA_LEVEL_OUT_0
USB1	USB1_TRACE_INEP_PKT_BUFF_AVAIL_IN_0	DEBUGSS0_DAVDMA_LEVEL_OUT_0

1.1.9 Interrupts (Outputs)

Table 1-9. Interrupts (Outputs)

Instance	Interrupt Output Line	Destination Interrupt
PINFUNCTION_CP_GEMAC_CPTS0_HW1TSPUSHin	PINFUNCTION_CP_GEMAC_CPTS0_HW1TSPUSHIN_CP_GEMAC_CPTS0_HW1TSPUSH_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_12
PINFUNCTION_CP_GEMAC_CPTS0_HW2TSPUSHin	PINFUNCTION_CP_GEMAC_CPTS0_HW2TSPUSHIN_CP_GEMAC_CPTS0_HW2TSPUSH_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_13
PINFUNCTION_EHRPWM0_SYNCIin	PINFUNCTION_EHRPWM0_SYNCIIN_EHRPWM0_SYNCI_OUT_0	EPWM0_EPWM_SYNCIN_IN_0
PINFUNCTION_EXTINTnin	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0	GICSS0_SPI_IN_256
	PINFUNCTION_EXTINTNIN_EXTINTN_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_203
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_OUTP_OUT_0	GICSS0_SPI_IN_48
	CMP_EVENT_INTROUTER0_OUTP_OUT_1	GICSS0_SPI_IN_49
	CMP_EVENT_INTROUTER0_OUTP_OUT_2	GICSS0_SPI_IN_50
	CMP_EVENT_INTROUTER0_OUTP_OUT_3	GICSS0_SPI_IN_51
	CMP_EVENT_INTROUTER0_OUTP_OUT_4	GICSS0_SPI_IN_52
	CMP_EVENT_INTROUTER0_OUTP_OUT_5	GICSS0_SPI_IN_53
	CMP_EVENT_INTROUTER0_OUTP_OUT_6	GICSS0_SPI_IN_54
	CMP_EVENT_INTROUTER0_OUTP_OUT_7	GICSS0_SPI_IN_55
	CMP_EVENT_INTROUTER0_OUTP_OUT_8	GICSS0_SPI_IN_56
	CMP_EVENT_INTROUTER0_OUTP_OUT_9	GICSS0_SPI_IN_57
	CMP_EVENT_INTROUTER0_OUTP_OUT_10	GICSS0_SPI_IN_58
	CMP_EVENT_INTROUTER0_OUTP_OUT_11	GICSS0_SPI_IN_59
	CMP_EVENT_INTROUTER0_OUTP_OUT_12	GICSS0_SPI_IN_60
	CMP_EVENT_INTROUTER0_OUTP_OUT_13	GICSS0_SPI_IN_61
	CMP_EVENT_INTROUTER0_OUTP_OUT_14	GICSS0_SPI_IN_62
	CMP_EVENT_INTROUTER0_OUTP_OUT_15	GICSS0_SPI_IN_63
	CMP_EVENT_INTROUTER0_OUTP_OUT_16	WKUP_R5FSS0_CORE0_INTR_IN_48
	CMP_EVENT_INTROUTER0_OUTP_OUT_17	WKUP_R5FSS0_CORE0_INTR_IN_49
	CMP_EVENT_INTROUTER0_OUTP_OUT_18	WKUP_R5FSS0_CORE0_INTR_IN_50
	CMP_EVENT_INTROUTER0_OUTP_OUT_19	WKUP_R5FSS0_CORE0_INTR_IN_51
	CMP_EVENT_INTROUTER0_OUTP_OUT_20	WKUP_R5FSS0_CORE0_INTR_IN_52
	CMP_EVENT_INTROUTER0_OUTP_OUT_21	WKUP_R5FSS0_CORE0_INTR_IN_53
	CMP_EVENT_INTROUTER0_OUTP_OUT_22	WKUP_R5FSS0_CORE0_INTR_IN_54
	CMP_EVENT_INTROUTER0_OUTP_OUT_23	WKUP_R5FSS0_CORE0_INTR_IN_55
	CMP_EVENT_INTROUTER0_OUTP_OUT_24	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_0
	CMP_EVENT_INTROUTER0_OUTP_OUT_25	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_1
	CMP_EVENT_INTROUTER0_OUTP_OUT_26	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_2
	CMP_EVENT_INTROUTER0_OUTP_OUT_27	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_3
	CMP_EVENT_INTROUTER0_OUTP_OUT_28	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_4

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
CMP_EVENT_INTROUTER0	CMP_EVENT_INTROUTER0_OUTP_OUT_29	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_5
	CMP_EVENT_INTROUTER0_OUTP_OUT_30	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_6
	CMP_EVENT_INTROUTER0_OUTP_OUT_31	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_7
	CMP_EVENT_INTROUTER0_OUTP_OUT_32	EPWM0_EPWM_SYNCIN_IN_0
	CMP_EVENT_INTROUTER0_OUTP_OUT_34	MCU_M4FSS0_CORE0_NVIC_IN_58
	CMP_EVENT_INTROUTER0_OUTP_OUT_35	MCU_M4FSS0_CORE0_NVIC_IN_59
	CMP_EVENT_INTROUTER0_OUTP_OUT_36	MCU_M4FSS0_CORE0_NVIC_IN_60
	CMP_EVENT_INTROUTER0_OUTP_OUT_37	MCU_M4FSS0_CORE0_NVIC_IN_61
CBASS_IPCSS0	CBASS_IPCSS0_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	CBASS_IPCSS0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
CBASS_CENTRAL2	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	CBASS_CENTRAL2_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
CTRL_MMR0	CTRL_MMR0_ACCESS_ERR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_39
	CTRL_MMR0_ACCESS_ERR_OUT_0	GICSS0_SPI_IN_129
	CTRL_MMR0_ACCESS_ERR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_128
CBASS0	CBASS0_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	CBASS0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
CBASS_DBG0	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	CBASS_DBG0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0	GICSS0_SPI_IN_32
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_32
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1	GICSS0_SPI_IN_33
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_33
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2	GICSS0_SPI_IN_34
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_2	WKUP_R5FSS0_CORE0_INTR_IN_34
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3	GICSS0_SPI_IN_35
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_35
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4	GICSS0_SPI_IN_36
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_4	WKUP_R5FSS0_CORE0_INTR_IN_36
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5	GICSS0_SPI_IN_37
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_5	WKUP_R5FSS0_CORE0_INTR_IN_37
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6	GICSS0_SPI_IN_38
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_6	WKUP_R5FSS0_CORE0_INTR_IN_38
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7	GICSS0_SPI_IN_39
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_7	WKUP_R5FSS0_CORE0_INTR_IN_39
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8	GICSS0_SPI_IN_40
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_8	WKUP_R5FSS0_CORE0_INTR_IN_40

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MAIN_GPIOMUX_INTROUTER0	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9	GICSS0_SPI_IN_41
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_9	WKUP_R5FSS0_CORE0_INTR_IN_41
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10	GICSS0_SPI_IN_42
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_10	WKUP_R5FSS0_CORE0_INTR_IN_42
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11	GICSS0_SPI_IN_43
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_11	WKUP_R5FSS0_CORE0_INTR_IN_43
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12	GICSS0_SPI_IN_44
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_12	WKUP_R5FSS0_CORE0_INTR_IN_44
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13	GICSS0_SPI_IN_45
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_13	WKUP_R5FSS0_CORE0_INTR_IN_45
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14	GICSS0_SPI_IN_46
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_14	WKUP_R5FSS0_CORE0_INTR_IN_46
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15	GICSS0_SPI_IN_47
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_15	WKUP_R5FSS0_CORE0_INTR_IN_47
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_16	ICSSM0_PR1_IEP0_CAP_INTR_REQ_IN_0
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_17	ICSSM0_PR1_IEP0_CAP_INTR_REQ_IN_1
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_18	ICSSM0_PR1_IEP0_CAP_INTR_REQ_IN_2
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_19	ICSSM0_PR1_IEP0_CAP_INTR_REQ_IN_3
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_20	ICSSM0_PR1_IEP0_CAP_INTR_REQ_IN_4
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_21	ICSSM0_PR1_IEP0_CAP_INTR_REQ_IN_5
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_22	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_24
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_23	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_25
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_24	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_16
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_25	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_17
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_26	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_18
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_27	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_19
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_28	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_20
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_29	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_21
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_30	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_22
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_31	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_23
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_32	ICSSM0_PR1_SLV_INTR_IN_18
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_33	ICSSM0_PR1_SLV_INTR_IN_25
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_34	MCU_M4FSS0_CORE0_NVIC_IN_15
	MAIN_GPIOMUX_INTROUTER0_OUTP_OUT_35	MCU_M4FSS0_CORE0_NVIC_IN_16

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
CBASS_INFRA1	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	CBASS_INFRA1_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
CBASS_MCASP0	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	CBASS_MCASP0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
CBASS_MISC_PERI0	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	CBASS_MISC_PERI0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
MCU_CBASS0	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_31
	MCU_CBASS0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_148
MCU_CTRL_MMR0	MCU_CTRL_MMR0_IPC_SET0_IPC_SET_IPCFG_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_0
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_39
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	GICSS0_SPI_IN_129
	MCU_CTRL_MMR0_ACCESS_ERR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_128
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0	GICSS0_SPI_IN_104
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_104
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1	GICSS0_SPI_IN_105
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_105
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2	GICSS0_SPI_IN_106
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_2	WKUP_R5FSS0_CORE0_INTR_IN_106
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3	GICSS0_SPI_IN_107
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_107
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_4	MCU_M4FSS0_CORE0_NVIC_IN_0
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_5	MCU_M4FSS0_CORE0_NVIC_IN_1
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_6	MCU_M4FSS0_CORE0_NVIC_IN_2
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_7	MCU_M4FSS0_CORE0_NVIC_IN_3

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
WKUP_MCU_GPIOMUX_INTROUTER0	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8	WKUP_ESM0_ESM_PLS_EVENT0_IN_88
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8	WKUP_ESM0_ESM_PLS_EVENT1_IN_88
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_8	WKUP_ESM0_ESM_PLS_EVENT2_IN_88
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9	WKUP_ESM0_ESM_PLS_EVENT0_IN_89
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9	WKUP_ESM0_ESM_PLS_EVENT1_IN_89
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_9	WKUP_ESM0_ESM_PLS_EVENT2_IN_89
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10	WKUP_ESM0_ESM_PLS_EVENT0_IN_90
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10	WKUP_ESM0_ESM_PLS_EVENT1_IN_90
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_10	WKUP_ESM0_ESM_PLS_EVENT2_IN_90
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11	WKUP_ESM0_ESM_PLS_EVENT0_IN_91
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11	WKUP_ESM0_ESM_PLS_EVENT1_IN_91
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_11	WKUP_ESM0_ESM_PLS_EVENT2_IN_91
	WKUP_MCU_GPIOMUX_INTROUTER0_OUTP_OUT_12	ICSSM0_PR1_SLV_INTR_IN_6
TIMESYNC_EVENT_ROUTER0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_8
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_1	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_9
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_2	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_10
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_3	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_11
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_4	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_12
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_5	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_13
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_6	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_14
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_7	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_15
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_8	ICSSM0_PR1_EDC0_LATCH0_IN_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_9	ICSSM0_PR1_EDC0_LATCH1_IN_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_10	CPSW0_CPTS_HW1_PUSH_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_11	CPSW0_CPTS_HW2_PUSH_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_12	CPSW0_CPTS_HW3_PUSH_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_13	CPSW0_CPTS_HW4_PUSH_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_14	CPSW0_CPTS_HW5_PUSH_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_15	CPSW0_CPTS_HW6_PUSH_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_16	CPSW0_CPTS_HW7_PUSH_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_17	CPSW0_CPTS_HW8_PUSH_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_19	EPWM0_EPWM_SYNCIN_IN_0

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
TIMESYNC_EVENT_ROUTER0	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_20	PINFUNCTION_SYNC0_OUTOUT_SYNC0_OUT_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_21	PINFUNCTION_SYNC1_OUTOUT_SYNC1_OUT_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_22	PINFUNCTION_SYNC2_OUTOUT_SYNC2_OUT_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_23	PINFUNCTION_SYNC3_OUTOUT_SYNC3_OUT_IN_0
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_24	ICSSM0_PR1_SLV_INTR_IN_7
	TIMESYNC_EVENT_ROUTER0_OUTL_OUT_25	ICSSM0_PR1_SLV_INTR_IN_8
WKUP_CTRL_MMR0	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_39
	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0	GICSS0_SPI_IN_129
	WKUP_CTRL_MMR0_ACCESS_ERR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_128
WKUP_CBASS0	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0	GICSS0_SPI_IN_133
	WKUP_CBASS0_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_147
WKUP_CBASS_SAFE1	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_31
	WKUP_CBASS_SAFE1_DEFAULT_ERR_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_148
PADCFG_CTRL0	PADCFG_CTRL0_ACCESS_ERR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_39
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	GICSS0_SPI_IN_129
	PADCFG_CTRL0_ACCESS_ERR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_128
MCU_PADCFG_CTRL0	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_39
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	GICSS0_SPI_IN_129
	MCU_PADCFG_CTRL0_ACCESS_ERR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_128
MCU_M4FSS0_ECC_AGGR_0	MCU_M4FSS0_ECC_AGGR_0_ECC_CORRECTED_ERR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_4
	MCU_M4FSS0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_5
MCU_M4FSS0_RAT_0	MCU_M4FSS0_RAT_0_EXP_INTR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_14
	MCU_M4FSS0_RAT_0_EXP_INTR_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_3
	MCU_M4FSS0_RAT_0_EXP_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_110
CPSW0	CPSW0_CPTS_COMP_OUT_0	PINFUNCTION_CP_GEMAC_CPTS0_TS_COMPOUT_CP_GEMAC_CPTS0_TS_COMP_IN_0
	CPSW0_CPTS_COMP_OUT_0	CMP_EVENT_INTROUTER0_IN_IN_24
	CPSW0_CPTS_GENF0_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_16

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
CPSW0	CPSW0_CPTS_GENF1_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_17
	CPSW0_CPTS_SYNC_OUT_0	PINFUNCTION_CP_GEMAC_CPTS0_TS_SYNCOUT_CP_GEMAC_CPTS0_TS_SYNC_IN_0
	CPSW0_CPTS_SYNC_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_18
	CPSW0_ECC_DED_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_67
	CPSW0_ECC_SEC_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_3
	CPSW0_EVNT_PEND_OUT_0	GICSS0_SPI_IN_134
	CPSW0_EVNT_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_134
	CPSW0_MDIO_PEND_OUT_0	GICSS0_SPI_IN_135
	CPSW0_MDIO_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_135
	CPSW0_STAT_PEND_OUT_0	GICSS0_SPI_IN_136
	CPSW0_STAT_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_136
csi_rx_if0	CSI_RX_IF0_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_66
	CSI_RX_IF0_CSI_ERR_IRQ_OUT_0	ESM0_ESM_LVL_EVENT_IN_0
	CSI_RX_IF0_CSI_ERR_IRQ_OUT_0	GICSS0_SPI_IN_175
	CSI_RX_IF0_CSI_FATAL_OUT_0	ESM0_ESM_LVL_EVENT_IN_70
	CSI_RX_IF0_CSI_IRQ_OUT_0	GICSS0_SPI_IN_173
	CSI_RX_IF0_CSI_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_72
	CSI_RX_IF0_CSI_LEVEL_OUT_0	GICSS0_SPI_IN_174
	CSI_RX_IF0_CSI_NONFATAL_OUT_0	ESM0_ESM_LVL_EVENT_IN_71
	CSI_RX_IF0_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_77
DCC0	DCC0_INTR_DONE_LEVEL_OUT_0	GICSS0_SPI_IN_128
	DCC0_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC0_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_112
DCC1	DCC1_INTR_DONE_LEVEL_OUT_0	GICSS0_SPI_IN_128
	DCC1_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC1_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_113
DCC2	DCC2_INTR_DONE_LEVEL_OUT_0	GICSS0_SPI_IN_128
	DCC2_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DCC2	DCC2_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_114
DCC3	DCC3_INTR_DONE_LEVEL_OUT_0	GICSS0_SPI_IN_128
	DCC3_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC3_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_115
DCC4	DCC4_INTR_DONE_LEVEL_OUT_0	GICSS0_SPI_IN_128
	DCC4_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC4_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_116
DCC5	DCC5_INTR_DONE_LEVEL_OUT_0	GICSS0_SPI_IN_128
	DCC5_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC5_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_117
DCC6	DCC6_INTR_DONE_LEVEL_OUT_0	GICSS0_SPI_IN_128
	DCC6_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_109
	DCC6_INTR_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_79
MCU_DCC0	MCU_DCC0_INTR_DONE_LEVEL_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_21
	MCU_DCC0_INTR_DONE_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_108
	MCU_DCC0_INTR_ERR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_37
DMASS0_ECC_AGGR_0	DMASS0_ECC_AGGR_0_ECC_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_9
	DMASS0_ECC_AGGR_0_ECC_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_10
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_0	GICSS0_SPI_IN_64
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_1	GICSS0_SPI_IN_65
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_2	GICSS0_SPI_IN_66
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_3	GICSS0_SPI_IN_67
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_4	GICSS0_SPI_IN_68
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_5	GICSS0_SPI_IN_69

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_6	GICSS0_SPI_IN_70
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_7	GICSS0_SPI_IN_71
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_8	GICSS0_SPI_IN_72
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_9	GICSS0_SPI_IN_73
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_10	GICSS0_SPI_IN_74
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_11	GICSS0_SPI_IN_75
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_12	GICSS0_SPI_IN_76
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_13	GICSS0_SPI_IN_77
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_14	GICSS0_SPI_IN_78
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_15	GICSS0_SPI_IN_79
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_16	GICSS0_SPI_IN_80
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_17	GICSS0_SPI_IN_81
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_18	GICSS0_SPI_IN_82
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_19	GICSS0_SPI_IN_83
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_20	GICSS0_SPI_IN_84
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_21	GICSS0_SPI_IN_85
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_22	GICSS0_SPI_IN_86
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_23	GICSS0_SPI_IN_87
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_24	GICSS0_SPI_IN_88
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_25	GICSS0_SPI_IN_89
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_26	GICSS0_SPI_IN_90
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_27	GICSS0_SPI_IN_91
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_28	GICSS0_SPI_IN_92
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_29	GICSS0_SPI_IN_93
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_30	GICSS0_SPI_IN_94
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_31	GICSS0_SPI_IN_95
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_32	GICSS0_SPI_IN_96
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_33	GICSS0_SPI_IN_97
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_34	GICSS0_SPI_IN_98
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_35	GICSS0_SPI_IN_99
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_36	GICSS0_SPI_IN_100
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_37	GICSS0_SPI_IN_101
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_38	GICSS0_SPI_IN_102
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_39	GICSS0_SPI_IN_103

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_40	WKUP_R5FSS0_CORE0_INTR_IN_64
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_41	WKUP_R5FSS0_CORE0_INTR_IN_65
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_42	WKUP_R5FSS0_CORE0_INTR_IN_66
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_43	WKUP_R5FSS0_CORE0_INTR_IN_67
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_44	WKUP_R5FSS0_CORE0_INTR_IN_68
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_45	WKUP_R5FSS0_CORE0_INTR_IN_69
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_46	WKUP_R5FSS0_CORE0_INTR_IN_70
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_47	WKUP_R5FSS0_CORE0_INTR_IN_71
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_48	WKUP_R5FSS0_CORE0_INTR_IN_72
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_49	WKUP_R5FSS0_CORE0_INTR_IN_73
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_50	WKUP_R5FSS0_CORE0_INTR_IN_74
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_51	WKUP_R5FSS0_CORE0_INTR_IN_75
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_52	WKUP_R5FSS0_CORE0_INTR_IN_76
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_53	WKUP_R5FSS0_CORE0_INTR_IN_77
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_54	WKUP_R5FSS0_CORE0_INTR_IN_78
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_55	WKUP_R5FSS0_CORE0_INTR_IN_79
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_56	WKUP_R5FSS0_CORE0_INTR_IN_80
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_57	WKUP_R5FSS0_CORE0_INTR_IN_81
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_58	WKUP_R5FSS0_CORE0_INTR_IN_82
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_59	WKUP_R5FSS0_CORE0_INTR_IN_83
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_60	WKUP_R5FSS0_CORE0_INTR_IN_84
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_61	WKUP_R5FSS0_CORE0_INTR_IN_85
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_62	WKUP_R5FSS0_CORE0_INTR_IN_86
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_63	WKUP_R5FSS0_CORE0_INTR_IN_87
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_64	WKUP_R5FSS0_CORE0_INTR_IN_88
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_65	WKUP_R5FSS0_CORE0_INTR_IN_89
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_66	WKUP_R5FSS0_CORE0_INTR_IN_90
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_67	WKUP_R5FSS0_CORE0_INTR_IN_91
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_68	WKUP_R5FSS0_CORE0_INTR_IN_92
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_69	WKUP_R5FSS0_CORE0_INTR_IN_93
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_70	WKUP_R5FSS0_CORE0_INTR_IN_94
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_71	WKUP_R5FSS0_CORE0_INTR_IN_95
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_72	WKUP_R5FSS0_CORE0_INTR_IN_8
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_73	WKUP_R5FSS0_CORE0_INTR_IN_9

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_74	WKUP_R5FSS0_CORE0_INTR_IN_10
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_75	WKUP_R5FSS0_CORE0_INTR_IN_11
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_76	WKUP_R5FSS0_CORE0_INTR_IN_12
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_77	WKUP_R5FSS0_CORE0_INTR_IN_13
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_78	WKUP_R5FSS0_CORE0_INTR_IN_14
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_79	WKUP_R5FSS0_CORE0_INTR_IN_15
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_80	ICSSM0_PR1_SLV_INTR_IN_21
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_81	ICSSM0_PR1_SLV_INTR_IN_29
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_82	ICSSM0_PR1_SLV_INTR_IN_30
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_83	ICSSM0_PR1_SLV_INTR_IN_31

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DMASS0_INTAGGR_0	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_168	MCU_M4FSS0_CORE0_NVIC_IN_32
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_169	MCU_M4FSS0_CORE0_NVIC_IN_33
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_170	MCU_M4FSS0_CORE0_NVIC_IN_34
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_171	MCU_M4FSS0_CORE0_NVIC_IN_35
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_172	MCU_M4FSS0_CORE0_NVIC_IN_54
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_173	MCU_M4FSS0_CORE0_NVIC_IN_55
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_174	MCU_M4FSS0_CORE0_NVIC_IN_56
	DMASS0_INTAGGR_0_INTAGGR_VINTR_PEND_OUT_175	MCU_M4FSS0_CORE0_NVIC_IN_57
TIMER0	TIMER0_INTR_PEND_OUT_0	GICSS0_SPI_IN_152
	TIMER0_TIMER_PWM_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_0
TIMER1	TIMER1_INTR_PEND_OUT_0	GICSS0_SPI_IN_153
	TIMER1_TIMER_PWM_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_1
TIMER2	TIMER2_INTR_PEND_OUT_0	GICSS0_SPI_IN_154
	TIMER2_TIMER_PWM_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_2
TIMER3	TIMER3_INTR_PEND_OUT_0	GICSS0_SPI_IN_155
	TIMER3_TIMER_PWM_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_3
TIMER4	TIMER4_INTR_PEND_OUT_0	GICSS0_SPI_IN_156
TIMER5	TIMER5_INTR_PEND_OUT_0	GICSS0_SPI_IN_157
TIMER6	TIMER6_INTR_PEND_OUT_0	GICSS0_SPI_IN_158
TIMER7	TIMER7_INTR_PEND_OUT_0	GICSS0_SPI_IN_159
MCU_TIMER0	MCU_TIMER0_INTR_PEND_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_4
MCU_TIMER1	MCU_TIMER1_INTR_PEND_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_5
MCU_TIMER2	MCU_TIMER2_INTR_PEND_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_6
MCU_TIMER3	MCU_TIMER3_INTR_PEND_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_7
WKUP_TIMER0	WKUP_TIMER0_INTR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_138
	WKUP_TIMER0_TIMER_CLKSTOP_WAKEUP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_28

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
WKUP_TIMER0	WKUP_TIMER0_TIMER_CLKSTOP_WAKEUP_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_5
WKUP_TIMER1	WKUP_TIMER1_INTR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_139
	WKUP_TIMER1_TIMER_CLKSTOP_WAKEUP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_29
	WKUP_TIMER1_TIMER_CLKSTOP_WAKEUP_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_6
ECAP0	ECAP0_ECAP_INT_OUT_0	GICSS0_SPI_IN_145
	ECAP0_ECAP_INT_OUT_0	ICSSM0_PR1_SLV_INTR_IN_10
ECAP1	ECAP1_ECAP_INT_OUT_0	GICSS0_SPI_IN_146
	ECAP1_ECAP_INT_OUT_0	ICSSM0_PR1_SLV_INTR_IN_3
ECAP2	ECAP2_ECAP_INT_OUT_0	GICSS0_SPI_IN_147
	ECAP2_ECAP_INT_OUT_0	ICSSM0_PR1_SLV_INTR_IN_4
ELM0	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0	GICSS0_SPI_IN_164
	ELM0_ELM_POROCPSINTERRUPT_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_164
MMCSD1	MMCSD1_EMMCSDSS_INTR_OUT_0	GICSS0_SPI_IN_115
	MMCSD1_EMMCSDSS_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_162
	MMCSD1_EMMCSDSS_RXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_58
	MMCSD1_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_59
	MMCSD1_EMMCSDSS_TXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_60
	MMCSD1_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_61
MMCSD2	MMCSD2_EMMCSDSS_INTR_OUT_0	GICSS0_SPI_IN_114
	MMCSD2_EMMCSDSS_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_163
	MMCSD2_EMMCSDSS_RXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_34
	MMCSD2_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_36
	MMCSD2_EMMCSDSS_TXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_49
	MMCSD2_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_65
MMCSD0	MMCSD0_EMMCSDSS_INTR_OUT_0	GICSS0_SPI_IN_165
	MMCSD0_EMMCSDSS_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_161
	MMCSD0_EMMCSDSS_RXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_54
	MMCSD0_EMMCSDSS_RXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_55

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MMCSD0	MMCSD0_EMMCSDSS_TXMEM_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_56
	MMCSD0_EMMCSDSS_TXMEM_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_57
EQEP0	EQEP0_EQEP_INT_OUT_0	GICSS0_SPI_IN_148
	EQEP0_EQEP_INT_OUT_0	ICSSM0_PR1_SLV_INTR_IN_13
EQEP1	EQEP1_EQEP_INT_OUT_0	GICSS0_SPI_IN_149
	EQEP1_EQEP_INT_OUT_0	ICSSM0_PR1_SLV_INTR_IN_16
EQEP2	EQEP2_EQEP_INT_OUT_0	GICSS0_SPI_IN_150
	EQEP2_EQEP_INT_OUT_0	ICSSM0_PR1_SLV_INTR_IN_17
ESM0	ESM0_ESM_INT_CFG_LVL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_0
	ESM0_ESM_INT_CFG_LVL_OUT_0	GICSS0_SPI_IN_180
	ESM0_ESM_INT_CFG_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_167
	ESM0_ESM_INT_HI_LVL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_1
	ESM0_ESM_INT_HI_LVL_OUT_0	GICSS0_SPI_IN_181
	ESM0_ESM_INT_HI_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_168
	ESM0_ESM_INT_LOW_LVL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_2
	ESM0_ESM_INT_LOW_LVL_OUT_0	GICSS0_SPI_IN_182
	ESM0_ESM_INT_LOW_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_169
WKUP_ESM0	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_11
	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_37
	WKUP_ESM0_ESM_INT_CFG_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_140
	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_12
	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_38

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
WKUP_ESM0	WKUP_ESM0_ESM_INT_HI_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_141
	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_13
	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_39
	WKUP_ESM0_ESM_INT_LOW_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_142
FSS0_FSAS_0	FSS0_FSAS_0_ECC_INTR_ERR_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_141
FSS0_OSPI_0	FSS0_OSPI_0_OSPI_ECC_CORR_LVL_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_11
	FSS0_OSPI_0_OSPI_ECC_UNCORR_LVL_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_74
	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0	GICSS0_SPI_IN_171
	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0	ICSSM0_PR1_SLV_INTR_IN_26
	FSS0_OSPI_0_OSPI_LVL_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_171
GICSS0	GICSS0_AXIM_ERR_OUT_0	ESM0_ESM_PLS_EVENT0_IN_166
	GICSS0_AXIM_ERR_OUT_0	ESM0_ESM_PLS_EVENT1_IN_166
	GICSS0_AXIM_ERR_OUT_0	ESM0_ESM_PLS_EVENT2_IN_166
	GICSS0_ECC_AGGR_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_12
	GICSS0_ECC_AGGR_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_75
	GICSS0_ECC_FATAL_OUT_0	ESM0_ESM_PLS_EVENT0_IN_167
	GICSS0_ECC_FATAL_OUT_0	ESM0_ESM_PLS_EVENT1_IN_167
	GICSS0_ECC_FATAL_OUT_0	ESM0_ESM_PLS_EVENT2_IN_167
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_154
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_155
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_2	WKUP_R5FSS0_CORE0_INTR_IN_156
	GICSS0_GIC_PWR0_WAKE_REQUEST_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_157

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GPIO0	GPIO0_GPIO_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_0
	GPIO0_GPIO_OUT_1	MAIN_GPIOMUX_INTROUTER0_IN_IN_1
	GPIO0_GPIO_OUT_2	MAIN_GPIOMUX_INTROUTER0_IN_IN_2
	GPIO0_GPIO_OUT_3	MAIN_GPIOMUX_INTROUTER0_IN_IN_3
	GPIO0_GPIO_OUT_4	MAIN_GPIOMUX_INTROUTER0_IN_IN_4
	GPIO0_GPIO_OUT_5	MAIN_GPIOMUX_INTROUTER0_IN_IN_5
	GPIO0_GPIO_OUT_6	MAIN_GPIOMUX_INTROUTER0_IN_IN_6
	GPIO0_GPIO_OUT_7	MAIN_GPIOMUX_INTROUTER0_IN_IN_7
	GPIO0_GPIO_OUT_8	MAIN_GPIOMUX_INTROUTER0_IN_IN_8
	GPIO0_GPIO_OUT_9	MAIN_GPIOMUX_INTROUTER0_IN_IN_9
	GPIO0_GPIO_OUT_10	MAIN_GPIOMUX_INTROUTER0_IN_IN_10
	GPIO0_GPIO_OUT_11	MAIN_GPIOMUX_INTROUTER0_IN_IN_11
	GPIO0_GPIO_OUT_12	MAIN_GPIOMUX_INTROUTER0_IN_IN_12
	GPIO0_GPIO_OUT_13	MAIN_GPIOMUX_INTROUTER0_IN_IN_13
	GPIO0_GPIO_OUT_14	MAIN_GPIOMUX_INTROUTER0_IN_IN_14
	GPIO0_GPIO_OUT_15	MAIN_GPIOMUX_INTROUTER0_IN_IN_15
	GPIO0_GPIO_OUT_16	MAIN_GPIOMUX_INTROUTER0_IN_IN_16
	GPIO0_GPIO_OUT_17	MAIN_GPIOMUX_INTROUTER0_IN_IN_17
	GPIO0_GPIO_OUT_18	MAIN_GPIOMUX_INTROUTER0_IN_IN_18
	GPIO0_GPIO_OUT_19	MAIN_GPIOMUX_INTROUTER0_IN_IN_19
	GPIO0_GPIO_OUT_20	MAIN_GPIOMUX_INTROUTER0_IN_IN_20
	GPIO0_GPIO_OUT_21	MAIN_GPIOMUX_INTROUTER0_IN_IN_21
	GPIO0_GPIO_OUT_22	MAIN_GPIOMUX_INTROUTER0_IN_IN_22
	GPIO0_GPIO_OUT_23	MAIN_GPIOMUX_INTROUTER0_IN_IN_23
	GPIO0_GPIO_OUT_24	MAIN_GPIOMUX_INTROUTER0_IN_IN_24
	GPIO0_GPIO_OUT_25	MAIN_GPIOMUX_INTROUTER0_IN_IN_25
	GPIO0_GPIO_OUT_26	MAIN_GPIOMUX_INTROUTER0_IN_IN_26
	GPIO0_GPIO_OUT_27	MAIN_GPIOMUX_INTROUTER0_IN_IN_27
	GPIO0_GPIO_OUT_28	MAIN_GPIOMUX_INTROUTER0_IN_IN_28
	GPIO0_GPIO_OUT_29	MAIN_GPIOMUX_INTROUTER0_IN_IN_29
	GPIO0_GPIO_OUT_30	MAIN_GPIOMUX_INTROUTER0_IN_IN_30
	GPIO0_GPIO_OUT_31	MAIN_GPIOMUX_INTROUTER0_IN_IN_31
	GPIO0_GPIO_OUT_32	MAIN_GPIOMUX_INTROUTER0_IN_IN_32
	GPIO0_GPIO_OUT_33	MAIN_GPIOMUX_INTROUTER0_IN_IN_33

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GPIO0	GPIO0_GPIO_OUT_34	MAIN_GPIOMUX_INTROUTER0_IN_IN_34
	GPIO0_GPIO_OUT_35	MAIN_GPIOMUX_INTROUTER0_IN_IN_35
	GPIO0_GPIO_OUT_36	MAIN_GPIOMUX_INTROUTER0_IN_IN_36
	GPIO0_GPIO_OUT_37	MAIN_GPIOMUX_INTROUTER0_IN_IN_37
	GPIO0_GPIO_OUT_38	MAIN_GPIOMUX_INTROUTER0_IN_IN_38
	GPIO0_GPIO_OUT_39	MAIN_GPIOMUX_INTROUTER0_IN_IN_39
	GPIO0_GPIO_OUT_40	MAIN_GPIOMUX_INTROUTER0_IN_IN_40
	GPIO0_GPIO_OUT_41	MAIN_GPIOMUX_INTROUTER0_IN_IN_41
	GPIO0_GPIO_OUT_42	MAIN_GPIOMUX_INTROUTER0_IN_IN_42
	GPIO0_GPIO_OUT_43	MAIN_GPIOMUX_INTROUTER0_IN_IN_43
	GPIO0_GPIO_OUT_44	MAIN_GPIOMUX_INTROUTER0_IN_IN_44
	GPIO0_GPIO_OUT_45	MAIN_GPIOMUX_INTROUTER0_IN_IN_45
	GPIO0_GPIO_OUT_46	MAIN_GPIOMUX_INTROUTER0_IN_IN_46
	GPIO0_GPIO_OUT_47	MAIN_GPIOMUX_INTROUTER0_IN_IN_47
	GPIO0_GPIO_OUT_48	MAIN_GPIOMUX_INTROUTER0_IN_IN_48
	GPIO0_GPIO_OUT_49	MAIN_GPIOMUX_INTROUTER0_IN_IN_49
	GPIO0_GPIO_OUT_50	MAIN_GPIOMUX_INTROUTER0_IN_IN_50
	GPIO0_GPIO_OUT_51	MAIN_GPIOMUX_INTROUTER0_IN_IN_51
	GPIO0_GPIO_OUT_52	MAIN_GPIOMUX_INTROUTER0_IN_IN_52
	GPIO0_GPIO_OUT_53	MAIN_GPIOMUX_INTROUTER0_IN_IN_53
	GPIO0_GPIO_OUT_54	MAIN_GPIOMUX_INTROUTER0_IN_IN_54
	GPIO0_GPIO_OUT_55	MAIN_GPIOMUX_INTROUTER0_IN_IN_55
	GPIO0_GPIO_OUT_56	MAIN_GPIOMUX_INTROUTER0_IN_IN_56
	GPIO0_GPIO_OUT_57	MAIN_GPIOMUX_INTROUTER0_IN_IN_57
	GPIO0_GPIO_OUT_58	MAIN_GPIOMUX_INTROUTER0_IN_IN_58
	GPIO0_GPIO_OUT_59	MAIN_GPIOMUX_INTROUTER0_IN_IN_59
	GPIO0_GPIO_OUT_60	MAIN_GPIOMUX_INTROUTER0_IN_IN_60
	GPIO0_GPIO_OUT_61	MAIN_GPIOMUX_INTROUTER0_IN_IN_61
	GPIO0_GPIO_OUT_62	MAIN_GPIOMUX_INTROUTER0_IN_IN_62
	GPIO0_GPIO_OUT_63	MAIN_GPIOMUX_INTROUTER0_IN_IN_63
	GPIO0_GPIO_OUT_64	MAIN_GPIOMUX_INTROUTER0_IN_IN_64
	GPIO0_GPIO_OUT_65	MAIN_GPIOMUX_INTROUTER0_IN_IN_65
	GPIO0_GPIO_OUT_66	MAIN_GPIOMUX_INTROUTER0_IN_IN_66
	GPIO0_GPIO_OUT_67	MAIN_GPIOMUX_INTROUTER0_IN_IN_67

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GPIO0	GPIO0_GPIO_OUT_68	MAIN_GPIOMUX_INTROUTER0_IN_IN_68
	GPIO0_GPIO_OUT_69	MAIN_GPIOMUX_INTROUTER0_IN_IN_69
	GPIO0_GPIO_OUT_70	MAIN_GPIOMUX_INTROUTER0_IN_IN_70
	GPIO0_GPIO_OUT_71	MAIN_GPIOMUX_INTROUTER0_IN_IN_71
	GPIO0_GPIO_OUT_72	MAIN_GPIOMUX_INTROUTER0_IN_IN_72
	GPIO0_GPIO_OUT_73	MAIN_GPIOMUX_INTROUTER0_IN_IN_73
	GPIO0_GPIO_OUT_74	MAIN_GPIOMUX_INTROUTER0_IN_IN_74
	GPIO0_GPIO_OUT_75	MAIN_GPIOMUX_INTROUTER0_IN_IN_75
	GPIO0_GPIO_OUT_76	MAIN_GPIOMUX_INTROUTER0_IN_IN_76
	GPIO0_GPIO_OUT_77	MAIN_GPIOMUX_INTROUTER0_IN_IN_77
	GPIO0_GPIO_OUT_78	MAIN_GPIOMUX_INTROUTER0_IN_IN_78
	GPIO0_GPIO_OUT_79	MAIN_GPIOMUX_INTROUTER0_IN_IN_79
	GPIO0_GPIO_OUT_80	MAIN_GPIOMUX_INTROUTER0_IN_IN_80
	GPIO0_GPIO_OUT_81	MAIN_GPIOMUX_INTROUTER0_IN_IN_81
	GPIO0_GPIO_OUT_82	MAIN_GPIOMUX_INTROUTER0_IN_IN_82
	GPIO0_GPIO_OUT_83	MAIN_GPIOMUX_INTROUTER0_IN_IN_83
	GPIO0_GPIO_OUT_84	MAIN_GPIOMUX_INTROUTER0_IN_IN_84
	GPIO0_GPIO_OUT_85	MAIN_GPIOMUX_INTROUTER0_IN_IN_85
	GPIO0_GPIO_OUT_86	MAIN_GPIOMUX_INTROUTER0_IN_IN_86
	GPIO0_GPIO_OUT_87	MAIN_GPIOMUX_INTROUTER0_IN_IN_87
	GPIO0_GPIO_OUT_88	MAIN_GPIOMUX_INTROUTER0_IN_IN_88
	GPIO0_GPIO_OUT_89	MAIN_GPIOMUX_INTROUTER0_IN_IN_89
	GPIO0_GPIO_OUT_90	MAIN_GPIOMUX_INTROUTER0_IN_IN_176
	GPIO0_GPIO_OUT_91	MAIN_GPIOMUX_INTROUTER0_IN_IN_177
	GPIO0_GPIO_BANK_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_190
	GPIO0_GPIO_BANK_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_56
	GPIO0_GPIO_BANK_OUT_1	MAIN_GPIOMUX_INTROUTER0_IN_IN_191
	GPIO0_GPIO_BANK_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_57
	GPIO0_GPIO_BANK_OUT_2	MAIN_GPIOMUX_INTROUTER0_IN_IN_192
	GPIO0_GPIO_BANK_OUT_3	MAIN_GPIOMUX_INTROUTER0_IN_IN_193
	GPIO0_GPIO_BANK_OUT_4	MAIN_GPIOMUX_INTROUTER0_IN_IN_194
	GPIO0_GPIO_BANK_OUT_5	MAIN_GPIOMUX_INTROUTER0_IN_IN_195
GPIO1	GPIO1_GPIO_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_90
	GPIO1_GPIO_OUT_1	MAIN_GPIOMUX_INTROUTER0_IN_IN_91

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GPIO1	GPIO1_GPIO_OUT_2	MAIN_GPIOMUX_INTROUTER0_IN_IN_92
	GPIO1_GPIO_OUT_3	MAIN_GPIOMUX_INTROUTER0_IN_IN_93
	GPIO1_GPIO_OUT_4	MAIN_GPIOMUX_INTROUTER0_IN_IN_94
	GPIO1_GPIO_OUT_5	MAIN_GPIOMUX_INTROUTER0_IN_IN_95
	GPIO1_GPIO_OUT_6	MAIN_GPIOMUX_INTROUTER0_IN_IN_96
	GPIO1_GPIO_OUT_7	MAIN_GPIOMUX_INTROUTER0_IN_IN_97
	GPIO1_GPIO_OUT_8	MAIN_GPIOMUX_INTROUTER0_IN_IN_98
	GPIO1_GPIO_OUT_9	MAIN_GPIOMUX_INTROUTER0_IN_IN_99
	GPIO1_GPIO_OUT_10	MAIN_GPIOMUX_INTROUTER0_IN_IN_100
	GPIO1_GPIO_OUT_11	MAIN_GPIOMUX_INTROUTER0_IN_IN_101
	GPIO1_GPIO_OUT_12	MAIN_GPIOMUX_INTROUTER0_IN_IN_102
	GPIO1_GPIO_OUT_13	MAIN_GPIOMUX_INTROUTER0_IN_IN_103
	GPIO1_GPIO_OUT_14	MAIN_GPIOMUX_INTROUTER0_IN_IN_104
	GPIO1_GPIO_OUT_15	MAIN_GPIOMUX_INTROUTER0_IN_IN_105
	GPIO1_GPIO_OUT_16	MAIN_GPIOMUX_INTROUTER0_IN_IN_106
	GPIO1_GPIO_OUT_17	MAIN_GPIOMUX_INTROUTER0_IN_IN_107
	GPIO1_GPIO_OUT_18	MAIN_GPIOMUX_INTROUTER0_IN_IN_108
	GPIO1_GPIO_OUT_19	MAIN_GPIOMUX_INTROUTER0_IN_IN_109
	GPIO1_GPIO_OUT_20	MAIN_GPIOMUX_INTROUTER0_IN_IN_110
	GPIO1_GPIO_OUT_21	MAIN_GPIOMUX_INTROUTER0_IN_IN_111
	GPIO1_GPIO_OUT_22	MAIN_GPIOMUX_INTROUTER0_IN_IN_112
	GPIO1_GPIO_OUT_23	MAIN_GPIOMUX_INTROUTER0_IN_IN_113
	GPIO1_GPIO_OUT_24	MAIN_GPIOMUX_INTROUTER0_IN_IN_114
	GPIO1_GPIO_OUT_25	MAIN_GPIOMUX_INTROUTER0_IN_IN_115
	GPIO1_GPIO_OUT_26	MAIN_GPIOMUX_INTROUTER0_IN_IN_116
	GPIO1_GPIO_OUT_27	MAIN_GPIOMUX_INTROUTER0_IN_IN_117
	GPIO1_GPIO_OUT_28	MAIN_GPIOMUX_INTROUTER0_IN_IN_118
	GPIO1_GPIO_OUT_29	MAIN_GPIOMUX_INTROUTER0_IN_IN_119
	GPIO1_GPIO_OUT_30	MAIN_GPIOMUX_INTROUTER0_IN_IN_120
	GPIO1_GPIO_OUT_31	MAIN_GPIOMUX_INTROUTER0_IN_IN_121
	GPIO1_GPIO_OUT_32	MAIN_GPIOMUX_INTROUTER0_IN_IN_122
	GPIO1_GPIO_OUT_33	MAIN_GPIOMUX_INTROUTER0_IN_IN_123
	GPIO1_GPIO_OUT_34	MAIN_GPIOMUX_INTROUTER0_IN_IN_124
	GPIO1_GPIO_OUT_35	MAIN_GPIOMUX_INTROUTER0_IN_IN_125

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GPIO1	GPIO1_GPIO_OUT_36	MAIN_GPIOMUX_INTROUTER0_IN_IN_126
	GPIO1_GPIO_OUT_37	MAIN_GPIOMUX_INTROUTER0_IN_IN_127
	GPIO1_GPIO_OUT_38	MAIN_GPIOMUX_INTROUTER0_IN_IN_128
	GPIO1_GPIO_OUT_39	MAIN_GPIOMUX_INTROUTER0_IN_IN_129
	GPIO1_GPIO_OUT_40	MAIN_GPIOMUX_INTROUTER0_IN_IN_130
	GPIO1_GPIO_OUT_41	MAIN_GPIOMUX_INTROUTER0_IN_IN_131
	GPIO1_GPIO_OUT_42	MAIN_GPIOMUX_INTROUTER0_IN_IN_132
	GPIO1_GPIO_OUT_43	MAIN_GPIOMUX_INTROUTER0_IN_IN_133
	GPIO1_GPIO_OUT_44	MAIN_GPIOMUX_INTROUTER0_IN_IN_134
	GPIO1_GPIO_OUT_45	MAIN_GPIOMUX_INTROUTER0_IN_IN_135
	GPIO1_GPIO_OUT_46	MAIN_GPIOMUX_INTROUTER0_IN_IN_136
	GPIO1_GPIO_OUT_47	MAIN_GPIOMUX_INTROUTER0_IN_IN_137
	GPIO1_GPIO_OUT_48	MAIN_GPIOMUX_INTROUTER0_IN_IN_138
	GPIO1_GPIO_OUT_49	MAIN_GPIOMUX_INTROUTER0_IN_IN_139
	GPIO1_GPIO_OUT_50	MAIN_GPIOMUX_INTROUTER0_IN_IN_140
	GPIO1_GPIO_OUT_51	MAIN_GPIOMUX_INTROUTER0_IN_IN_141
	GPIO1_GPIO_OUT_52	MAIN_GPIOMUX_INTROUTER0_IN_IN_142
	GPIO1_GPIO_OUT_53	MAIN_GPIOMUX_INTROUTER0_IN_IN_143
	GPIO1_GPIO_OUT_54	MAIN_GPIOMUX_INTROUTER0_IN_IN_144
	GPIO1_GPIO_OUT_55	MAIN_GPIOMUX_INTROUTER0_IN_IN_145
	GPIO1_GPIO_OUT_56	MAIN_GPIOMUX_INTROUTER0_IN_IN_146
	GPIO1_GPIO_OUT_57	MAIN_GPIOMUX_INTROUTER0_IN_IN_147
	GPIO1_GPIO_OUT_58	MAIN_GPIOMUX_INTROUTER0_IN_IN_148
	GPIO1_GPIO_OUT_59	MAIN_GPIOMUX_INTROUTER0_IN_IN_149
	GPIO1_GPIO_OUT_60	MAIN_GPIOMUX_INTROUTER0_IN_IN_150
	GPIO1_GPIO_OUT_61	MAIN_GPIOMUX_INTROUTER0_IN_IN_151
	GPIO1_GPIO_OUT_62	MAIN_GPIOMUX_INTROUTER0_IN_IN_152
	GPIO1_GPIO_OUT_63	MAIN_GPIOMUX_INTROUTER0_IN_IN_153
	GPIO1_GPIO_OUT_64	MAIN_GPIOMUX_INTROUTER0_IN_IN_154
	GPIO1_GPIO_OUT_65	MAIN_GPIOMUX_INTROUTER0_IN_IN_155
	GPIO1_GPIO_OUT_66	MAIN_GPIOMUX_INTROUTER0_IN_IN_156
	GPIO1_GPIO_OUT_67	MAIN_GPIOMUX_INTROUTER0_IN_IN_157
	GPIO1_GPIO_OUT_68	MAIN_GPIOMUX_INTROUTER0_IN_IN_158
	GPIO1_GPIO_OUT_69	MAIN_GPIOMUX_INTROUTER0_IN_IN_159

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
GPIO1	GPIO1_GPIO_OUT_70	MAIN_GPIOMUX_INTROUTER0_IN_IN_160
	GPIO1_GPIO_OUT_71	MAIN_GPIOMUX_INTROUTER0_IN_IN_161
	GPIO1_GPIO_BANK_OUT_0	MAIN_GPIOMUX_INTROUTER0_IN_IN_180
	GPIO1_GPIO_BANK_OUT_1	MAIN_GPIOMUX_INTROUTER0_IN_IN_181
	GPIO1_GPIO_BANK_OUT_2	MAIN_GPIOMUX_INTROUTER0_IN_IN_182
	GPIO1_GPIO_BANK_OUT_3	MAIN_GPIOMUX_INTROUTER0_IN_IN_183
	GPIO1_GPIO_BANK_OUT_4	MAIN_GPIOMUX_INTROUTER0_IN_IN_184
MCU_GPIO0	MCU_GPIO0_GPIO_OUT_0	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_0
	MCU_GPIO0_GPIO_OUT_1	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_1
	MCU_GPIO0_GPIO_OUT_2	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_2
	MCU_GPIO0_GPIO_OUT_3	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_3
	MCU_GPIO0_GPIO_OUT_4	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_4
	MCU_GPIO0_GPIO_OUT_5	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_5
	MCU_GPIO0_GPIO_OUT_6	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_6
	MCU_GPIO0_GPIO_OUT_7	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_7
	MCU_GPIO0_GPIO_OUT_8	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_8
	MCU_GPIO0_GPIO_OUT_9	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_9
	MCU_GPIO0_GPIO_OUT_10	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_10
	MCU_GPIO0_GPIO_OUT_11	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_11
	MCU_GPIO0_GPIO_OUT_12	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_12
	MCU_GPIO0_GPIO_OUT_13	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_13
	MCU_GPIO0_GPIO_OUT_14	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_14
	MCU_GPIO0_GPIO_OUT_15	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_15
	MCU_GPIO0_GPIO_OUT_16	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_16
	MCU_GPIO0_GPIO_OUT_17	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_17
	MCU_GPIO0_GPIO_OUT_18	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_18
	MCU_GPIO0_GPIO_OUT_19	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_19
	MCU_GPIO0_GPIO_OUT_20	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_20
	MCU_GPIO0_GPIO_OUT_21	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_21
	MCU_GPIO0_GPIO_OUT_22	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_22
	MCU_GPIO0_GPIO_OUT_23	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_23
	MCU_GPIO0_GPIO_BANK_OUT_0	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_30
	MCU_GPIO0_GPIO_BANK_OUT_1	WKUP_MCU_GPIOMUX_INTROUTER0_IN_IN_31
	MCU_GPIO0_GPIO_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_18

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_GPIO0	MCU_GPIO0_GPIO_LVL_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_2
GPMC0	GPMC0_GPMC_SDMAREQ_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_26
	GPMC0_GPMC_SINTERRUPT_OUT_0	GICSS0_SPI_IN_138
	GPMC0_GPMC_SINTERRUPT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_103
WKUP_GTC0	WKUP_GTC0_GTC_PUSH_EVENT_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_11
WKUP_icemelter0	WKUP_ICEMELTER0_PSC_FORCE_POWER_ON_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_23
	WKUP_ICEMELTER0_PSC_FORCE_POWER_ON_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_3
ICSSM0	ICSSM0_ISO_RESET_PROTCOL_ACK_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_53
	ICSSM0_ISO_RESET_PROTCOL_ACK_OUT_0	GICSS0_SPI_IN_167
	ICSSM0_ISO_RESET_PROTCOL_ACK_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_170
	ICSSM0_PR1_ECC_DED_ERR_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_76
	ICSSM0_PR1_ECC_SEC_ERR_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_13
	ICSSM0_PR1_EDC0_SYNC0_OUT_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_10
	ICSSM0_PR1_EDC0_SYNC1_OUT_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_9
	ICSSM0_PR1_EDIO0_WD_TRIIG_OUT_0	ESM0_ESM_LVL_EVENT_IN_68
	ICSSM0_PR1_HOST_INTR_PEND_OUT_0	GICSS0_SPI_IN_120
	ICSSM0_PR1_HOST_INTR_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_120
	ICSSM0_PR1_HOST_INTR_PEND_OUT_1	GICSS0_SPI_IN_121
	ICSSM0_PR1_HOST_INTR_PEND_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_121
	ICSSM0_PR1_HOST_INTR_PEND_OUT_2	GICSS0_SPI_IN_122
	ICSSM0_PR1_HOST_INTR_PEND_OUT_2	WKUP_R5FSS0_CORE0_INTR_IN_122
	ICSSM0_PR1_HOST_INTR_PEND_OUT_3	GICSS0_SPI_IN_123
	ICSSM0_PR1_HOST_INTR_PEND_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_123
	ICSSM0_PR1_HOST_INTR_PEND_OUT_4	GICSS0_SPI_IN_124

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
ICSSM0	ICSSM0_PR1_HOST_INTR_PEND_OUT_4	WKUP_R5FSS0_CORE0_INTR_IN_124
	ICSSM0_PR1_HOST_INTR_PEND_OUT_5	GICSS0_SPI_IN_125
	ICSSM0_PR1_HOST_INTR_PEND_OUT_5	WKUP_R5FSS0_CORE0_INTR_IN_125
	ICSSM0_PR1_HOST_INTR_PEND_OUT_6	EPWM0_EPWM_SYNCIN_IN_0
	ICSSM0_PR1_HOST_INTR_PEND_OUT_6	MCU_M4FSS0_CORE0_NVIC_IN_51
	ICSSM0_PR1_HOST_INTR_PEND_OUT_6	GICSS0_SPI_IN_126
	ICSSM0_PR1_HOST_INTR_PEND_OUT_6	WKUP_R5FSS0_CORE0_INTR_IN_126
	ICSSM0_PR1_HOST_INTR_PEND_OUT_7	MCU_M4FSS0_CORE0_NVIC_IN_52
	ICSSM0_PR1_HOST_INTR_PEND_OUT_7	GICSS0_SPI_IN_127
	ICSSM0_PR1_HOST_INTR_PEND_OUT_7	WKUP_R5FSS0_CORE0_INTR_IN_127
	ICSSM0_PR1_HOST_INTR_REQ_OUT_0	CMP_EVENT_INTROUTER0_IN_IN_0
	ICSSM0_PR1_HOST_INTR_REQ_OUT_1	CMP_EVENT_INTROUTER0_IN_IN_1
	ICSSM0_PR1_HOST_INTR_REQ_OUT_2	CMP_EVENT_INTROUTER0_IN_IN_2
	ICSSM0_PR1_HOST_INTR_REQ_OUT_3	CMP_EVENT_INTROUTER0_IN_IN_3
	ICSSM0_PR1_HOST_INTR_REQ_OUT_4	CMP_EVENT_INTROUTER0_IN_IN_4
	ICSSM0_PR1_HOST_INTR_REQ_OUT_5	CMP_EVENT_INTROUTER0_IN_IN_5
	ICSSM0_PR1_HOST_INTR_REQ_OUT_6	CMP_EVENT_INTROUTER0_IN_IN_6
	ICSSM0_PR1_HOST_INTR_REQ_OUT_7	CMP_EVENT_INTROUTER0_IN_IN_7
	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_0	CMP_EVENT_INTROUTER0_IN_IN_8
	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_1	CMP_EVENT_INTROUTER0_IN_IN_9
	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_2	CMP_EVENT_INTROUTER0_IN_IN_10
	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_3	CMP_EVENT_INTROUTER0_IN_IN_11
	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_4	CMP_EVENT_INTROUTER0_IN_IN_12
	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_5	CMP_EVENT_INTROUTER0_IN_IN_13
	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_6	CMP_EVENT_INTROUTER0_IN_IN_14
	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_7	CMP_EVENT_INTROUTER0_IN_IN_15

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
ICSSM0	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_8	CMP_EVENT_INTROUTER0_IN_IN_16
	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_9	CMP_EVENT_INTROUTER0_IN_IN_17
	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_10	CMP_EVENT_INTROUTER0_IN_IN_18
	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_11	CMP_EVENT_INTROUTER0_IN_IN_19
	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_12	CMP_EVENT_INTROUTER0_IN_IN_20
	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_13	CMP_EVENT_INTROUTER0_IN_IN_21
	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_14	CMP_EVENT_INTROUTER0_IN_IN_22
	ICSSM0_PR1_IEP0_CMP_INTR_REQ_OUT_15	CMP_EVENT_INTROUTER0_IN_IN_23
	ICSSM0_PR1_RX_SOF_INTR_REQ_OUT_0	GICSS0_SPI_IN_244
	ICSSM0_PR1_RX_SOF_INTR_REQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_244
	ICSSM0_PR1_RX_SOF_INTR_REQ_OUT_1	GICSS0_SPI_IN_245
	ICSSM0_PR1_RX_SOF_INTR_REQ_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_245
	ICSSM0_PR1_TX_SOF_INTR_REQ_OUT_0	GICSS0_SPI_IN_246
	ICSSM0_PR1_TX_SOF_INTR_REQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_246
	ICSSM0_PR1_TX_SOF_INTR_REQ_OUT_1	GICSS0_SPI_IN_247
	ICSSM0_PR1_TX_SOF_INTR_REQ_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_247
DDPA0	DDPA0_DDPA_INTR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_18
	DDPA0_DDPA_INTR_OUT_0	GICSS0_SPI_IN_177
	DDPA0_DDPA_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_177
DSS0	DSS0_DISPC_INTR_REQ_0_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_40
	DSS0_DISPC_INTR_REQ_0_OUT_0	GICSS0_SPI_IN_116
	DSS0_DISPC_INTR_REQ_0_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_24
	DSS0_DISPC_INTR_REQ_1_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_41
	DSS0_DISPC_INTR_REQ_1_OUT_0	GICSS0_SPI_IN_117
	DSS0_DISPC_INTR_REQ_1_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_25
EPWM0	EPWM0_EPWM_ETINT_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_36
	EPWM0_EPWM_ETINT_OUT_0	GICSS0_SPI_IN_229
	EPWM0_EPWM_ETINT_OUT_0	ICSSM0_PR1_SLV_INTR_IN_11
	EPWM0_EPWM_SYNCO_O_OUT_0	TIMESYNC_EVENT_ROUTER0_IN_IN_8
	EPWM0_EPWM_SYNCOUT_OUT_0	EPWM1_EPWM_SYNCIN_IN_0
	EPWM0_EPWM_TRIPZINT_OUT_0	ICSSM0_PR1_SLV_INTR_IN_24

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
EPWM0	EPWM0_EPWM_TRIPZINT_OUT_0	GICSS0_SPI_IN_230
EPWM1	EPWM1_EPWM_ETINT_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_37
	EPWM1_EPWM_ETINT_OUT_0	GICSS0_SPI_IN_231
	EPWM1_EPWM_ETINT_OUT_0	ICSSM0_PR1_SLV_INTR_IN_14
	EPWM1_EPWM_SYNCOUT_OUT_0	EPWM2_EPWM_SYNCIN_IN_0
	EPWM1_EPWM_TRIPZINT_OUT_0	ICSSM0_PR1_SLV_INTR_IN_24
	EPWM1_EPWM_TRIPZINT_OUT_0	GICSS0_SPI_IN_233
EPWM2	EPWM2_EPWM_ETINT_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_38
	EPWM2_EPWM_ETINT_OUT_0	GICSS0_SPI_IN_234
	EPWM2_EPWM_ETINT_OUT_0	ICSSM0_PR1_SLV_INTR_IN_5
	EPWM2_EPWM_TRIPZINT_OUT_0	ICSSM0_PR1_SLV_INTR_IN_24
	EPWM2_EPWM_TRIPZINT_OUT_0	GICSS0_SPI_IN_235
GPU0	GPU0_GPU_OS_IRQ_OUT_0	GICSS0_SPI_IN_118
	GPU0_GPU_OS_IRQ_OUT_1	GICSS0_SPI_IN_119
PBIST0	PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_164
	PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_164
	PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_164
	PBIST0_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_114
	PBIST0_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_157
PBIST1	PBIST1_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_165
	PBIST1_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_165
	PBIST1_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_165
	PBIST1_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_116
	PBIST1_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_156
WKUP_PBIST0	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_170
	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_170

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
WKUP_PBIST0	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_170
	WKUP_PBIST0_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_115
	WKUP_PBIST0_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_158
WKUP_VTM0	WKUP_VTM0_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_139
	WKUP_VTM0_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_11
	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_29
	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_137
	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_8
	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	GICSS0_SPI_IN_183
	WKUP_VTM0_THERM_LVL_GT_TH1_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_183
	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_30
	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_138
	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_10
	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	GICSS0_SPI_IN_184
	WKUP_VTM0_THERM_LVL_GT_TH2_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_184
	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_28
	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_136
	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_9
	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	GICSS0_SPI_IN_185
	WKUP_VTM0_THERM_LVL_LT_TH0_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_185
	WKUP_VTM0_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_140
	WKUP_VTM0_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_12
MAILBOX0_CLUSTER_0	MAILBOX0_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_0	GICSS0_SPI_IN_108
	MAILBOX0_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_1	GICSS0_SPI_IN_109
	MAILBOX0_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_254
	MAILBOX0_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_2	MCU_M4FSS0_CORE0_NVIC_IN_50

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MAILBOX0_CLUSTER_0	MAILBOX0_CLUSTER_0_MAILBOX_CLUSTER_PEND_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_255
MCAN0	MCAN0_MCANSS_ECC_CORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_16
	MCAN0_MCANSS_ECC_UNCORR_LVL_INT_OUT_0	ESM0_ESM_LVL_EVENT_IN_78
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	GICSS0_SPI_IN_186
	MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_186
	MCAN0_MCANSS_FE_OUT_0	PDMA0_MCANSS_MAIN_0_FE_IN_0
	MCAN0_MCANSS_FE_OUT_1	PDMA0_MCANSS_MAIN_0_FE_IN_1
	MCAN0_MCANSS_FE_OUT_2	PDMA0_MCANSS_MAIN_0_FE_IN_2
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	GICSS0_SPI_IN_187
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_187
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	GICSS0_SPI_IN_188
	MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_188
	MCAN0_MCANSS_TX_DMA_OUT_0	PDMA0_MCANSS_MAIN_0_TX_IN_0
	MCAN0_MCANSS_TX_DMA_OUT_1	PDMA0_MCANSS_MAIN_0_TX_IN_1
	MCAN0_MCANSS_TX_DMA_OUT_2	PDMA0_MCANSS_MAIN_0_TX_IN_2
MCU_MCAN0	MCU_MCAN0_MCANSS_ECC_CORR_LVL_INT_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_16
	MCU_MCAN0_MCANSS_ECC_UNCORR_LVL_INT_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_17
	MCU_MCAN0_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_42
	MCU_MCAN0_MCANSS_MCAN_LVL_INT_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_43
	MCU_MCAN0_MCANSS_MCAN_LVL_INT_OUT_1	MCU_M4FSS0_CORE0_NVIC_IN_44

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_MCAN1	MCU_MCAN1_MCANSS_ECC_CORR_LVL_INT_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_18
	MCU_MCAN1_MCANSS_ECC_UNCORR_LVL_INT_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_19
	MCU_MCAN1_MCANSS_EXT_TS_ROLLOVER_LVL_INT_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_45
	MCU_MCAN1_MCANSS_MCAN_LVL_INT_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_46
	MCU_MCAN1_MCANSS_MCAN_LVL_INT_OUT_1	MCU_M4FSS0_CORE0_NVIC_IN_47
MCASP0	MCASP0_REC_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_0_RX_IN_0
	MCASP0_REC_INTR_PEND_OUT_0	GICSS0_SPI_IN_267
	MCASP0_REC_INTR_PEND_OUT_0	ICSSM0_PR1_SLV_INTR_IN_22
	MCASP0_XMIT_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_0_TX_IN_0
	MCASP0_XMIT_INTR_PEND_OUT_0	GICSS0_SPI_IN_268
	MCASP0_XMIT_INTR_PEND_OUT_0	ICSSM0_PR1_SLV_INTR_IN_23
MCASP1	MCASP1_REC_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_1_RX_IN_0
	MCASP1_REC_INTR_PEND_OUT_0	GICSS0_SPI_IN_269
	MCASP1_REC_INTR_PEND_OUT_0	ICSSM0_PR1_SLV_INTR_IN_2
	MCASP1_XMIT_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_1_TX_IN_0
	MCASP1_XMIT_INTR_PEND_OUT_0	GICSS0_SPI_IN_270
	MCASP1_XMIT_INTR_PEND_OUT_0	ICSSM0_PR1_SLV_INTR_IN_1
MCASP2	MCASP2_REC_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_2_RX_IN_0
	MCASP2_REC_INTR_PEND_OUT_0	GICSS0_SPI_IN_271
	MCASP2_REC_INTR_PEND_OUT_0	ICSSM0_PR1_SLV_INTR_IN_28

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCASP2	MCASP2_XMIT_DMA_EVENT_REQ_OUT_0	PDMA2_MCASP_MAIN_2_TX_IN_0
	MCASP2_XMIT_INTR_PEND_OUT_0	GICSS0_SPI_IN_272
	MCASP2_XMIT_INTR_PEND_OUT_0	ICSSM0_PR1_SLV_INTR_IN_27
MCRC64_0	MCRC64_0_DMA_EVENT_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_28
	MCRC64_0_DMA_EVENT_OUT_1	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_29
	MCRC64_0_DMA_EVENT_OUT_2	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_30
	MCRC64_0_DMA_EVENT_OUT_3	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_31
	MCRC64_0_INT_MCRC_OUT_0	GICSS0_SPI_IN_166
	MCRC64_0_INT_MCRC_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_119
MCU_MCRC64_0	MCU_MCRC64_0_INT_MCRC_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_25
	MCU_MCRC64_0_INT_MCRC_OUT_0	GICSS0_SPI_IN_192
	MCU_MCRC64_0_INT_MCRC_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_192
I2C0	I2C0_POINTRPEND_OUT_0	GICSS0_SPI_IN_193
	I2C0_POINTRPEND_OUT_0	ICSSM0_PR1_SLV_INTR_IN_9
	I2C0_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_193
I2C1	I2C1_POINTRPEND_OUT_0	GICSS0_SPI_IN_194
	I2C1_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_194
I2C2	I2C2_POINTRPEND_OUT_0	GICSS0_SPI_IN_195
	I2C2_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_195
I2C3	I2C3_POINTRPEND_OUT_0	GICSS0_SPI_IN_196
	I2C3_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_196
MCU_I2C0	MCU_I2C0_POINTRPEND_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_17
	MCU_I2C0_POINTRPEND_OUT_0	GICSS0_SPI_IN_139
	MCU_I2C0_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_197
WKUP_I2C0	WKUP_I2C0_CLKSTOP_WAKEUP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_143
	WKUP_I2C0_CLKSTOP_WAKEUP_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_0
	WKUP_I2C0_POINTRPEND_OUT_0	GICSS0_SPI_IN_197
	WKUP_I2C0_POINTRPEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_190
pllfracf2_ssmod_16fft0	PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_128
	PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_54
pllfracf2_ssmod_16fft1	PLLFRACF2_SSMOD_16FFT1_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_129
	PLLFRACF2_SSMOD_16FFT1_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_55
pllfracf2_ssmod_16fft12	PLLFRACF2_SSMOD_16FFT12_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_132
	PLLFRACF2_SSMOD_16FFT12_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_58
pllfracf2_ssmod_16fft15	PLLFRACF2_SSMOD_16FFT15_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_133
	PLLFRACF2_SSMOD_16FFT15_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_59

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
pllfracf2_ssmod_16fft16	PLLFRACF2_SSMOD_16FFT16_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_8
	PLLFRACF2_SSMOD_16FFT16_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_7
pllfracf2_ssmod_16fft17	PLLFRACF2_SSMOD_16FFT17_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_7
	PLLFRACF2_SSMOD_16FFT17_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_22
pllfracf2_ssmod_16fft2	PLLFRACF2_SSMOD_16FFT2_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_130
	PLLFRACF2_SSMOD_16FFT2_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_56
pllfracf2_ssmod_16fft8	PLLFRACF2_SSMOD_16FFT8_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_131
	PLLFRACF2_SSMOD_16FFT8_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_57
MCU_pllfracf2_ssmod_16fft0	MCU_PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_134
	MCU_PLLFRACF2_SSMOD_16FFT0_LOCKLOSS_IPCFG_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_47
PSRAMECC_16K0	PSRAMECC_16K0_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_18
	PSRAMECC_16K0_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_80
PSRAMECC0	PSRAMECC0_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_29
	PSRAMECC0_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_90
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_CTI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_175
	WKUP_R5FSS0_CORE0_ECC_CORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_30

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
WKUP_R5FSS0_CORE0	WKUP_R5FSS0_CORE0_ECC_UNCORRECTED_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_91
	WKUP_R5FSS0_CORE0_EXP_INTR_OUT_0	ESM0_ESM_LVL_EVENT_IN_124
	WKUP_R5FSS0_CORE0_EXP_INTR_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_4
	WKUP_R5FSS0_CORE0_PMU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_58
	WKUP_R5FSS0_CORE0_VALFIQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_59
	WKUP_R5FSS0_CORE0_VALIRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_60
WKUP_R5FSS0_COMMON0	WKUP_R5FSS0_COMMON0_COMMRX_LEVEL_0_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_5
	WKUP_R5FSS0_COMMON0_COMMTX_LEVEL_0_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_6
	WKUP_R5FSS0_COMMON0_ECC_DE_TO_ESM_0_OUT_0	ESM0_ESM_LVL_EVENT_IN_40
	WKUP_R5FSS0_COMMON0_ECC_SE_TO_ESM_0_OUT_0	ESM0_ESM_LVL_EVENT_IN_42
WKUP_rtcss0	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0	GICSS0_SPI_IN_132
	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_97
	WKUP_RTCSS0_RTC_EVENT_PEND_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_7
RTI0	RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_160
	RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_160
	RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_160
	RTI0_INTR_WWD_OUT_0	GICSS0_SPI_IN_252
RTI1	RTI1_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_161
	RTI1_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_161
	RTI1_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_161
	RTI1_INTR_WWD_OUT_0	GICSS0_SPI_IN_253
RTI2	RTI2_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_177
	RTI2_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_177
	RTI2_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_177
	RTI2_INTR_WWD_OUT_0	GICSS0_SPI_IN_254
RTI3	RTI3_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_178
	RTI3_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_178
	RTI3_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_178
	RTI3_INTR_WWD_OUT_0	GICSS0_SPI_IN_255
RTI15	RTI15_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_162
	RTI15_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_162
	RTI15_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_162
	RTI15_INTR_WWD_OUT_0	GICSS0_SPI_IN_178
MCU_RTI0	MCU_RTI0_INTR_WWD_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_19

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_RTI0	MCU_RTI0_INTR_WWD_OUT_0	WKUP_ESM0_ESM_PLS_EVENT0_IN_85
	MCU_RTI0_INTR_WWD_OUT_0	WKUP_ESM0_ESM_PLS_EVENT1_IN_85
	MCU_RTI0_INTR_WWD_OUT_0	WKUP_ESM0_ESM_PLS_EVENT2_IN_85
WKUP_RTI0	WKUP_RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT0_IN_163
	WKUP_RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT1_IN_163
	WKUP_RTI0_INTR_WWD_OUT_0	ESM0_ESM_PLS_EVENT2_IN_163
	WKUP_RTI0_INTR_WWD_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_30
SA3_SS0_DMSS_ECCAGGR_0	SA3_SS0_DMSS_ECCAGGR_0_DMSS_ECC_DED_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_118
	SA3_SS0_DMSS_ECCAGGR_0_DMSS_ECC_SEC_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_119
SA3_SS0_INTAGGR_0	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_4	GICSS0_SPI_IN_112
	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_5	GICSS0_SPI_IN_113
	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_6	WKUP_R5FSS0_CORE0_INTR_IN_7
	SA3_SS0_INTAGGR_0_INTAGGR_VINTR_OUT_7	MCU_M4FSS0_CORE0_NVIC_IN_8
SA3_SS0_SA_UL_0	SA3_SS0_SA_UL_0_SA_UL_ECC_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_120
	SA3_SS0_SA_UL_0_SA_UL_ECC_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_121
	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0	GICSS0_SPI_IN_160
	SA3_SS0_SA_UL_0_SA_UL_PKA_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_16
	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0	GICSS0_SPI_IN_161
	SA3_SS0_SA_UL_0_SA_UL_TRNG_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_17
A53SS0	A53SS0_CNTHPIRQ0_OUT_0	GICSS0_PPI0_0_IN_26
	A53SS0_CNTHPIRQ1_OUT_0	GICSS0_PPI0_1_IN_26

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
A53SS0	A53SS0_CNTHPIRQ2_OUT_0	GICSS0_PPI0_2_IN_26
	A53SS0_CNTHPIRQ3_OUT_0	GICSS0_PPI0_3_IN_26
	A53SS0_CNTPNSIRQ0_OUT_0	GICSS0_PPI0_0_IN_30
	A53SS0_CNTPNSIRQ1_OUT_0	GICSS0_PPI0_1_IN_30
	A53SS0_CNTPNSIRQ2_OUT_0	GICSS0_PPI0_2_IN_30
	A53SS0_CNTPNSIRQ3_OUT_0	GICSS0_PPI0_3_IN_30
	A53SS0_CNTPSIRQ0_OUT_0	GICSS0_PPI0_0_IN_29
	A53SS0_CNTPSIRQ1_OUT_0	GICSS0_PPI0_1_IN_29
	A53SS0_CNTPSIRQ2_OUT_0	GICSS0_PPI0_2_IN_29
	A53SS0_CNTPSIRQ3_OUT_0	GICSS0_PPI0_3_IN_29
	A53SS0_CNTVIRQ0_OUT_0	GICSS0_PPI0_0_IN_27
	A53SS0_CNTVIRQ1_OUT_0	GICSS0_PPI0_1_IN_27
	A53SS0_CNTVIRQ2_OUT_0	GICSS0_PPI0_2_IN_27
	A53SS0_CNTVIRQ3_OUT_0	GICSS0_PPI0_3_IN_27
	A53SS0_COMMIRQ0_OUT_0	GICSS0_PPI0_0_IN_22
	A53SS0_COMMIRQ1_OUT_0	GICSS0_PPI0_1_IN_22
	A53SS0_COMMIRQ2_OUT_0	GICSS0_PPI0_2_IN_22
	A53SS0_COMMIRQ3_OUT_0	GICSS0_PPI0_3_IN_22
	A53SS0_CTIIRQ0_OUT_0	GICSS0_PPI0_0_IN_24
	A53SS0_CTIIRQ0_OUT_0	GICSS0_PPI0_1_IN_17
	A53SS0_CTIIRQ0_OUT_0	GICSS0_PPI0_2_IN_17
	A53SS0_CTIIRQ0_OUT_0	GICSS0_PPI0_3_IN_17
	A53SS0_CTIIRQ1_OUT_0	GICSS0_PPI0_0_IN_18
	A53SS0_CTIIRQ1_OUT_0	GICSS0_PPI0_1_IN_24
	A53SS0_CTIIRQ1_OUT_0	GICSS0_PPI0_2_IN_18
	A53SS0_CTIIRQ1_OUT_0	GICSS0_PPI0_3_IN_18
	A53SS0_CTIIRQ2_OUT_0	GICSS0_PPI0_0_IN_19
	A53SS0_CTIIRQ2_OUT_0	GICSS0_PPI0_1_IN_19
	A53SS0_CTIIRQ2_OUT_0	GICSS0_PPI0_2_IN_24
	A53SS0_CTIIRQ2_OUT_0	GICSS0_PPI0_3_IN_19
	A53SS0_CTIIRQ3_OUT_0	GICSS0_PPI0_0_IN_20
	A53SS0_CTIIRQ3_OUT_0	GICSS0_PPI0_1_IN_20
	A53SS0_CTIIRQ3_OUT_0	GICSS0_PPI0_2_IN_20
	A53SS0_CTIIRQ3_OUT_0	GICSS0_PPI0_3_IN_24

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
A53SS0	A53SS0_ECC_ECCAGGR0_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_24
	A53SS0_ECC_ECCAGGR0_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_94
	A53SS0_ECC_ECCAGGR1_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_25
	A53SS0_ECC_ECCAGGR1_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_93
	A53SS0_ECC_ECCAGGR2_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_45
	A53SS0_ECC_ECCAGGR2_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_46
	A53SS0_ECC_ECCAGGR3_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_47
	A53SS0_ECC_ECCAGGR3_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_48
	A53SS0_ECC_ECCAGGR_COREPAC_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_26
	A53SS0_ECC_ECCAGGR_COREPAC_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_95
	A53SS0_EXTERRIRQ_OUT_0	ESM0_ESM_LVL_EVENT_IN_144
	A53SS0_INTERRIRQ_OUT_0	ESM0_ESM_LVL_EVENT_IN_145
	A53SS0_PMUIRQ0_OUT_0	GICSS0_PPI0_0_IN_23
	A53SS0_PMUIRQ1_OUT_0	GICSS0_PPI0_1_IN_23
	A53SS0_PMUIRQ2_OUT_0	GICSS0_PPI0_2_IN_23
	A53SS0_PMUIRQ3_OUT_0	GICSS0_PPI0_3_IN_23
	A53SS0_VCPUMNTIRQ0_OUT_0	GICSS0_PPI0_0_IN_25
	A53SS0_VCPUMNTIRQ1_OUT_0	GICSS0_PPI0_1_IN_25
	A53SS0_VCPUMNTIRQ2_OUT_0	GICSS0_PPI0_2_IN_25
	A53SS0_VCPUMNTIRQ3_OUT_0	GICSS0_PPI0_3_IN_25
COMPUTE_CLUSTER0_PBIST_0	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT0_IN_176
	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT1_IN_176
	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0	ESM0_ESM_PLS_EVENT2_IN_176
	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_CPU_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_113
	COMPUTE_CLUSTER0_PBIST_0_DFT_PBIST_SAFETY_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_44
TIMEOUT0	TIMEOUT0_TIMED_OUT_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_63
	TIMEOUT0_TIMED_OUT_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_26
	TIMEOUT0_TIMED_OUT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_152
DDR16SS0	DDR16SS0_DDRSS_CONTROLLER_OUT_0	GICSS0_SPI_IN_151
	DDR16SS0_DDRSS_CONTROLLER_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_151
	DDR16SS0_DDRSS_DRAM_ECC_CORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_6
	DDR16SS0_DDRSS_DRAM_ECC_UNCORR_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_69

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
DDR16SS0	DDR16SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0	GICSS0_SPI_IN_172
	DDR16SS0_DDRSS_PLL_FREQ_CHANGE_REQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_181
	DDR16SS0_DDRSS_V2A_OTHER_ERR_LVL_OUT_0	ESM0_ESM_LVL_EVENT_IN_110
DEBUGSS0	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	GICSS0_SPI_IN_201
	DEBUGSS0_AQCMPINTR_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_201
	DEBUGSS0_CTM_LEVEL_OUT_0	GICSS0_SPI_IN_202
	DEBUGSS0_CTM_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_202
	DEBUGSS0_DAVDMA_LEVEL_OUT_0	DMASS0_INTAGGR_0_INTAGGR_LEVI_PEND_IN_27
	DEBUGSS0_DAVDMA_LEVEL_OUT_0	USB0_TRACE_INEP_PKT_BUFF_AVAIL_IN_0
	DEBUGSS0_DAVDMA_LEVEL_OUT_0	USB1_TRACE_INEP_PKT_BUFF_AVAIL_IN_0
DFTSS0	DFTSS0_DFT_SAFETY_123_OUT_0	ESM0_ESM_LVL_EVENT_IN_98
	DFTSS0_DFT_SAFETY_MULTI_OUT_0	ESM0_ESM_LVL_EVENT_IN_99
	DFTSS0_DFT_SAFETY_ONE_OUT_0	ESM0_ESM_LVL_EVENT_IN_100
WKUP_TIMEOUT0	WKUP_TIMEOUT0_TIMED_OUT_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_63
	WKUP_TIMEOUT0_TIMED_OUT_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_26
	WKUP_TIMEOUT0_TIMED_OUT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_152
WKUP_ECC_AGGR0	WKUP_ECC_AGGR0_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_20
	WKUP_ECC_AGGR0_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_23
	WKUP_ECC_AGGR0_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_21
	WKUP_ECC_AGGR0_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_24
WKUP_DEEPSLEEP_SOURCES0	WKUP_DEEPSLEEP_SOURCES0_WAKEUP_EVENT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_27
PSC0_ECC_AGGR_0	PSC0_ECC_AGGR_0_FW_CH_BR_ECC_AGGR_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_22
	PSC0_ECC_AGGR_0_FW_CH_BR_ECC_AGGR_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_23
PSC0_FW_0		
PSC0	PSC0_PSC_ALLINT_OUT_0	GICSS0_SPI_IN_203
	PSC0_PSC_ALLINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_146
MCU_TIMEOUT0	MCU_TIMEOUT0_TRANS_ERR_LVL_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_62
	MCU_TIMEOUT0_TRANS_ERR_LVL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_27
	MCU_TIMEOUT0_TRANS_ERR_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_153
MCU_TIMEOUT1	MCU_TIMEOUT1_TRANS_ERR_LVL_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_62

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_TIMEOUT1	MCU_TIMEOUT1_TRANS_ERR_LVL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_27
	MCU_TIMEOUT1_TRANS_ERR_LVL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_153
MCU_MCU_16FF0	MCU_MCU_16FF0_VDD_CORE_GLDTC_STAT_THRESH_HI_FLAG_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_101
	MCU_MCU_16FF0_VDD_CORE_GLDTC_STAT_THRESH_LOW_FLAG_IPCFG_OUT_0	ESM0_ESM_LVL_EVENT_IN_102
MCU_ECC_AGGR0	MCU_ECC_AGGR0_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_14
	MCU_ECC_AGGR0_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_15
WKUP_PSC0	WKUP_PSC0_PSC_ALLINT_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_20
	WKUP_PSC0_PSC_ALLINT_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_145
PDMA0	PDMA0_ECC_DED_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_88
	PDMA0_ECC_SEC_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_15
PDMA1	PDMA1_ECC_DED_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_89
	PDMA1_ECC_SEC_PEND_OUT_0	ESM0_ESM_LVL_EVENT_IN_28
MCU_PRG_MCU_5POKS0	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT0_IN_64
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT1_IN_64
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT2_IN_64
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT0_IN_65
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT1_IN_65
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT2_IN_65
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT0_IN_66
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT1_IN_66
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT2_IN_66
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT0_IN_69
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT1_IN_69
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT2_IN_69
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT0_IN_70
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT1_IN_70
	MCU_PRG_MCU_5POKS0_POK_PGOOD_OV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT2_IN_70
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT0_IN_71
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT1_IN_71
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT2_IN_71
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT0_IN_72
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT1_IN_72

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_PRG_MCU_5POKS0	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT2_IN_72
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT0_IN_73
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT1_IN_73
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT2_IN_73
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT0_IN_76
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT1_IN_76
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT2_IN_76
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT0_IN_77
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT1_IN_77
	MCU_PRG_MCU_5POKS0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT2_IN_77
MCU_PRG_MCU0	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT0_IN_78
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT1_IN_78
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_0	WKUP_ESM0_ESM_PLS_EVENT2_IN_78
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT0_IN_79
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT1_IN_79
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_1	WKUP_ESM0_ESM_PLS_EVENT2_IN_79
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT0_IN_80
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT1_IN_80
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_2	WKUP_ESM0_ESM_PLS_EVENT2_IN_80
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT0_IN_81
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT1_IN_81
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_3	WKUP_ESM0_ESM_PLS_EVENT2_IN_81
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT0_IN_82
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT1_IN_82
	MCU_PRG_MCU0_POK_PGOOD_UV_OUT_N_TO_ESM_OUT_4	WKUP_ESM0_ESM_PLS_EVENT2_IN_82
ECC_AGGR0	ECC_AGGR0_CORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_2
	ECC_AGGR0_UNCORR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_1
WKUP_SAFE_ECC_AGGR0	WKUP_SAFE_ECC_AGGR0_CORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_20
	WKUP_SAFE_ECC_AGGR0_UNCORR_LEVEL_OUT_0	WKUP_ESM0_ESM_LVL_EVENT_IN_21
MCSPI0	MCSPI0_DMA_READ_EVENT_OUT_0	PDMA0_SPI_MAIN_0_RX_IN_0
	MCSPI0_DMA_READ_EVENT_OUT_1	PDMA0_SPI_MAIN_0_RX_IN_1
	MCSPI0_DMA_READ_EVENT_OUT_2	PDMA0_SPI_MAIN_0_RX_IN_2
	MCSPI0_DMA_READ_EVENT_OUT_3	PDMA0_SPI_MAIN_0_RX_IN_3
	MCSPI0_DMA_WRITE_EVENT_OUT_0	PDMA0_SPI_MAIN_0_TX_IN_0

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCSPI0	MCSPI0_DMA_WRITE_EVENT_OUT_1	PDMA0_SPI_MAIN_0_TX_IN_1
	MCSPI0_DMA_WRITE_EVENT_OUT_2	PDMA0_SPI_MAIN_0_TX_IN_2
	MCSPI0_DMA_WRITE_EVENT_OUT_3	PDMA0_SPI_MAIN_0_TX_IN_3
	MCSPI0_INTR_SPI_OUT_0	GICSS0_SPI_IN_204
	MCSPI0_INTR_SPI_OUT_0	ICSSM0_PR1_SLV_INTR_IN_12
	MCSPI0_INTR_SPI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_204
MCSPI1	MCSPI1_DMA_READ_EVENT_OUT_0	PDMA0_SPI_MAIN_1_RX_IN_0
	MCSPI1_DMA_READ_EVENT_OUT_1	PDMA0_SPI_MAIN_1_RX_IN_1
	MCSPI1_DMA_READ_EVENT_OUT_2	PDMA0_SPI_MAIN_1_RX_IN_2
	MCSPI1_DMA_READ_EVENT_OUT_3	PDMA0_SPI_MAIN_1_RX_IN_3
	MCSPI1_DMA_WRITE_EVENT_OUT_0	PDMA0_SPI_MAIN_1_TX_IN_0
	MCSPI1_DMA_WRITE_EVENT_OUT_1	PDMA0_SPI_MAIN_1_TX_IN_1
	MCSPI1_DMA_WRITE_EVENT_OUT_2	PDMA0_SPI_MAIN_1_TX_IN_2
	MCSPI1_DMA_WRITE_EVENT_OUT_3	PDMA0_SPI_MAIN_1_TX_IN_3
	MCSPI1_INTR_SPI_OUT_0	GICSS0_SPI_IN_205
	MCSPI1_INTR_SPI_OUT_0	ICSSM0_PR1_SLV_INTR_IN_15
	MCSPI1_INTR_SPI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_205
MCSPI2	MCSPI2_DMA_READ_EVENT_OUT_0	PDMA0_SPI_MAIN_2_RX_IN_0
	MCSPI2_DMA_READ_EVENT_OUT_1	PDMA0_SPI_MAIN_2_RX_IN_1
	MCSPI2_DMA_READ_EVENT_OUT_2	PDMA0_SPI_MAIN_2_RX_IN_2
	MCSPI2_DMA_READ_EVENT_OUT_3	PDMA0_SPI_MAIN_2_RX_IN_3
	MCSPI2_DMA_WRITE_EVENT_OUT_0	PDMA0_SPI_MAIN_2_TX_IN_0
	MCSPI2_DMA_WRITE_EVENT_OUT_1	PDMA0_SPI_MAIN_2_TX_IN_1
	MCSPI2_DMA_WRITE_EVENT_OUT_2	PDMA0_SPI_MAIN_2_TX_IN_2
	MCSPI2_DMA_WRITE_EVENT_OUT_3	PDMA0_SPI_MAIN_2_TX_IN_3
	MCSPI2_INTR_SPI_OUT_0	GICSS0_SPI_IN_206
	MCSPI2_INTR_SPI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_206
MCU_MCSPI0	MCU_MCSPI0_INTR_SPI_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_22

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_MCSPI0	MCU_MCSPI0_INTR_SPI_OUT_0	GICSS0_SPI_IN_208
	MCU_MCSPI0_INTR_SPI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_207
MCU_MCSPI1	MCU_MCSPI1_INTR_SPI_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_23
	MCU_MCSPI1_INTR_SPI_OUT_0	GICSS0_SPI_IN_209
	MCU_MCSPI1_INTR_SPI_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_208
UART0	UART0_USART_DMA_OUT_0	PDMA1_USART_MAIN_0_TX_IN_0
	UART0_USART_DMA_OUT_1	PDMA1_USART_MAIN_0_RX_IN_0
	UART0_USART_IRQ_OUT_0	GICSS0_SPI_IN_210
	UART0_USART_IRQ_OUT_0	ICSSM0_PR1_SLV_INTR_IN_19
	UART0_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_210
UART1	UART1_USART_DMA_OUT_0	PDMA1_USART_MAIN_1_TX_IN_0
	UART1_USART_DMA_OUT_1	PDMA1_USART_MAIN_1_RX_IN_0
	UART1_USART_IRQ_OUT_0	GICSS0_SPI_IN_211
	UART1_USART_IRQ_OUT_0	ICSSM0_PR1_SLV_INTR_IN_0
	UART1_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_211
UART2	UART2_USART_DMA_OUT_0	PDMA1_USART_MAIN_2_TX_IN_0
	UART2_USART_DMA_OUT_1	PDMA1_USART_MAIN_2_RX_IN_0
	UART2_USART_IRQ_OUT_0	GICSS0_SPI_IN_212
	UART2_USART_IRQ_OUT_0	ICSSM0_PR1_SLV_INTR_IN_20
	UART2_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_212
UART3	UART3_USART_DMA_OUT_0	PDMA1_USART_MAIN_3_TX_IN_0
	UART3_USART_DMA_OUT_1	PDMA1_USART_MAIN_3_RX_IN_0
	UART3_USART_IRQ_OUT_0	GICSS0_SPI_IN_213
	UART3_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_213
UART4	UART4_USART_DMA_OUT_0	PDMA1_USART_MAIN_4_TX_IN_0
	UART4_USART_DMA_OUT_1	PDMA1_USART_MAIN_4_RX_IN_0
	UART4_USART_IRQ_OUT_0	GICSS0_SPI_IN_214
	UART4_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_214
UART5	UART5_USART_DMA_OUT_0	PDMA1_USART_MAIN_5_TX_IN_0
	UART5_USART_DMA_OUT_1	PDMA1_USART_MAIN_5_RX_IN_0
	UART5_USART_IRQ_OUT_0	GICSS0_SPI_IN_215
	UART5_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_215
UART6	UART6_USART_DMA_OUT_0	PDMA1_USART_MAIN_6_TX_IN_0
	UART6_USART_DMA_OUT_1	PDMA1_USART_MAIN_6_RX_IN_0
	UART6_USART_IRQ_OUT_0	GICSS0_SPI_IN_216
	UART6_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_216

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
MCU_UART0	MCU_UART0_USART_IRQ_OUT_0	MCU_M4FSS0_CORE0_NVIC_IN_24
	MCU_UART0_USART_IRQ_OUT_0	GICSS0_SPI_IN_217
	MCU_UART0_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_217
WKUP_UART0	WKUP_UART0_CLKSTOP_WAKEUP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_144
	WKUP_UART0_CLKSTOP_WAKEUP_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_1
	WKUP_UART0_USART_IRQ_OUT_0	GICSS0_SPI_IN_218
	WKUP_UART0_USART_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_219
USB0	USB0_A_ECC_AGGR_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_35
	USB0_A_ECC_AGGR_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_111
	USB0_HOST_SYSTEM_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_32
	USB0_IRQ_OUT_0	GICSS0_SPI_IN_220
	USB0_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_220

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
USB0	USB0_IRQ_OUT_1	GICSS0_SPI_IN_221
	USB0_IRQ_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_221
	USB0_IRQ_OUT_2	GICSS0_SPI_IN_222
	USB0_IRQ_OUT_2	WKUP_R5FSS0_CORE0_INTR_IN_222
	USB0_IRQ_OUT_3	GICSS0_SPI_IN_223
	USB0_IRQ_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_223
	USB0_IRQ_OUT_4	GICSS0_SPI_IN_224
	USB0_IRQ_OUT_4	WKUP_R5FSS0_CORE0_INTR_IN_224
	USB0_IRQ_OUT_5	GICSS0_SPI_IN_225
	USB0_IRQ_OUT_5	WKUP_R5FSS0_CORE0_INTR_IN_225
	USB0_IRQ_OUT_6	GICSS0_SPI_IN_226
	USB0_IRQ_OUT_6	WKUP_R5FSS0_CORE0_INTR_IN_226
	USB0_IRQ_OUT_7	GICSS0_SPI_IN_227
	USB0_IRQ_OUT_7	WKUP_R5FSS0_CORE0_INTR_IN_227
	USB0_MISC_LEVEL_OUT_0	GICSS0_SPI_IN_228
	USB0_MISC_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_228
	USB0_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_61
	USB0_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_9
USB1	USB1_A_ECC_AGGR_CORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_146
	USB1_A_ECC_AGGR_UNCORRECTED_ERR_LEVEL_OUT_0	ESM0_ESM_LVL_EVENT_IN_147
	USB1_HOST_SYSTEM_ERROR_OUT_0	ESM0_ESM_LVL_EVENT_IN_33
	USB1_IRQ_OUT_0	GICSS0_SPI_IN_258
	USB1_IRQ_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_230
	USB1_IRQ_OUT_1	GICSS0_SPI_IN_259
	USB1_IRQ_OUT_1	WKUP_R5FSS0_CORE0_INTR_IN_231
	USB1_IRQ_OUT_2	GICSS0_SPI_IN_260
	USB1_IRQ_OUT_2	WKUP_R5FSS0_CORE0_INTR_IN_232
	USB1_IRQ_OUT_3	GICSS0_SPI_IN_261
	USB1_IRQ_OUT_3	WKUP_R5FSS0_CORE0_INTR_IN_233
	USB1_IRQ_OUT_4	GICSS0_SPI_IN_262
	USB1_IRQ_OUT_4	WKUP_R5FSS0_CORE0_INTR_IN_234
	USB1_IRQ_OUT_5	GICSS0_SPI_IN_263
	USB1_IRQ_OUT_5	WKUP_R5FSS0_CORE0_INTR_IN_235
	USB1_IRQ_OUT_6	GICSS0_SPI_IN_264

Table 1-9. Interrupts (Outputs) (continued)

Instance	Interrupt Output Line	Destination Interrupt
USB1	USB1_IRQ_OUT_6	WKUP_R5FSS0_CORE0_INTR_IN_236
	USB1_IRQ_OUT_7	GICSS0_SPI_IN_265
	USB1_IRQ_OUT_7	WKUP_R5FSS0_CORE0_INTR_IN_237
	USB1_MISC_LEVEL_OUT_0	GICSS0_SPI_IN_266
	USB1_MISC_LEVEL_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_238
	USB1_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0	WKUP_R5FSS0_CORE0_INTR_IN_62
	USB1_USB_WAKEUP_CLKSTOP_WAKEUP_OUT_0	WKUP_DEEPSLEEP_SOURCES0_ISAM62_DM_WAKEUP_DEEPSLEEP_SOURCES_IN_10