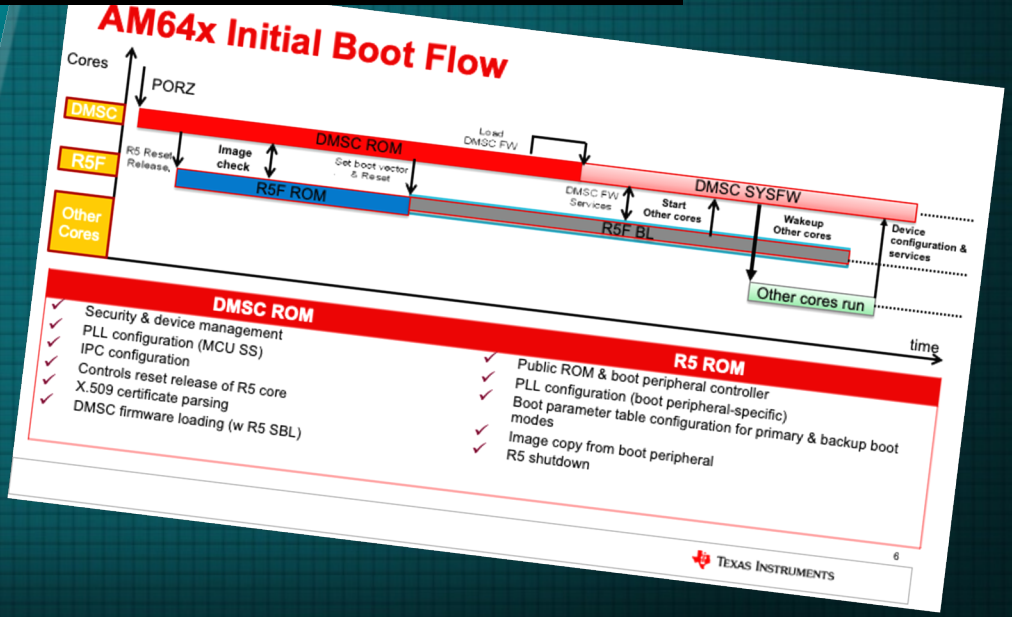
AM64X LINUX BOOT PROCESS

FROM DEVICE INITIALIZATION TO KERNEL PROMPT



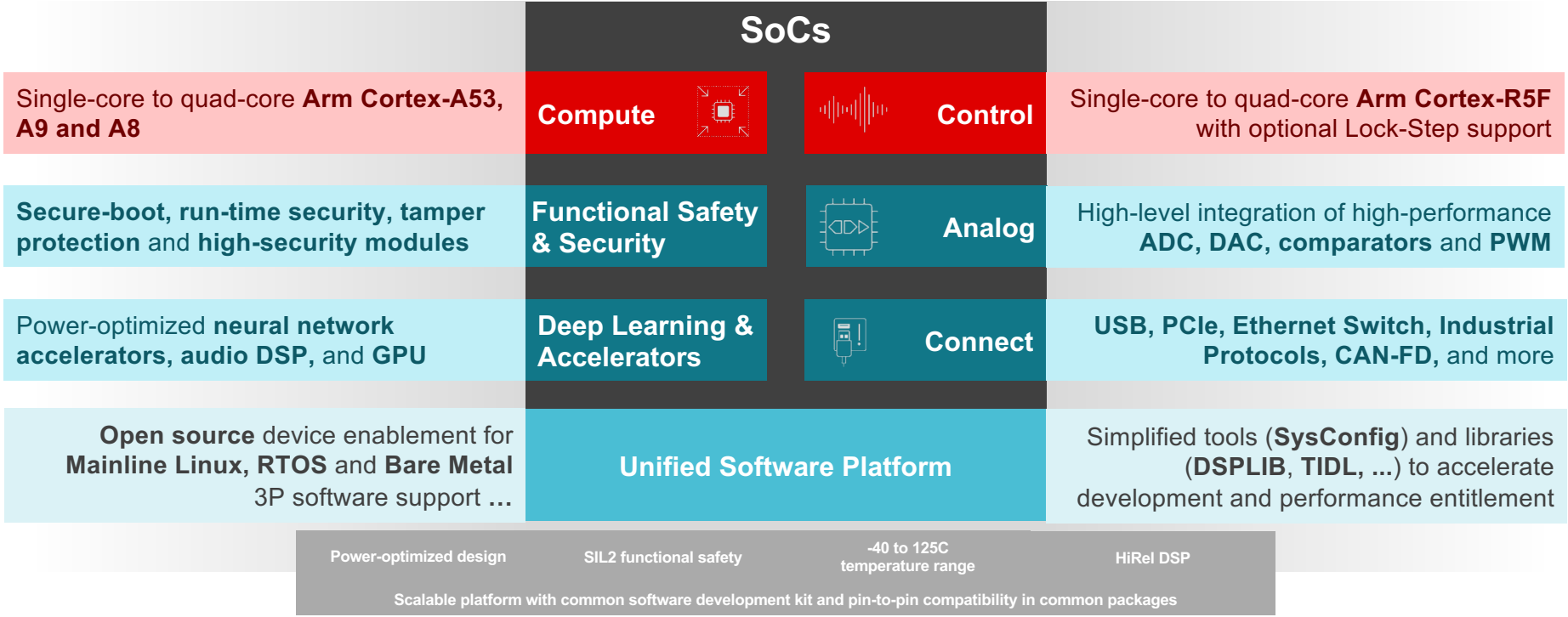
Agenda

- Short Overview
- Device Initialization Process
- Boot Architecture and Flow
- Linux Boot Flow
- Demo: Linux Boot on AM64x EVM
- Summary

Sitara overview

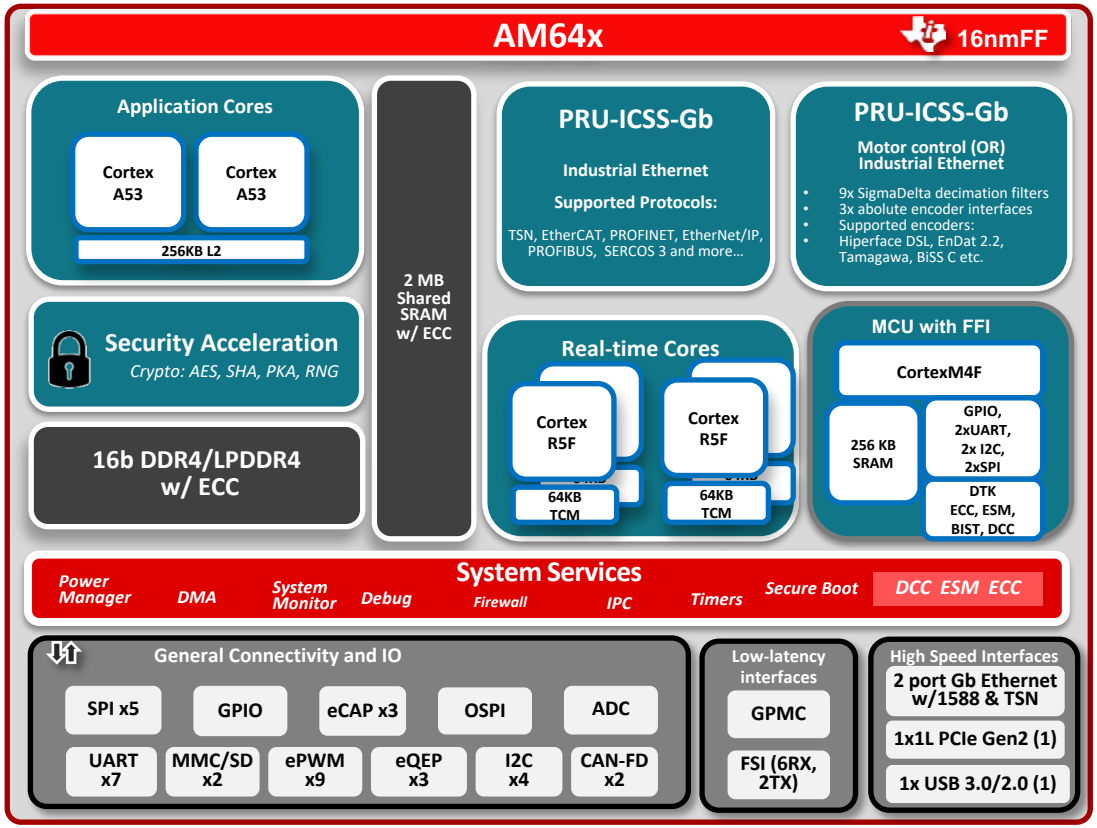
Sitara™ Arm® Processors
Texas Instruments

Scalable, cost-optimized portfolio with accelerators, analog integration, robust connectivity, security and functional safety designed for industrial markets



AM64x (17mm x 17mm) Cortex®-A53 based processors

- **Cores & Memory**
  - Dual Cortex-A53 up to 1GHz
  - Dual or Quad Cortex-R5F up to 800MHz
  - >2MB on-chip SRAM
  - ECC on all critical memories
  - 16b LPDDR4/DDR4 controller with **inline** ECC
- **Functional safety features**
  - 400MHz Cortex-M4F subsystem has **freedom from interference** to enable usage as a safety monitor
    - Dedicated Peripherals I2C, SPI, UART & GPIO
    - Tightly coupled memory of 256KB
  - Diagnostic tool kit for entire SoC voltage, temp, clock, ECC monitors and Error signaling
- **2xPRU-ICSS-Gb**
  - Enables up to 2x Gb industrial Ethernet protocols
  - 1x industrial Ethernet protocol + motor control current and position feedback
- **Peripheral / IO Highlight**
  - GPMC (32b parallel bus) and FSI (serial connection for use with TI's C2000 MCUs) offer low-latency interfaces to motor control front-end
  - PCIe Gen2, USB3.0/2.0, and 2-port Gb Ethernet Switch CPSW provide high-speed (Gbps) connectivity options
  - RS485 support on UART
  - Octal/Quad-SPI with execution-in-place support
- **Integrated analog**
  - 8-channel, 12-bit ADC with 4 Msps
  - Simplified power solution, Integrated Voltage Monitors
- **Package**
  - 17.2 x 17.2mm, 0.8mm ball pitch

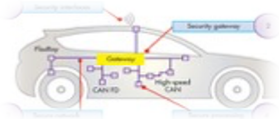


(1) PCIe and USB 3.0 share the same SERDES

Sitara built around a unified software platform

100% code compatibility

Industrial HMI / Auto Cluster



Telematics and Gateway

FAC / Motor Drives

Network & Control

System Performance

Connections from sensor to cloud

Integration and System Cost

Safety

&

Security

TI supported tools and partner ecosystem

AM64x Boot Overview

Device Initialization Process

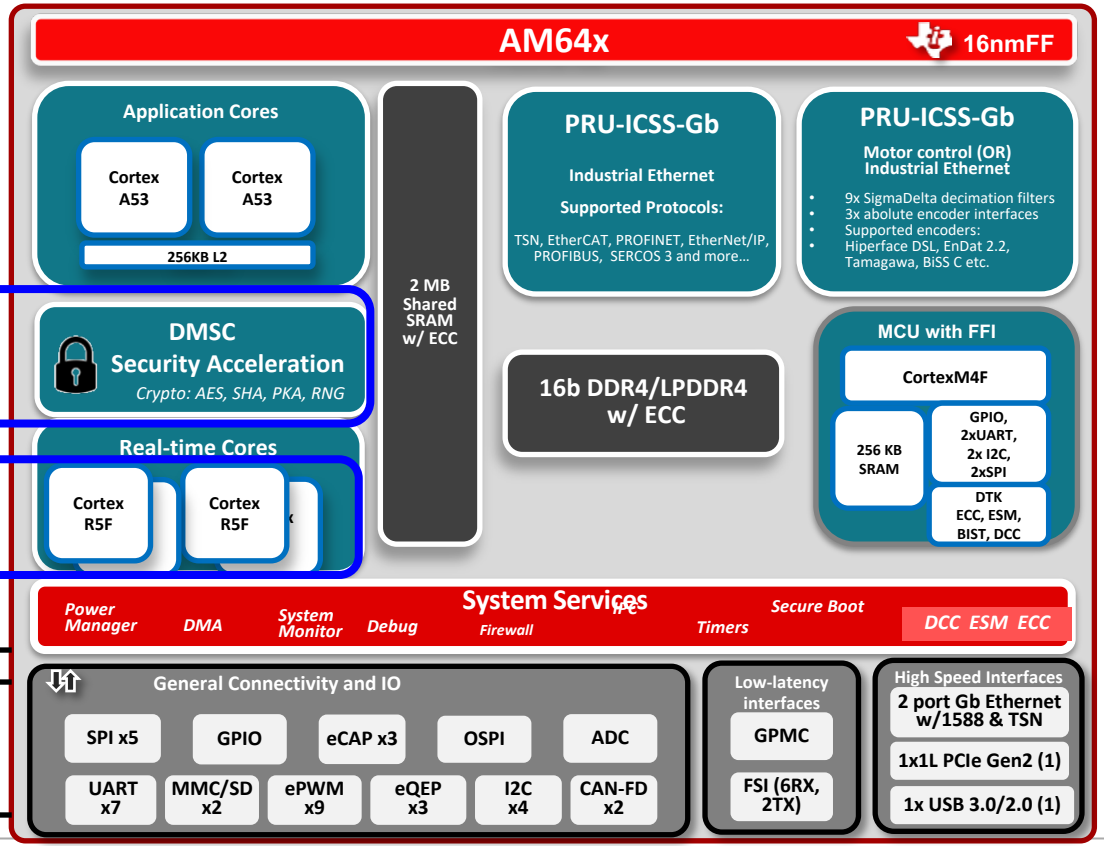
- **Preinitialization:** Power, clock, and control connections must be present, and the boot configuration pins must be held at the desired logical levels.
- **Power, clock, reset ramp sequence:** Specific sequence that is applied by the power-management chip(s)
- **ROM code:** Two ROM codes that operate together (DMSC ROM & R5 ROM). Responsible for finding, downloading, and executing the initial software (SBL/SPL)
- **Initial software (SBL or SPL) :** Software that loads, prepares, and passes control to application software or to a high-level operating system (HLOS)
  - Secondary Boot Loader (SBL) for RTOS or generic boot
  - Secondary Program Loader (SPL) for U-Boot
- **High-Level Operating System (HLOS)** or other SW applications that run on other core(s)

The first two steps above are hardware-oriented, but the specific flow is also related to the settings of the system configuration (Boot Mode) pins of the device.

AM64x Common Boot Architecture

- DMSC – Security Domain
- MCU R5 – Boot Control

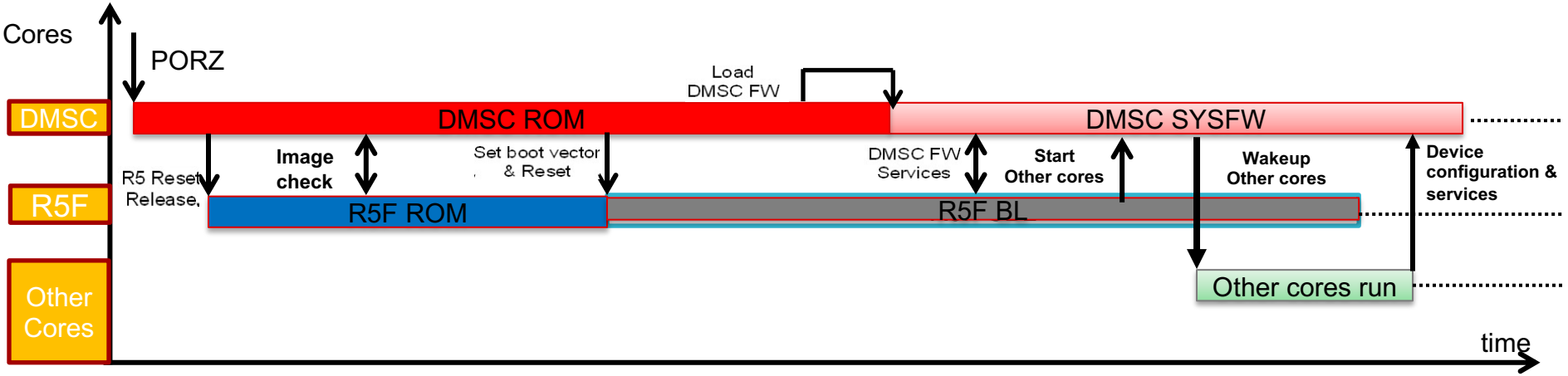
Boot Mode Pins [15:0]



Boot Flow Overview – Terminology

- **DMSC** – Device Management & Security Controller:
  - Controller that runs the first set of instructions on AM6x device
  - Executes the DMSC ROM code after reset
- **Cortex-R5F** – Boot Controller:
  - Cortex-R5F core that controls the rest of the boot flow of the device, after it has been released from reset by the DMSC
  - Executes the R5 ROM code after reset
- **R5 SBL** or **SPL** – Secondary bootloader:
  - Code loaded by R5, via the selected boot method via Boot Mode pins, and authenticated by the DMSC
  - MCU R5 runs this code after the ROM execution to start the flow for booting all the other cores on the device
- **SYSFW** – System Firmware (for DMSC):
  - DMSC “steady-state” firmware loaded by R5 and imported & authenticated by the DMSC. After the SYSFW image has been verified, the DMSC starts executing it.

AM64x Initial Boot Flow



DMSC ROM

- ✓ Security & device management
- ✓ PLL configuration (MCU SS)
- ✓ IPC configuration
- ✓ Controls reset release of R5 core
- ✓ X.509 certificate parsing
- ✓ DMSC firmware loading (w R5 SBL)

R5 ROM

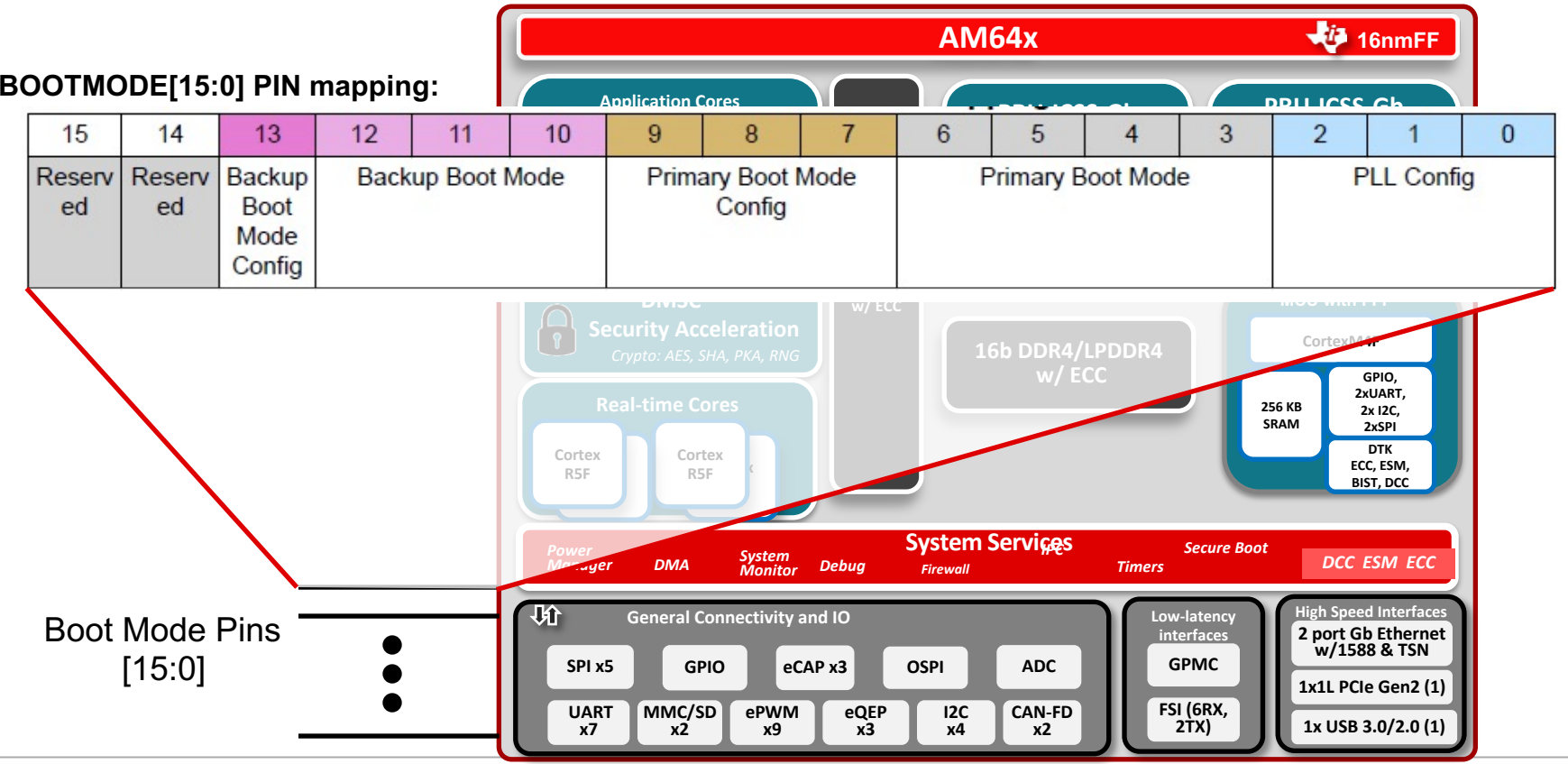
- ✓ Public ROM & boot peripheral controller
- ✓ PLL configuration (boot peripheral-specific)
- ✓ Boot parameter table configuration for primary & backup boot modes from Boot Mode Pins
- ✓ Image copy from memory or peripheral
- ✓ R5 shutdown

Questions

Boot Mode Pins

BOOTMODE[15:0] PIN mapping:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Backup Boot Mode Config	Backup Boot Mode			Primary Boot Mode Config			Primary Boot Mode				PLL Config		



Boot Mode Pins [15:0]

BOOTMODE PLL Config

BOOTMODE[15:0] PIN mapping:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Backup Boot Mode Config	Backup Boot Mode			Primary Boot Mode Config			Primary Boot Mode				PLL Config		

PLL Reference Clock Selection:

PLL Config Pins			Ref Clock (MHz)
B2	B1	B0	
0	0	0	19.2
0	0	1	20
0	1	0	24
0	1	1	25
1	0	0	26
1	0	1	27(1)
1	1	0	Reserved
1	1	1	Reserved

BOOTMODE Primary Boot Mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Backup Boot Mode Config	Backup Boot Mode			Primary Boot Mode Config			Primary Boot Mode				PLL Config		

Primary Boot Mode Config							Primary Boot Mode
B9	B8	B7	B6	B5	B4	B3	
Reserved	Reserved	Reserved	0	0	0	0	Reserved
Speed	Iclk	Csel	0	0	0	1	OSPI
Reserved	Iclk	Csel	0	0	1	0	QSPI
Reserved	Mode	Csel	0	0	1	1	SPI
Clkout	Delay	Link stat	0	1	0	0	Ethernet RGMII
Clkout	Clk src	Reserved	0	1	0	1	Ethernet RMII
Bus reset	Reserved	Addr	0	1	1	0	I2C
Reserved	Reserved	Reserved	0	1	1	1	UART
Port	Reserved	Fs/raw	1	0	0	0	MMCSD card
Reserved	Reserved	Reserved	1	0	0	1	eMMC
Core Volt	Mode	Lane Swap	1	0	1	0	USB
Reserved	Reserved	Reserved	1	0	1	1	GPMC NAND
Reserved	Reserved	Reserved	1	1	0	0	GPMC NOR
Reserved	Reserved	Clocking	1	1	0	1	PCIe
SFPD	Read Cmd	Mode	1	1	1	0	xSPI
Reserved	Reserved	No/Dev	1	1	1	1	No-boot/Dev boot

More information in Ch. 4 of TRM

BOOTMODE Primary Boot Mode - Configuration

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Backup Boot Mode Config	Backup Boot Mode			Primary Boot Mode Config			Primary Boot Mode				PLL Config		

Value	Description
0	MMC Port 0 (8 bit width)
1	MMC Port 1 (4 bit width)

Value	Description
0	Filesystem Mode
1	Raw Mode

Primary Boot Mode Config							Primary Boot Mode
B9	B8	B7	B6	B5	B4	B3	
eserved						0	Reserved
Iclk						1	OSPI
Iclk						0	QSPI
Mode						1	SPI
Delay						0	Ethernet RGMII
Clkout	Clk src	Reserved	0	1	0	1	Ethernet RMII
Bus reset	Reserved	Addr	0	1	1	0	I2C
Reserved	Reserved	Reserved	0	1	1	1	UART
Port	Reserved	Fs/raw	1	0	0	0	MMCSD card
Reserved	Reserved	Reserved	1	0	0	1	eMMC
Core Volt	Mode	Lane Swap	1	0	1	0	USB
Reserved	Reserved	Reserved	1	0	1	1	GPMC NAND
Reserved	Reserved	Reserved	1	1	0	0	GPMC NOR
Reserved	Reserved	Clocking	1	1	0	1	PCIe
SFPD	Read Cmd	Mode	1	1	1	0	xSPI
Reserved	Reserved	No/Dev	1	1	1	1	No-boot/Dev boot

More information in Ch. 4 of TRM

Boot Image Format

- All boot images need X.509 certificate appended with boot binary for both General Purpose (GP) and High Secure (HS) devices.
- The X.509 certificate is described in RFC5280. Section 4.1 describes the format.
- Boot ROM uses an extension of standard X.509 certificate.

R5-BL image format:

- R5 reset vector provides entry point of R5-BL binary
- Boot extensions of X.509 certificate contains destination address and boot core information.

DMSC SYSFW firmware image format:

- M3 reset vector should be the entry point of DMSC firmware binary
- Boot extensions of X.509 certificate should be updated for destination address and boot core.

DMSC SYSFW

Overview:

- Centralized control of SoC system functions including power management, resource management, and security services.
- DMSC firmware uses TI SCI protocol messages from all cores.

SYSFW Roles:

- Resource management:
  - Initial device setup
  - Resource allocation
- Power management:
  - Device power modes control
  - Clock/Reset control
  - PM services to OS (Idle, etc.)
  - Low power mode entry/exit
- Security:
  - Firewall management
  - Key management
  - Runtime secure services

Hand off from DMSC ROM to SYSFW:

- DMSC SYSFW loading:
  - R5 ROM loads the DMSC SYSFW to OCRAM.
  - DMSC ROM check integrity and loads firmware to its internal memory and passes control to firmware.
- Board configuration for SYSFW module initialization:
  - Base configuration initialization
  - PM initialization
  - RM initialization
  - Security initialization
- Board configuration module enables one-time (per boot), application-specific configuration.

R5 Boot Loader (SBL or SPL)

R5 Boot Loader Functions:

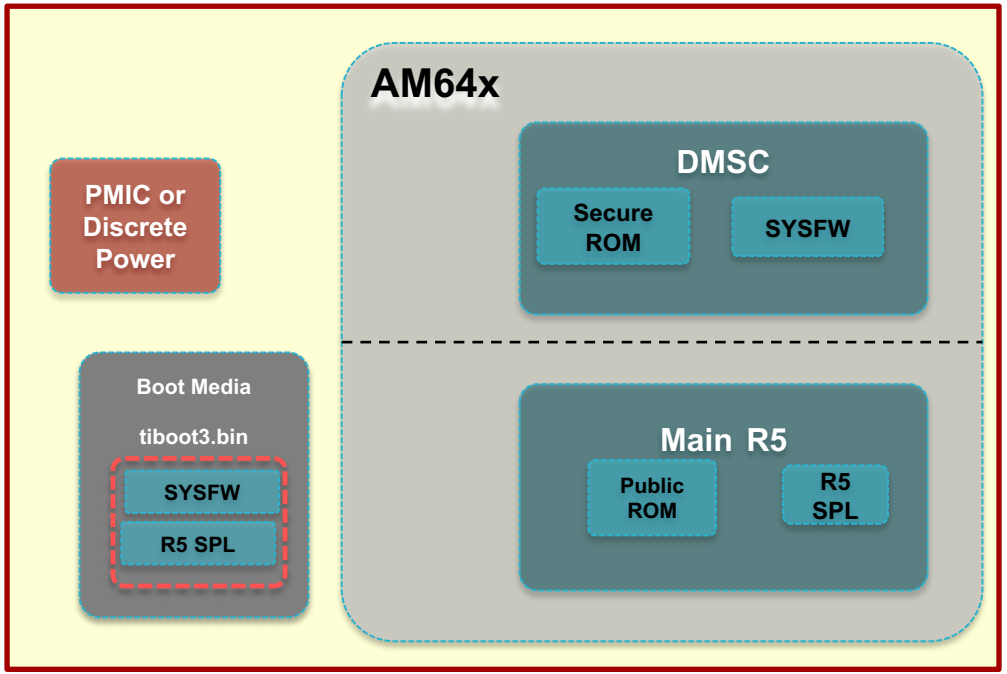
- Executes from internal memory (OC RAM) and small part of ATCM memory
- Initialization of MCU subsystem
- Enables MCU UART for debug logging
- Sends board configuration messages to initialize SYSFW
- Configures PinMux and configures DDR and remaining initialization
- Loads application image(s) for each of the core(s) into device memory
- Communicates with system firmware to setup the clocks for cores and releases them from reset
- Starts execution on slave cores at entry point of corresponding applications
- MCU core then starts executing from entry point for its own application and exits R5 Boot Loader

Linux Boot Flow

Boot Flow Overview – Terminology (Linux)

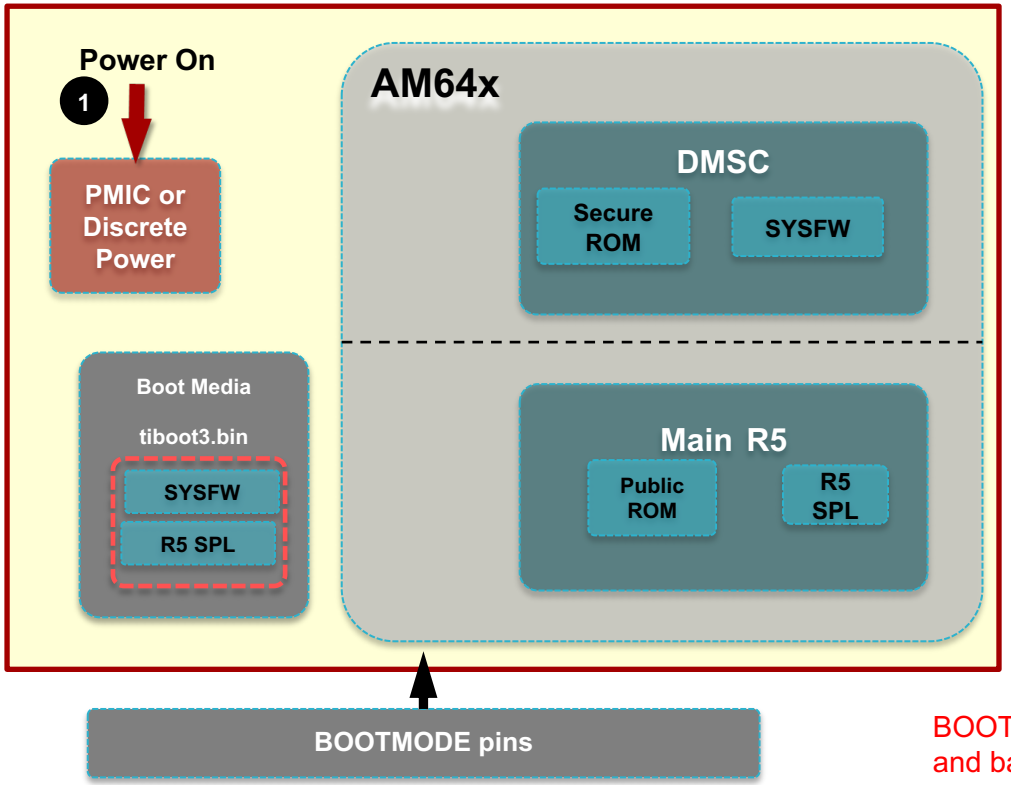
- **ATF** – ARM Trusted Firmware:
  - ARMv8 secure firmware for the Cortex-A cores on the device.
  - Acts as the 'Secure Monitor' on A53 and handles A53 initialization as well as loading of the subsequent secure & non-secure images to be run on the A53 cores.
- **OPTEE** – Open Portable Trusted Execution Environment:
  - An open-source TEE maintained by Linaro. Used as the Secure-world OS running on the A53 cores. Loaded as part of the ATF initialization sequence for the Cortex-A cores.
- **A53 SPL** – U-Boot Secondary Program Loader:
  - The SPL is loaded by ATF as the first Non-secure code that is started on the A53
- **U-boot** – Bootloader for A53 Linux and for SW on other R5 cores

Linux Boot Flow (1/2)



BOOTMODE pins value is latched upon POR, and select primary and backup boot modes and peripheral configuration.

Linux Boot Flow (1/2)

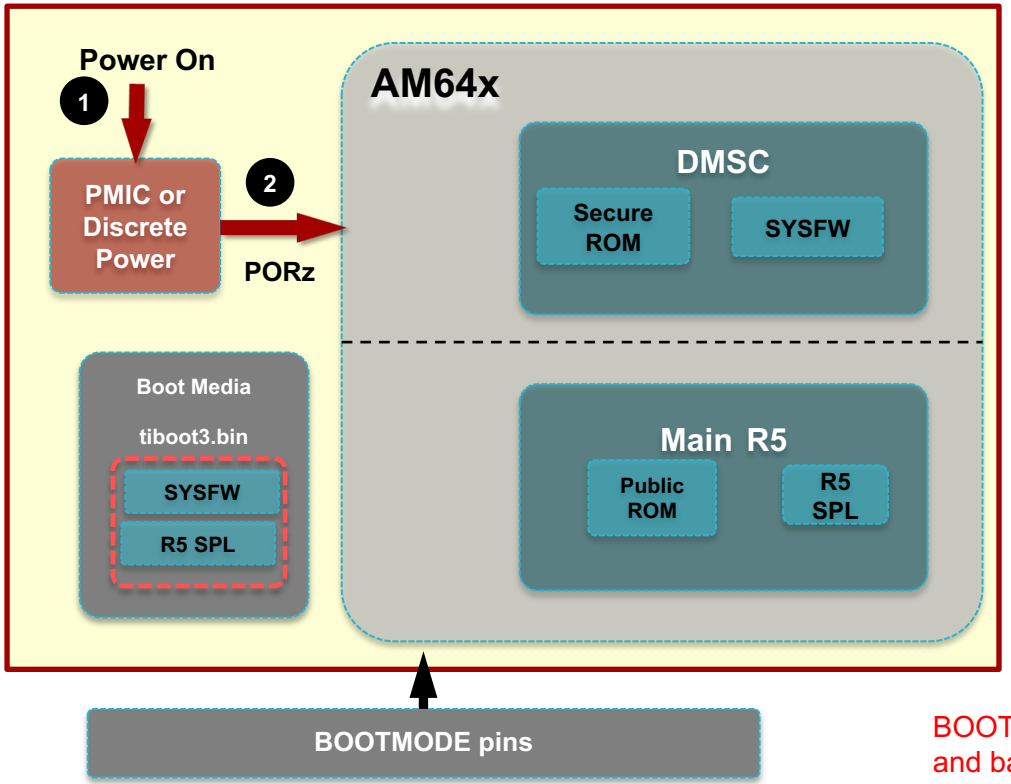


Initial Boot Flow (mandatory)

1. System Power On

BOOTMODE pins value is latched upon POR, and select primary and backup boot modes and peripheral configuration.

Linux Boot Flow (1/2)

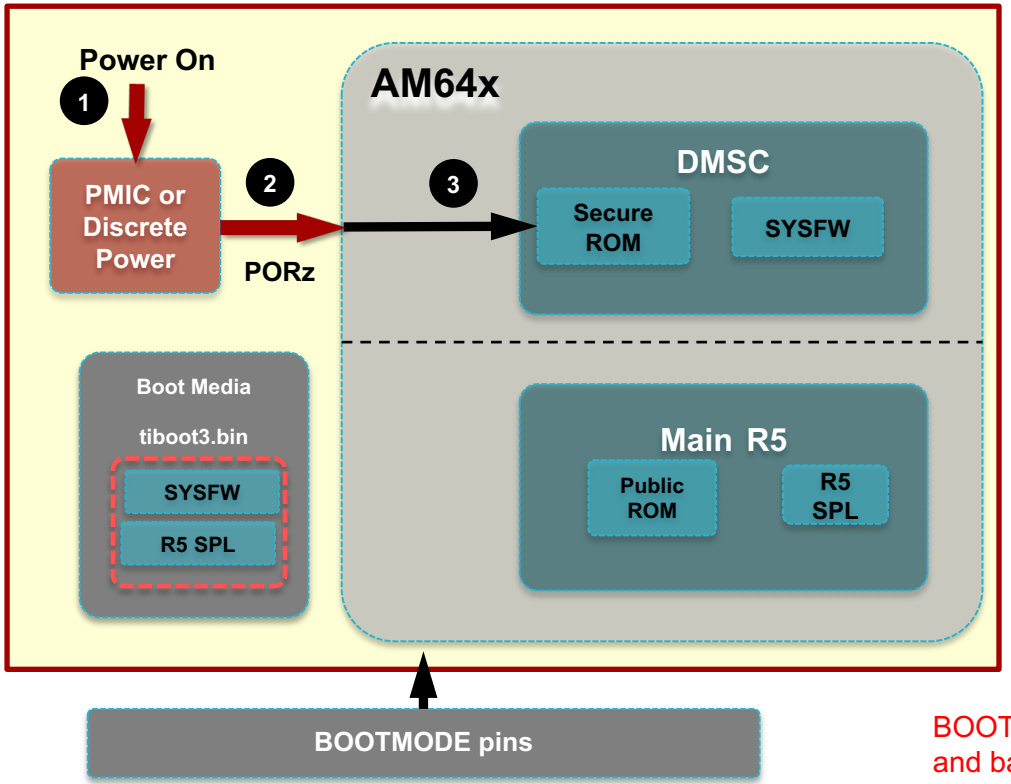


Initial Boot Flow (mandatory)

1. System Power On
2. PMIC releases SoC PoRz

BOOTMODE pins value is latched upon POR, and select primary and backup boot modes and peripheral configuration.

Linux Boot Flow (1/2)

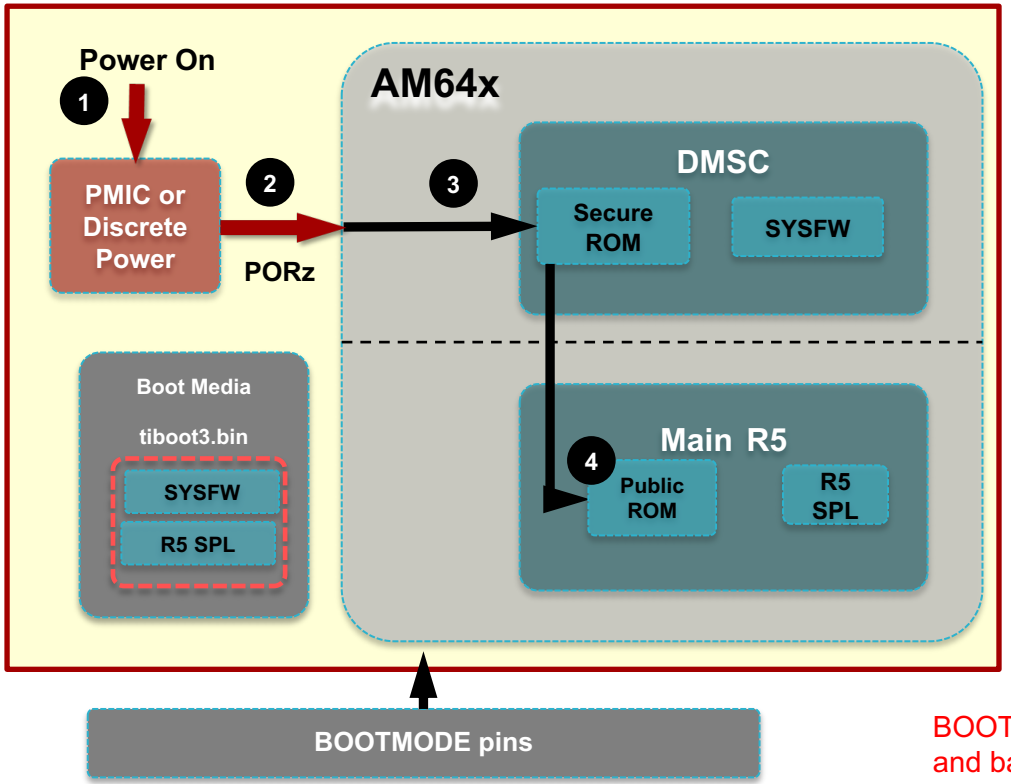


Initial Boot Flow (mandatory)

1. System Power On
2. PMIC releases SoC PoRz
3. DMSC ROM Starts/Basic Init

BOOTMODE pins value is latched upon POR, and select primary and backup boot modes and peripheral configuration.

Linux Boot Flow (1/2)

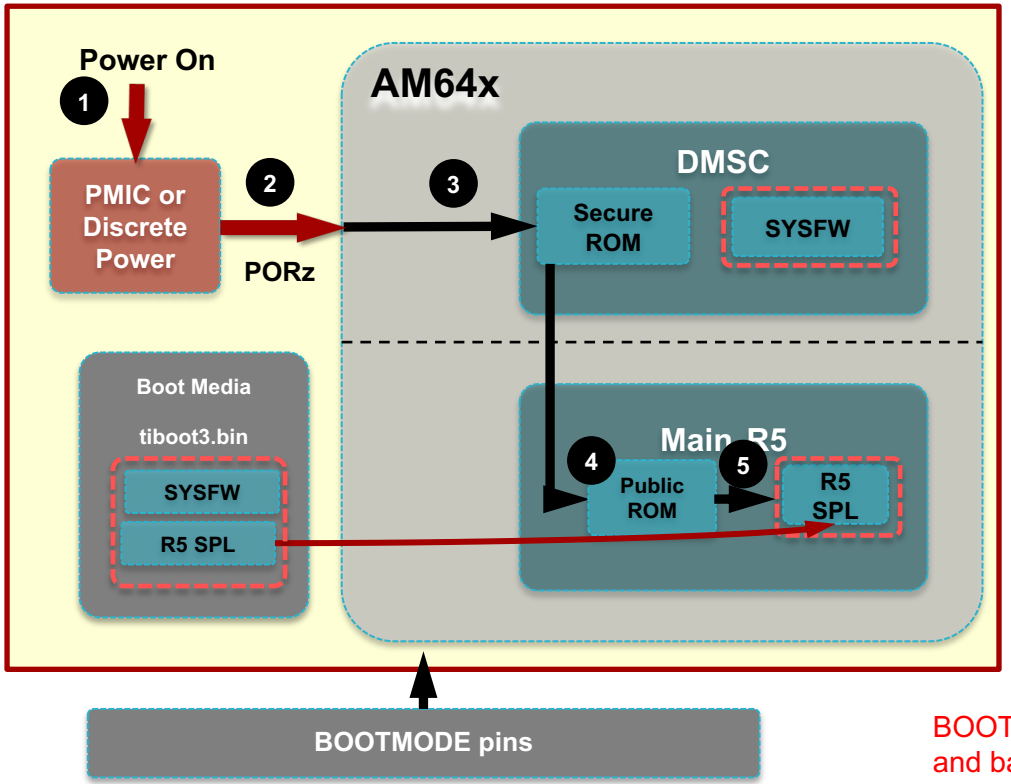


Initial Boot Flow (mandatory)

1. System Power On
2. PMIC releases SoC PoRz
3. DMSC ROM Starts/Basic Init
4. Main R5 ROM starts / Boot Periph Init

BOOTMODE pins value is latched upon POR, and select primary and backup boot modes and peripheral configuration.

Linux Boot Flow (1/2)

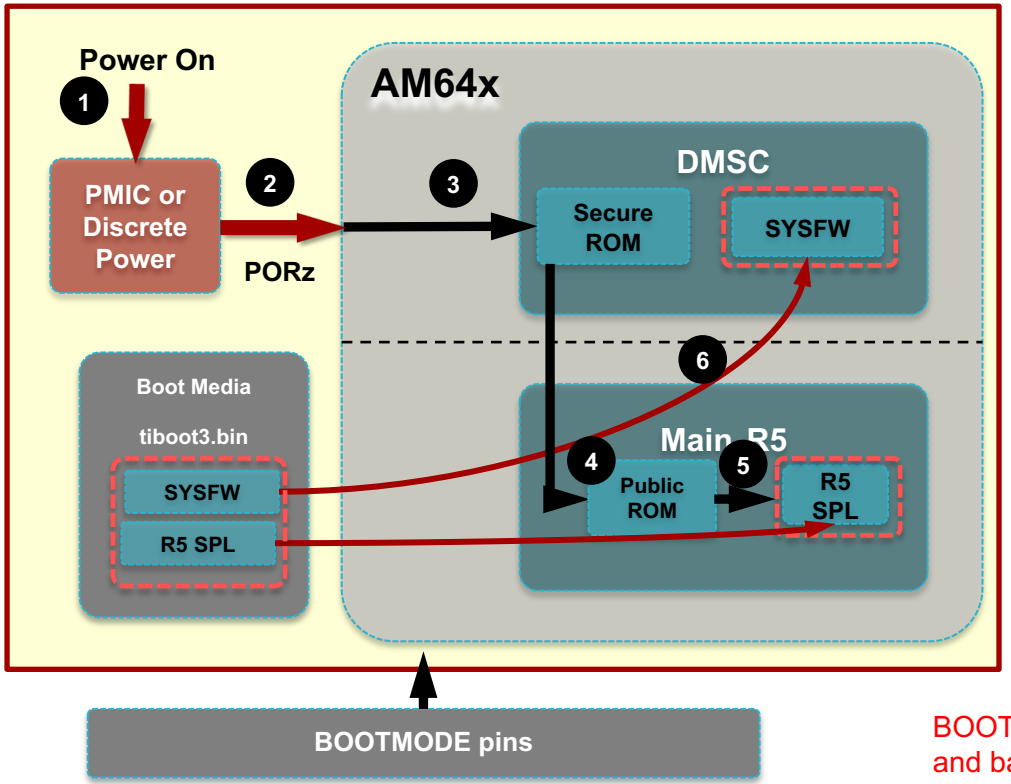


Initial Boot Flow (mandatory)

1. System Power On
2. PMIC releases SoC PoRz
3. DMSC ROM Starts/Basic Init
4. Main R5 ROM starts / Boot Periph Init
5. Main R5 ROM loads & starts R5 SPL

BOOTMODE pins value is latched upon POR, and select primary and backup boot modes and peripheral configuration.

Linux Boot Flow (1/2)

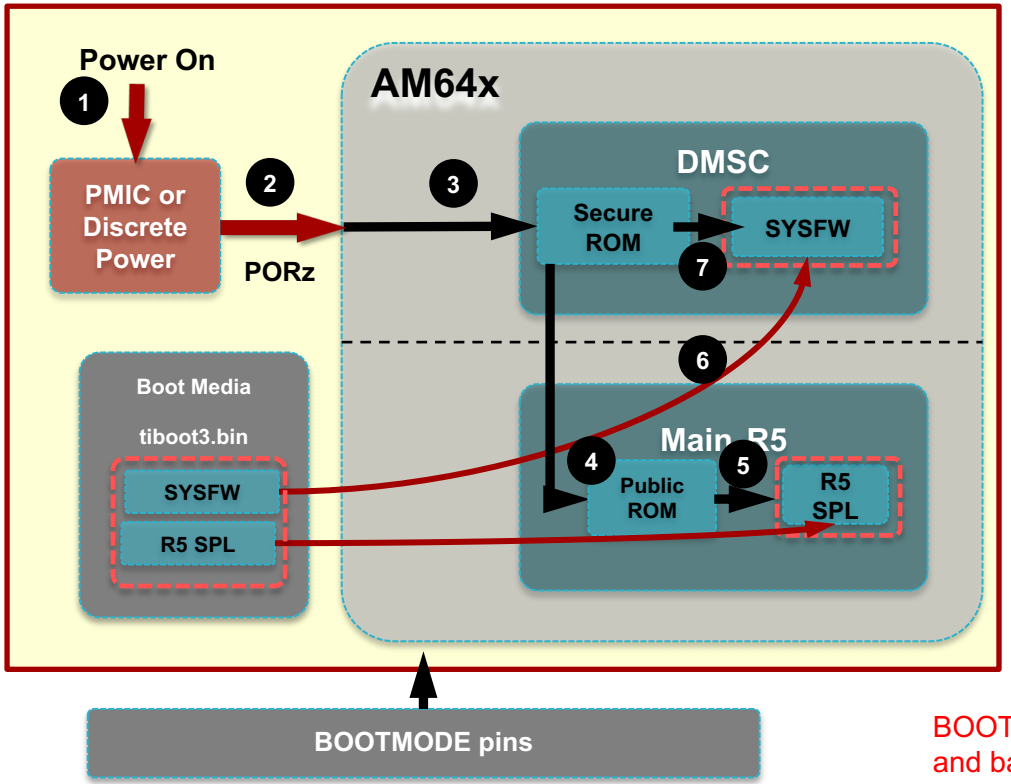


Initial Boot Flow (mandatory)

1. System Power On
2. PMIC releases SoC PoRz
3. DMSC ROM Starts/Basic Init
4. Main R5 ROM starts / Boot Periph Init
5. Main R5 ROM loads & starts R5 SPL
6. DMSC ROM loads SYSFW

BOOTMODE pins value is latched upon POR, and select primary and backup boot modes and peripheral configuration.

Linux Boot Flow (1/2)



Initial Boot Flow (mandatory)

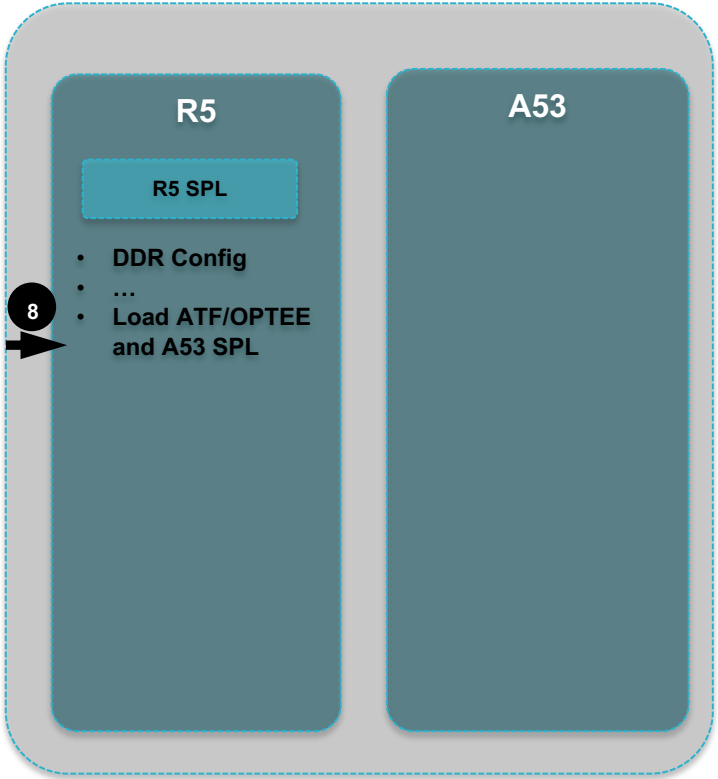
1. System Power On
2. PMIC releases SoC PoRz
3. DMSC ROM Starts/Basic Init
4. Main R5 ROM starts / Boot Periph Init
5. Main R5 ROM loads & starts R5 SPL
6. DMSC ROM loads SYSFW
7. DMSC starts SYSFW

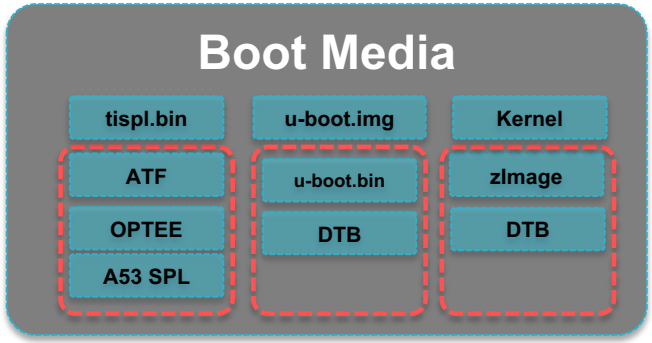
BOOTMODE pins value is latched upon POR, and select primary and backup boot modes and peripheral configuration.

Linux Boot Flow (2/2)

Continued Boot

8. R5 SPL initialization sequence

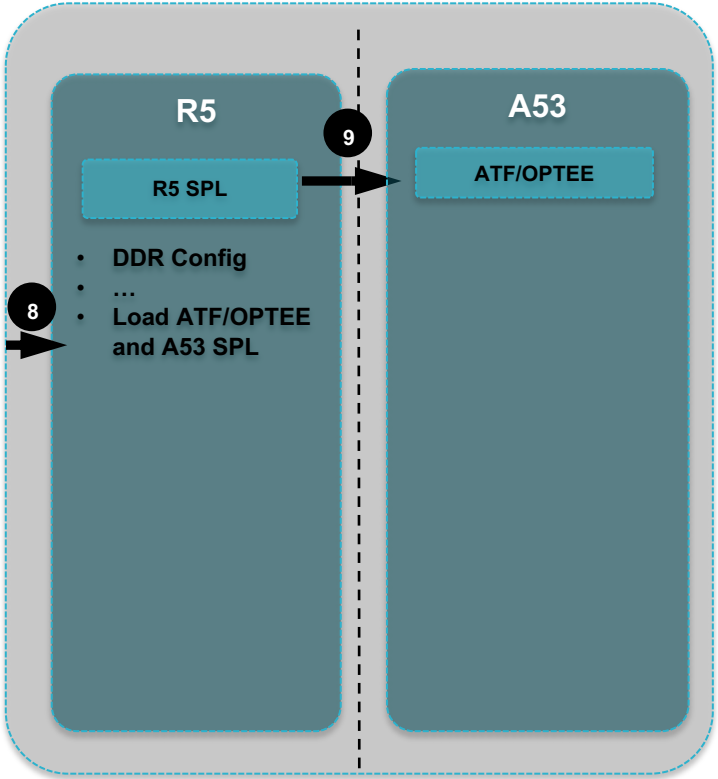


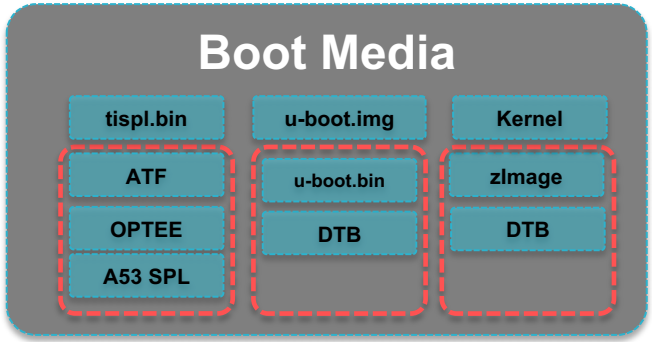


Linux Boot Flow (2/2)

Continued Boot

8. R5 SBL initialization sequence
9. R5 SBL load/start A53 ATF/OPTEE

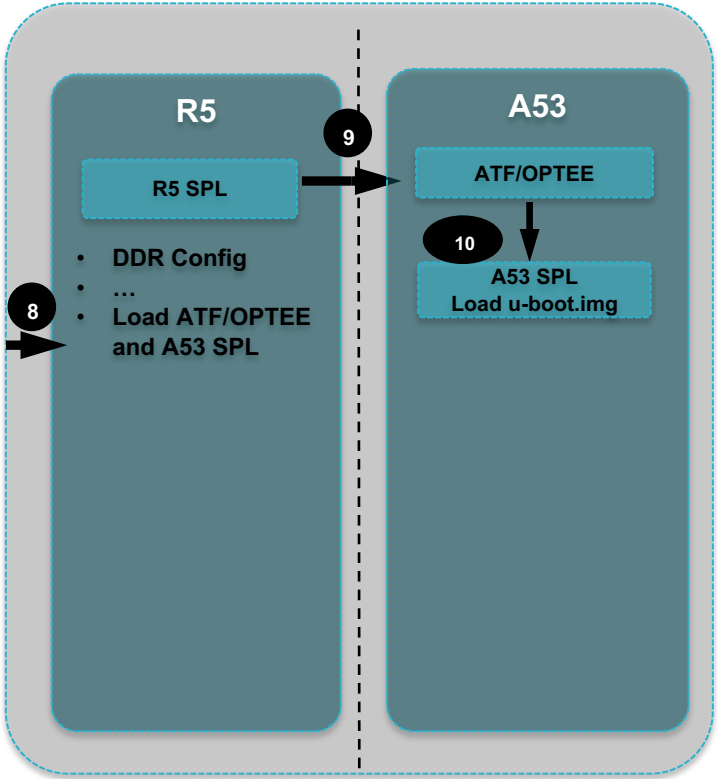


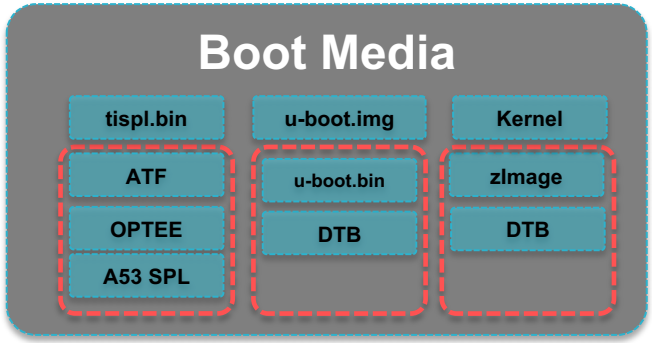


Linux Boot Flow (2/2)

Continued Boot

8. R5 SBL initialization sequence
9. R5 SBL load/start A53 ATF/OPTEE
10. R5 SBL load/start A53 SPL

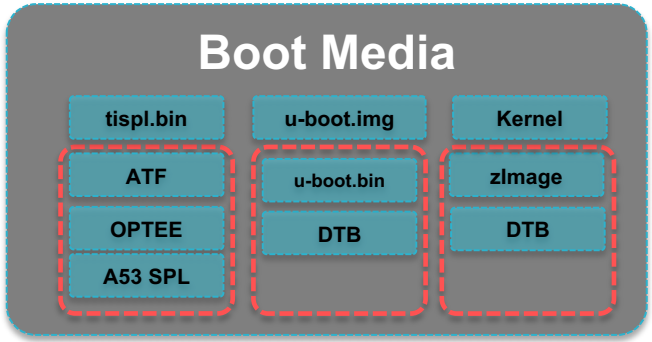


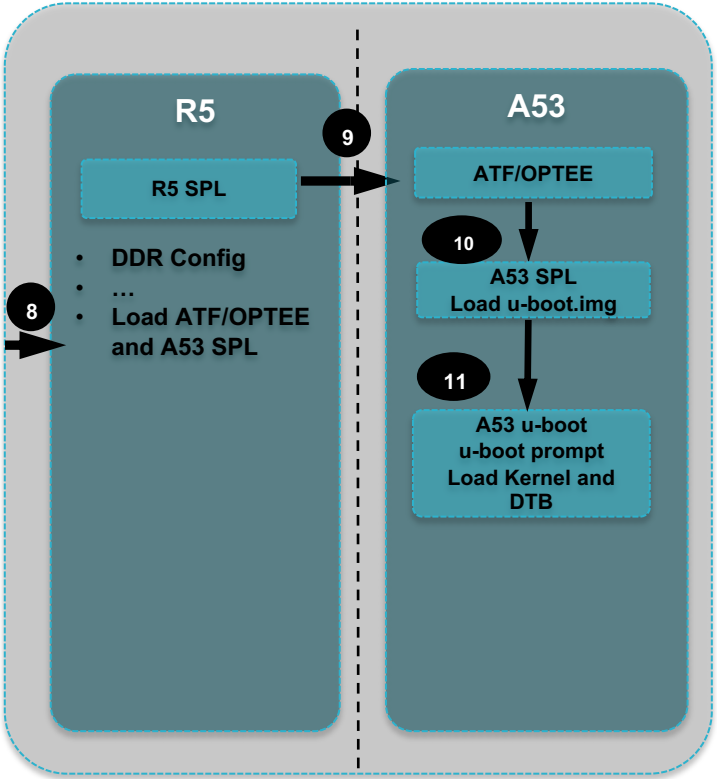


Linux Boot Flow (2/2)

Continued Boot

8. R5 SBL initialization sequence
9. R5 SBL load/start A53 ATF/OPTEE
10. R5 SBL load/start A53 SPL
11. A53 SPL load/start u-boot

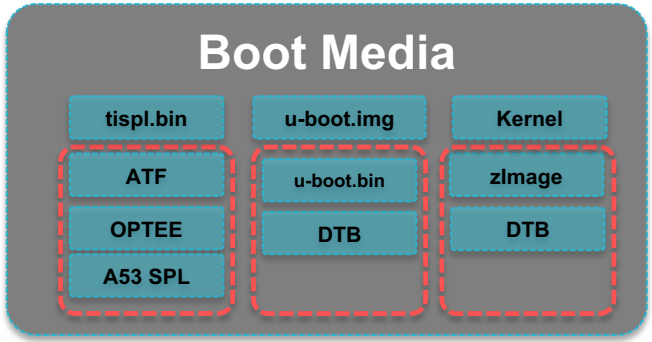


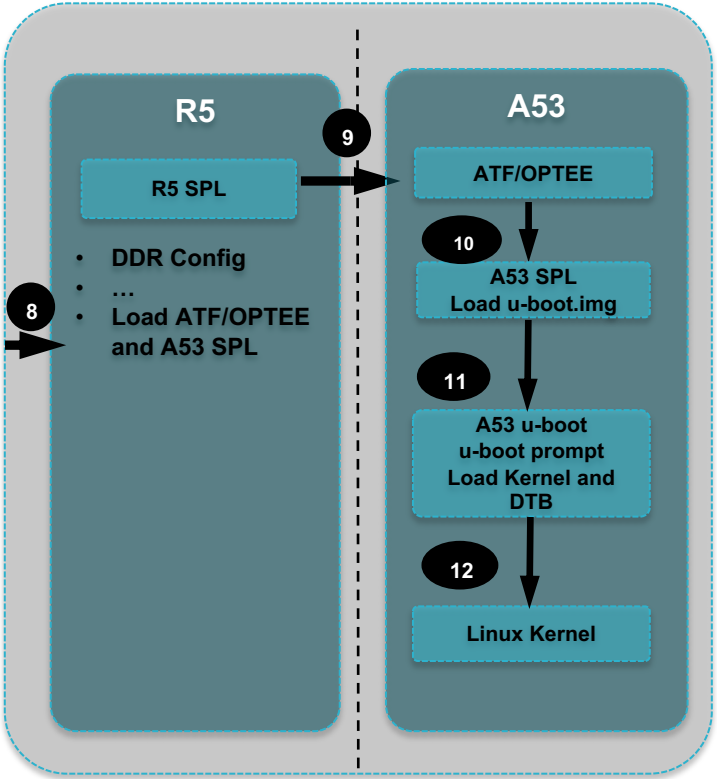


Linux Boot Flow (2/2)

Continued Boot

8. R5 SBL initialization sequence
9. R5 SBL load/start A53 ATF/OPTEE
10. R5 SBL load/start A53 SPL
11. A53 SPL load/start u-boot
12. A53 u-boot starts kernel



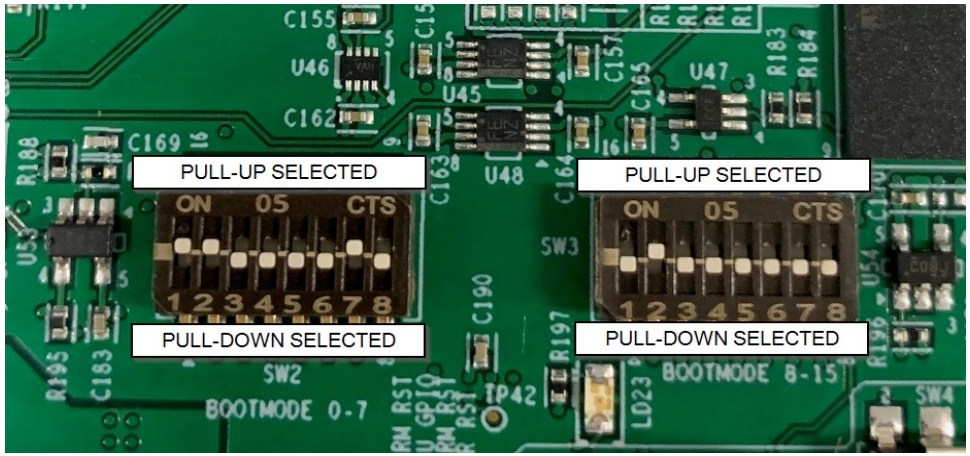


Booting Linux on AM64x EVM

BOOTMODE Switch on AM64x EVM

The following boot modes are supported on AM64x EVM (subject to change):

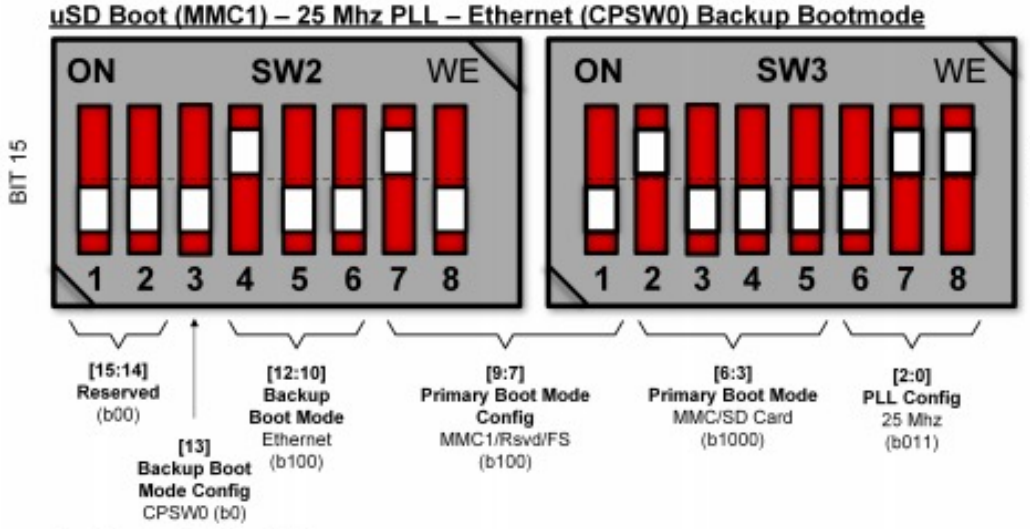
1. OSPI
2. MMC1 - SD Card
3. MMC0 - eMMC installed
4. USB - host mode with bulk storage
5. USB - device boot DFU
6. UART
7. No-Boot

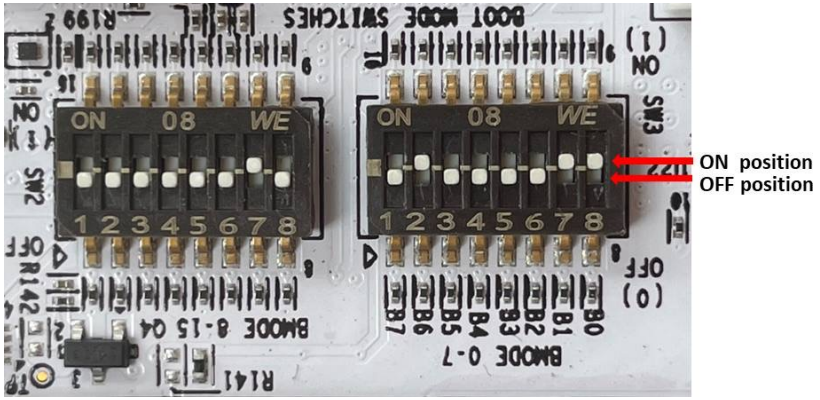


BOOTMODE Switch on AM64x SK

The following boot modes are supported on AM64x SK (subject to change):

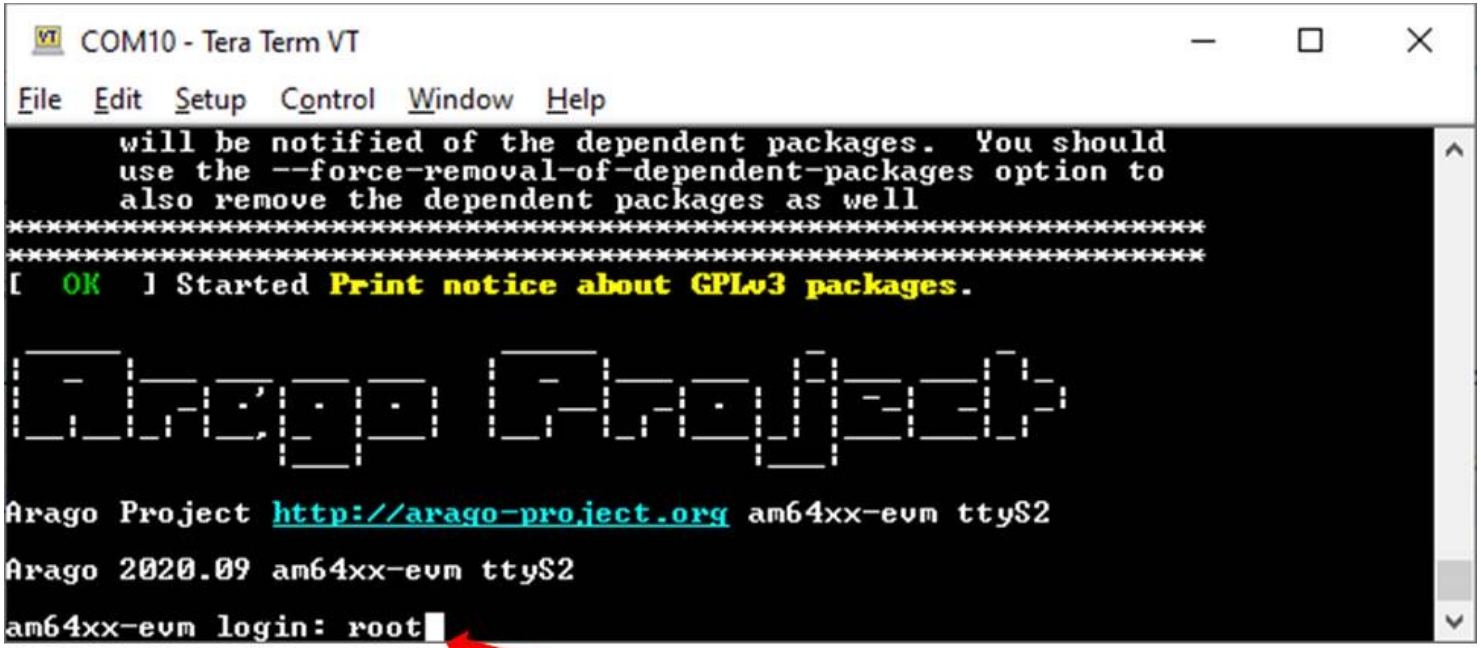
1. OSPI
2. MMC1 - SD Card
4. USB - host mode with bulk storage
5. USB - device boot DFU
6. UART
7. Ethernet Planned in future
8. No-Boot





Booting Linux on AM64x EVM

Quick start guide on booting Linux on AM64x GP EVM and SK:
AM64x GPEVM Quick Start Guide | AM64x SK Quick Start Guide



Enter “root” at the login prompt

Backup

Reference

AM64x Software Development Kit (SDK)

- https://www.ti.com/tool/PROCESSOR-SDK-AM64X

AM64x Linux SDK User Guide

- https://software-dl.ti.com/processor-sdk-linux/esd/AM64X/latest/exports/docs/devices/AM64X/index.html

SYSFW User Guide:

- http://software-dl.ti.com/tisci/esd/latest/index.html

AM64x EVM:

- https://www.ti.com/tool/TMDS64GPEVM

AM64x SK board:

- https://www.ti.com/tool/SK-AM64