Rev	Date	By	History
V0.1	3/12/2021	BMc	**PDN Diag updates:** 1. Initial capture J721S2 Leo + Tulip PDN-6A/I6A from AEP EVM Dual Leo2 + Hera1 Interim PDN-0A v1.1
V0.2	11/03/2021	RE	1. Added Dual Voltage LDO for compliant, high-speed SD Card operation 2. Added proposed SK Edge board 1st Stage power conversion with Enable Logic Test Automation block. 3. Captured initial system power seq timing diagram
V0.3	11/04/2021	BMc	1. Updated Flex LP8733 Orderable PN (OPN) & PMIC block symbol with OTP ID = 0x4E 2. Labelled power resources for alignment to PDN analysis & easy reference to system pwr seq timing 3. Added Notes & potential AND gate logic on SOC_PWR_EN control signal
V0.7	3/17/2021	BMc	1. Changed 1st stage pre-regulator control signal from VSYS_1V8_PG (pulled up to VSYS_3V3) to VSYS_1V8 2. Updated VDA_LN_1V8 power rail name to VDDA_1V8 to align with SCH net name 3. Updated title to “AM68x” & from PDN-6B to PDN-6H to align with AM68x Power Solutions app note (SLDA060) that defines consistent PDN-ID scheme based upon power rail mapping across all PDNs 4. Updated power seq timing by A. Changing control signal name from SYS_EN to SYS_MCU_EN in order to match SCH net names. B. Adding “room temp, bench measurements” from power seq verification scope captures.
V0.8	3/23/2023	BMc	Updated for a few power seq bench meas for clarification on VSYS_3V3, VSYS_5V0, VDD_SD_DV & PORz.
V0.9	3/29/2023	BMc	Updated power down Time Stamp #2 from 1.0ms to 2.5ms to align with AEP EVM & DM timing.
V0.10	10/14/24	BMc	Updated PDN & Pwr Seq diag titles & SoC block from “TDA4VE” to “AM68”
V0.11	8/7/25	BMc	Updated PDN’s power mapping to supply VDD_MCU & VDD_MCU_WAKE1 from VDD_CORE_0V8 power rail while keeping LP8733 Buck0 as source for VDDAR_MCU, VDDAR_CPU & VDDAR_CORE. Updated Pwr Seq diagram to changed power rail name from VDD_MCU_0V85 to VDD_RAM_0V85 and move VDD_MCU & VDD_MCU_WAKE1 input supplies to VDD_CORE_0V8 rail.

AM68 SK Edge AI - Flex + Tulip PDN-6H

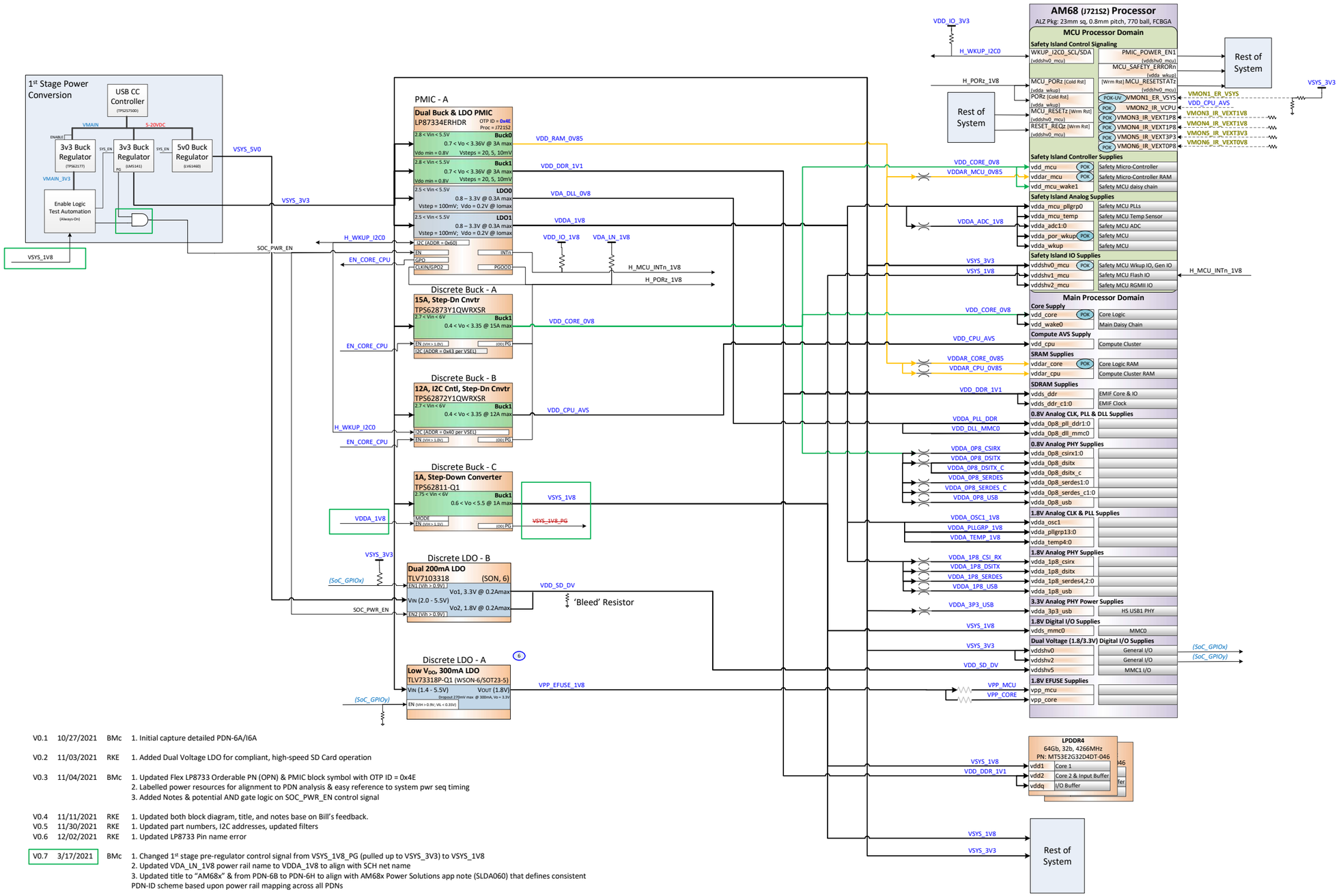
(Power Rail & GPIO Mapping Overview)

Flex PMIC, PN LP87334ERHDR-Q1 (TI OTP ID = 4E)
Tulip Buck, PN TPS62873Y1QWRXSR
Tulip Buck, PN TPS62872Y1QWRXSR

V0.10 10/14/24 BMc Updated PDN diag to show SoC block from "TDA4VE" to "AM68"
V0.11 8/7/25 BMc Updated power mapping to supply VDD_MCU & VDD_MCU_WAKE1 from VDD_CORE_0V8 power rail while keeping LP8733 Buck0 as source for VDDAR_MCU, VDDAR_CPU & VDDAR_CORE.

Features Supported :

1. J721S2 Superset Use-Case Performance with 2.0GHz clock and Peak Power est.
2. Supports J721S2 Junction Temperature (Tj) up to 105C
3. 32Gb LPDDR4 Memory, Dual 32b Interfaces at 4266MTs
4. Supports both 3.3V and 1.8V digital IO
5. Includes capacity on IO rails to support variety of peripherals (xSPI Flash, eMMC, etc)
6. Supports UHS-I compliant SD cards (Dual-Voltage IO)
7. High Secure/Field Securable Device Support
8. No Low/Partial Power Modes Support (MCU-only, Retention, etc)



V0.1 10/27/2021 BMc 1. Initial capture detailed PDN-6A/I6A

V0.2 11/03/2021 RKE 1. Added Dual Voltage LDO for compliant, high-speed SD Card operation

V0.3 11/04/2021 BMc 1. Updated Flex LP8733 Orderable PN (OPN) & PMIC block symbol with OTP ID = 0x4E
2. Labelled power resources for alignment to PDN analysis & easy reference to system pwr seq timing
3. Added Notes & potential AND gate logic on SOC_PWR_EN control signal

V0.4 11/11/2021 RKE 1. Updated both block diagram, title, and notes base on Bill's feedback.
V0.5 11/30/2021 RKE 1. Updated part numbers, I2C addresses, updated filters
V0.6 12/02/2021 RKE 1. Updated LP8733 Pin name error

V0.7 3/17/2021 BMc 1. Changed 1st stage pre-regulator control signal from VSYS_1V8_PG (pulled up to VSYS_3V3) to VSYS_1V8
2. Updated VDA_LN_1V8 power rail name to VDDA_1V8 to align with SCH net name
3. Updated title to "AM68x" & from PDN-6B to PDN-6H to align with AM68x Power Solutions app note (SLDA060) that defines consistent PDN-ID scheme based upon power rail mapping across all PDNs

AM68 SK Edge AI - Flex + Tulip PDN-6H

Flex PMIC, PN LP8733**4E**RHDR-Q1 (TI OTP ID = **4E**)
Tulip Buck, PN TPS62873Y1QWRXSR
Tulip Buck, PN TPS62872Y1QWRXSR

Rev	Date	By	Desc
V0.1	11/11/2021	RKE	Initial capture of pwr seqs beginning with with Bill's comments..
V0.7	3/15/2023	BMc	Changed control signal name from SYS_EN to SYS_MCU_EN in order to match SCH net names. Added room temp bench measurements from power seq verification scope captures.
V0.8	3/23/2023	BMc	Updated for a few power seq bench meas for clarification on VSYS_3V3, VSYS_5V0, VDD_SD_DV & PORz.
V0.9	3/29/2023	BMc	Updated power down Time Stamp #2 from 1.0ms to 2.5ms to align with AEP EVM & DM timing.
V0.10	10/14/24	BMc	Updated PDN diag to show SoC block from "TDA4VE" to "AM68"
V0.11	8/7/25	BMc	Updated Pwr Seq diagram to changed power rail name from VDD_MCU_0V85 to VDD_RAM_0V85.

Legend:

System Time
Measured Time (~Ta = 25C)
Device Time
Board Power Rail – Active State / Control Signal Nets / SoC voltage domains
Power Resource
NVM Settings, Pwr Rsc: (Resource, Current Capacity, Boot Voltage, Delay After Enable [us], Slew Rate [mV/us])
GPIO Rsc: (GPIO# = Function, Ref Voltage, Output Buffer Type, Logic @ T=0, Elapsed Time [us], Logic @ elapsed time)

*Indicates signals &/or power rails that transition during power sequences*

Verified per NVM file

Power Rail Count: | *NVM Settings, Pwr-Up Seq* | **Board Power & Logic Nets:**

EN_LM5141_ON
Dscrt: Logic, Base Bd
(Cntrl = dscrt_logic)

1# VSYS_3V3
Dscrt: LM5141, Base Bd
(Cntrl = SYS_EN)

2# VSYS_5V0
Dscrt: LM61460, Base Bd
(Cntrl = SYS_EN)

3# VDD_SD_DV
Dscrt: TPS7103318
(Cntrl = SYS_EN)

SYS_MCU_EN
Dscrt: Logic, Base Bd
(Cntrl = dscrt_logic)

4# VDDA_1V8
LP8733 PMIC
(LDO_1, 0.3A, 1.8V, 0us, 15mV/us)

5# VSYS_1V8
Dscrt Buck: TPS62811
(Cntrl = VDA_LN_1V8)

6# VDD_CPU_AVS
TPS62872 PMIC
(Buck_1, 12.0A, 0.8V, 1000us, 1ms/0.7 – 1.3ms)

EN_CORE_CPU
LP8733 PMIC
(GPIO_1 = GPO, PP, Low -> High, 1000us, NA)

7# VDD_CORE_0V8
TPS62873 PMIC
(Buck_1, 15.0A, 0.8V, 1000us, 1ms/0.7 – 1.3ms)

8# VDA_DLL_0V8
LP8733 PMIC
(LDO_0, 0.5A, 0.8V, 1000us, 15mV/us)

9# VDD_RAM_0V85
LP8733 PMIC
(Buck_0, 3.0A, 0.85V, 3000us, 7.5mV/us)

10# VDD_DDR_1V1
LP8733 PMIC
(Buck_1, 3A, 1.1V, 3000us, 7.5mV/us)

EN_EFUSE_VPP
J721S2 SOC
(GPIO = GPO, PP, Low, No transition)

11# VPP_EFUSE_1V8
Dscrt LDO: TLV73318P-Q1
(Cntrl = EN_EFUSE_VPP)

H_MCU_PORz_1V8
LP8733 PMIC
(GPIO_2 = GPO, OD, Low -> High, 11000us, NA)

H_XI_OSC0

H_SYSBOOT[15:0]