Replacing Micron MT29F2G08ABBEA with Macronix MX30UF2G18AC

1. Introduction

This application note is a guide for migrating to the Macronix MX30UF2G18AC from the Micron® MT29F2G08ABBEA 2Gb, 1.8V, x8, NAND flash memory.

The document does not provide detailed information on the individual devices, but highlights the major similarities and differences between them. The comparison covers the general features, performance, command codes and other differences.

The information in this document is based on datasheets listed in Section 11. Newer versions of the datasheets may override the contents of this document.

2. Features

Both flash device families have similar features and functions as shown in Tables 2-1.

Table 2-1: Feature Comparison

Feature	Macronix MX30UF2G18AC	Micron MT29F2G08ABAEA
Vcc Voltage Range	1.7V ~ 1.95V	1.7V ~ 1.95V
Operating Temperature	-40℃ ~ 85℃	-40℃ ~ 85℃
Interface	ONFI 1.0 Standard	ONFI 1.0 Standard
Block Size	128KB+4KB	128KB+4KB
Bus Width	x8	x8
Page Size	2KB+64B	2KB+64B
Cache Read/Program Size	2KB+64B	2KB+64B
Plane Size	2 Planes x 1024 Blocks/Plane	2 Planes x 1024 Blocks/Plane
ECC Requirement	4b/528B	4b/528B
Internal ECC Option	**N/A**	Enabled by command
Block Protection	Yes	Yes
OTP Size	30 pages	30 pages
Guaranteed Good Blocks at Shipping	Block 0 (with 4-bit ECC)	Block 0 (with 1-bit ECC)
Unique ID	ONFI standard	ONFI standard
First Command	-	Reset (FFh)
ID Code	**C2h**/AAh/90h/15h/06h	**2Ch**/AAh/90h/15h/06h
ONFI Signature	4Fh/4Eh/46h/49h	4Fh/4Eh/46h/49h
Data Retention	10 Years	10 Years
Endurance	100K Cycles	100K Cycles
Package	48-TSOP (12x20mm) 48-VFBGA (6x8mm)	48-TSOP (12x20mm) 63-VFBGA (9x11mm)

Performance

Tables 3-1 and 3-2 show Macronix and Micron NAND flash have similar Read/Write performance.

Table 3-1: Read Performance (Read Latency and Sequential Read)

Read Function	Macronix MX30UF2G18AC	Micron MT29F2G08ABBEA
Read Latency time (tR)	25us (max.)	25us (max.)
Sequential Read time (tRC)	25ns (min.)	25ns (min.)

Table 3-2: Write Performance (Program and Erase)

Write Function	Macronix MX30UF2G18AC	Micron MT29F2G08ABBEA
Page Program time (tPROG)	320us (typ.) / 600us (max.)	200us (typ.) / 600us (max.)
Block Erase time (tERASE)	1ms (typ.) / 3.5ms (max.)	0.7ms (typ.) / 3ms (max.)
NOP	4 (max.)	4 (max.)
Write/Erase Cycles*[1] (Endurance)	100,000	100,000

Note: 100K Endurance cycle with ECC protection.

3. DC Characteristics

Read/Write power requirements (Table 4-1) and I/O voltage limits (Table 4-2) are similar.

Table 4-1: Read / Write Current

DC Characteristic	Macronix MX30UF2G18AC	Micron MT29F2G08ABBEA
Sequential Read Current (ICC1)	23mA (typ.) / 30mA (max.)	13mA (typ.) / 20mA (max.)
Program Current (ICC2)	23mA (typ.) / 30mA (max.)	10mA (typ.) / 20mA (max.)
Erase Current (ICC3)	15mA (typ.) / 30mA (max.)	10mA (typ.) / 20mA (max.)
Standby Current – CMOS	10uA (typ.) / 50uA (max.)	10uA (typ.) / 50uA (max.)

Table 4-2: Input / Output Voltage

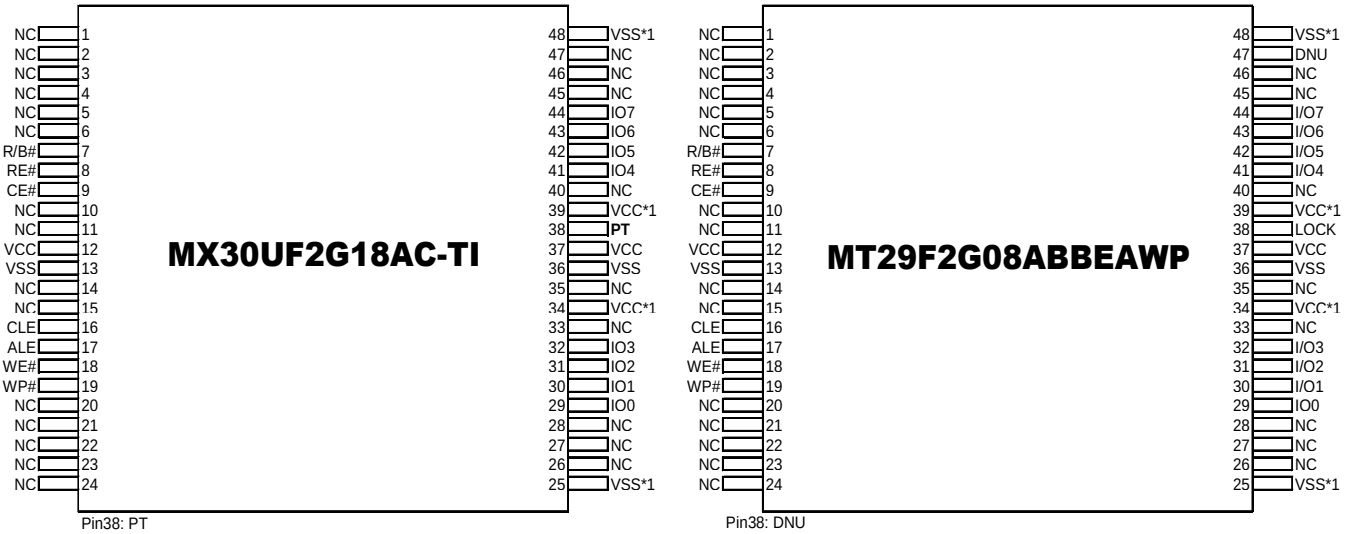
DC Characteristic	Macronix MX30UF2G18AC	Micron MT29F2G08ABBEA
Input Low Voltage (VIL)	-0.3V (min.) / 0.2VCC (max.)	-0.3V (min.) / 0.2Vcc (max.)
Input High Voltage (VIH)	0.8VCC (min.) / VCC+0.3V (max.)	0.8Vcc (min.) / Vcc+0.3V (max.)
Output Low Voltage (VOL)	0.1V (max.)	0.1V (max.)
Output High Voltage (VOH)	VCC-0.1 (min.)	VCC-0.1 (min.)

5. Package Pin/Ball Definition

The Micron MT29F2G08ABBEA can be replaced by the Macronix MX30UF2G18AC without pin conflicts. The 48-TSOP pin #38 is designated “PT” which is a Chip Protection function on the MX30UF2G18AC-TI, and on the MT29F2G08ABBEA it is designated as “LOCK” with a similar function. If this pin has been left floating or is driven low, then there is no issue as the Macronix PT pin has a weak internal pull down. This is true for the Macronix 63-VFBGA PT ball E3, and Micron LOCK ball G5 as well. Tables 5-1 and 5-2 show differences in pin assignments between the Macronix and Micron devices.

The 48-TSOP Package physical dimensions are similar to each other.

Figure 5-1: 48-TSOP (12x20mm) Package and Pin Layout Comparison (x8)



Note:
1. These pins might not be connected internally. However it is recommended to connect these pins to power(or ground) as designated for ONFI compatibility.

Table 5-1: 48-TSOP Package Pin Definition

Brand	Macronix	Micron	Note
Part Name	MX30UF2G18AC-TI	MT29F2G08ABBEAWP	
#38 pin	PT*[1]	LOCK	Pin functions are compatible.
#47 pin	NC	DNU	If pins are left unconnected, both pin functions are compatible

Note: PT pin has internal weak pull low. It enables the protection function if active. Please refer to the datasheet for more details.

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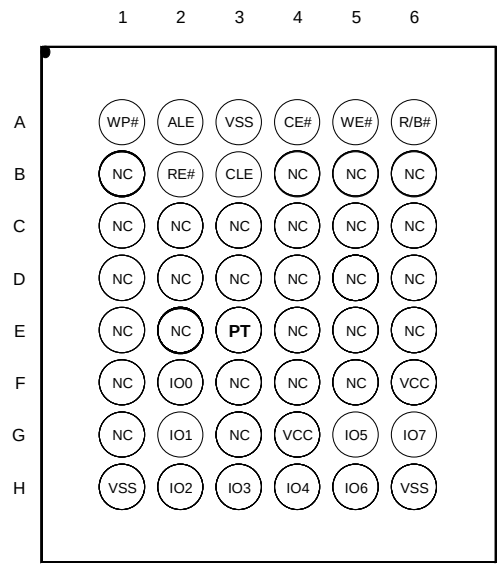
The 6x8mm 48-VFBGA and 9x11mm 63-VFBGA pinouts and ball pitch are compatible. The ball diameter of the Macronix 48-VFBGA is 0.40mm, which is smaller than Micron's 0.45mm ball used on the 63-VFBGA. For detailed information, please refer to the individual datasheets.

Figure 5-2: 48-VFBGA vs 63-VFBGA Package and Ball Layout Comparison

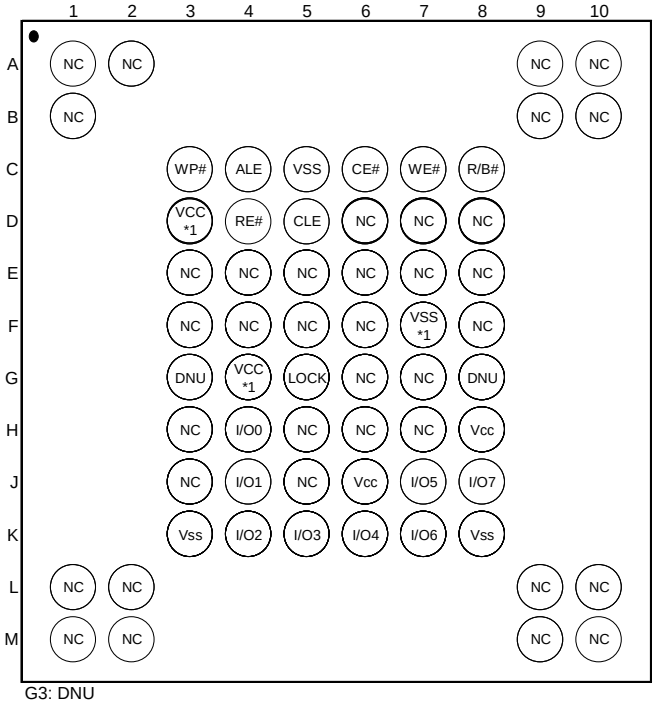
MX30UF2G18AC-XQI (6 x 8 x 1 mm)



E3: PT

Note:
1. These pins might not be connected internally. However it is recommended to connect these pins to power(or ground) as designated for ONFI compatibility.

MT29F2G08ABBEAH4 (9 x 11 x 1 mm)



G3: DNU
G5: LOCK
G8: DNU

Table 5-2: 63-VFBGA Package Ball Definition

Macronix	Micron	Note
MX30UF2G18AC-XQI	MT29F2G08ABBEAH4	
ball E3 = PT*[1]	ball G5 = LOCK	Pin functions are compatible.
balls E1 and E6 = NC	balls G3 and G8 = DNU	If pins are left unconnected, both pin functions are compatible

Note: PT pin has internal weak pull low. It enables the protection function if active. Please refer to the datasheet for more details.

6. Command Set

Basic command sets and status checking methods are similar (Table 6-1 and 6-2). Micron offers additional non-ONFI two plane commands, as well as a few commands used for block protection which are not listed in Table 6-2 (see datasheet for details).

Table 6-1: Command Table

Command	Macronix MX30UF2G18AC		Micron MT29F2G08ABBEA	
	1st Cycle	2nd Cycle	1st Cycle	2nd Cycle
Random Data Input	85h	-	85h	-
Random Data Output	05h	E0h	05h	E0h
Cache Read Begin	00h	31h	00h	31h
Read Mode	00h	30h	00h	30h
Cache Read End	3Fh	-	3Fh	-
Read ID	90h	-	90h	-
Reset	FFh	-	FFh	-
Page Program	80h	10h	80h	10h
Cache Program	80h	15h	80h	15h
Block Erase	60h	D0h	60h	D0h
Read Status	70h	-	70h	-
Read Parameter Page	ECh	-	ECh	-
Unique ID Read	EDh		EDh	
Set Feature	EFh		EFh	
Get Feature	EEh		EEh	
Status Enhance Read	78h		78h	
Block Protection Status Read	7Ah		7Ah	

Table 6-2: Two-Plane Command Table

Command	Macronix MX30UF2G18AC				Micron MT29F2G08ABBEA			
	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle
ONFI 2 Plane Program	80h	11h	80h	10h	80h	11h	80h	10h
ONFI 2 Plane Cache Program	80h	11h	80h	15h	80h	11h	80h	15h
ONFI 2 Plane Block Erase	60h	D1h	60h	D0h	60h	D1h	60h	D0h

6-2 Status Register

When a flash Read, Program, or Erase operation is in progress, either the “Ready/Busy# Pin Checking” or “Status Output Checking” method may be used to monitor the operation. Both are standard NAND flash algorithms and can be used for both device families. Table 6-3 shows that Status Output content provided by the Read Status command (70h) is compatible. Table 6-4 shows that Two–plane Status provided by the Status Enhance Read command (78h) is compatible. If internal ECC is enabled in the Micron device, SR[3] indicates that up to 4-bits have been corrected and that the page should be rewritten. This function is not needed for the Macronix device, as it does not support internal ECC generation. Macronix also provides an internal ECC (or ECC Free) part with a different part number.

Table 6-3: Status Output

Status Output	Macronix MX30UF2G18AC	Micron MT29F2G08ABBEA
SR[0]	PGM/ERS/RAD status: Pass/Fail	PGM/ERS/READ status: Pass/Fail
SR[1]	Cache Program status: Pass/Fail	Cache Program status: Pass/Fail
SR[2]	Reserved	Reserved
SR[3]	Reserved	Rewrite Recommended
SR[4]	Reserved	Reserved
SR[5]	PGM/ERS/Read internal controller: Ready/Busy	PGM/ERS/Read internal controller: Ready/Busy
SR[6]	PGM/ERS/Read status: Ready/Busy	PGM/ERS/Read status: Ready/Busy
SR[7]	Write Protect	Write Protect

Table 6-4: Two-plane Status Output

Status Output	Macronix MX30UF2G18AC	Micron MT29F2G08ABBEA
SR[0]	Selected Plane PGM/ERS/READ status: Pass/Fail	Selected Plane PGM/ERS/READ status: Pass/Fail
SR[1]	Selected Plane Cache Program status: Pass/Fail	Selected Plane Cache Program status: Pass/Fail
SR[2]	Reserved	Reserved
SR[3]	Reserved	Reserved
SR[4]	Reserved	Reserved
SR[5]	PGM/ERS/Read internal controller: Ready/Busy	PGM/ERS/Read internal controller: Ready/Busy
SR[6]	PGM/ERS/Read status: Ready/Busy	PGM/ERS/Read status: Ready/Busy
SR[7]	Write Protect	Write Protect

7. Read ID Command

The ID codes of the MT29F2G08ABBEA and MX30UF2G18AC are identical except for the first byte which indicates the Manufacturer (Table 7-1). The same command set is used to read both IDs.

Table 7-1: Manufacturer and Device IDs

ID code		Macronix MX30UF2G18AC	Micron MT29F2G08ABBEA
Value		**C2h**/AAh/90h/15h/06h	**2Ch**/AAh/90h/15h/06h
1st Byte		Manufacturer Code	Manufacturer Code
2nd Byte		Device Identifier	Device Identifier
3rd Byte	bit 1- 0	Number of Die per Chip Enable	Number of Die per Chip Enable
	bit 3 - 2	Cell Structure	Cell Structure
	bit 5 - 4	Number of Simultaneously Programmed Pages	Number of Simultaneously Programmed Pages
	bit 6	Interleaved Programming Between Multiple Chips	Interleaved Programming Between Multiple Chips
	bit 7	Cache Program	Cache Program
4th Byte	bit 1- 0	Page Size (exclude Spare Area)	Page Size (exclude Spare Area)
	bit 2	Size of Spare Area (Byte per 512Byte)	Size of Spare Area (Byte per 512Byte)
	bit 7, 3	Sequential Read Cycle Time (tRC)	Serial Access Time (tRC)
	bit 5 - 4	Block Size (exclude Spare Area)	Block Size (exclude Spare Area)
	bit 6	Organization	Organization
5th Byte	bit 1- 0	ECC Level Requirement	ECC Level Requirement
	bit 3 - 2	Number of Plane per CE	Number of Plane per CE
	bit 6 - 4	Plane Size	Plane Size
	bit 7	Reserved	Internal ECC Enabled/Disabled

8. Power-Up Timing

Macronix and Micron® power-up sequences are similar, but the timing is slightly different. Although both devices use 1.7V (VCC min.) as the start point, timing references are different. Check the system timing to determine if adjustments are needed.

Table 8-1: Power-Up Timing

H/W Timing Characteristic	Macronix MX30UF2G18AC	Micron MT29F2G08ABBEA
Vcc (min.) to WE# low	1ms (max.)*[1]	N/A
Vcc (min.) to R/B# high	N/A	100us (max.)
Vcc (min.) to R/B# low	10us (max.)	10us (max.)
Vcc ramp start to R/B# low	N/A	50us (min.)

Note: Micron requires Reset command as first command, but Macronix does not.

Macronix requires an initialization delay during power on.

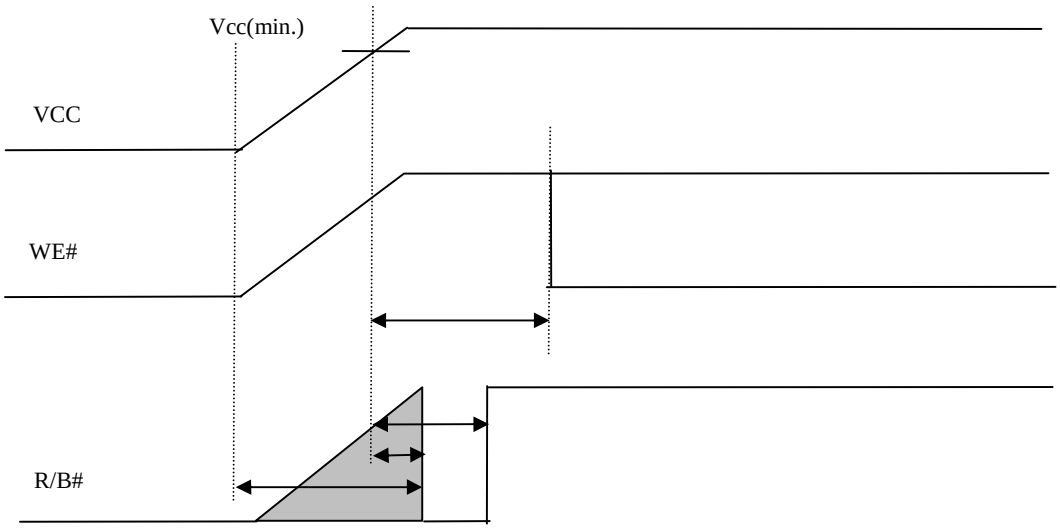


Figure 8-1: Power-Up Timing

9. Block Protection

Both NAND flash have the ability to Hardware Write Protect the entire array if the WP# pin is low.

Both flashes also have the ability to lock contiguous groups of blocks, but the methods are different.

Micron uses their LOCK pin to enable the Block Protect commands at power up, which can be used to define an address range of blocks to be protected.

Similarly, Macronix uses the PT pin (if high at power-up) to enable BP (Block Protect) bits. If enabled, the entire array comes up protected by volatile BP bits. The BP bits can be changed to protect or unprotect different regions of the memory array using the “Set Feature” cmd = EFh with Feature Adr = A0h and the data value of the BP bit setting. Additionally, we can lock the BP bits by setting the “SP” Solid Protect Bit = 1. Once the SP bit has been set, the only way to unlock the BP bits, is with the next power cycle. The SP bit can be set = 1, with the same method used to set the BP bits, using Set Feature command EFh with feature adr = A0h+data. To verify the Sub-Feature data is set correctly, we can read the data value with the Get Feature cmd = EEh + Feature Adr A0h (to read BP bit setting). We can check if a block is protected or if the SP bit is set, using the “Block Protect Status Read” cmd = 7Ah + Block Address.

10. Summary

Macronix MX30UF2G18AC and Micron® MT29F2G08ABBEA NAND share the same basic Read, Program, and Erase commands, have similar features and pinouts, have the same Page, Block, Spare Area size, both require 4bit ECC, and are both ONFI 1.0 compatible. Overall, device migration may require minimal or no firmware modifications. If the Micron internal ECC generation function is required, Macronix may offer this function as well, in a different part number (please contact Macronix sales).

11. References

Table 11-1 shows the datasheet versions used for comparison in this application note. For the most current, detailed Macronix specification, please refer to the Macronix website at http://www.macronix.com

Table 11-1: Datasheet Version

Datasheet	Location	Date Issue	Revision
MX30UF2G18AC	Website	Jan. 15, 2015	Rev. 0.00
MT29F2G08ABBEA	-	Oct. 2012	Rev. O

Note: Macronix data sheet is subject to change without notice.

12. Appendix

Cross Reference Table 12-1 shows basic part number and package information for the Macronix MX30UF2G18AC and Micron® MT29F2G08ABBEA products.

Table 12-1: Part Number Cross Reference

Macronix Part No.	Micron Part No.	Package	Dimension
MX30UF2G18AC-TI	MT29F2G08ABBEAWP	48-TSOP	12x20mm
MX30UF2G18AC-XQI	MT29F2G08ABBEAH4	VFBGA	Micron 63-VFBGA= 9x11mm Macronix 48-VFBGA = 6x8mm

13. Revision History

Revision	Description	Date
1.0	Initial Release	Mar. 14, 2015

Replacing Micron MT29F2G08ABBEA with Macronix MX30UF2G18AC

For the contact and order information, please visit Macronix's Web site at: http://www.macronix.com