Alert J784S2 vE5 & J742S2 vE2 EVM System Updates

Notifying customers of EVM performance updates across both J784S4 & J742S2 EVMs and any J7 design using a universal PDN-3x scheme.

V1.0 9/12/2024

J784S4 (PROC141E5) & J742S2 (PROC184E2) Key Updates

		Critically
1.	Optimize HCPS-A CPU Buck Regulator Performance	High
2.	Optimize HCPS-B CORE Buck Regulator Performance	High
3.	PMIC TPS6594133A NVM Updates	High
4.	New “PDN Type” Selection for PMIC GPIO8	Medium
5.	Optional “WDOG Disable” Control for PMIC GPIO9	Medium
6.	SoC Cold Boot after MCU_PWRGRP_IRQn fault	Medium
7.	Discrete LDO (TPS74501P-Q1) ramp-up & ramp-down slew rates	Medium
8.	PMIC LDO cold temperature stability for large capacitive loads	Low
9.	Optional SoC eFuse programming interface & LDO performance	Low

Notes:
1) All updates apply for both J784S4 EVM (PROC141E5 SCH, BOM & PCB) & J742S2 EVM (PROC184E2 SCH, BOM & PCB).
2) Please see vE5 SCH, BOM & PCB files for complete details since this Alert doc does not list all vE5 updates. There are more minor updates (removing unused provisioned nets &/or components) in SCH, BOM & PCB.

Updated vE5 SCH & PDN-3A, -3F, -3G & -3M Diagrams

- **While the vE5 PCB is being updated, this Alert notice, vE5 SCH & PDN block diagrams are available on TI's CDDS (links below).**

  CDDS: Folder - Jacinto7 Product Series/J7 Family/Alert/Alert J784S4 vE5 and J742S2 vE2 EVM System Updates:
  US - https://cdds.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.17069.18257&latestRevision=true

  CDDS: Folder - Jacinto7 Product Series/J784S4/EVM/J784S4 EVM PROC141E5_SCH-E5:
  US - https://cdds.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.6743.44754&latestRevision=true

  CDDS: Folder - Jacinto7 Product Series/J784S4/EVM/J784S4 Single PMIC and HCPS PDN-3A -3F -3G -3M Variants:
  US - https://cdds.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.1397.3181&latestRevision=true

  PWR_MAIN_EN_SOC

- **Once vE5 EVM is released, the vE5 SCH, PCB & PDN design source files will be available on TI's EVM website (link below).**

  TI Website – J784S4XEVM: J784S4XEVM Evaluation board | TI.com

Universal PDN Updates | Implementation Guidance

J7 Generic PNs	J7 Orderable PNs	PDN Types Iso -3A to -3F Grp -3G to -3M	Item 1 & 2 J784S4 only HCPS[1] Optz[2]	Item 3 PMIC NVM v5	Item 4 PMIC GPIO8 = PDN Type	Item 5 PMIC GPIO9 Dis WD Option[4]	Item 6 Exiting MCU Fault[3]	Item 7 Dscrt LDO Slew Rate	Item 8 PMIC LDO No Load Stbly	Item 9 LDO for Efuse Prgm Option[4]
J721E	TDA4VM DRA829	Isolated Grouped	NA[2]	R R	NA R	R R	R LPM	R NA	E	R R
J7200	DRA821	Isolated Grouped	NA[2]	R R	NA R	R R	R LPM	R NA	E	R R
J721S2	TDA4AL TDA4VL TDA4VME	Isolated Grouped	NA[2]	R R	NA R	R R	R LPM	R NA	E	R R
J784S4	TDA4AP TDA4VP TDA4AH TDA4VH	Isolated Grouped	E	R R	NA R	R R	R LPM	R NA	E	R R
J722S	TDA4AEN TDA4VEN	Isolated Grouped	NA[2]	R R	NA R	R R	R LPM	R NA	E	R R
J742S2	TDA4APE TDA4VPE	Isolated Grouped	NA[2]	R R	NA R	R R	R LPM	R NA	E	R R

Legend: R = Required; E = Design Enhancement; NA = Not Applicable; LPM = Required if the Grouped PDN supports a Low Power Mode (LPM)

Notes:
1. HCPS = High Current Power Stage
2. Similar buck converter loop performance & bulk capacitance optimizations may be possible for other J7xxx designs, please review specific J7xxx load step simulations and consult TPS6287x-Q1 FAE for any additional support.
3. Exiting MCU Fault only applies to systems supporting Functional Safety targets (ASIL-D/-B, etc.)
4. Updates are not required if design does not implement an optional feature.

Optimizing HCPS Buck Regulator Performance

Summary | Optimizing HCPS Buck Performance

- **Criticality:** High
- **Description:**
  HCPS-A & -B buck regulator loop performance have been optimized to provide higher bandwidth, allowing quicker load step responses while maintaining good phase margins.
- **Key Updates (SCH & PCB Impacts):**
  - Updated HCPS-A & -B buck load step simulation results with SoC Tj = +125C

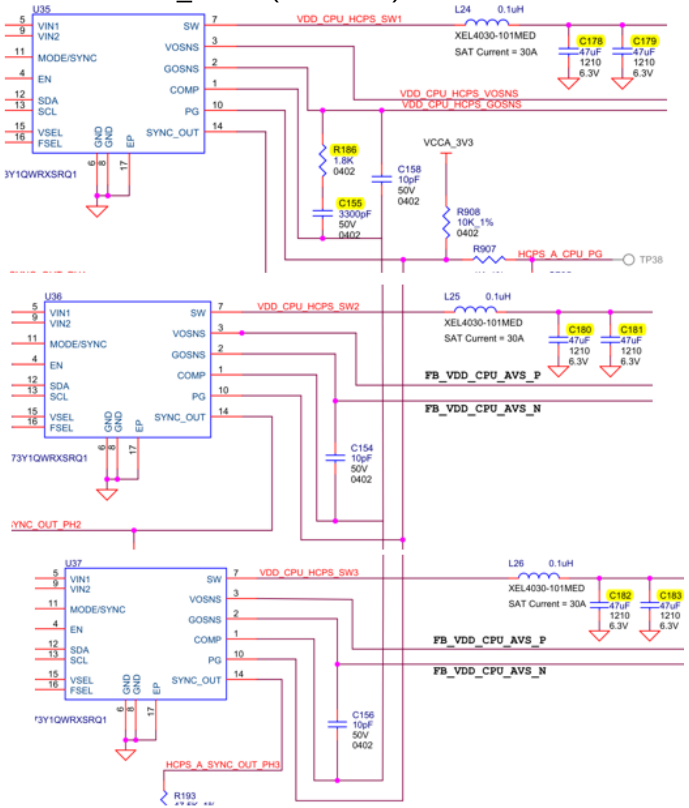
1. HCPS-A supplying VDD_CPU_AVS
   - CPU pk load step = 35.5A (46 - 10.5) in 1us
   - Transient supply noise, Vnpk = +/- 2.8% max
   - Local Cz per Phase = 10uF => 30uF total
   - PoL Cz => 900uF total
     (Note: Capacitance, Cz, derived after derating Cnom)
   - Buck Loop Phase Margin = 50.9 deg
   - Buck Loop Gain Cross Freq = 211kHz

2. HCPS-B supplying VDD_CORE_0V8
   - CORE pk load step = 16.1A (24.1 - 8) in 1us
   - Transient supply noise, Vnpk = +/- 3.1% max
   - Local Cz per Phase = 22uF => 44uF total
   - PoL Cz = 400uF total
     (Note: Capacitance, Cz, derived after derating Cnom)
   - Buck Loop Phase Margin = 45.9 deg
   - Buck Loop Gain Cross Freq = 260kHz

Summary | Optimizing HCPS Buck Performance

- **Update #1: HCPS-A, 3-Phase Buck for VDD_CPU_AVS**
- Buck loop compensation settings:
  - PROC141E4_SCH
    - Rz = 1.8k (R186)
    - Cc = 3,300pF (C155)
    - Cc2 = 10pF
  - PROC141E5_SCH (Impacts)
    - Rz = 2.4k (R186)
    - Cc = 1,500pF (C155)
    - Cc2 = 10pF
- Local Cz per phase (Cz = Cnom derated by 50%) :
  - PROC141E4_SCH
    - Cz_out per phase = 47uF
      (Note: Cz = Cnom derated by 50%)
    - Cnom_out per phase = 94uF (C178 & 179; C180 & 181; C182 & 183)
  - PROC141E5_SCH (Impacts)
    - Cz_out per phase = 11uF
    - Cnom_out per phase = 22uF (C178; C180; C181)
      - PN: GCM32ER70J226KE19L, CERAMIC 22uF 6.3V 10% X7R AUTO 1210
      - DNI 3x capacitors (C179; C181; C182)

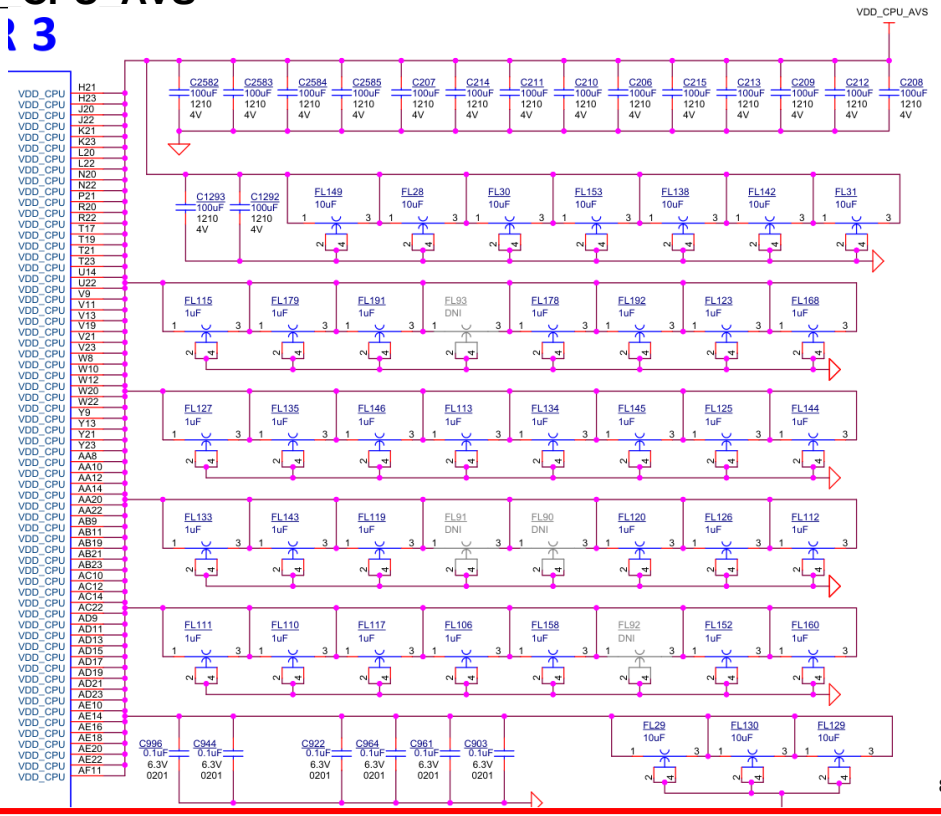
PROC141E4_ SCH (Nov 2022)



Summary | Optimizing HCPS Buck Performance

- **Update #1: HCPS-A, 3-Phase Buck for VDD_CPU_AVS**
- Point of Load Cz (Cz = Cnom typ derated by 50%):
  - PROC141E4_SCH
    - PoL Cz = 1698 x 50% = 849uF
      (1698 x 47% = 900uF)
    - Cnom_load = (16x100uF + 7x10uF + 28x1uF)
      (1600 + 70 + 28) = 1698uF
  - PROC141E5_SCH No Impacts for 47% derating

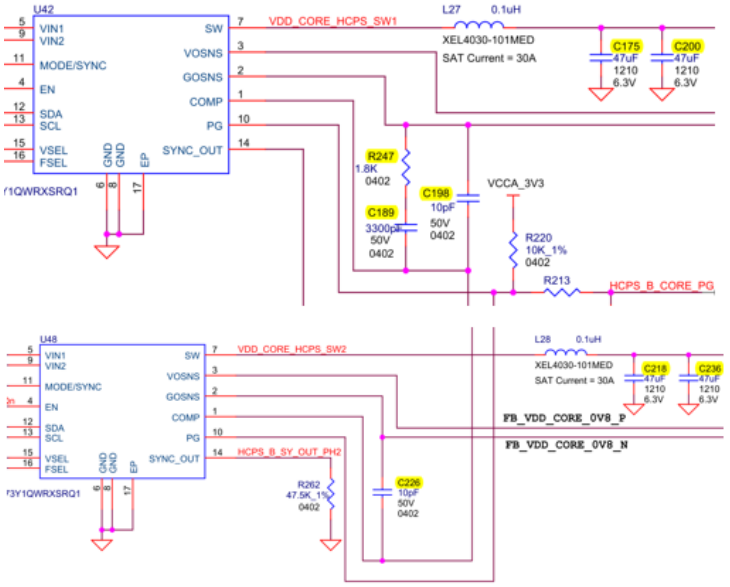
PROC141E4_ SCH (Nov 2022)



Summary | Optimizing HCPS Buck Performance

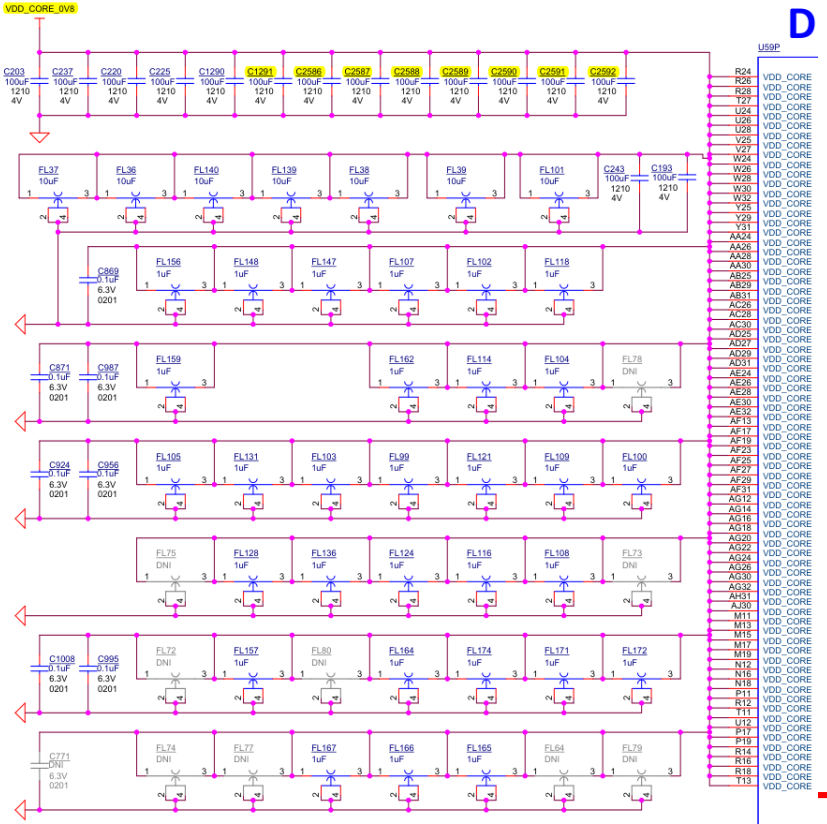
- **Update #2: HCPS-B, 2-Phase Buck for VDD_CORE_0V8**
- Buck loop compensation settings:
  - PROC141E4_SCH
    - Rz = 1.8k (R247)
    - Cc = 3,300pF (C189)
    - Cc2 = 10pF (C198 & C226)
  - PROC141E5_SCH (Impacts)
    - Rz = 1.2k (R247)
    - Cc = 4,700pF (C189)
    - Cc2 = 20pF (C198 & C226)
- Local Cz per phase (Cz = Cnom derated by 50%) :
  - PROC141E4_SCH
    - Cz_out per phase = 47uF
      (Note: Cz = Cnom derated by 50%)
    - Cnom_out per phase = 94uF (C175 & C200; C218 & C236)
  - PROC141E5_SCH (Impacts)
    - Cz_out per phase = 23.5uF
    - Cnom_out per phase = 47uF (C175; C218)
      - DNI 2x capacitors (C200; C236)

PROC141E4_ SCH (Nov 2022)



Summary | Optimizing HCPS Buck Performance

- **Update #2: HCPS-B, 2-Phase Buck for VDD_CORE_0V8** PROC141E4_ SCH (Nov 2022)
- Point of Load Cz (Cz = Cnom typ derated by 50%) :
  - PROC141E4_SCH
    - PoL Cz = 1600 x 50% = 800uF
    - PoL Cnom = (15x100uF + 7x10uF + 30x1uF)
      (1500 + 70 + 30) = 1600uF
  - PROC141E5_SCH Impacts, reduce PoL Cz
    - PoL Cz = 800 x 50% = 400uF
    - PoL Cnom = (7x100uF + 7x10uF + 30x1uF)
      (700 + 70 + 30) = 800uF
      - DNI 8x capacitors (C1291, C2586 - C2592)



PMIC TPS6594133A NVM Updates

Summary | TPS6594133A NVM Updates

- **Criticality:** High
- **Description:**
  The TPS6594133A-Q1 PMIC NVM revisions implement key updates that could impact existing J784S4 systems form, fit & function if designs were fully aligned to J784S4 EVM vE4 (PROC141E4_SCH) released in Nov 2022.
- PMIC ‘133A NVM v3 was initially Released to Manufacturing (RTM) in Jan 2023

TPS6594133A NVM | Revision History

Revision	Release Date	Comments
0.0	April 25, 2022	
1.0	August 8, 2022	
2.0	October 10, 2022	TI J784S4 EVM Samples
3.0	December 15, 2022	RTM’d in January 2023
4.0	Only released in sample units	
5.0	March 1, 2024	PCN released and all parts received after March 1st , 2024 contain Rev 5

Note: Please see “TPS6594133A NVM Rev History” for complete details in Reference Section below.

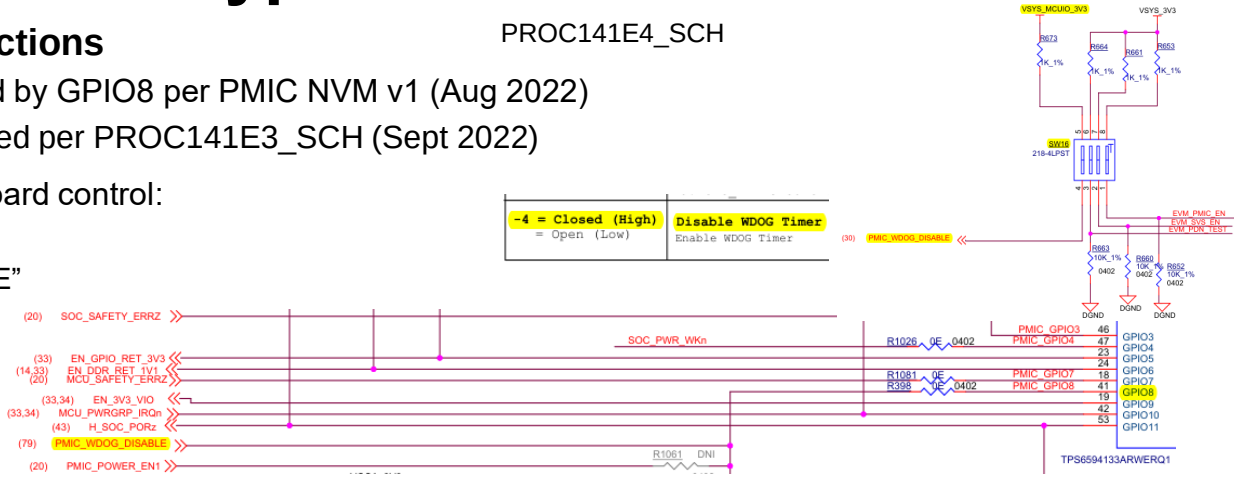
Summary | TPS6594133A NVM Updates

- **Update #3: New NVM creates 1x PMIC PN for multiple J7xxx SoC PDN schemes (Impacts):**
  - PMIC VCCA auto-detection of PMIC's input voltage using either 3.3V or 5V (NVM v2, Oct 2022).
  - Re-assign GPIO8 as "PDN Type" board setting for PMIC initialization control (NVM v2, Oct 2022):
    - Low = Isolated MCU & Main PDN Type => Buck5 supplies VDD_MCU_0V85 rail & included in power sequences
    - High = Grouped MCU & Main PDN Type => Buck5 disabled & removed from power sequences. VDD_MCU & VDD_CORE are supplied from VDD_CORE_0V8. After SoC boot, SW can reassign Buck5 for peripheral devices
    - Wdog timer disabled by default to enable GPIO8 to define "PDN Type" as a higher priority control across PDNs
  - Enable Wdog Timer by default & move "PMIC_WDOG_DISABLE" from GPIO8 to GPIO9 (NVM v5, Mar 2024) .
    - Avoids possibility that production units could miss a Wdog Timer flag if a random fault keeps the system from booting & loading SW needed to enable Wdog Timer function.
    - Optional "PMIC_WDOG_DISABLE" board control is desirable for EVM testing, product integration & trouble-shooting tasks. Avoids needing SW to issue I2C writes to disable Wdog timer after boot.
    - PMIC enables WDog timer by default with 13min long window for MCU SW to complete WDog timer configuration after nRSTOUT (PORz) asserts high
  - Increase LDO2 Vout OV/UV default threshold from 5 to 10% (NVM v5, Mar 2024).
    - When LDO2 is used as load switch, aligns PMIC's LDO2 & VCCA VMON windows since both are supplied by VSYS_3V3. Customer has option to reduce VMON after system boot.
  - Updated power up sequences to resolve J7 SoC i2406 Errata (NVM v5, Mar 2024).

Summary | New “PDN Type" Selection for GPIO8

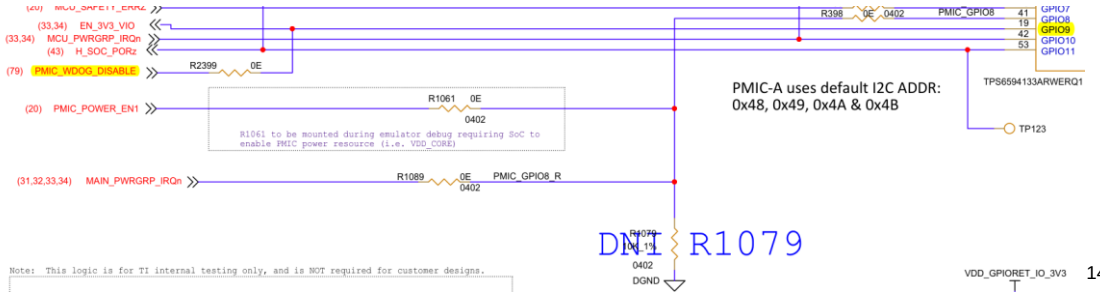
- **Update #4: PMIC GPIO8 connections**
  - “PMIC_WDOG Disable” supported by GPIO8 per PMIC NVM v1 (Aug 2022)
  - Wake-up EVMs used PCB designed per PROC141E3_SCH (Sept 2022)
- Optional “PMIC_WDOG_DISABLE” board control:
  - PROC141E3/E4_SCH
    - Originally “PMIC_WDOG_DIABLE” net connected to R398 (0-ohm) & interface to PMIC GPIO8

PROC141E4_SCH



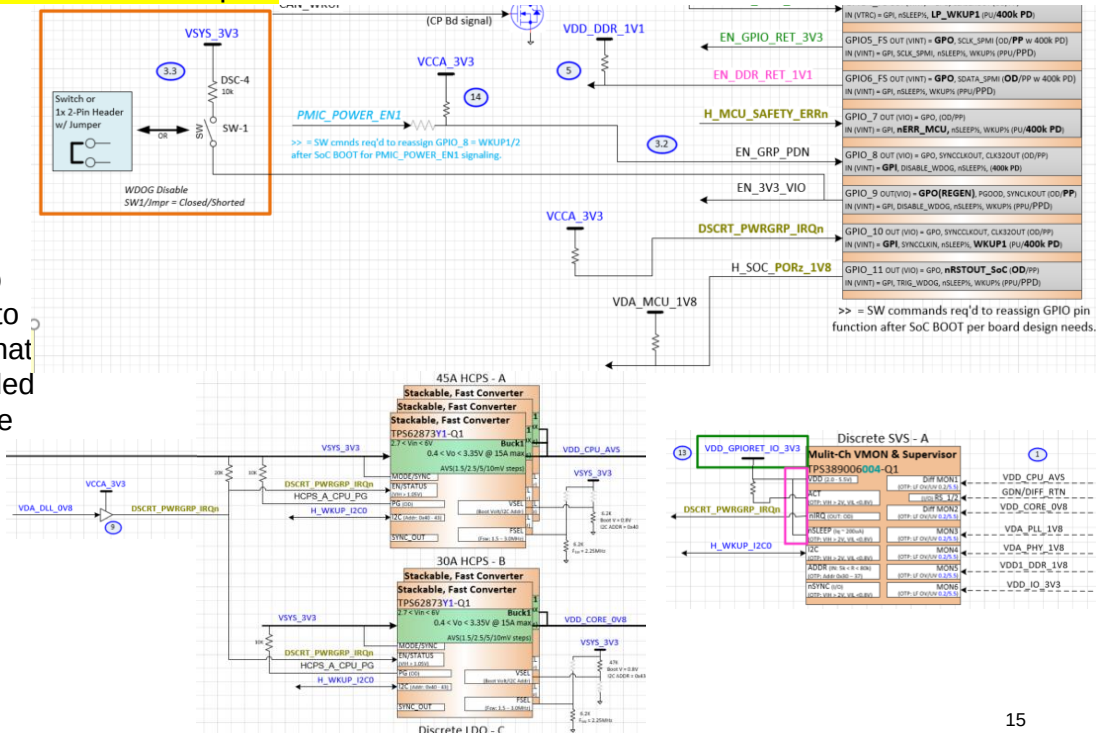
  - PROC141E5_SCH (Impacts)
    GPIO8 now supports a new “PDN Type” PMIC initialization control
    Example: MAIN_PWRGRP_IRQn net connected to GPIO8 for EVM’s Isolated MCU & Main PDN-3A. Net is held low by low-voltage translator to keep HCPS-A & -B disabled until correct power up seq time step. Therefore, GPIO8 (PDN Type) latches a logic low to set Isolated MCU & Main PDN type.

PROC141E5_SCH



Summary | New PDN Type GPIO8 Interface

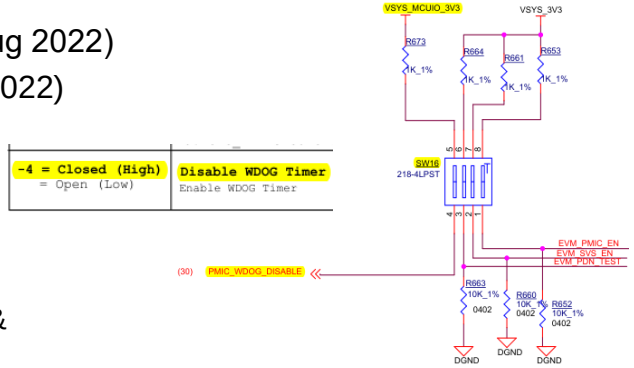
- **Example PMIC GPIO8 connection for Grouped MCU & Main PDN-3G thru -3M**
- Detailed J784S4 PDN-3G diagram snap-shots are shown as examples:
  - EN_GRP_PDN net connected to GPIO8 is pulled-up to VSYS_3V3. Enabling the PMIC to latch a logic high during early portion of power up seq, resulting in Buck5 being disabled & removed from power up seq as desired for Grouped MCU & Main PDN-3G to -3M schemes.
  - MCU_PWRGRP_IRQn net that is connected to GPIO10 for Isolated PDNs has been renamed to DSCRT_PWRGRP_IRQn. This distinguishes that only 1 common IRQn interface to PMIC is needed for both SVS-A & -B to provide VMON coverage across all discrete power resources.
  - MAIN_PWRGRP_IRQn net that is connected to GPIO8 for Isolated PDNs is no longer needed since MCU & Main supplies are now grouped. Hence, GPIO8 can be used as a new “PDN Type” setting by installing an Rpu.



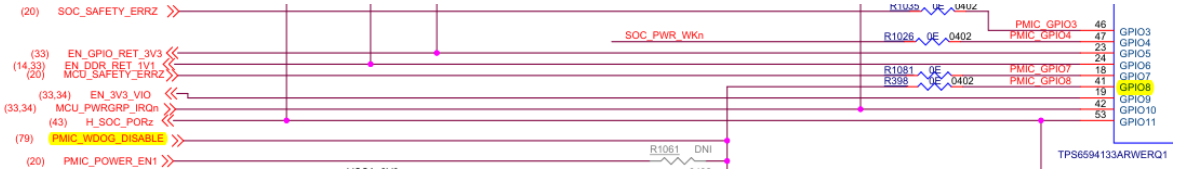
Summary | Optional “WDOG Disable” for GPIO9

- **Update #5: PMIC GPIO9 connections**
  - “PMIC_WDOG Disable” supported by GPIO8 per PMIC NVM v1 (Aug 2022)
  - Wake-up EVMs used PCB designed per PROC141E3_SCH (Sept 2022)

PROC141E4_SCH



- Optional “PMIC_WDOG_DISABLE” board control:
  - PROC141E3/E4_SCH
    - Originally “PMIC_WDOG_DISABLE” net connected to R398 (0-ohm) & interface to PMIC GPIO8



  - PROC141E5_SCH (Impacts)
    - “PMIC_WDOG_DISABLE” net moved to GPIO9

PROC141E5_SCH

Exiting MCU_PWRGRP_IRQn fault condition

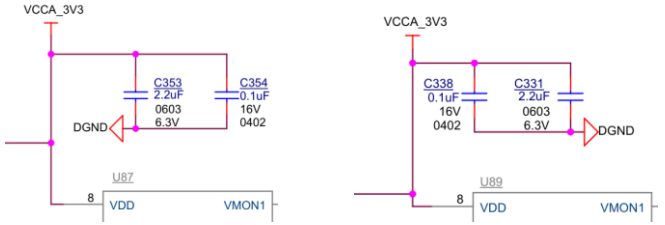
Summary | SoC Cold Boot after MCU_PWRGRP_IRQn fault

- **Criticality:** High
- **Description:** Previously asserted MCU_PWRGRP_IRQn will abort SoC system cold boot attempts.
- **Key Updates (Impacts):**
  - SVS-A & -B supply connections need to change from “Always On” VCCA_3V3 to VDD_MCUIO_3V3 sourced from PMIC’s LDO2. This enables the PMIC to clear an SVS asserted IRQn when executing an SoC power down seq before entering into Safe Recovery State (SRS) & attempting a system recovery by executing an SoC power up seq.
- **Explanation**
  - If a fault occurs on a discrete power device monitored by SVS-A covering SoC’s Main supplies, then the MAIN_PWRGRP_IRQn net will assert causing PMIC to immediately set “SOC Power Error” trigger, resulting in PFSM executing the “PWR_SOC_ERR” state transition to the “MCU ONLY” destination state (for details see Table 5-1 in Powering Jacinto 7 SoC For Isolated Power Groups With TPS6594133A-Q1 + Dual HCPS (ti.com)). System SW running on MCU can use I2C comm to identify the fault & clear SVS-A’s IRQn by register writes if an SoC re-boot is desired.
  - If a fault occurs on a discrete power device monitored by SVS-B covering SoC’s MCU supplies, then the MCU_PWRGRP_IRQn net will assert causing PMIC to immediately set “MCU Power Error” trigger, resulting in PFSM executing the “TO_SAFE_ORDERLY” state transition to the “SAFE” destination state (for details see Table 5-1 in Powering Jacinto 7 SoC For Isolated Power Groups With TPS6594133A-Q1 + Dual HCPS (ti.com)).
    - Once the SAFE state has been entered, MCU I2C comm to clear SVS-B IRQn will not be possible since all SoC supplies are disabled. PMIC will attempt a maximum of 16x SOC cold boots over a period of time while the PMIC is in SRS. SVS-B’s previously asserted IRQn will remain asserted if the SVS is powered from always on VCCA_3V3 & cause the PMIC to abort any new SoC power up seq.
  - Same issue & fix applies for Grouped MCU & Main PDN types (-3G to -3M) when DSCRT_PWRGRP_IRQn asserts.

Summary | SoC Cold Boot after MCU_PWRGRP_IRQn fault

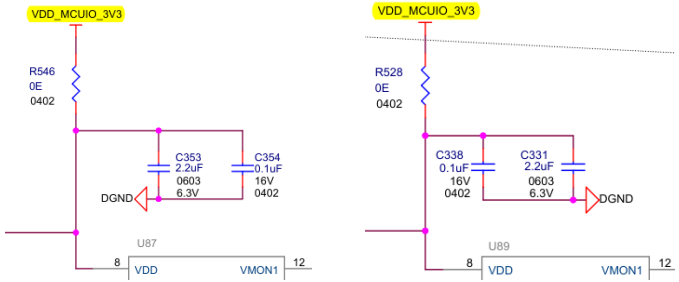
- **Update #6: Clearing asserted MCU_PWRGRP_IRQ**
- Safety Voltage Supervisors (TPS389006004-Q1) supply connection
  - PROC141E4_SCH
    - Connected to VCCA_3V3 = “always on” VSYS_3V3

PROC141E4_SCH



  - PROC141E5_SCH (Impacts)
    - Connect to VDD_MCUIO_3V3 supplied from PMIC LDO2 for PDN-3A to -3F.

PROC141E5_SCH



    - Connect to VDD_GPIORET_IO_3V3 supplied from PMIC LDO2 for PDN-3G to -3M. (Source remains the same but net name changes due to Grouped MCU & Main PDN type.)

Discrete LDO Ramping Slew Rates

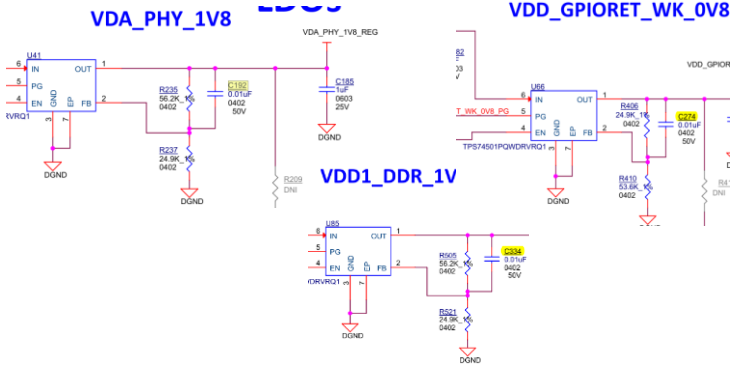
Summary | Discrete LDO Ramping Slew Rates

- **Criticality:** Medium
- **Description:** Discrete LDOs (TPS74501P-Q1) used to supply power rails VDD_PHY_1V8, VDD_GPIORET_WK_0V8 & VDD1_DDR_1V8 have excessive ramp-up & down slew rates impacting desired power sequences. Optional feed-forward caps (Cff) were installed for improved noise & PSRR performance but previous J7 EVMs have not needed or used Cff caps.
- **Key Updates (Impacts):**
  1. Remove optional 0.01uF feed-forward caps (Cff) from all 3x TPS74501P-Q1 LDOs

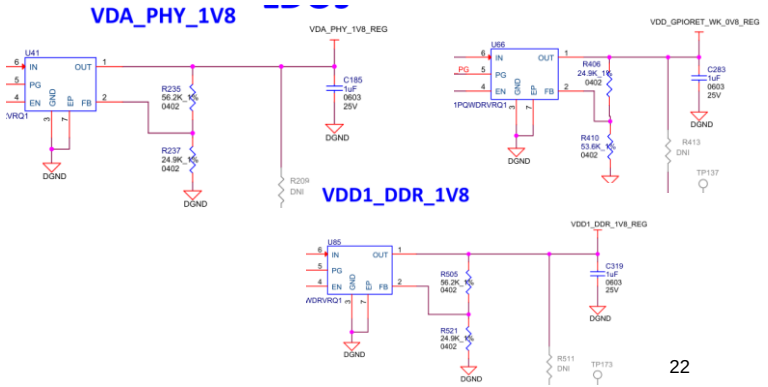
Summary | Discrete LDO Ramping Slew Rates

- **Update #7: Improve discrete LDO slew rates**
- Remove TPS74501P-Q1 optional feed-forward caps (Cff)
  - PROC141E4_SCH
    - C192, C274 & C334 = 0.01uF
  - PROC141E5_SCH (Impacts)
    - Remove C192, C274 & C334

PROC141E4_SCH



PROC141E5_SCH



PMIC LDO cold temperature stability

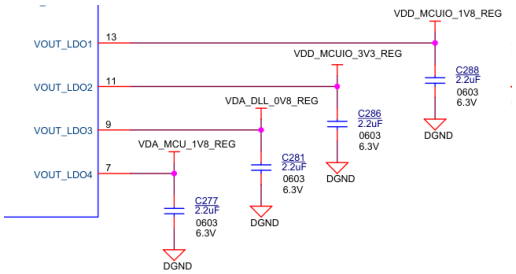
Summary | PMIC LDO cold temperature stability

- **Criticality:** Low
- **Description:** PMIC's LDO3 output voltage stability for output capacitance exceeding data sheet max rating of 20uF at cold temperatures can be improved by installing a 10mA "bleed resistor" per PMIC team recommendation.
- **Key Updates (Impacts):**
  1. Add a 10mA "bleed resistor" on LDO3 Vout for a minimum load to avoid possible supply oscillations at low temperatures following LDO enabling with no load prior to booting SoC.

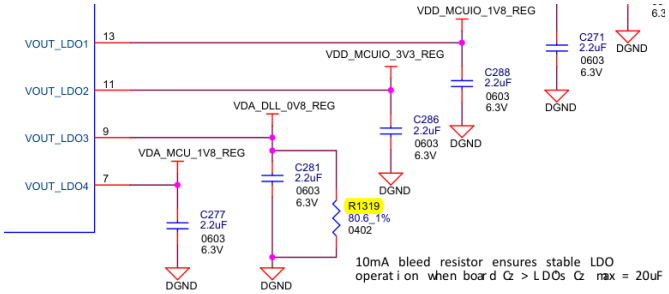
Summary | PMIC LDO cold temperature stability

- **Update #8: PMIC LDO3 Coz > 20uF capacitance**
- LDO3 supplies power rail VDA_DLL_0V8
  - PROC141Ex_SCH
    - VDA_DLL_0V8 rail supports 4x DDR & 1x MMC0 PLL input supplies that require low freq, low noise performance with 1.0 & 10uF decoupling caps recommended.
    - Cnom total = Cnom_local + Cnom_PoL = 2.2uF + 5x11uF = 57.2uF
    - Cz total = 57.2 x 50% = 28.6uF > 20uF max Cz
  - PROC141E5_SCH (Impacts)
    - Add 80.6 ohm R1319 to LDO3 Vout
      - 10mA bleed resistor to VDA_DLL_0V8
      - Recommended by PMIC team to avoid instability & oscillations especially at start-up when LDO loads are not active yet.

PROC141E4_SCH



PROC141E5_SCH



Optional eFuse Interface & VPP LDO PN

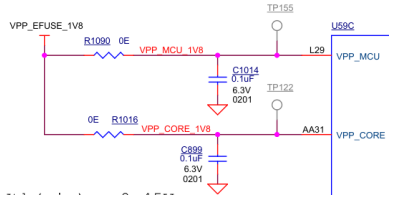
Summary | Optional eFuse Interface & LDO drive

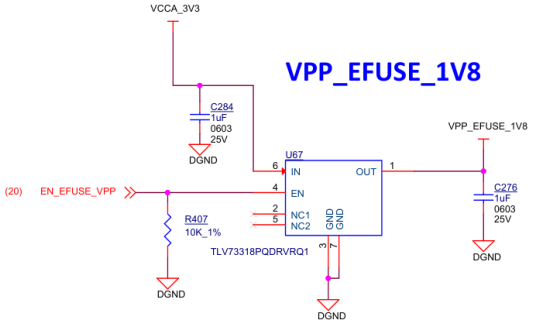
- **Criticality:** Low
- **Description:** The optional SoC eFuse interface for customer programming should only connect to VPP_MCU. A new LDO part number with better transit response and increased output drive current provides more robust eFuse burning performance.
- **Key Updates (Impacts):**
  1. Remove any connection to SoC's VPP_CORE input supply.
  2. Improved LDO performance by changing LDO from TLV73318P-Q1, 300mA LDO to new TPS7A2118P-Q1, 500mA LDO.

Summary | Optional eFuse Interface & LDO drive

- **Update #9: Optional customer eFuse programming**
- Only MCU eFuse support customer programming & improve LDO drive strength for burning customer eFuses
  - PROC141Ex_SCH
    - Originally install 2x 0-ohms at R1090 & R1016
    - Originally U67 used a 300mA LDO (TLV73318P-Q1)

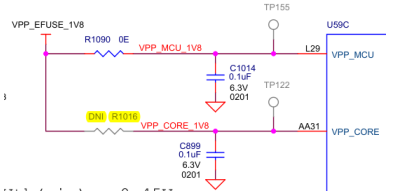
PROC141E4_SCH

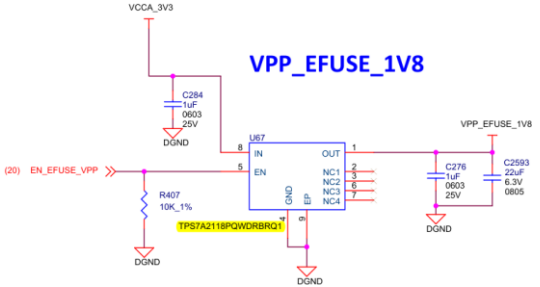




PROC141E5_SCH

- PROC141E5_SCH (Impacts)
  - DNI 0-ohm at R1016
  - Replace U67 with 500mA LDO (TPS7A2118P-Q1)





Rev History

Date	Rev	Author	Description
6/25/2024	0.3	Bill McCracken	Draft for TI internal team reviews
7/16/2024	0.4	Bill McCracken	Updated following EP & PMIC team review. Need PMIC team updates to slide #10.
7/19/2024	0.5	Bill McCracken	Updated slide 10 & added full PMIC ‘133A NVM Rev History slides in Ref Section below.
7/23/2024	0.6	Bill McCracken	Expanded Alert document to include J742S2 EVM
7/29/2024	0.7	Bill McCracken	Clarified last 3x key updates (#s 7 – 9) slides (pgs 19, 22 & 25).
	0.8	Bill McCracken	Clarified Title page’s sub-title to include “and any J7 design using a universal PDN-3x scheme” Clarified Key Updates (slide #2), Note #2 to review vE5 files for more details & minor updates as follows: “… details since this Alert doc does not list all vE5 updates. There are more minor updates (removing unused provisioned nets &/or components) in SCH, BOM & PCB.”
8/8/2024	0.9	Bill McCracken	Added new slide #3 to provide CDDS links to vE5 SCH & PDN diagram files while PCB is being updated and after EVM is released the TI website link for downloading all source files.
9/12/2024	1.0	Bill McCracken	Added Universal PDN Updates Implementation Guidance summary across different J7xxx & PDN Types

Reference Section

TPS6594133A NVM | Revision History

Revision	Release Date	Comments
0.0	April 25, 2022	
1.0	August 8, 2022	
2.0	October 10, 2022	TI J784S4 EVM Samples
3.0	December 15, 2022	RTM’d in January 2023
4.0	Only released in sample units	
5.0	March 1, 2024	PCN released and all parts received after March 1st , 2024 contain Rev 5

TPS6594133A NVM | Revision Details

Rev	Change	Impact of Change
1.0	GPIO Retention Entry/Exit Handling – If Wake signal triggers while being armed, PMIC will enter Retention and then immediately exit.	Prevents PMIC from getting stuck in Retention
	Power Down Sequence Timing Changes -Updated power down seq of VDA_DLL_0V8 to shift disabling from 2.5ms to 1.0ms due to ~1ms delay in VDA_DLL_0V8 RC discharge before VDD_CPU_AVS & VDD_CORE_0V8 are disabled by VDA_DLL_0V8 dropping below 0.6V FET Von threshold. -Updated power down seq of VDD_MCU_0V85 to shift disabling from 2.5ms to 2.0ms to ~align with disabling of VDD_CPU_AVS & VDD_CORE_0V8.	Overall sequence time remains the same. Better power down seq when using discrete component rails to align with J7 SoC DM recommended seq.
	At startup, all PMIC power resources/rails mapped to a single MCU_PWR_ERR group	• Enables 1x PMIC PN to support both Grouped & Isolated PDN board designs • Grouped MCU & Main PDNs (3G to 3M) need 1x PMIC power group to enable fault on any monitored rail to cause an orderly shutdown. • Isolated MCU & Main PDNs (3A to 3F) will need MCU SW to create 2x power groups (MCU & Main) by writing 0x1E to PMIC register 0x44

TPS6594133A NVM | Revision Details

Rev	Change	Impact of Change
2.0	VCCA input voltage level auto-detection	Enables 1x PMIC PN to support PDNs with VCCA voltage of 5V or 3.3V
	Watchdog Timer disabled	• GPIO8 used for PMIC config control • MCU SW will need to start watchdog timer as part of enabling full FuSa features
	GPIO8 logic level latched before 3ms time step of power up sequence & directs PMIC to configure internal resources: • Low = Creates 2x power groups; Enables BUCK5 per power up seq • High = Creates 1x power group; Removes BUCK5 from power up seq	• Isolated MCU & Main PDNs (3A to 3F) need 2x power groups, use Buck5 for VDD_MCU_0V85 rail & connect MAIN_PWRGRP_IRQn to GPIO8 for discrete power resource monitoring. • Grouped MCU & Main PDNs (3G to 3M) need 1x power group, removes Buck5 from pwr up seq (Buck5 can be reassigned by SW config to supply a peripheral rail after SoC & SW boot-up) & connects GPIO8 to pull-up resistor to set logic high.

TPS6594133A NVM | Revision Details

Rev	Change	Impact of Change
2.0	Removed any2ota sequence	PMIC OTA preparation sequence is no longer available. Unused during normal operation.
	Fixed GPIO10 response during normal operation	Prevents PMIC from getting stuck after MCU_PWRGRP_IRQn triggers a recovery attempt
3.0	Adjusted internal setting for improved BUCK reliability	No impact to function

TPS6594133A NVM | Revision Details

Rev	Change	Impact of Change
4.0	Watchdog enabled by default with 1 sec long window	MCU SW must boot and configure watchdog within 1 second of nRSTOUT going high
	Change default GPIO9 function from GPIO to WD_DISABLE	GPIO9 starts as an input to set WD_PWRHOLD bit, then changes to an output. **In Development:** Customer has *option* to use external PU resistor to set WD_PWRHOLD =1 **In End Equipment:** No impact to function
	TO_ACTIVE sequence has 500us delay between LDO3 and BUCK5	In systems with split power groups, PMIC BUCK5 powers up fully before PMIC LDO3. Overall sequence time remains the same.
	LDO2 OV/UV Threshold changed from 5% to 10%	When used as 3.3V load switch, PG Window will match that of VCCA. Customer can tighten after boot.

*Error found EN_I2C_CRC sequence, only on Rev4

TPS6594133A NVM | Revision Details

Rev	Change	Impact of Change
5.0	Watchdog Long Window set to 13 minutes.	MCU SW must boot and configure watchdog within 13 minutes of nRSTOUT going high
	Fixed EN_I2C_CRC sequence error	MCU can use I2C_2 FSM Trigger to enable I2C CRC

Rev 4 I2C_CRC_EN Error and Workaround

- **What**: Setting I2C_2 FSM Trigger high to enable the I2C CRC does not work on Rev 4 of TPS6594133A
- **Why:** Implementation of changes for watchdog and GPIO9 for disable watchdog pushed NVM over the memory limit
- **Affected Revisions:** Only Rev 4 is impacted. This was fixed in Rev 5
- **Software Workaround:** Instead of using the I2C_2 FSM trigger, please use SW workaround described on next page

SW Workaround Steps

1. Write to I2C base address 0x48:
    a. Value: 0x34
    b. To register: 0x54
2. Unlock procedure: (Warning all of these writes must be separate commands with no other I2C communication on the line in between)
    a. Write to I2C base address 0x48:
        A. Value: 0x98
        B. To register: 0xA2
    b. Write to I2C base address 0x48:
        A. Value: 0xB8
        B. To register: 0xA2
    c. Write to I2C base address 0x48:
        A. Value: 0x13
        B. To register: 0xA2
    d. Write to I2C base address 0x48:
        A. Value: 0x7D
        B. To register: 0xA2
    e. Finished with unlock, verify by reading back on register 0xA3, value from readback is 0xC0
3. Write to I2C base address 0x49:
    a. Value: 0x06
    b. To register: 0x1A
4. CRC is now enabled, can use CRC writing or I2C commands without CRC w/ padding CRC value
    a. If padding with I2C, use part **c.**
5. Write to I2C base address 0x48:
    a. Value: 0x02
    b. To register: 0xEF
    c. CRC Value to follow: 0x0C
6. Wait 2ms
7. Write to I2C base address 0x48:
    a. Value: 0x30
    b. To register: 0x54
    c. CRC Value to follow: 0x4A
8. Write to I2C base address 0x48:
    a. Value: 0x00
    b. To register: 0xA2
    c. CRC Value to follow: 0xB0
9. Done