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REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR
0.20	15 Sep. 2022	DVT1 Board release	qxn
0.21	Nov. 10, 2022	1. Modify all crystal CL value to match frequency 2. Add serial termination resistors for RGB data lane 3. Add CMC on HDMI output 4. Use WKUP_CLKOUT0 for WiFi 5. Use MCU_OBSCLK0 for GBE 6. Increase resistance on all board LEDs 7. Remove R243 TP_INT Pulldown 8. Add ferrite bead on Grove and QWIIC 9. Add feed forward capacitor on TLV62595 10. Remove ESDs on HDMI TMDS signals	qxn
0.22	Dc. 12, 2022	1. Add feed forward capacitor on TLV62595 2. Remove ESDs on HDMI TMDS signals 3. Add ferrite bead on HDMI shield 4. Change R16 and R80 to 0R 5. Change pullup resistors to 2.2k on I2C0-I2C3 6. Change FB30 and FB31 to 0R	qxn
1.0	Dc. 27, 2022	1. Add testpoint to QWIIC 2. Add serial resistors on I2C0 - I2C3 SCL 3. Add more capacitors on VDD_1V2 4. Add 0R on HDMI shield 5. Add series resistor on SPE LED control	qxn

Main

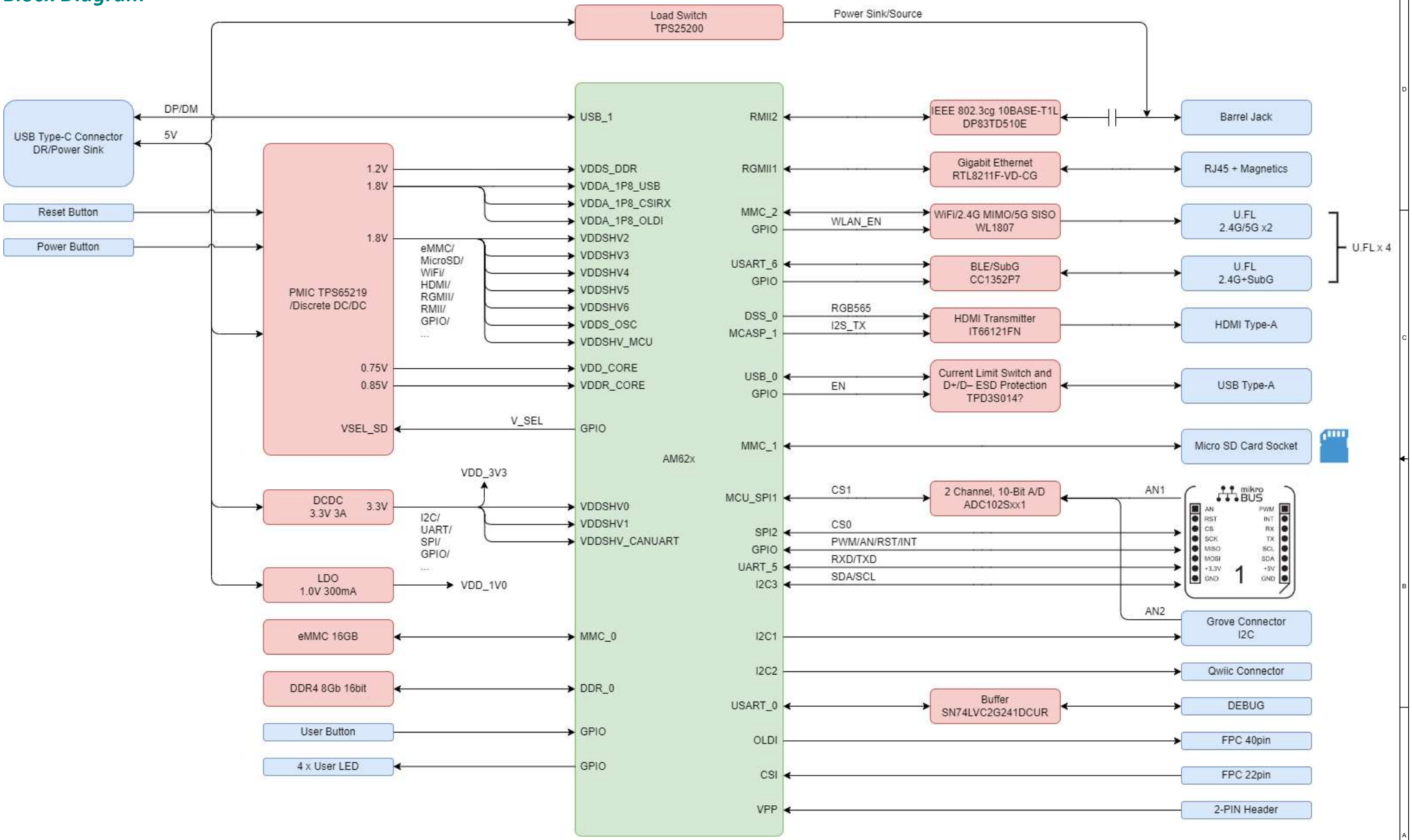
seeed studio https://www.seeedstudio.com

Title: BeaglePlay

Size:	Document Number:	Rev:
A3	001_Revision History	v1.0

Draw By:	Date:	Sheet:
qxn	Monday, March 06, 2023	1 of 22

Block Diagram



Main

seeed studio	https://www.seeedstudio.com	
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Size: A3	Document Number: 002_Block Diagram	Rev: v1.0
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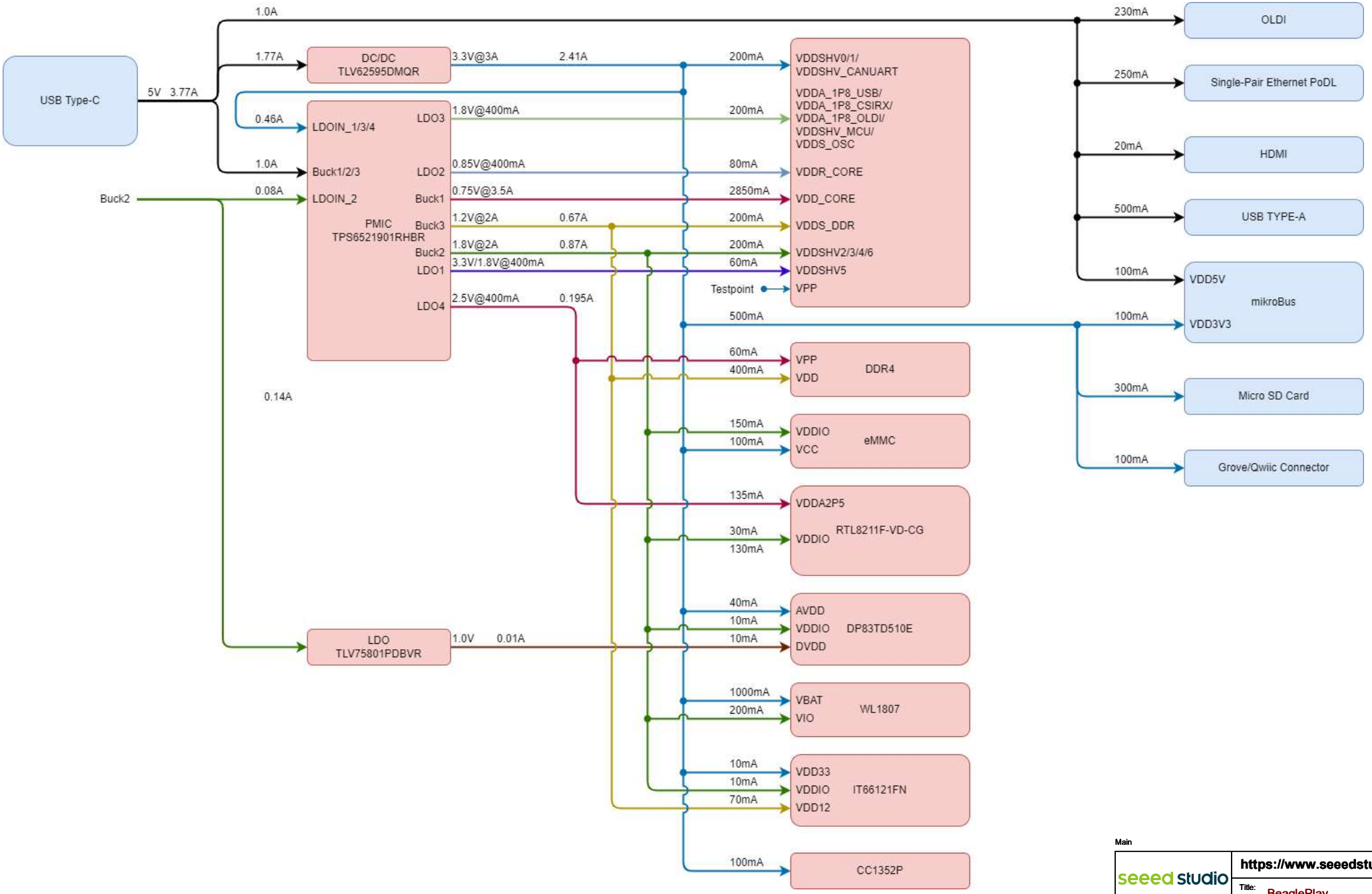
Power tree



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seeed studio	https://www.seeedstudio.com	
	Title: BeaglePlay	
Size: A3	Document Number: 003_Power Tree	Rev: v1.0
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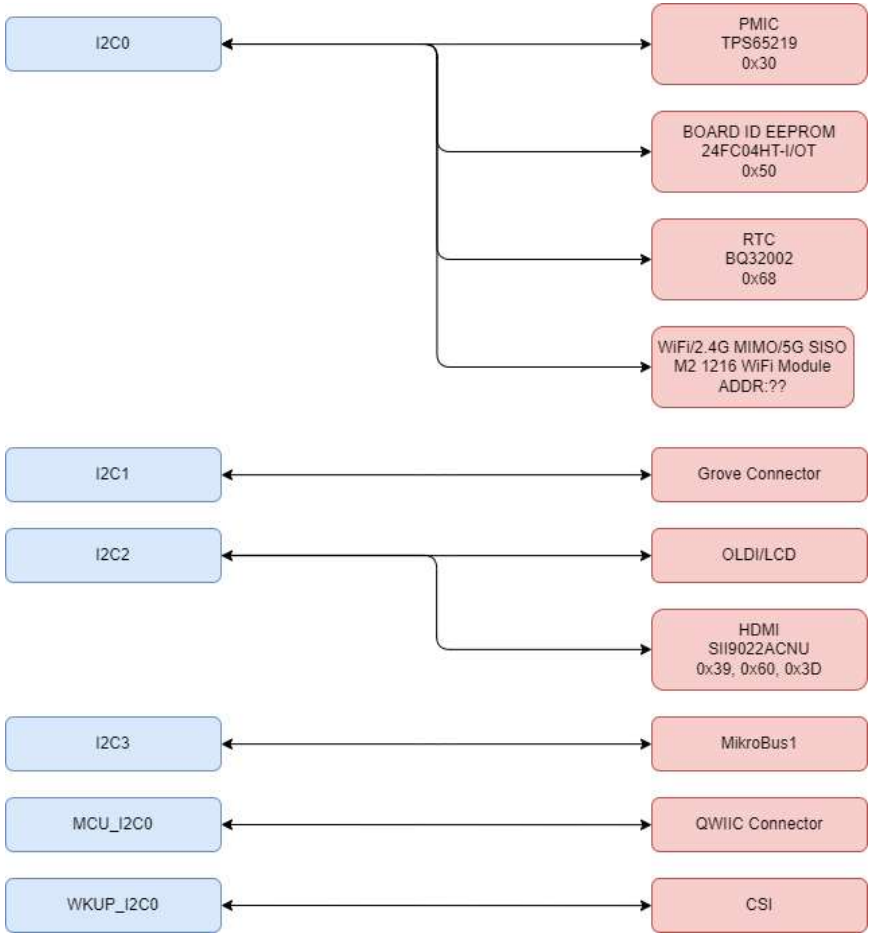
I2C Usage Diagram



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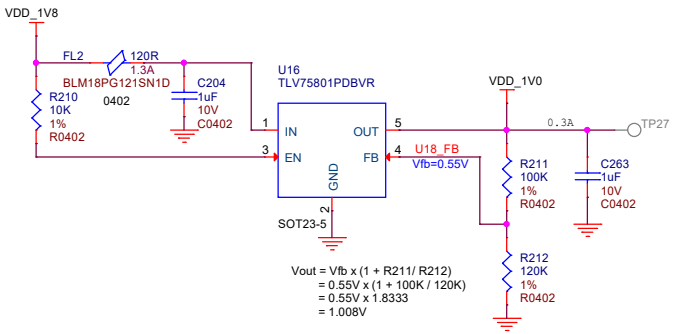
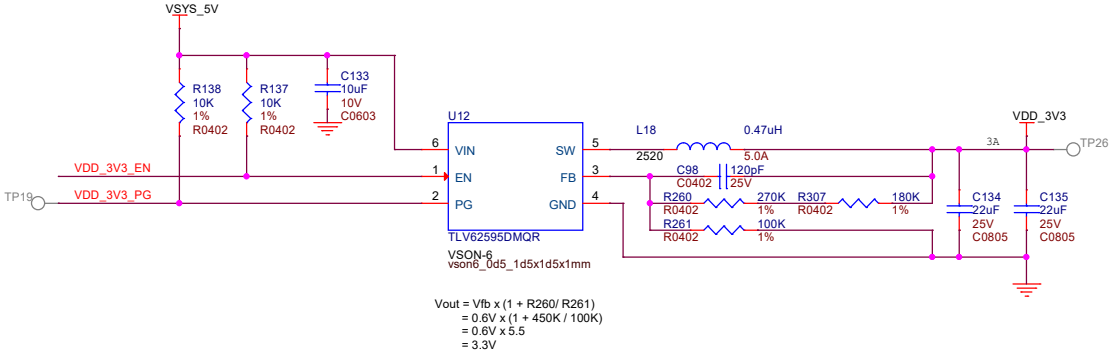
	Title: BeaglePlay	
Size: A3	Document Number: 004_I2C Usage Diagram	Rev: v1.0
Draw By: qxn	Date: Tuesday, December 27, 2022	Sheet: 4 of 22

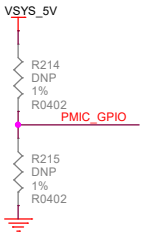
LDO 1V0



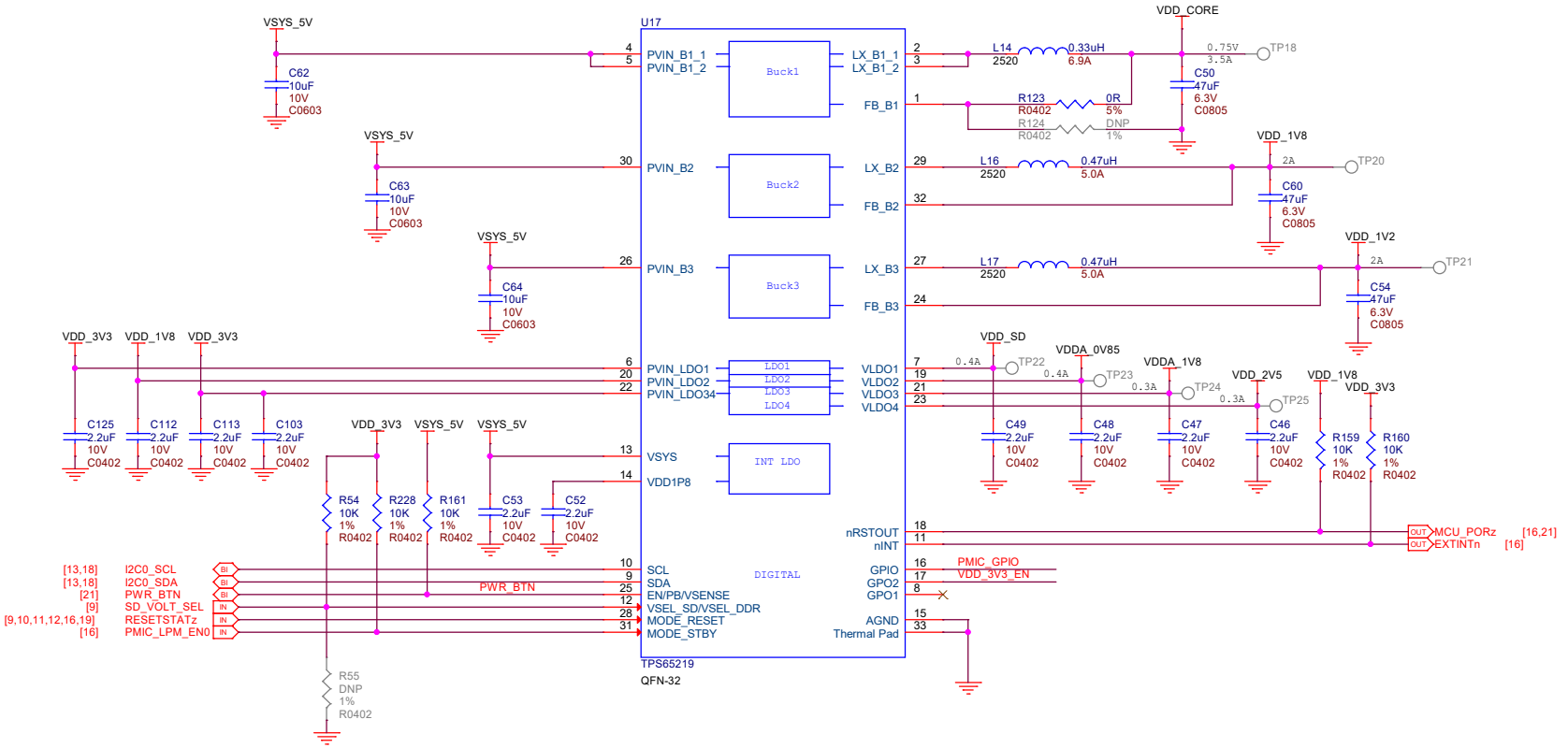
DCDC 3V3



PMIC_Strap option



PMIC



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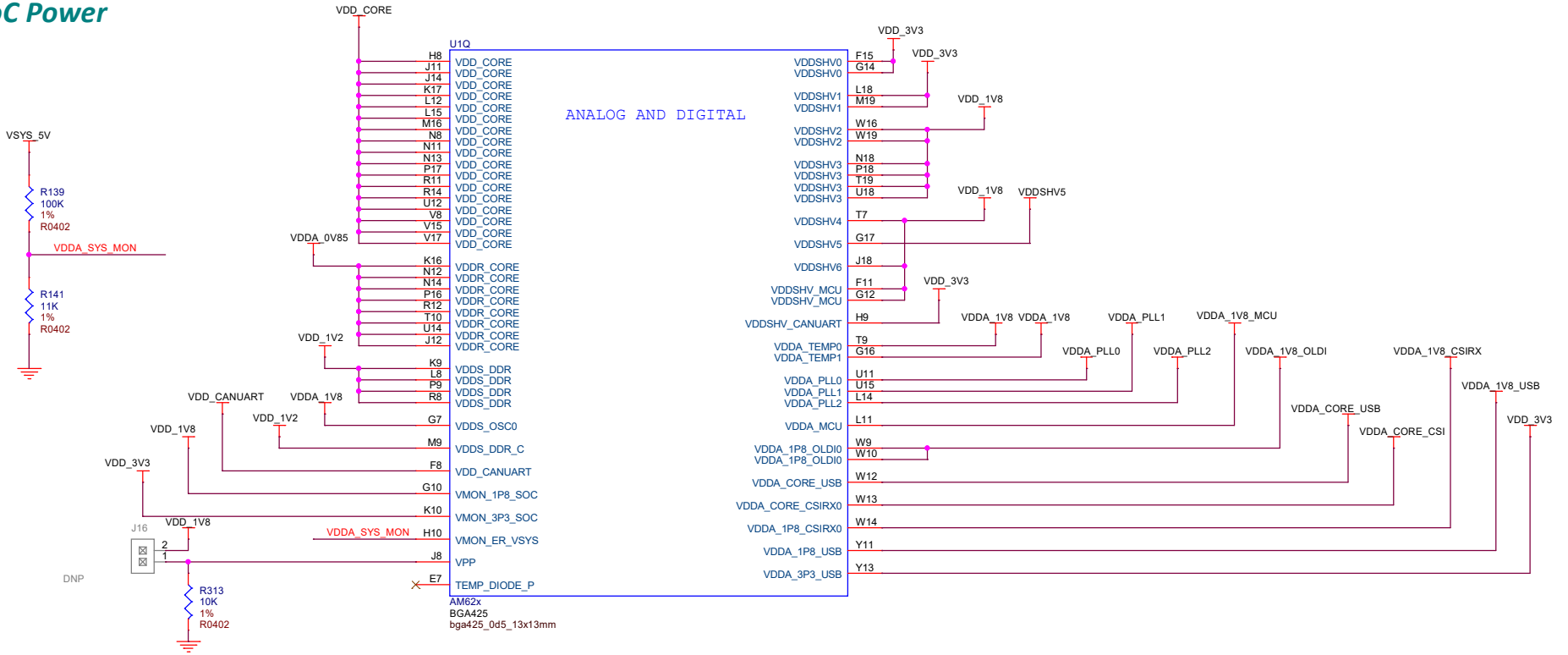
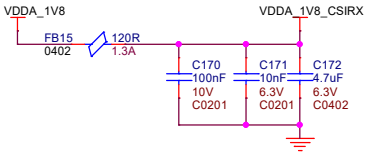
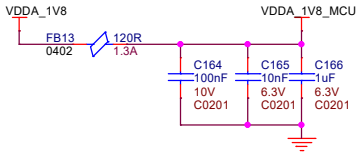
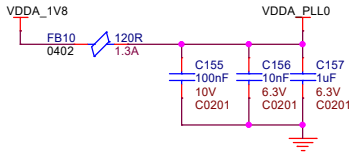
seeed studio	https://www.seeedstudio.com	
	Title: BeaglePlay	
Size: A3	Document Number: 005_DCDC & PMIC	Rev: v1.0
Draw By: qxn	Date: Tuesday, December 27, 2022	Sheet: 5 of 22

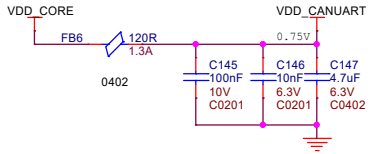
SoC Power

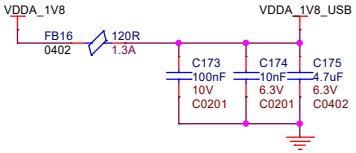


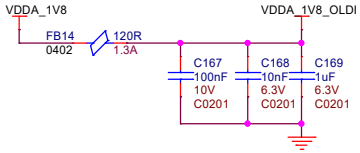


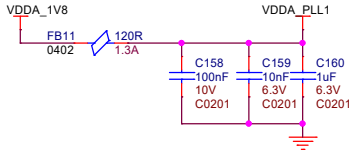


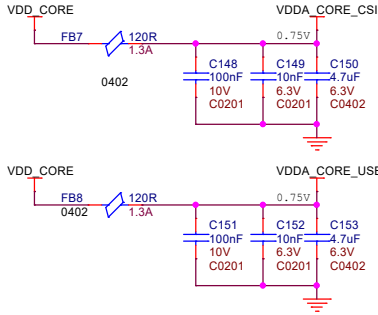


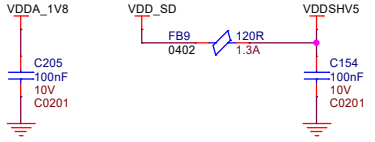


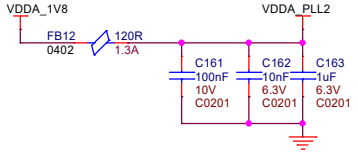












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seeed studio	https://www.seeedstudio.com	
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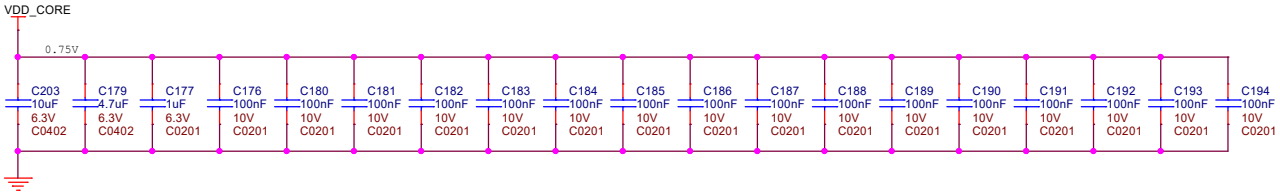
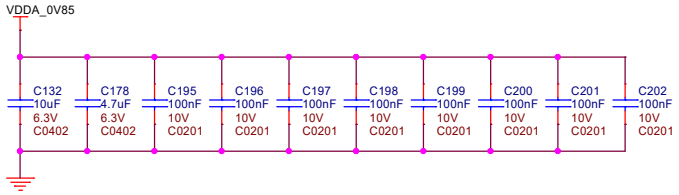
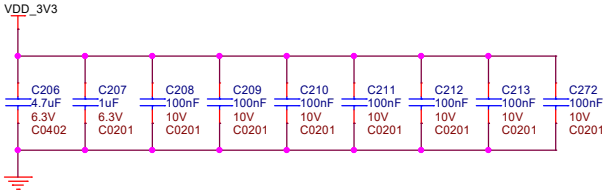
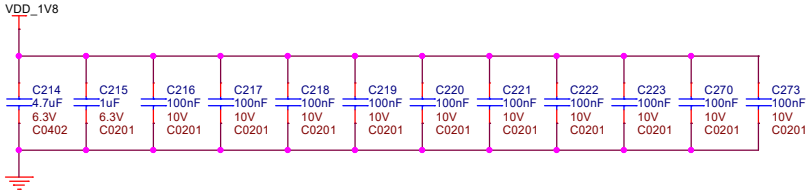
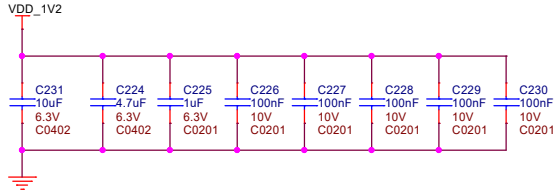
SoC DCAPs

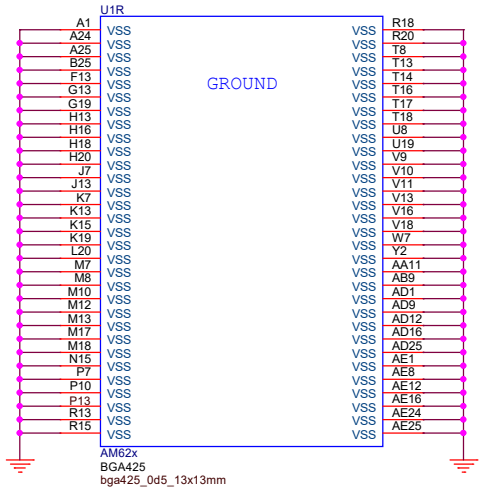


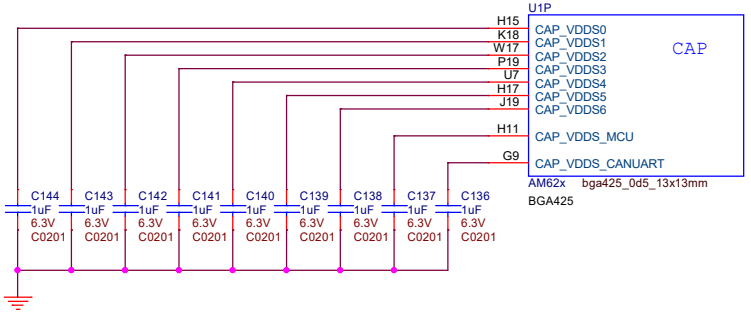












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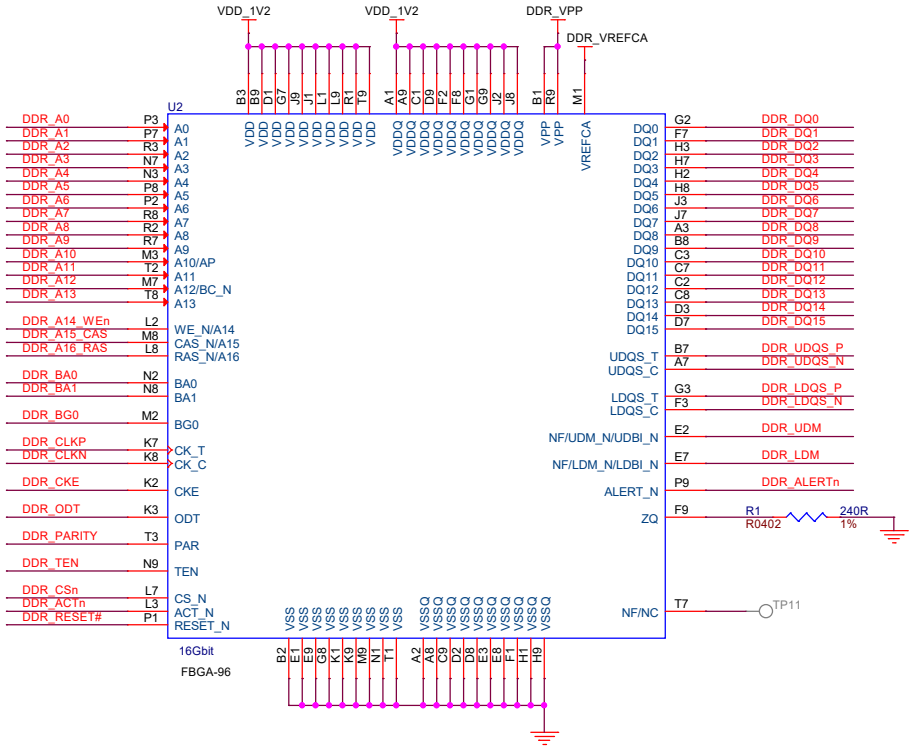
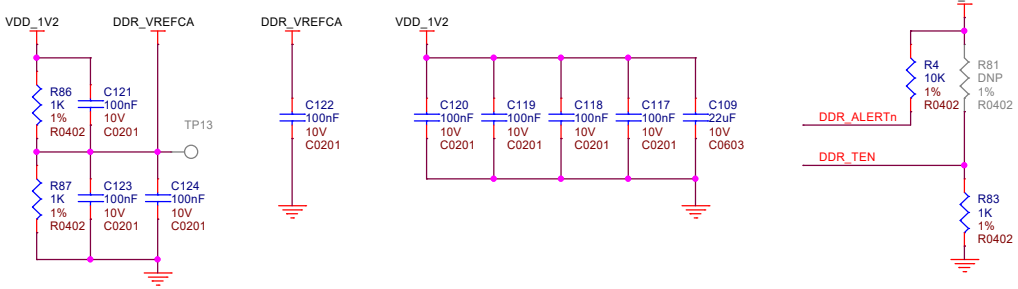
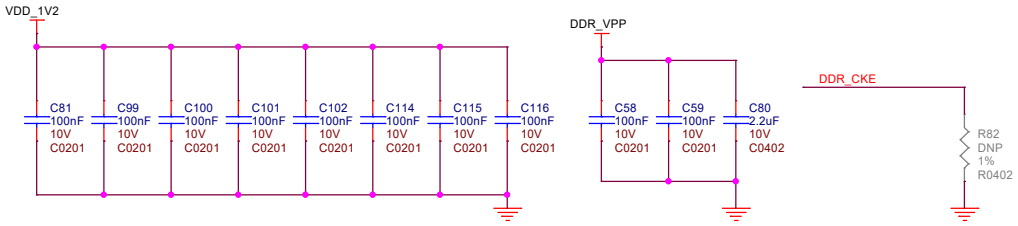
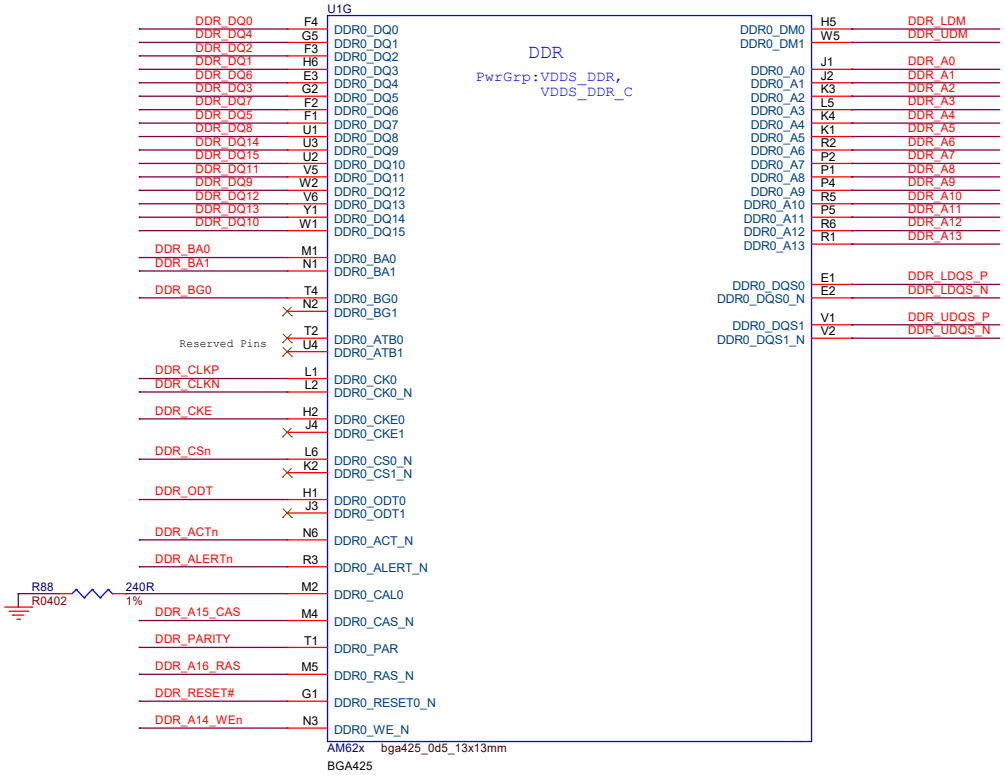
DDR4

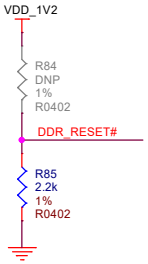




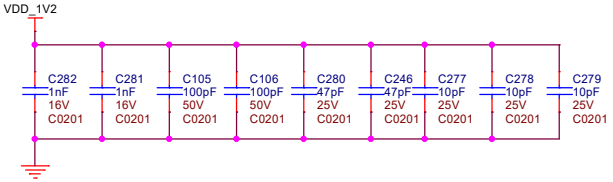


SoC DDR controller





NOTE: DDR DQ Lines Swapped
Within Data Byte



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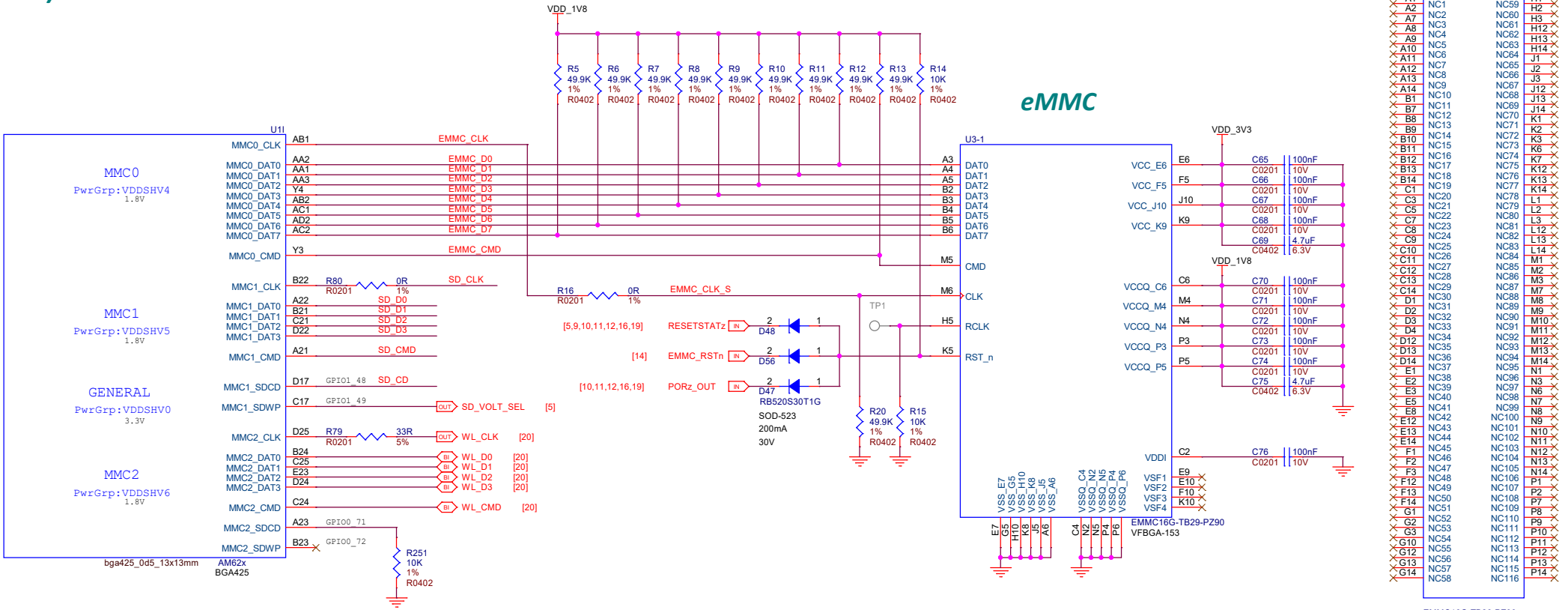
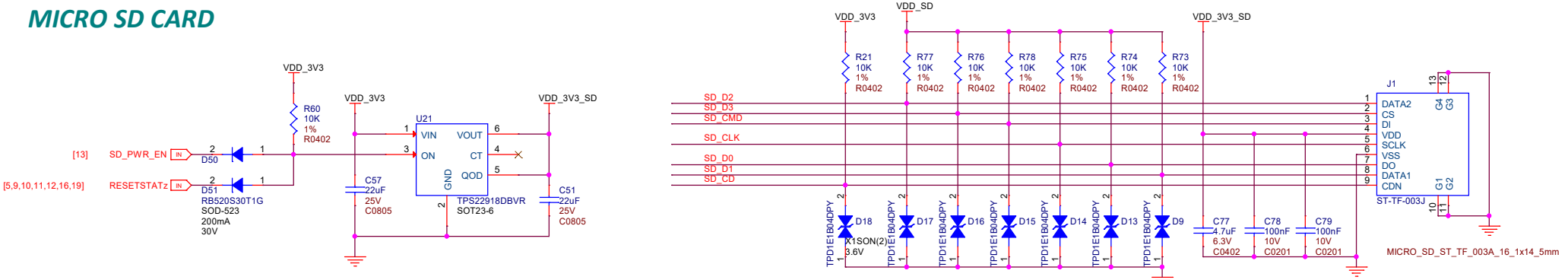
seeed studio	https://www.seeedstudio.com	
	Title: BeaglePlay	
Size: A3	Document Number: 008_SoC DDR & DDR4	Rev: v1.0
Draw By: qxn	Date: Tuesday, December 27, 2022	Sheet: 8 of 22

eMMC/SD



eMMC

MICRO SD CARD



Main

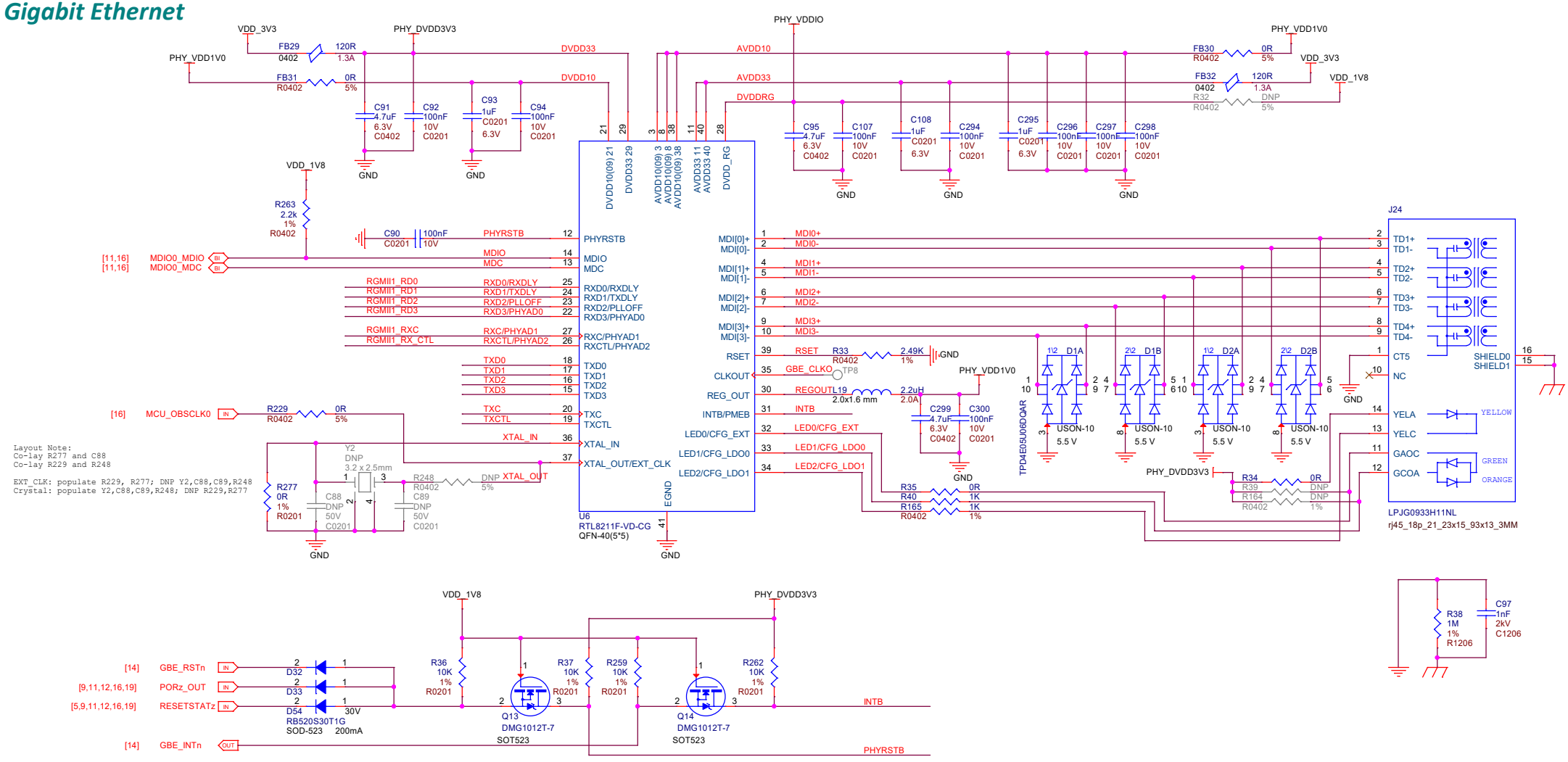
seeed studio

https://www.seeedstudio.com

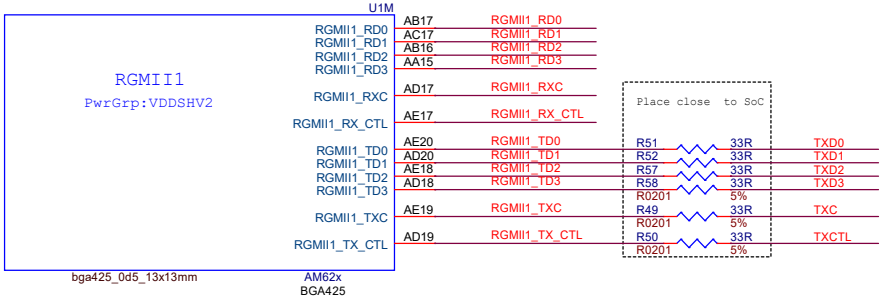
Title: BeaglePlay

Size: A3	Document Number: 009_SoC SDIO & eMMC & SD	Rev: v1.0
Draw By: qxn	Date: Tuesday, December 27, 2022	Sheet: 9 of 22

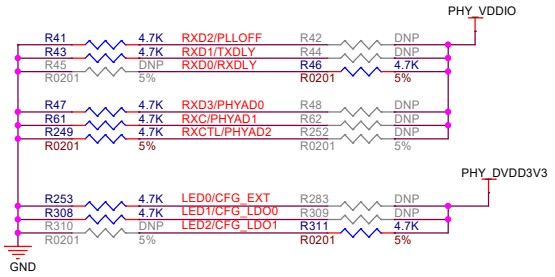
Gigabit Ethernet



SoC MAC 1.8V



Strap options




```
CFG_EXT = 0, CFG_LDO[1:0] = 10 :   Internal 1.8V
PHY_AD[2:0] = 000:                 PHY Addr 000
PHY_PLLOF = 0 :                    Enable PLL
PHY_TXDLY = 0 :                    TX delay: 0ns
PHY_RXDLY = 1 :                    RX delay: 2ns
```

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seeed studio	https://www.seeedstudio.com	
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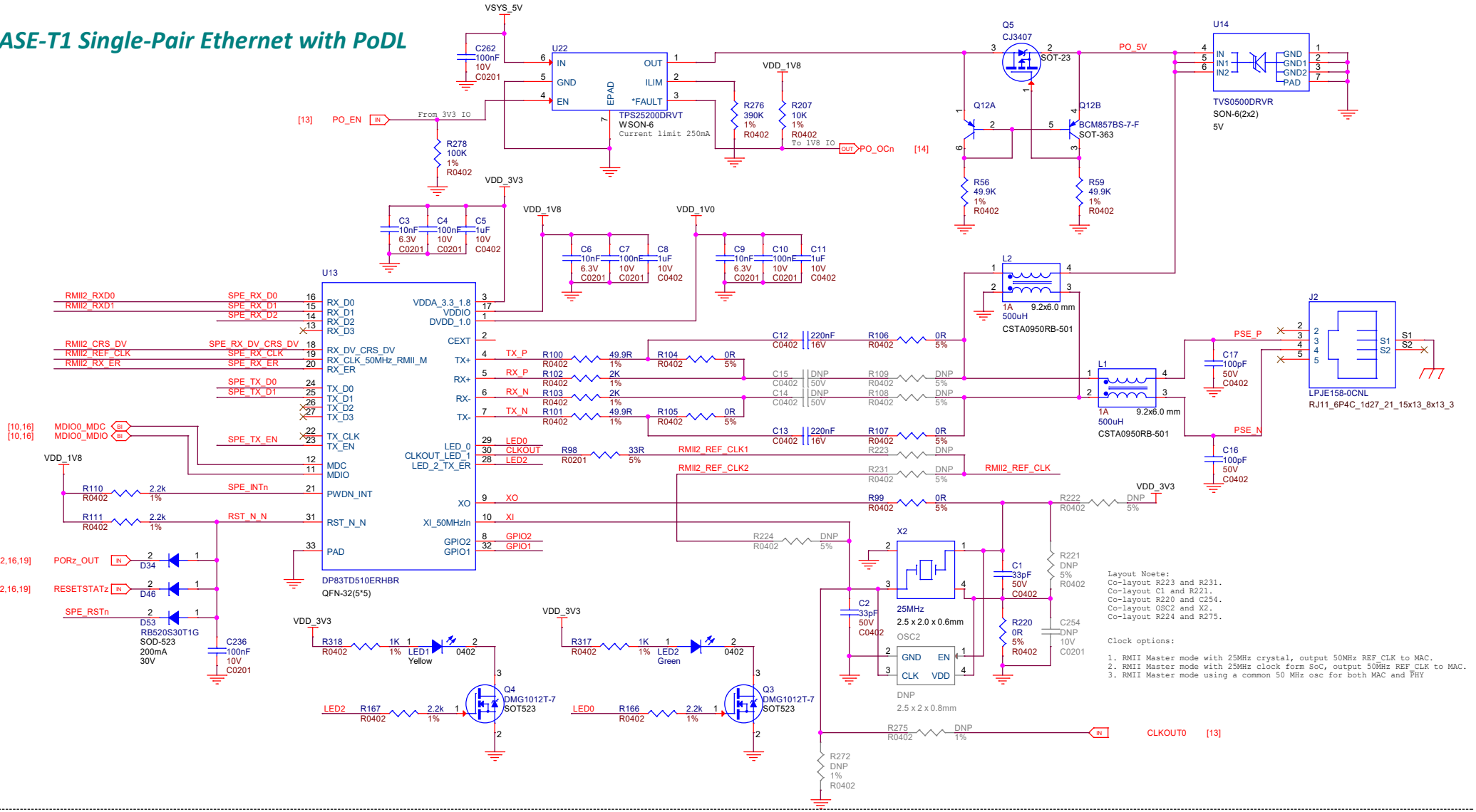
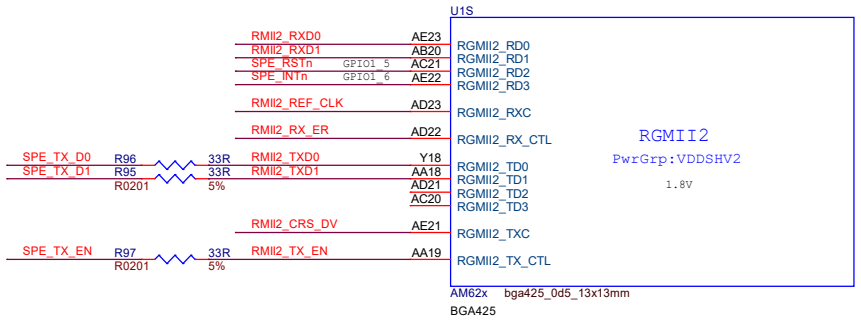
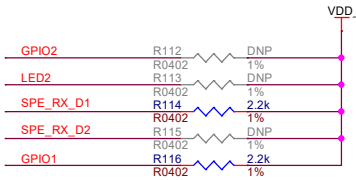
10BASE-T1 Single-Pair Ethernet with PoDL



SoC MAC 1.8V



Strap options



Strap options:
1.PHY ADDR: 0b0001
GPIO1: External PH
RX_ER: Internal PD
RX_D0: Internal PD
RX_D3: Internal PD
2.VGltage level: 2.4V&1.0V p2p
LED2: Internal PD
3.Mode: RMII Master
RX_D1: External PU
LED0: Internal PD
4.RMII MODE: CRS_DV
RX_D2: Internal PD
5.Termination: 50 Ohm
GPIO2: Internal PD
6.Clockout: 25MHz
RX_DV: Internal PD

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seeed studio	https://www.seeedstudio.com	
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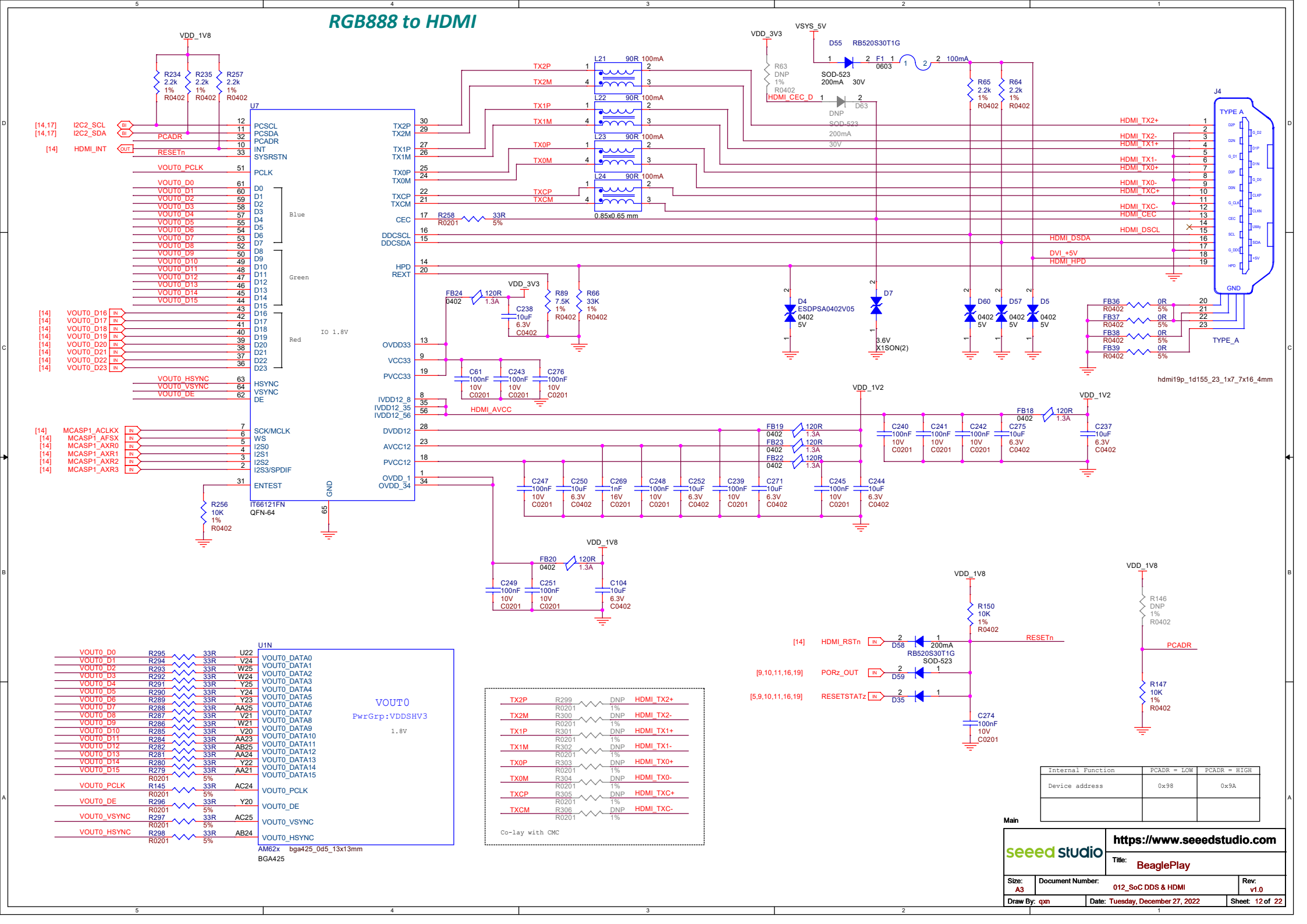
RGB888 to HDMI



Internal Function	PCADR = LOW	PCADR = HIGH
Device address	0x98	0x9A

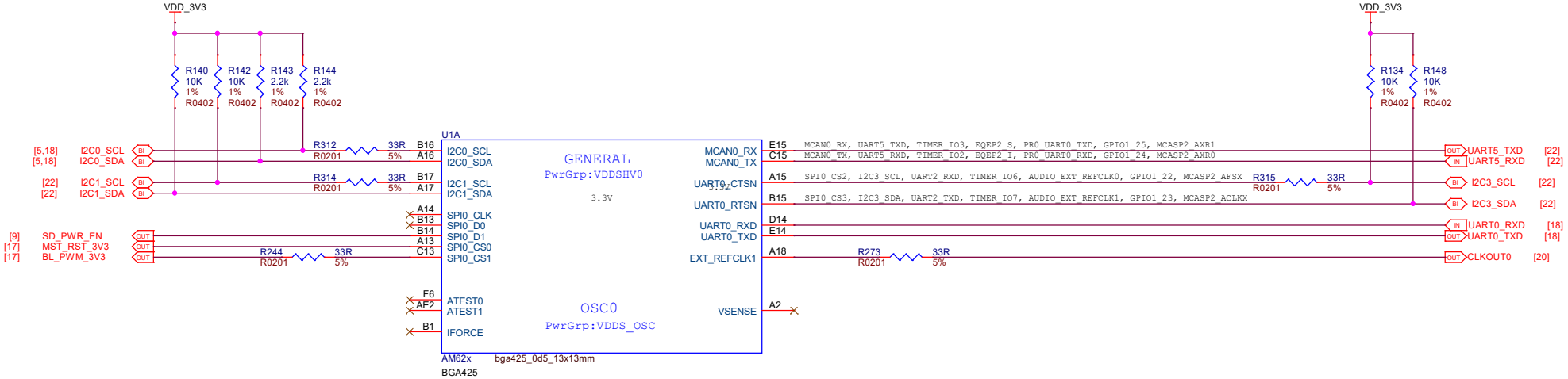
Main

seeed studio https://www.seeedstudio.com

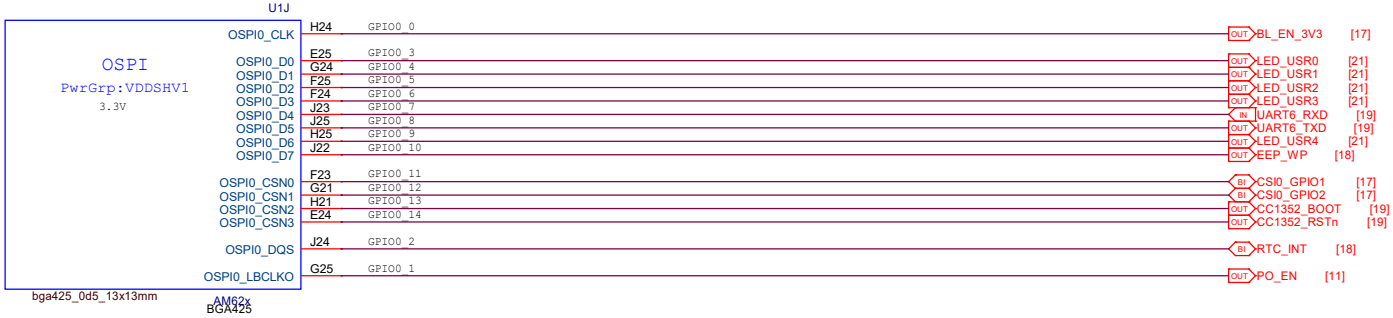
Title: BeaglePlay

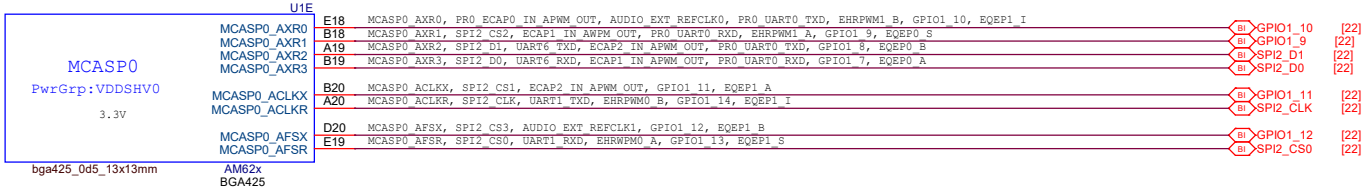
Size: A3	Document Number: 012_SoC DDS & HDMI	Rev: v1.0
Draw By: qxn	Date: Tuesday, December 27, 2022	Sheet: 12 of 22

SoC GPIO 3.3V



SoC GPIO 3.3V





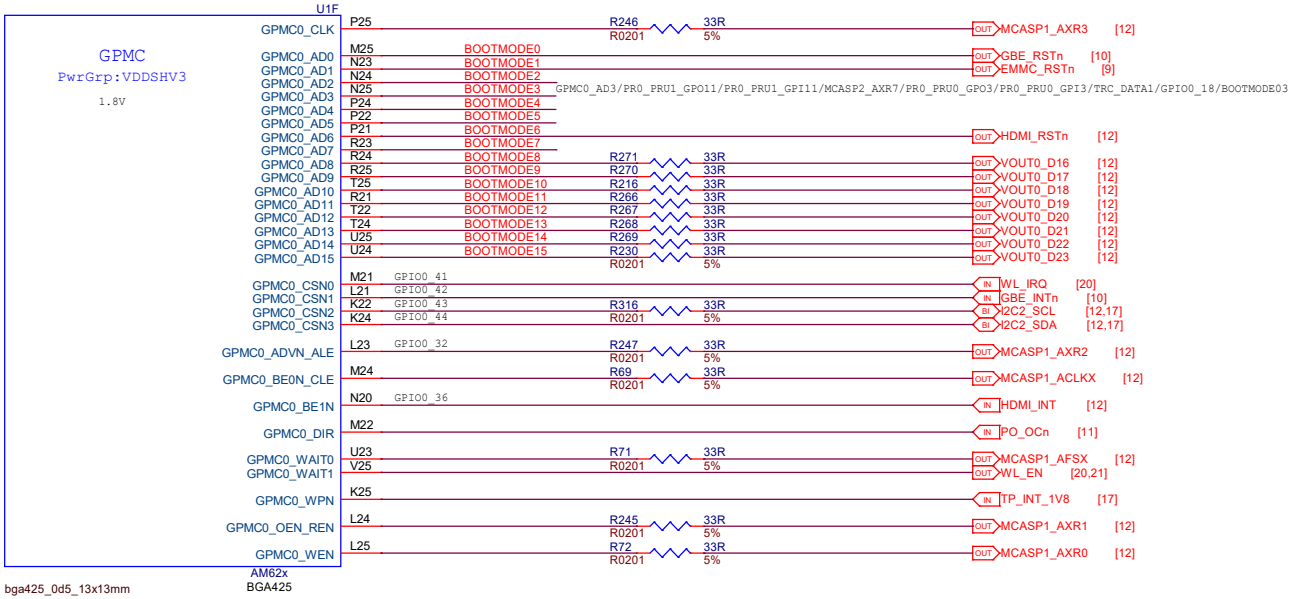
Main

seeed studio

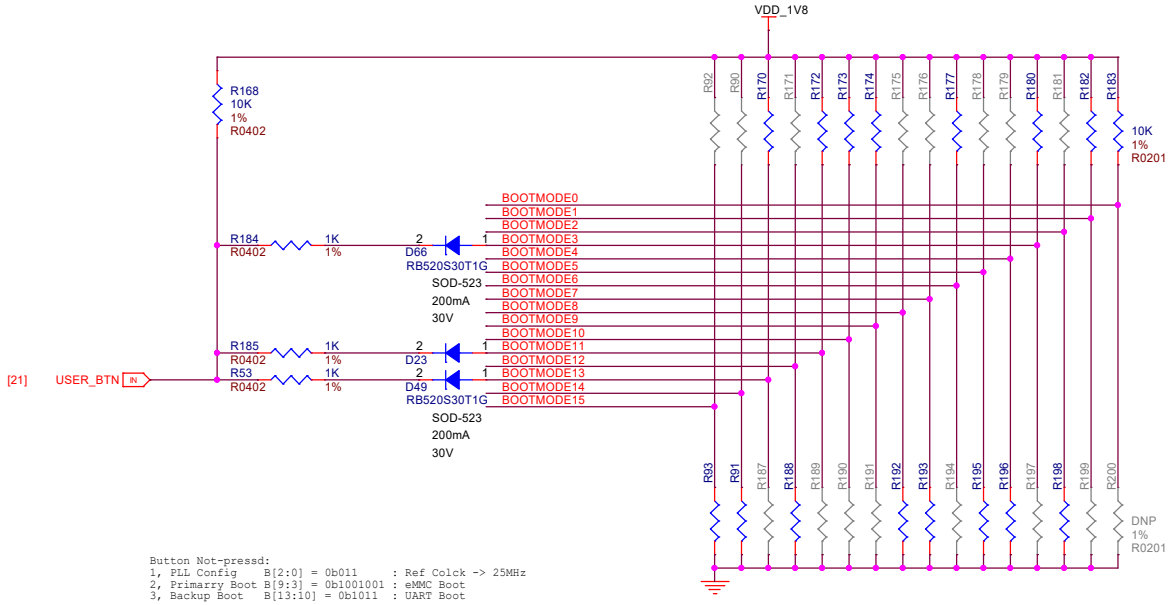
https://www.seeedstudio.com

Title: BeaglePlay		
Size: A3	Document Number: 013_SoC GPIO 3.3V	Rev: v1.0
Draw By: qxn	Date: Tuesday, December 27, 2022	Sheet: 13 of 22

SoC GPIO 1.8V



Bootstrap




```
Button Not-pressd:
1, PLL Config    B[2:0] = 0b011     : Ref Colck -> 25MHz
2, Primarry Boot B[9:3] = 0b1001001 : eMMC Boot
3, Backup Boot   B[13:10] = 0b1011  : UART Boot

Button Pressd:
1, PLL Config    B[2:0] = 0b011     : Ref Colck -> 25MHz
2, Primarry Boot B[9:3] = 0b1001000 : SDCard FS Boot
3, Backup Boot   B[13:10] = 0b0001  : USB DFU Boot
```

Main

seeed studio	https://www.seeedstudio.com	
	Title: BeaglePlay	
Size: A3	Document Number: 014_SoC GPIO 1.8V & Bootstrap	Rev: v1.0
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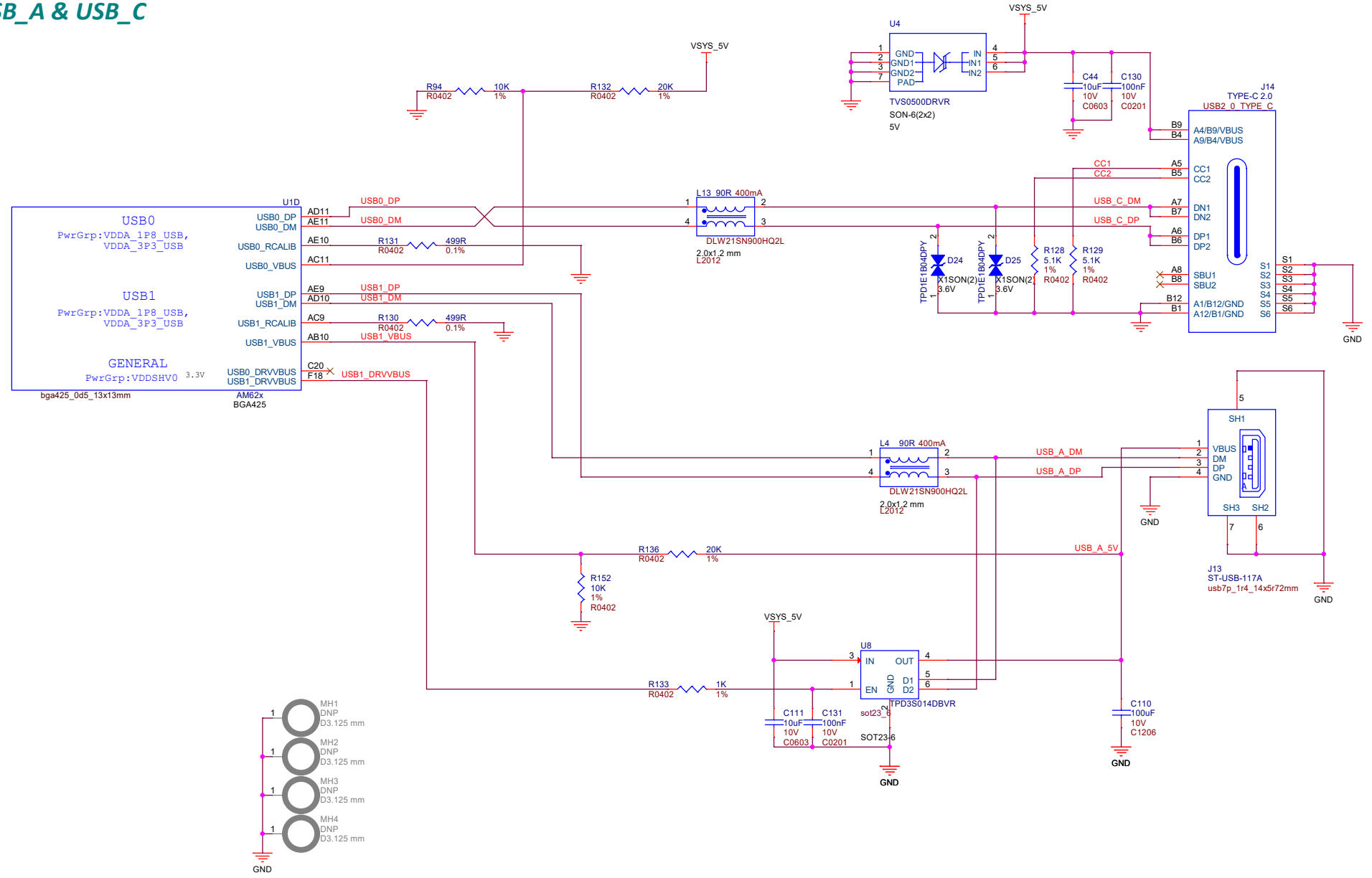
USB_A & USB_C



Main

seeed studio	https://www.seeedstudio.com	
	Title: BeaglePlay	
Size: A3	Document Number: 015_SoC USB & USB_A & USB_C	Rev: v1.0
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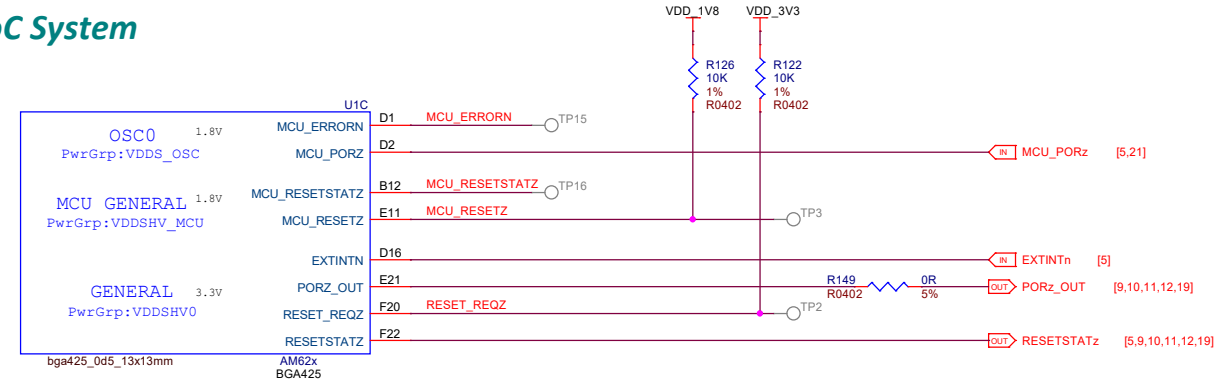
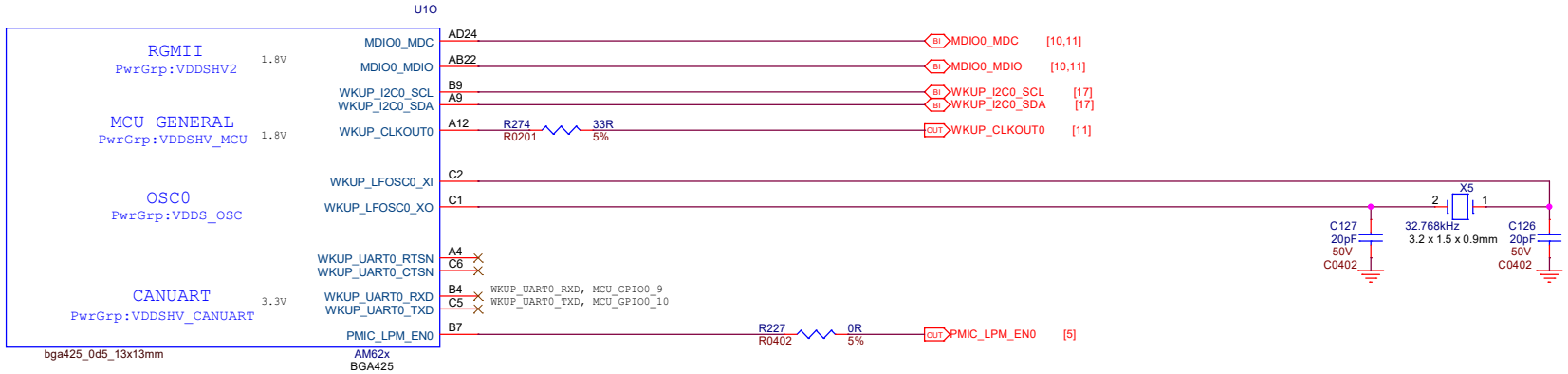
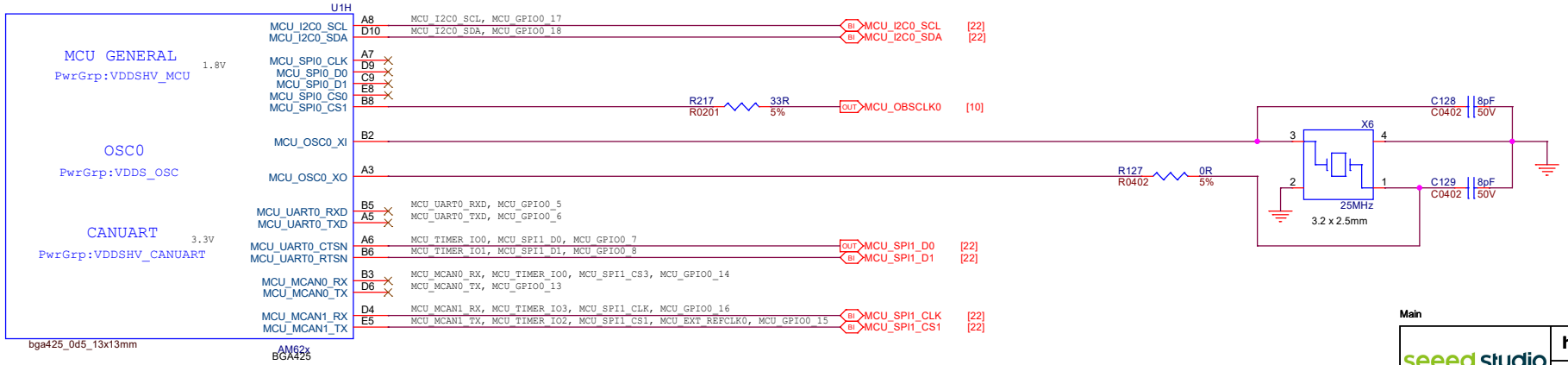
SoC System



WKUP Domain



MCU Domain



Main

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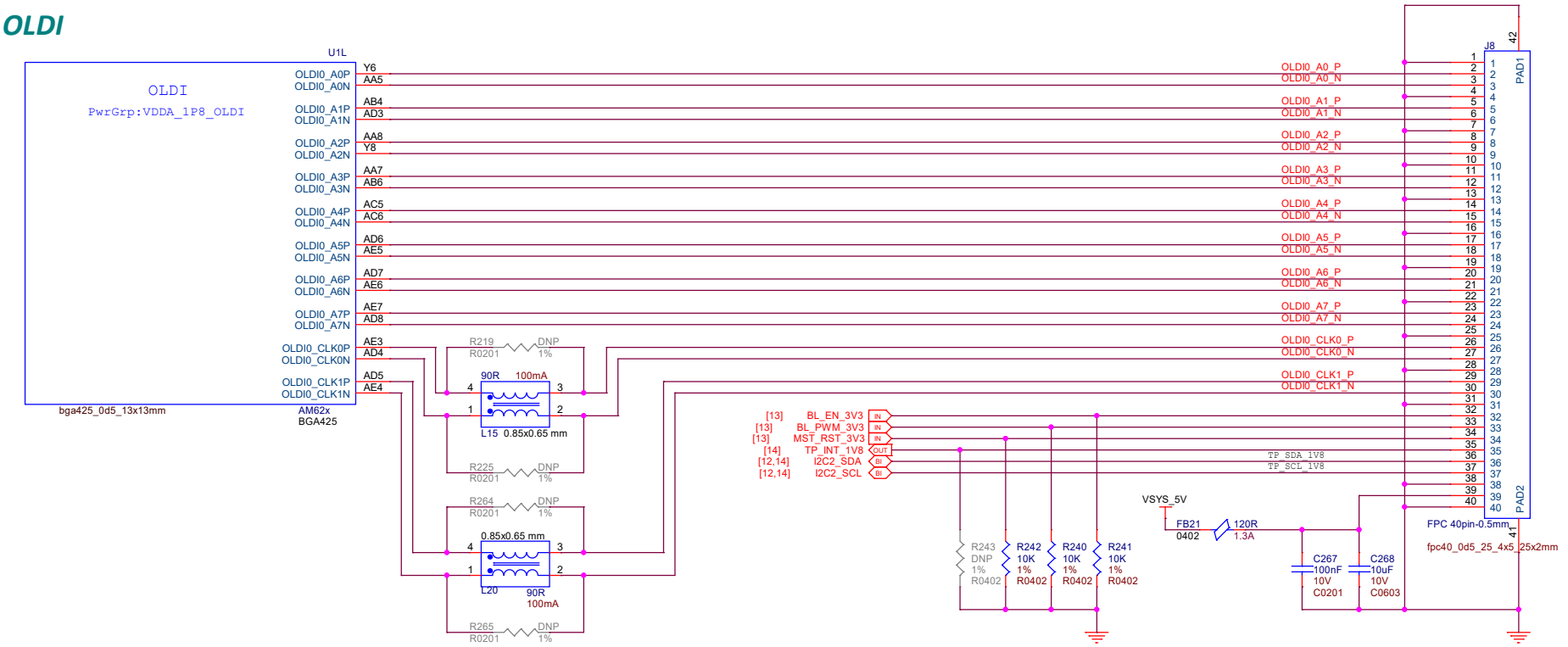
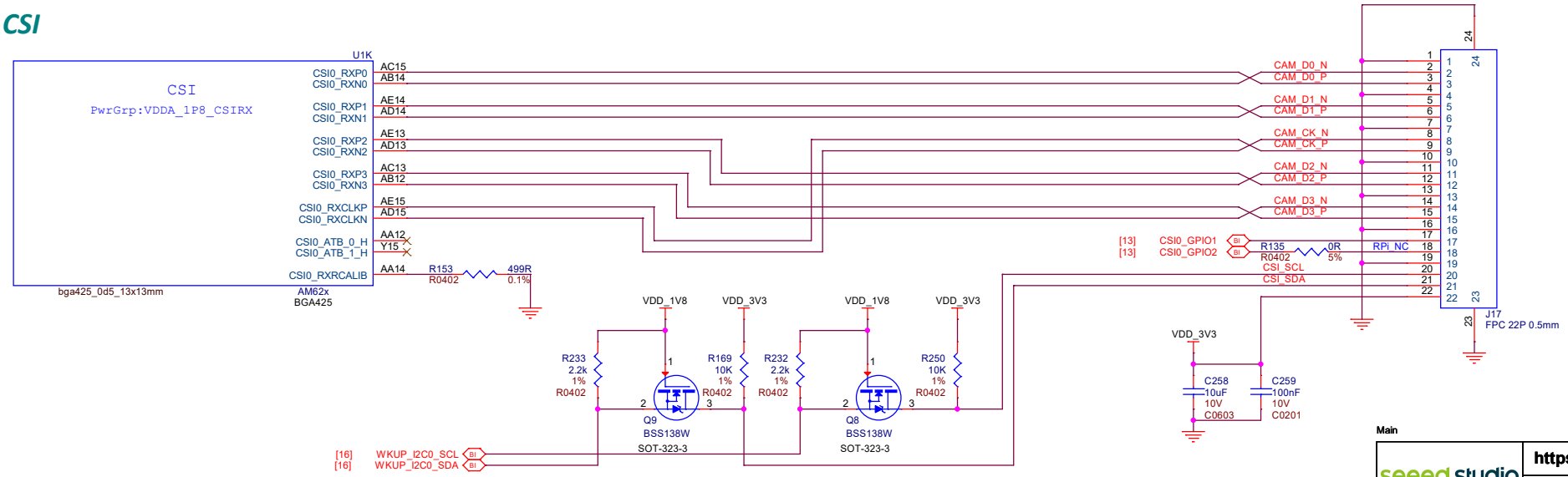
OLDI



CSI



Main

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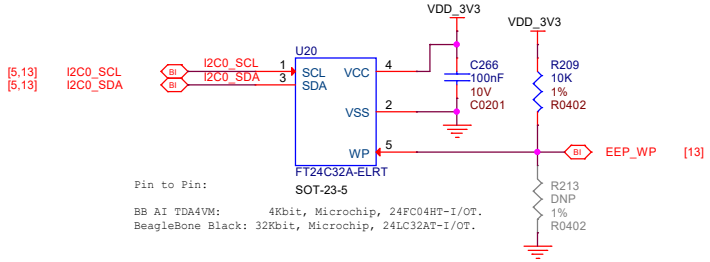
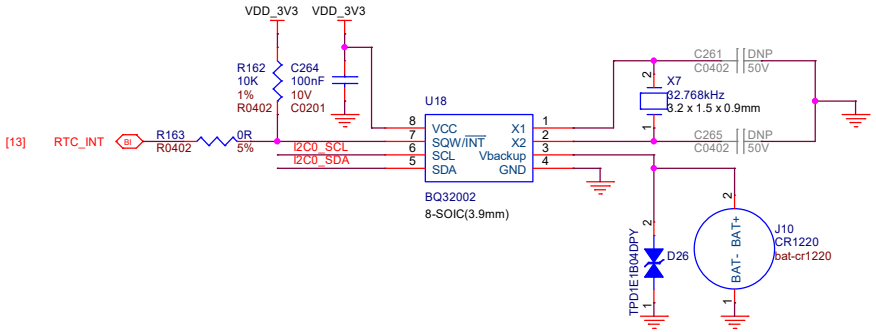
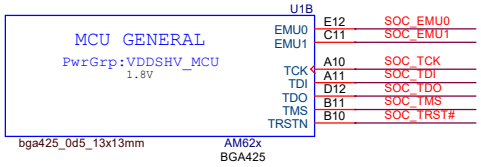
BOARD ID EEPROM 4Kbit



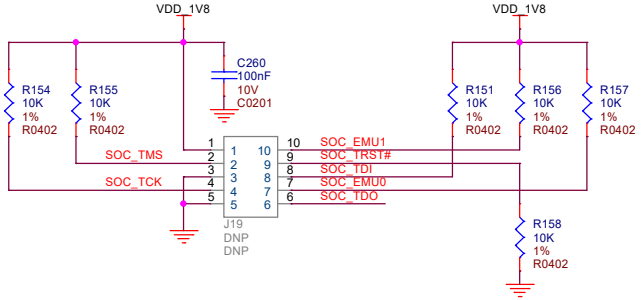
RTC



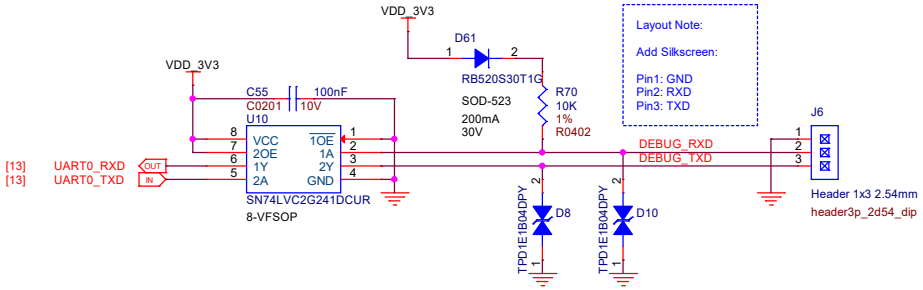
JTAG



Tag-Connect



Debug



Main

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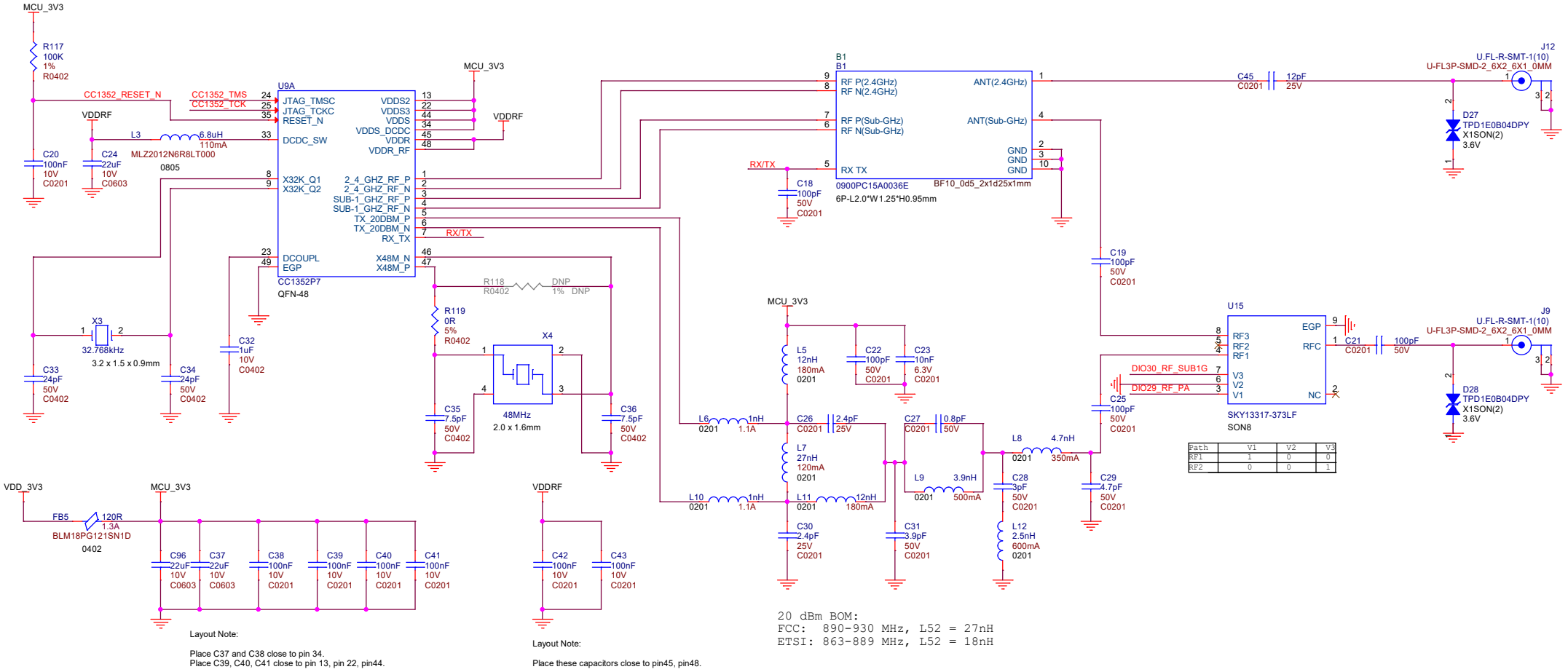
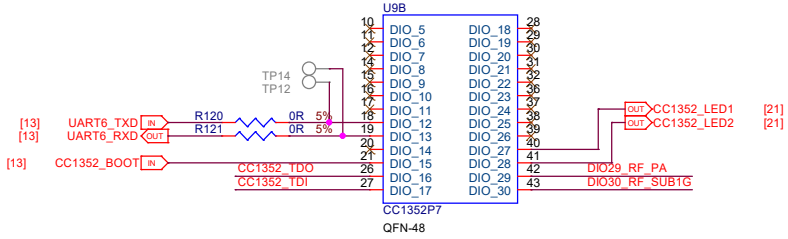
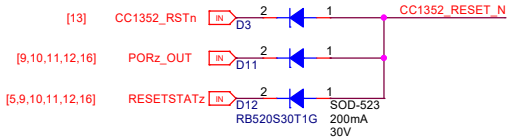
CC1352P RF



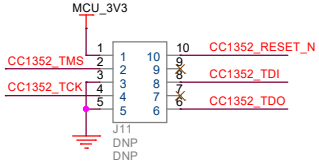
CC1352P GPIO



RESET



CC1352P JTAG Tag-Connect



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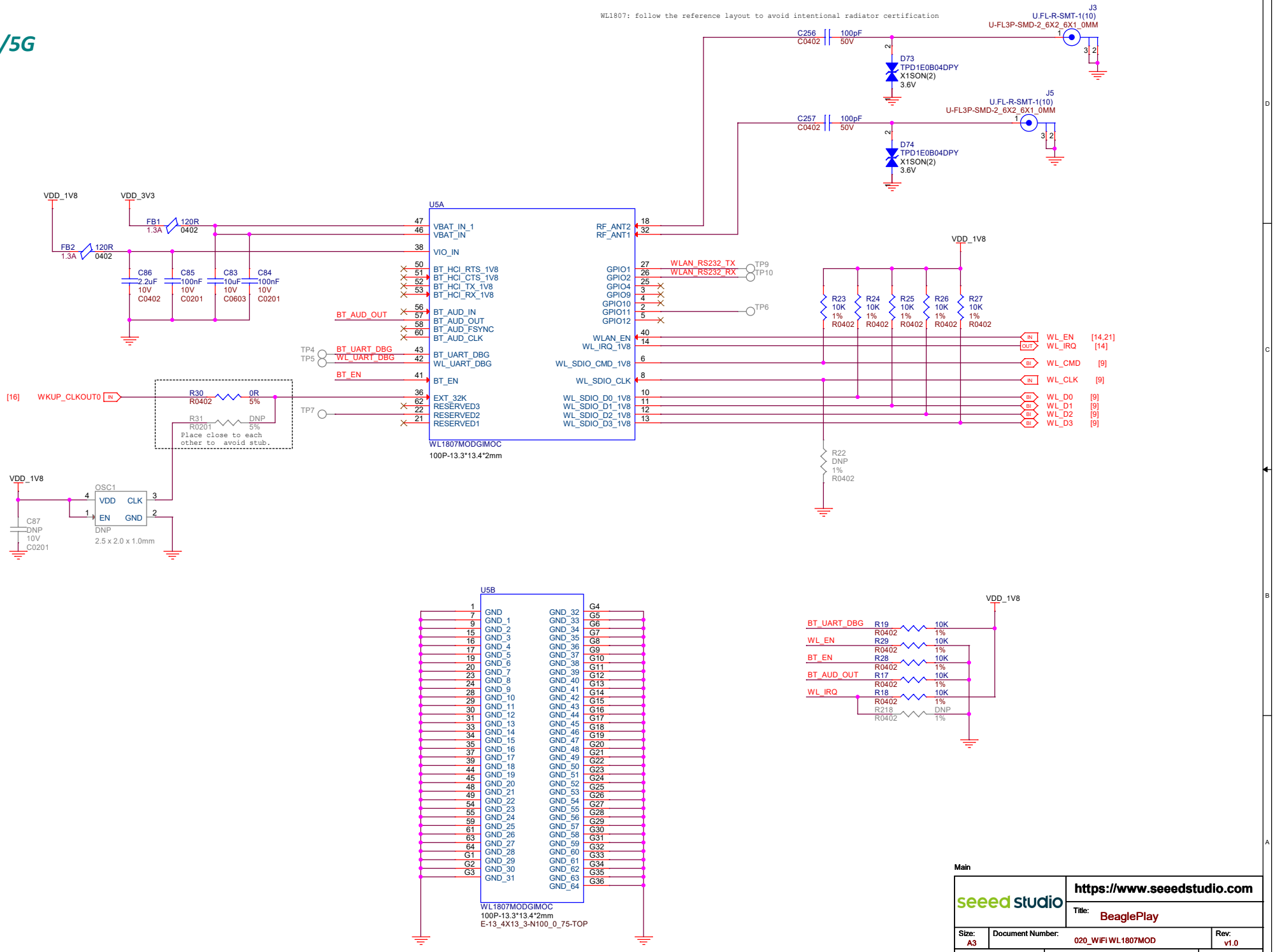
WiFi 2.4G/5G



Main

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Size: A3	Document Number: 020_WiFi WL1807MOD	Rev: v1.0
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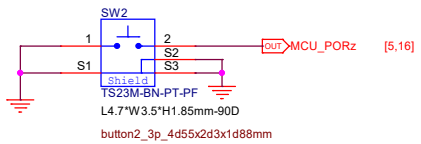
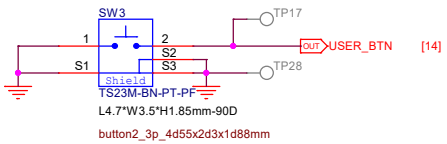
Reset Button

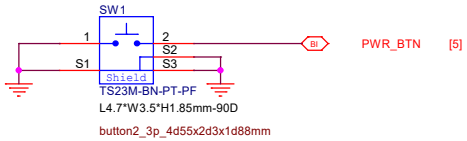


User Button

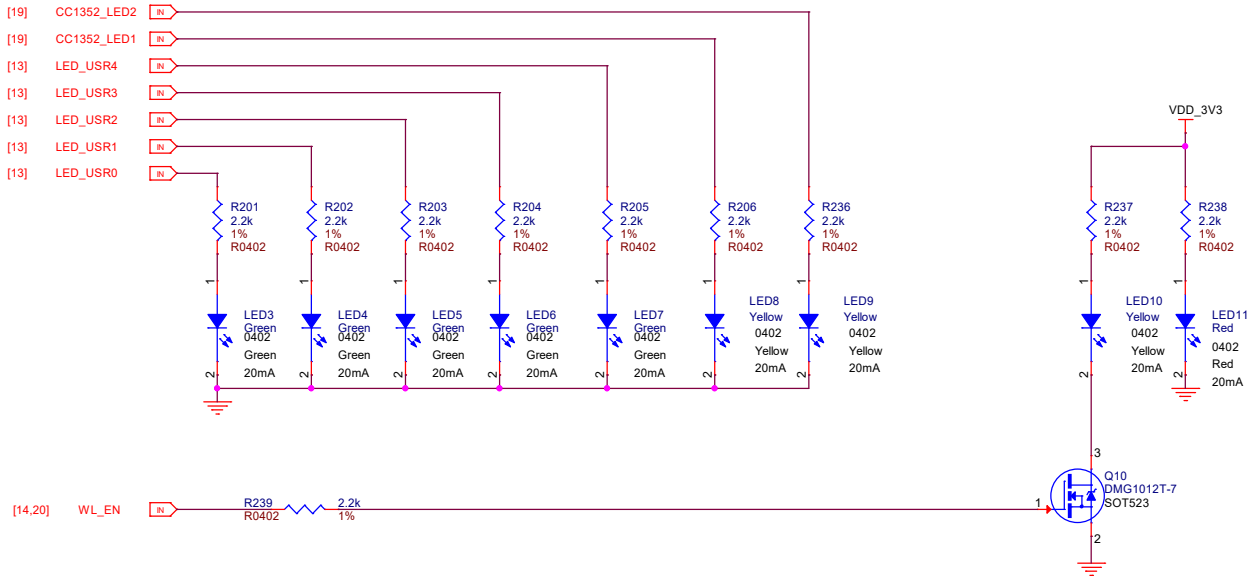
Layout Noete:
Place TP17 and TP28 close to each othter, keep 2.54mm spacing.



Power Button



LEDs



Main

seeed studio	https://www.seeedstudio.com	
	Title: BeaglePlay	
Size: A3	Document Number: 021_BUTTONs & LEDs	Rev: v1.0
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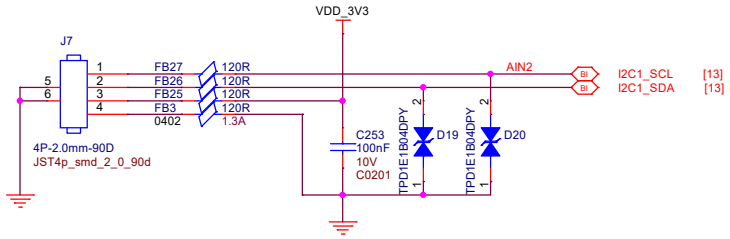
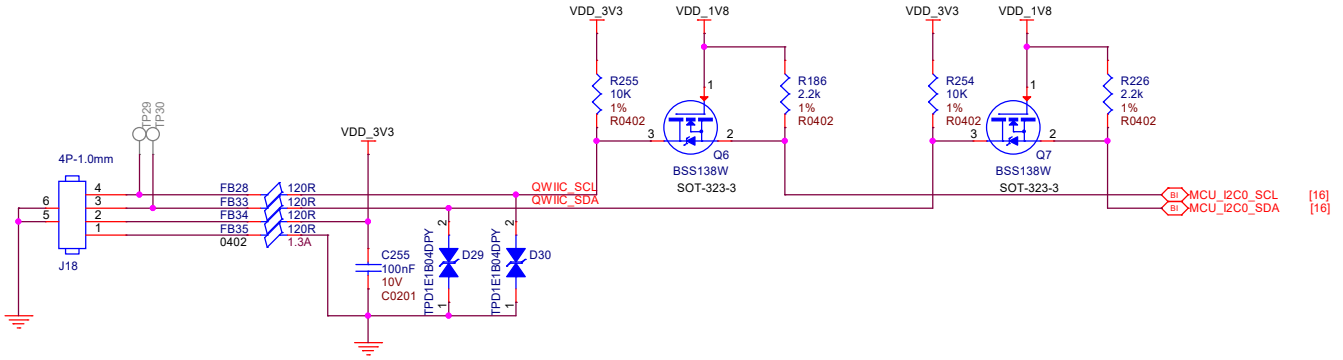
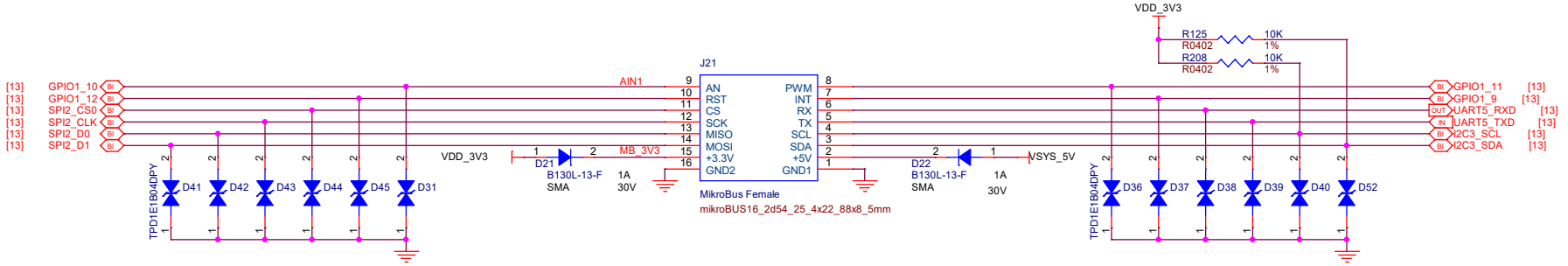
Grove Connector



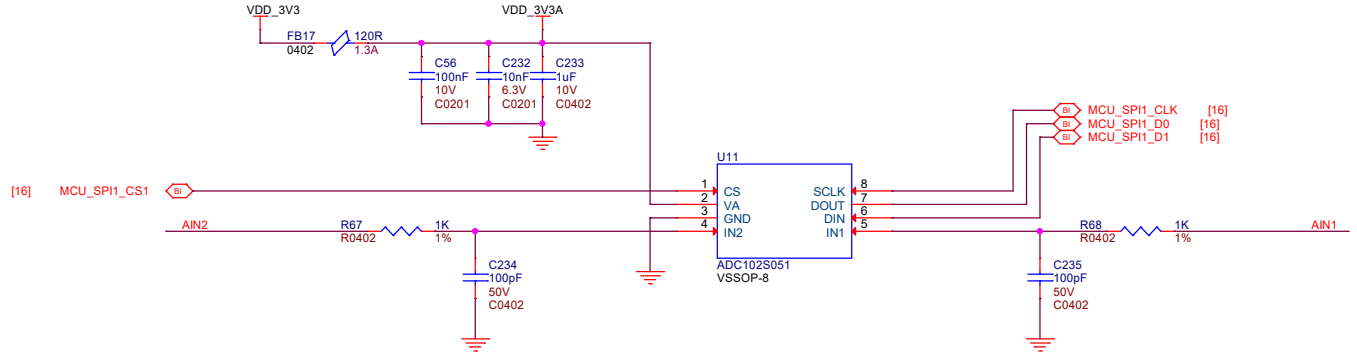
QWIIC Connector



MikroBus



ADC



Main

seeed studio

https://www.seeedstudio.com

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Size: A3	Document Number: 022_GROVE &QWIIC &MikroBus &ADC	Rev: v1.0
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