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019	019_CC1352P
020	020_WiFi WL1807MOD
021	021_BUTTONs & LEDs
022	022_GROVE &QWIIC &MikroBus &ADC

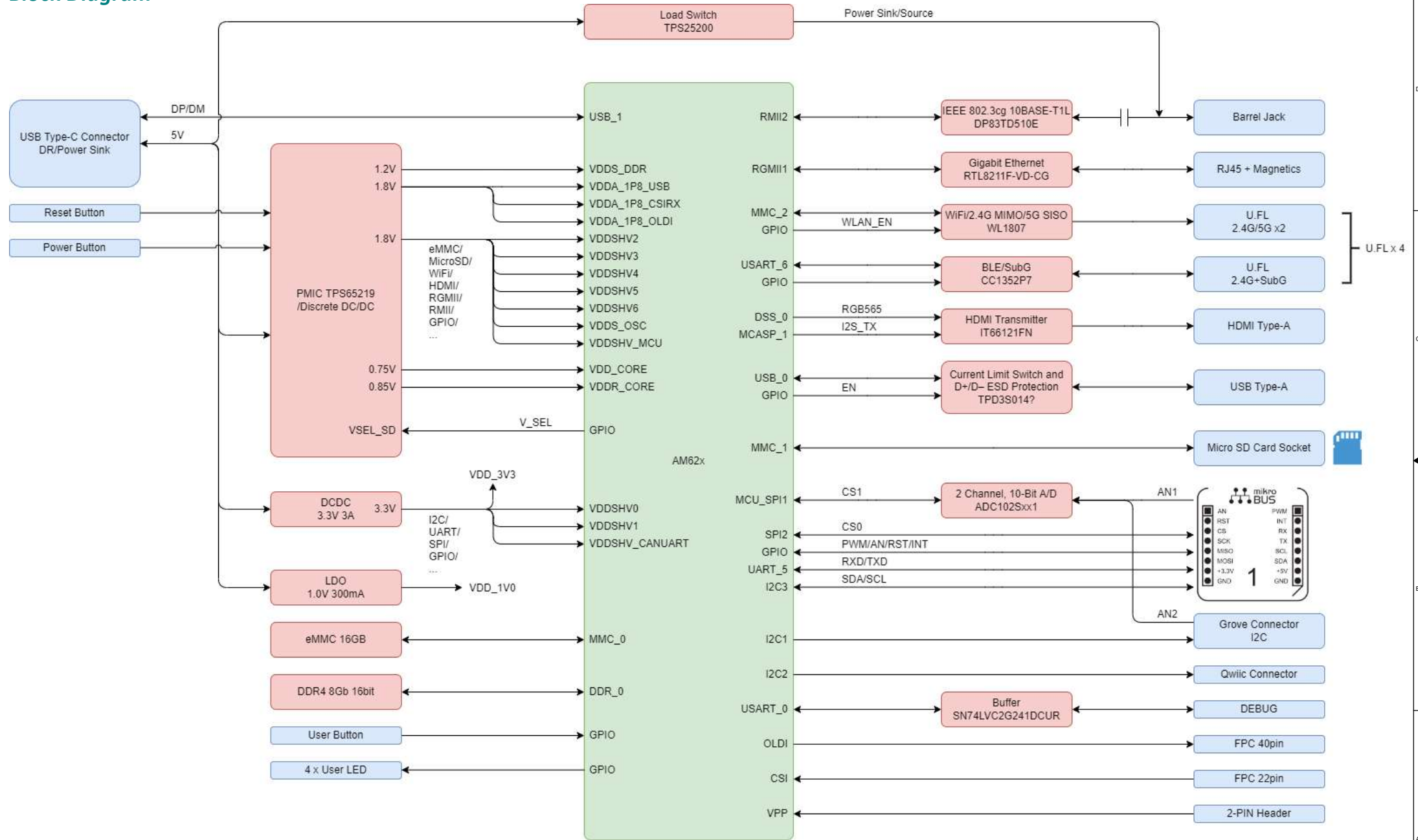
REVISION HISTORY			
VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR
0.20	15 Sep. 2022	DVT1 Board release	qxn
0.21	Nov. 10, 2022	<ol style="list-style-type: none"> <li>1. Modify all crystal CL value to match frequency</li> <li>2. Add serial termination resistors for RGB data lane</li> <li>3. Add CMC on HDMI output</li> <li>4. Use WKUP_CLKOUT0 for WiFi</li> <li>5. Use MCU_OBSCLK0 for GBE</li> <li>6. Increase resistance on all board LEDs</li> <li>7. Remove R243 TP_INT Pulldown</li> <li>8. Add ferrite bead on Grove and QWIIC</li> <li>9. Add feed forward capacitor on TLV62595</li> <li>10. Remove ESDs on HDMI TMDS signals</li> </ol>	qxn
0.22	Dc. 12, 2022	<ol style="list-style-type: none"> <li>1. Add feed forward capacitor on TLV62595</li> <li>2. Remove ESDs on HDMI TMDS signals</li> <li>3. Add ferrite bead on HDMI shield</li> <li>4. Change R16 and R80 to 0R</li> <li>5. Change pullup resistors to 2.2k on I2C0-I2C3</li> <li>6. Change FB30 and FB31 to 0R</li> </ol>	qxn
1.0	Dc. 27, 2022	<ol style="list-style-type: none"> <li>1. Add testpoint to QWIIC</li> <li>2. Add serial resistors on I2C0 - I2C3 SCL</li> <li>3. Add more capacitors on VDD_1V2</li> <li>4. Add 0R on HDMI shield</li> <li>5. Add series resistor on SPE LED control</li> </ol>	qxn

Main

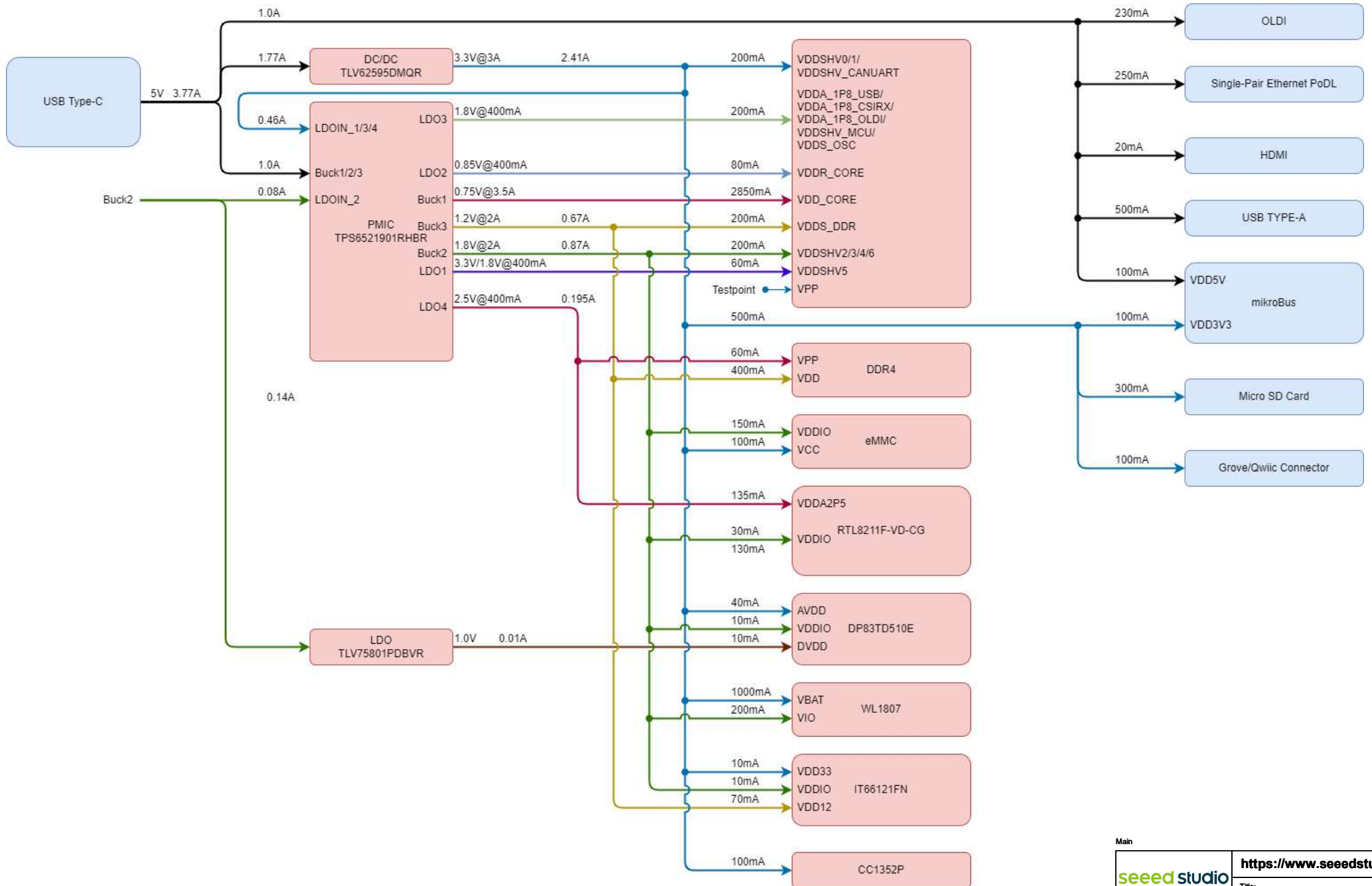
		<a href="https://www.seeedstudio.com">https://www.seeedstudio.com</a>	
		Title: <b>BeaglePlay</b>	
Size: A3	Document Number: 001_Revision History	Rev: v1.0	
Draw By: qxn	Date: Monday, March 06, 2023	Sheet: 1 of 22	



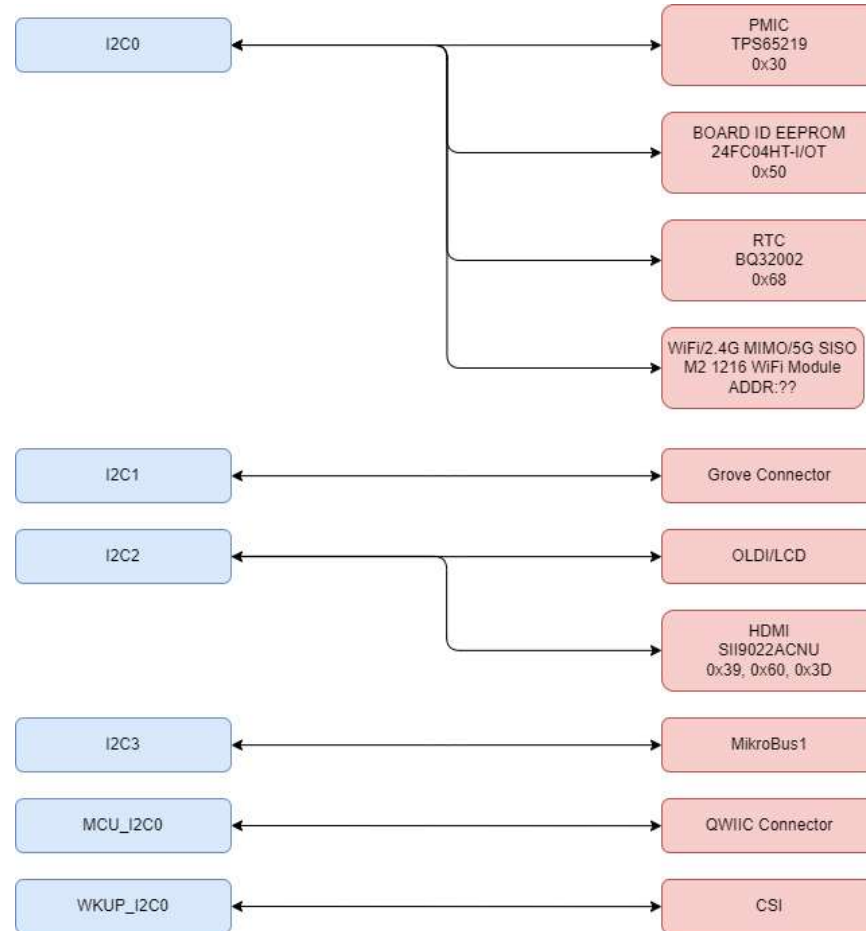
# Block Diagram



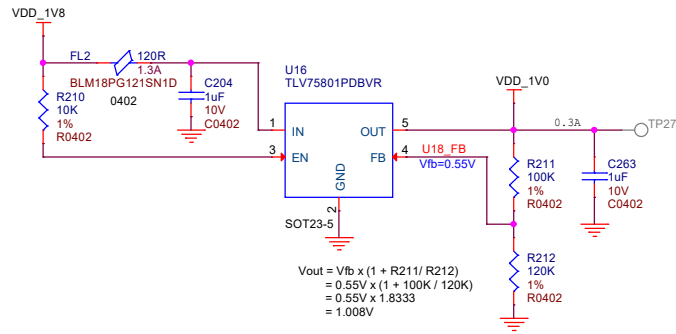
# Power tree



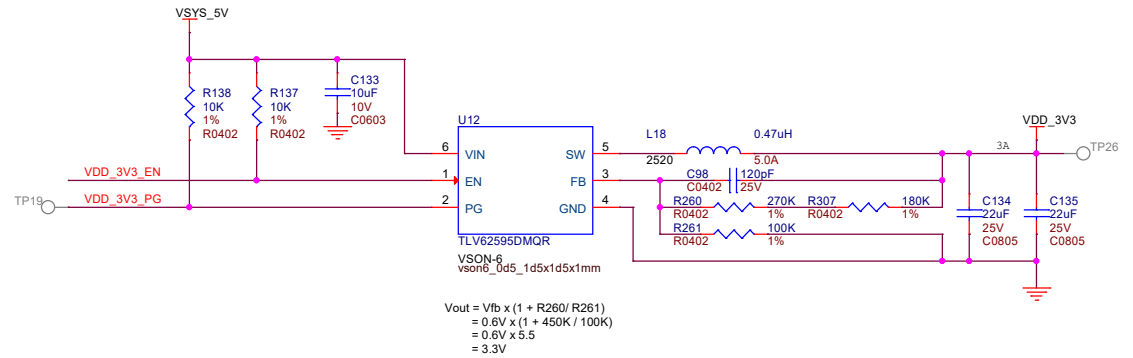
# I2C Usage Diagram



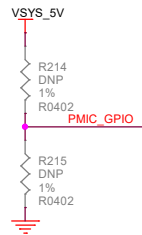
## LDO 1V0



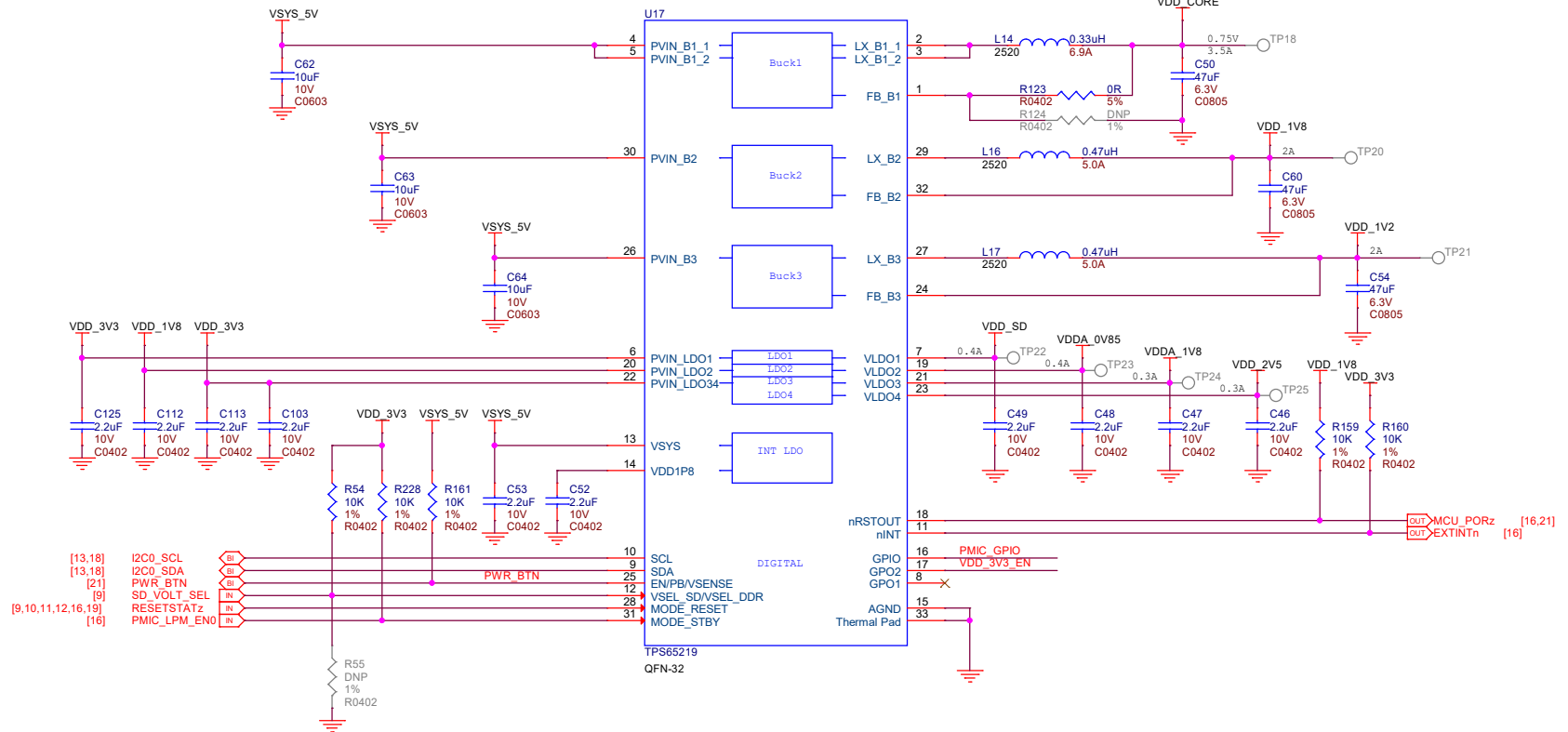
## DCDC 3V3



## PMIC\_Strap option

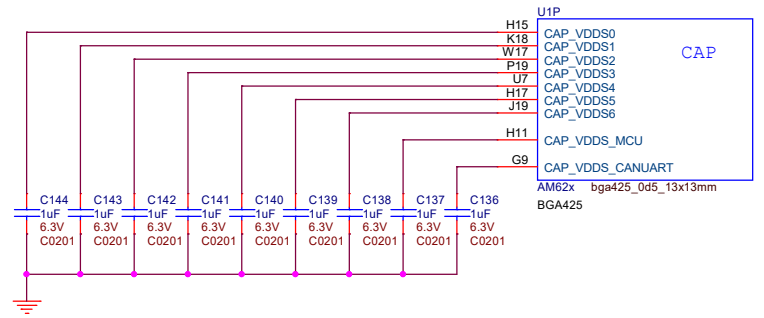
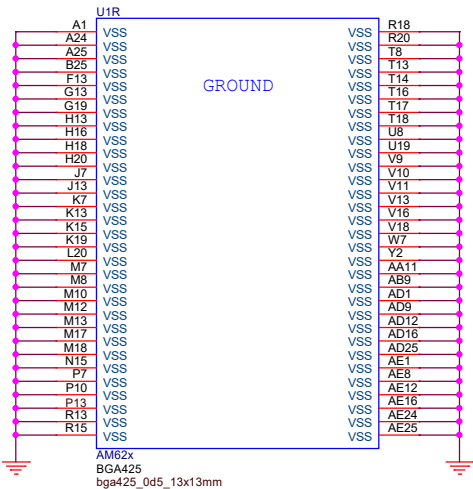
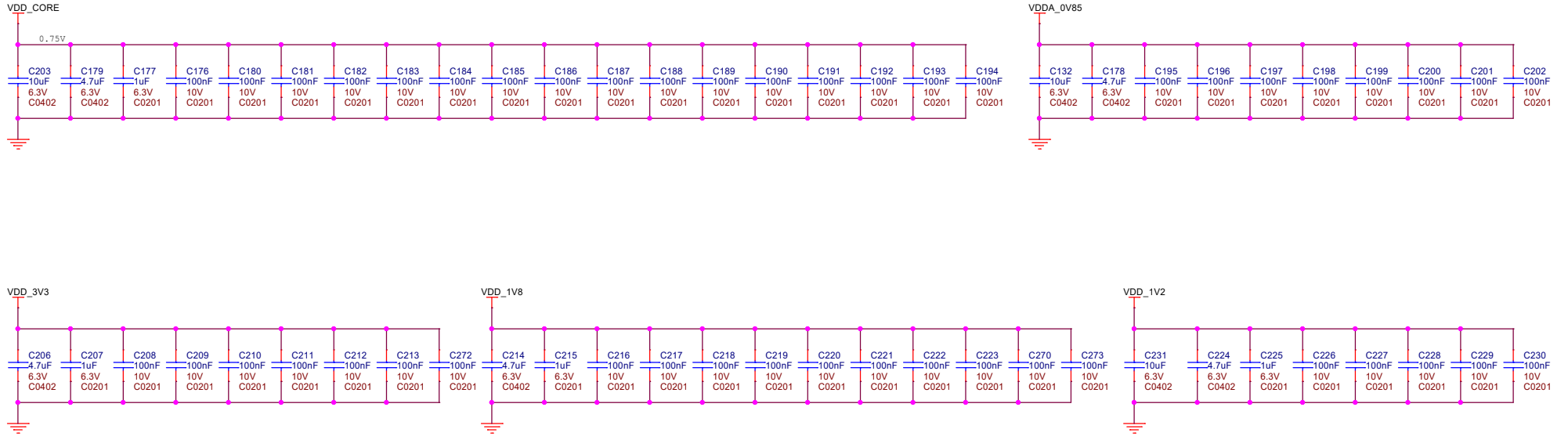


## PMIC





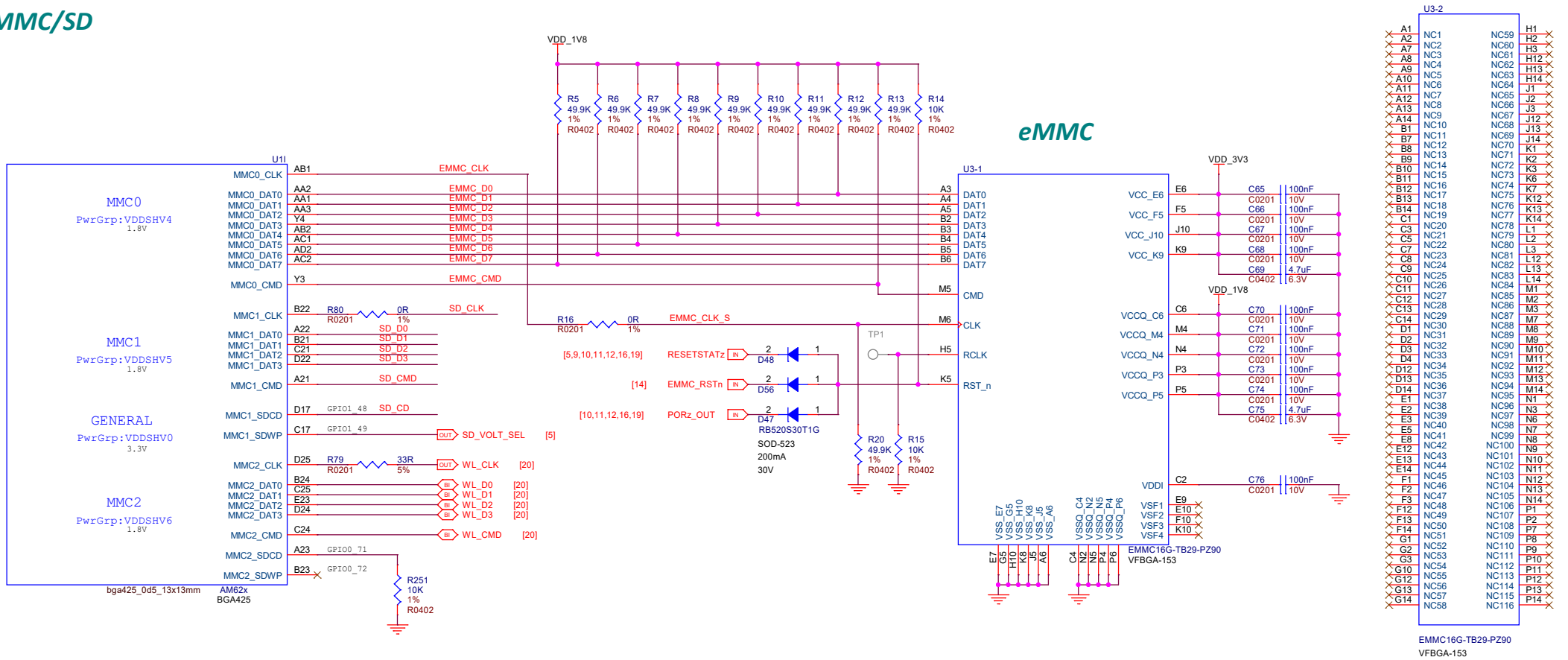
# SoC DCAPs



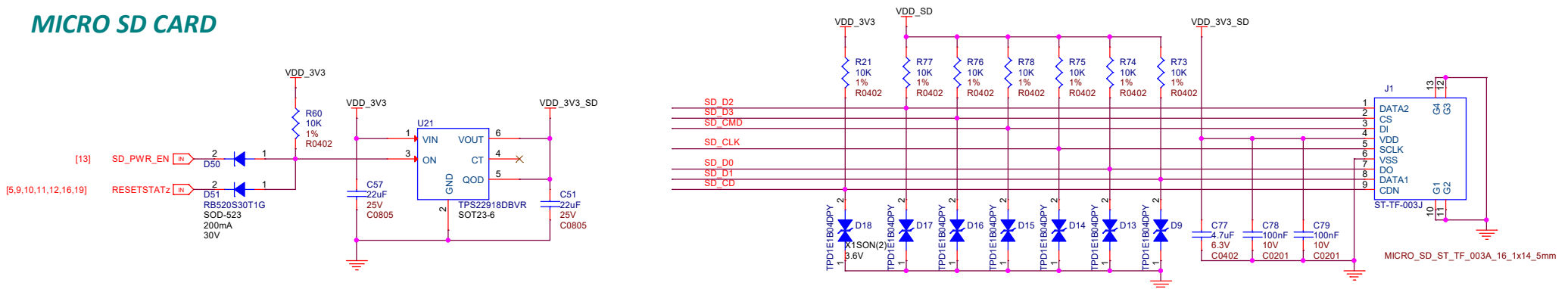




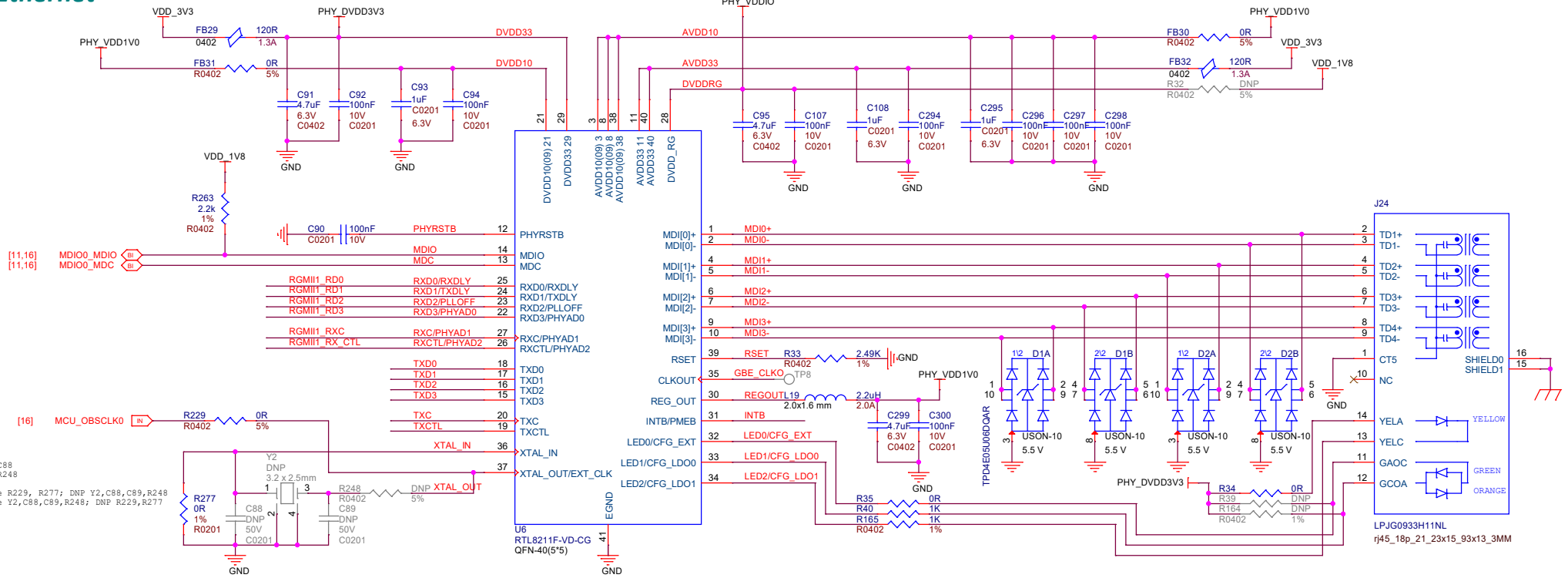
# eMMC/SD



# MICRO SD CARD



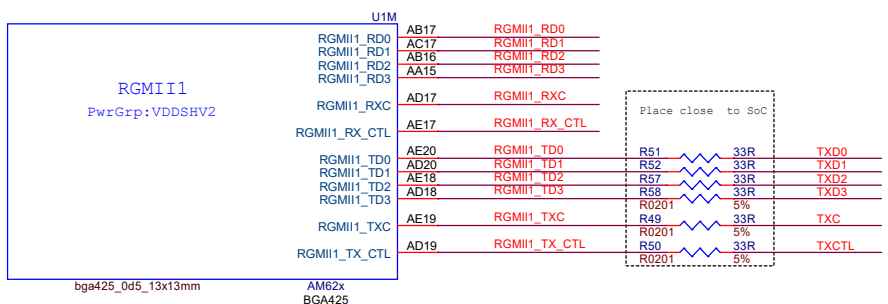
# Gigabit Ethernet



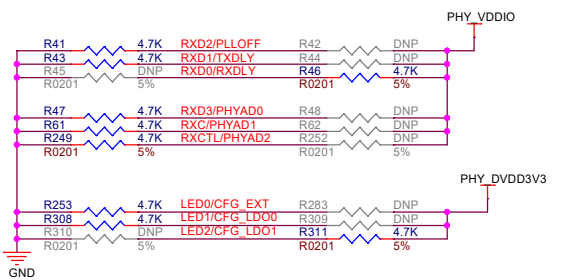
Layout Note:  
Co-lay R277 and C88  
Co-lay R229 and R248

EXT CLK: populate R229, R277; DNP Y2, C88, C99, R248  
Crystal: populate Y2, C88, C89, R248; DNP R229, R277

# SoC MAC 1.8V



# Strap options



CFG\_EXT = 0, CFG\_LDO[1:0] = 10 : Internal 1.8V  
PHY Ad[2:0] = 000 : PHY Addr 000  
PHY PLLOFF = 0 : Enable PLL  
PHY TXDLY = 0 : TX delay: 0ns  
PHY RXDLY = 1 : RX delay: 2ns

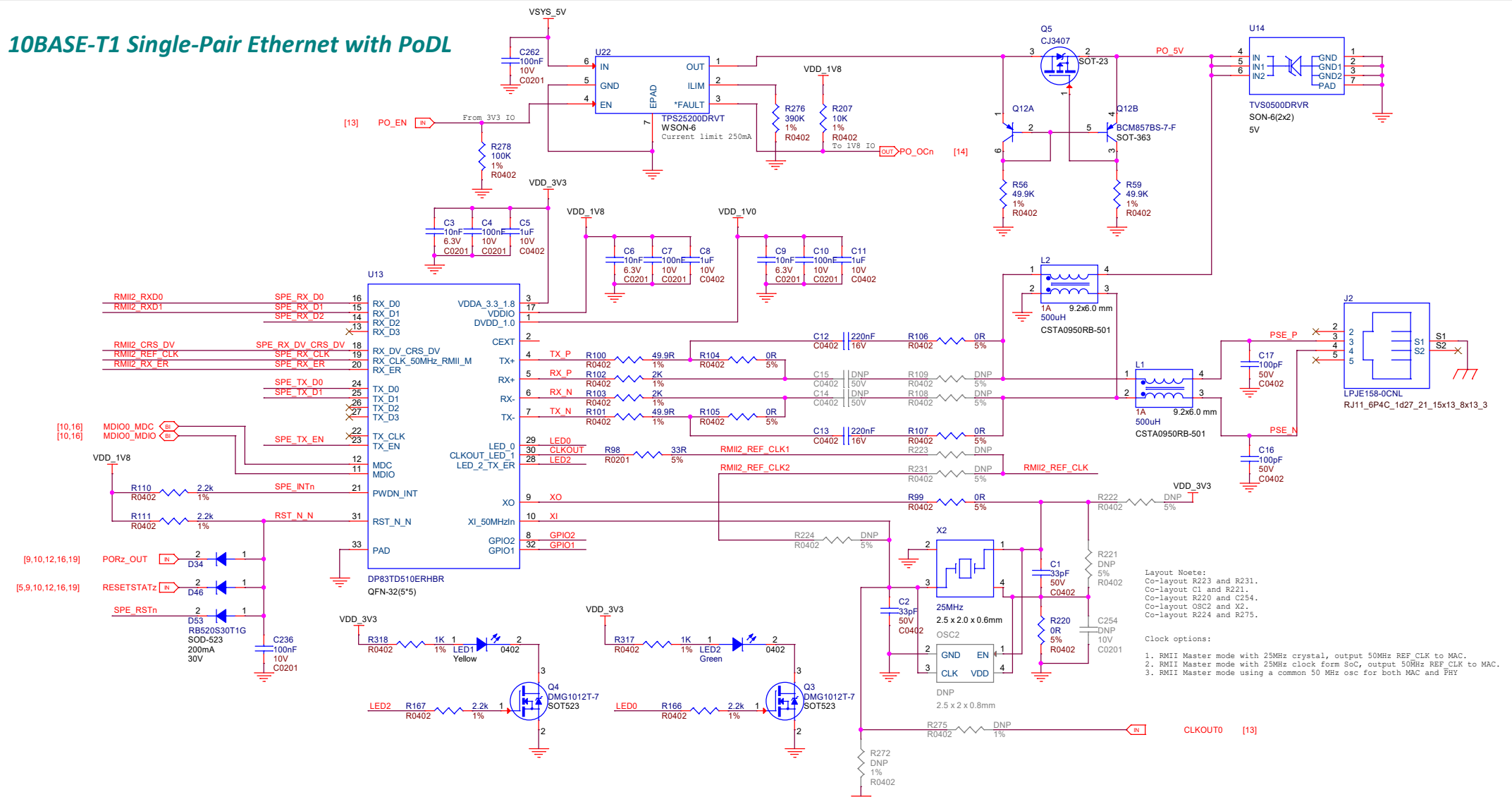
Main

**seed studio** <https://www.seeedstudio.com>

Title: **BeaglePlay**

Size: A3	Document Number: 010_SoC RGMII & GBE PHY	Rev: v1.0
Draw By: qxn	Date: Tuesday, December 27, 2022	Sheet: 10 of 22

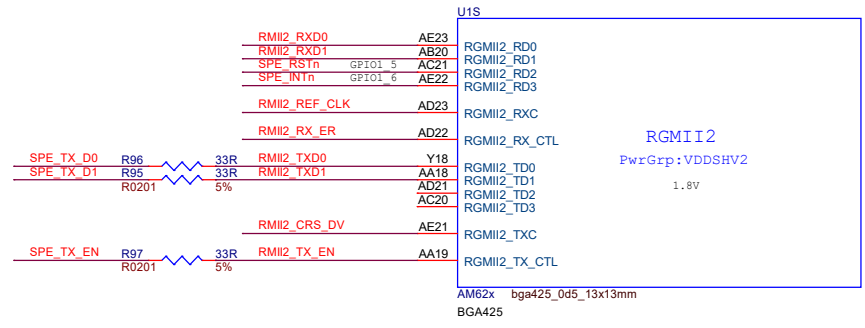
# 10BASE-T1 Single-Pair Ethernet with PoDL



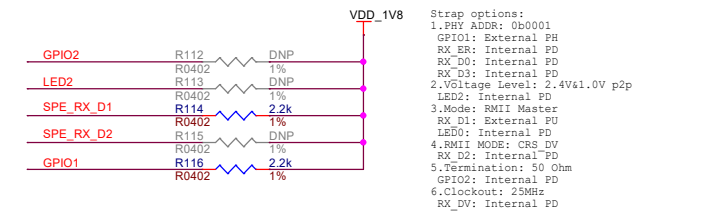
Layout Note:  
 Co-layout R223 and R231.  
 Co-layout C1 and R221.  
 Co-layout R220 and C254.  
 Co-layout OSC2 and X2.  
 Co-layout R224 and R275.

Clock options:  
 1. RMI2 Master mode with 25MHz crystal, output 50MHz REF\_CLK to MAC.  
 2. RMI2 Master mode with 25MHz clock form SoC, output 50MHz REF\_CLK to MAC.  
 3. RMI2 Master mode using a common 50 MHz osc for both MAC and PHY

## SoC MAC 1.8V



## Strap options



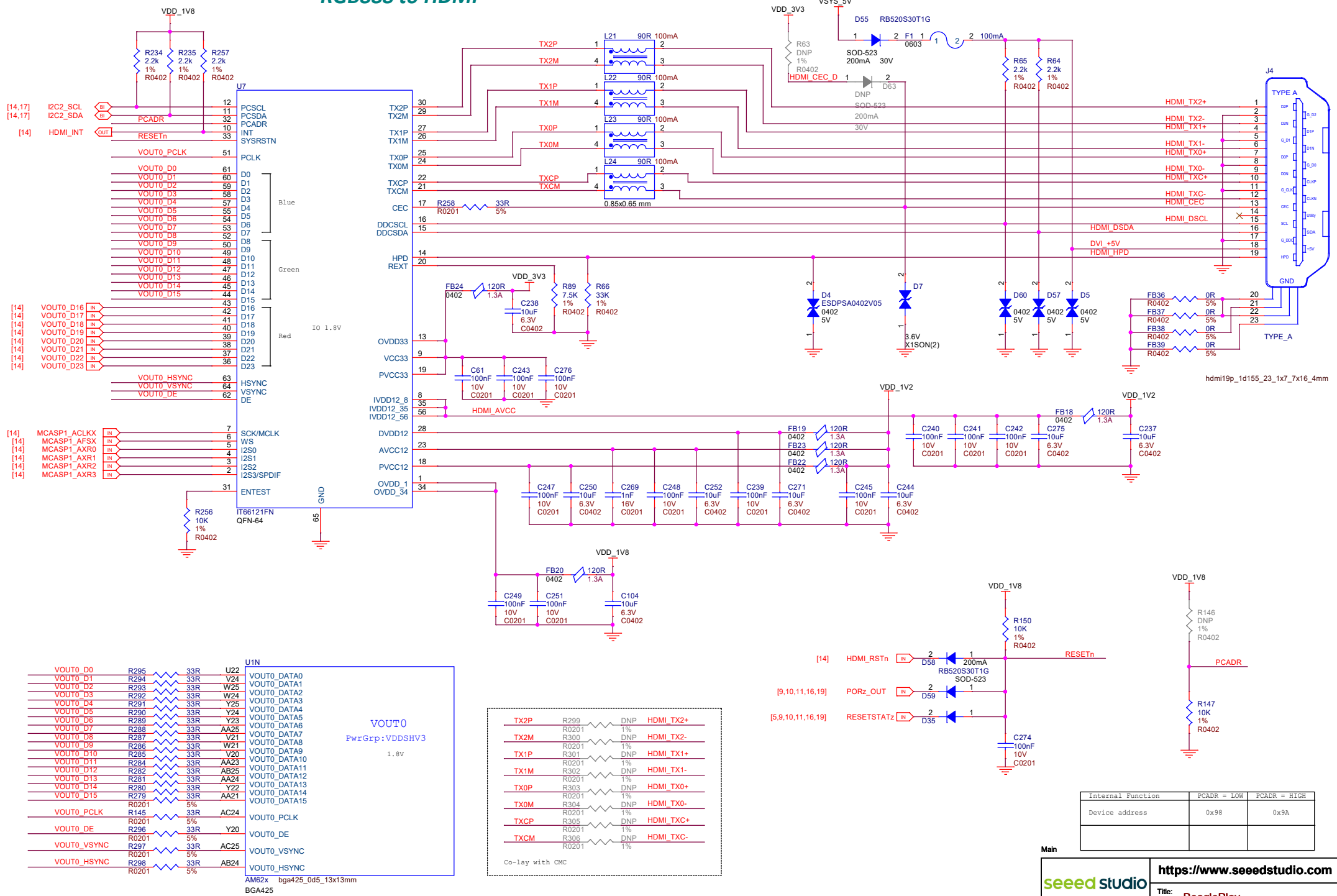
Main

seed studio <https://www.seeedstudio.com>

Title: **BeaglePlay**

Size: A3	Document Number: 011_SoC_RMI2 & SPE_PHY	Rev: v1.0
Draw By: qm	Date: Thursday, December 29, 2022	Sheet: 11 of 22

# RGB888 to HDMI



Pin	Label	Value	Component	Pin	Label	Value	Component
7	MCASP1_ACLKX	IN		7	SCK/MCLK		
6	MCASP1_AFSX	IN		5	WS		
4	MCASP1_AXR0	IN		4	I2S0		
3	MCASP1_AXR1	IN		3	I2S1		
2	MCASP1_AXR2	IN		2	I2S2		
2	MCASP1_AXR3	IN		2	I2S3/SPDIF		
31	ENTST			34	OVDD_34		
12	PCSCS			30	TX2P		
11	PCSDA			29	TX2M		
32	PCADR			1	TX1P		
10	PCADR			4	TX1M		
33	RESETn			1	TX0P		
51	PCLK			4	TX0M		
61	VOUT0_D0			2	TXCP		
60	VOUT0_D1			3	TXCM		
59	VOUT0_D2			17	CEC		
58	VOUT0_D3			16	DDCSCL		
57	VOUT0_D4			15	DDCSDA		
55	VOUT0_D5			14	HPD		
54	VOUT0_D6			20	REXT		
53	VOUT0_D7			13	OVDD33		
52	VOUT0_D8			9	VCC33		
50	VOUT0_D9			19	PVCC33		
49	VOUT0_D10			8	IVDD12_8		
48	VOUT0_D11			35	IVDD12_35		
47	VOUT0_D12			56	IVDD12_56		
46	VOUT0_D13			28	DVDD12		
45	VOUT0_D14			23	AVCC12		
44	VOUT0_D15			18	PVCC12		
43	VOUT0_D16			1	OVDD_1		
42	VOUT0_D17			34	OVDD_34		
41	VOUT0_D18						
40	VOUT0_D19						
39	VOUT0_D20						
38	VOUT0_D21						
37	VOUT0_D22						
36	VOUT0_D23						
63	VOUT0_HS						
64	VOUT0_VS						
62	VOUT0_DE						
5	VOUT0_PCLK						
6	VOUT0_D0						
7	VOUT0_D1						
8	VOUT0_D2						
9	VOUT0_D3						
10	VOUT0_D4						
11	VOUT0_D5						
12	VOUT0_D6						
13	VOUT0_D7						
14	VOUT0_D8						
15	VOUT0_D9						
16	VOUT0_D10						
17	VOUT0_D11						
18	VOUT0_D12						
19	VOUT0_D13						
20	VOUT0_D14						
21	VOUT0_D15						
22	VOUT0_HS						
23	VOUT0_VS						
24	VOUT0_DE						
25	VOUT0_PCLK						
26	VOUT0_D0						
27	VOUT0_D1						
28	VOUT0_D2						
29	VOUT0_D3						
30	VOUT0_D4						
31	VOUT0_D5						
32	VOUT0_D6						
33	VOUT0_D7						
34	VOUT0_D8						
35	VOUT0_D9						
36	VOUT0_D10						
37	VOUT0_D11						
38	VOUT0_D12						
39	VOUT0_D13						
40	VOUT0_D14						
41	VOUT0_D15						
42	VOUT0_HS						
43	VOUT0_VS						
44	VOUT0_DE						
45	VOUT0_PCLK						
46	VOUT0_D0						
47	VOUT0_D1						
48	VOUT0_D2						
49	VOUT0_D3						
50	VOUT0_D4						
51	VOUT0_D5						
52	VOUT0_D6						
53	VOUT0_D7						
54	VOUT0_D8						
55	VOUT0_D9						
56	VOUT0_D10						
57	VOUT0_D11						
58	VOUT0_D12						
59	VOUT0_D13						
60	VOUT0_D14						
61	VOUT0_D15						
62	VOUT0_HS						
63	VOUT0_VS						
64	VOUT0_DE						

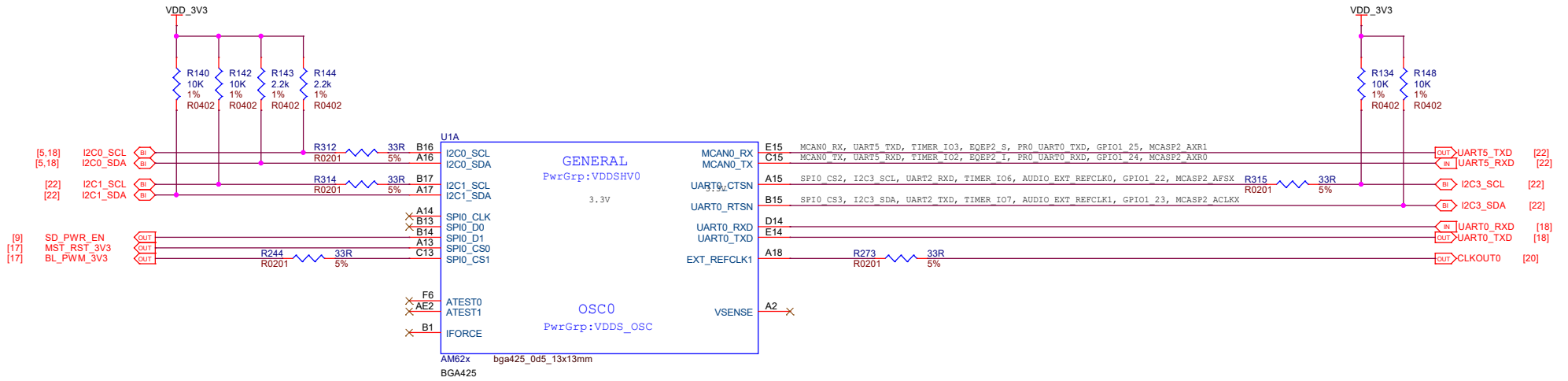
Label	Value	Component	Label	Value	Component
TX2P	R299	DNP	HDMI_TX2+		
TX2M	R0201	1%	HDMI_TX2-		
TX1P	R0201	1%	HDMI_TX1+		
TX1M	R301	DNP	HDMI_TX1-		
TX0P	R302	DNP	HDMI_TX0+		
TX0M	R0201	1%	HDMI_TX0-		
TXCP	R303	DNP	HDMI_TXC+		
TXCM	R0201	1%	HDMI_TXC-		

Co-layer with CMC

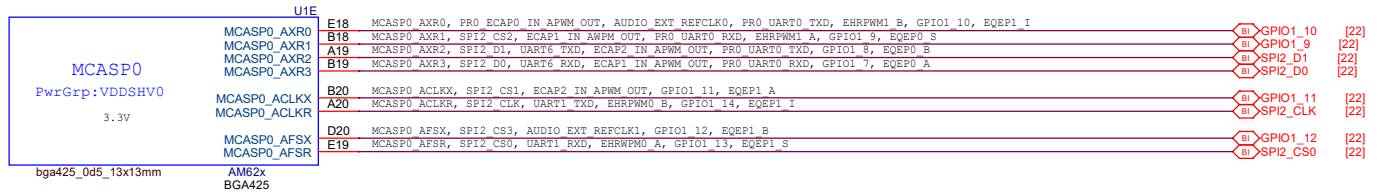
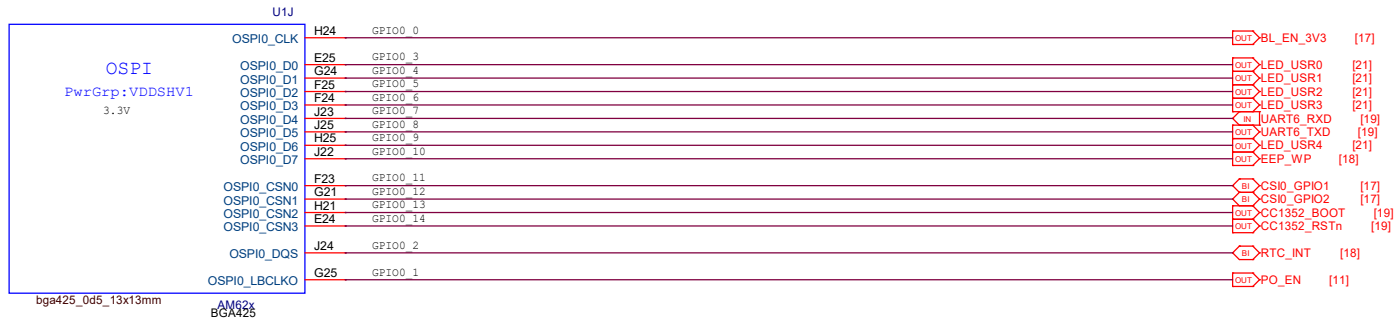
Internal Function	PCADR = LOW	PCADR = HIGH
Device address	0x98	0x9A

**seed studio** <https://www.seedstudio.com>  
**BeaglePlay**  
 Size: A3 | Document Number: 012\_SoC DDS & HDMI | Rev: v1.0  
 Draw By: qxn | Date: Tuesday, December 27, 2022 | Sheet: 12 of 22

# SoC GPIO 3.3V



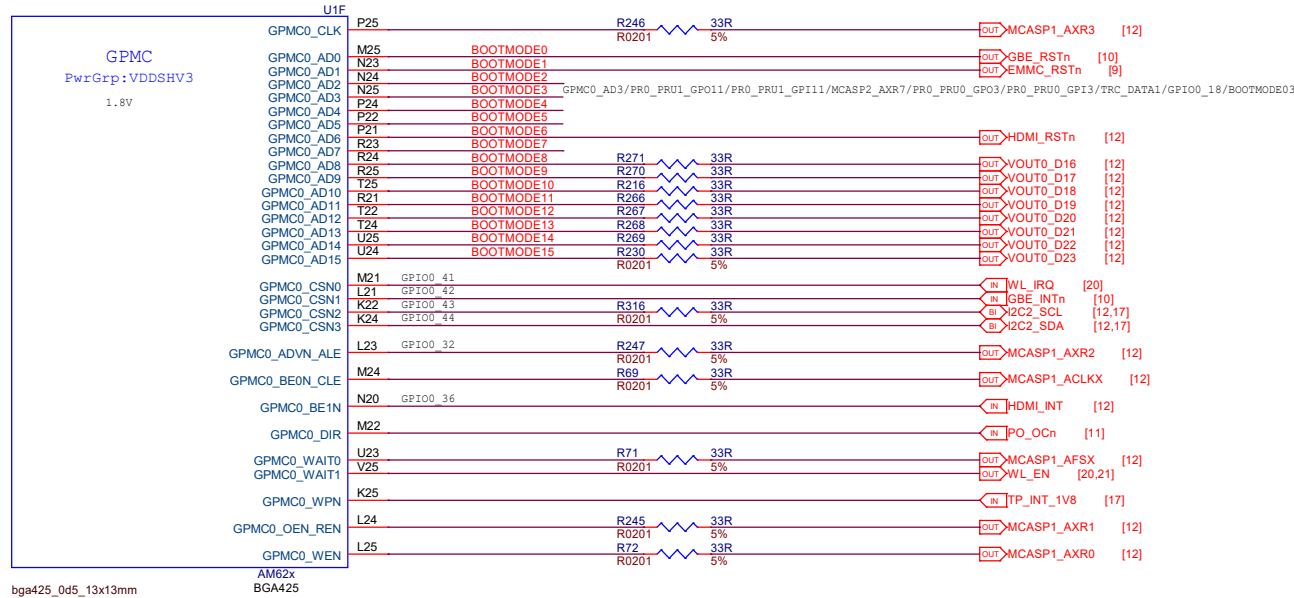
# SoC GPIO 3.3V



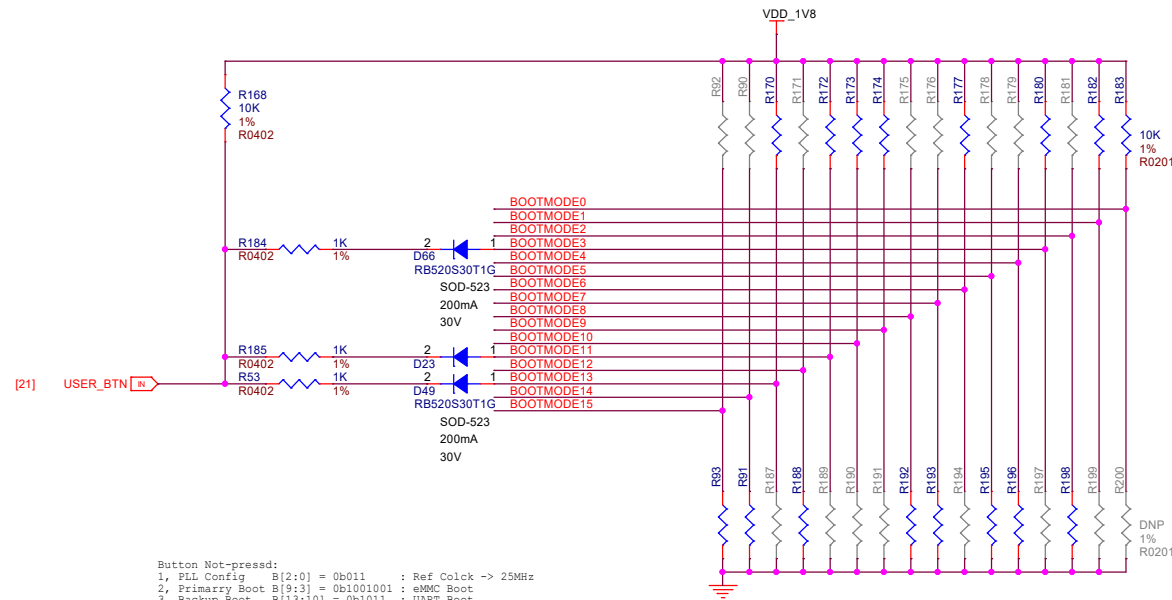
Main

<b>seeed studio</b>		<a href="https://www.seeedstudio.com">https://www.seeedstudio.com</a>	
		Title: <b>BeaglePlay</b>	
Size: <b>A3</b>	Document Number: <b>013_SoC GPIO 3.3V</b>	Rev: <b>v1.0</b>	
Draw By: <b>qxn</b>	Date: <b>Tuesday, December 27, 2022</b>	Sheet: <b>13 of 22</b>	

# SoC GPIO 1.8V



# Bootstrap



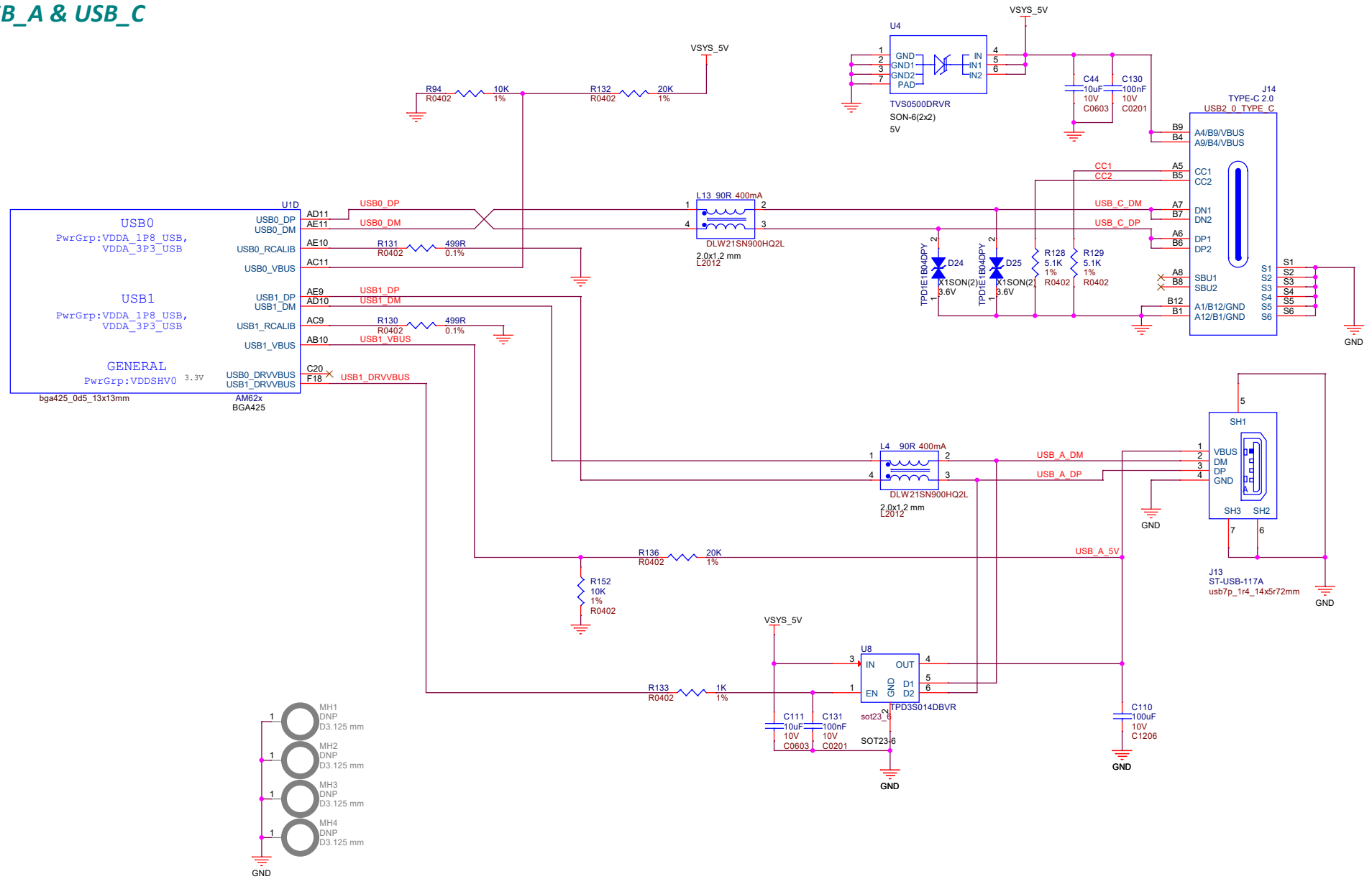
Button Not-pressed:  
 1, PLL Config B[2:0] = 0b011 : Ref Colck -> 25MHz  
 2, Primary Boot B[9:3] = 0b1001001 : eMMC Boot  
 3, Backup Boot B[13:10] = 0b1011 : UART Boot

Button Pressed:  
 1, PLL Config B[2:0] = 0b011 : Ref Colck -> 25MHz  
 2, Primary Boot B[9:3] = 0b1001000 : SDCard FS Boot  
 3, Backup Boot B[13:10] = 0b0001 : USB DFU Boot

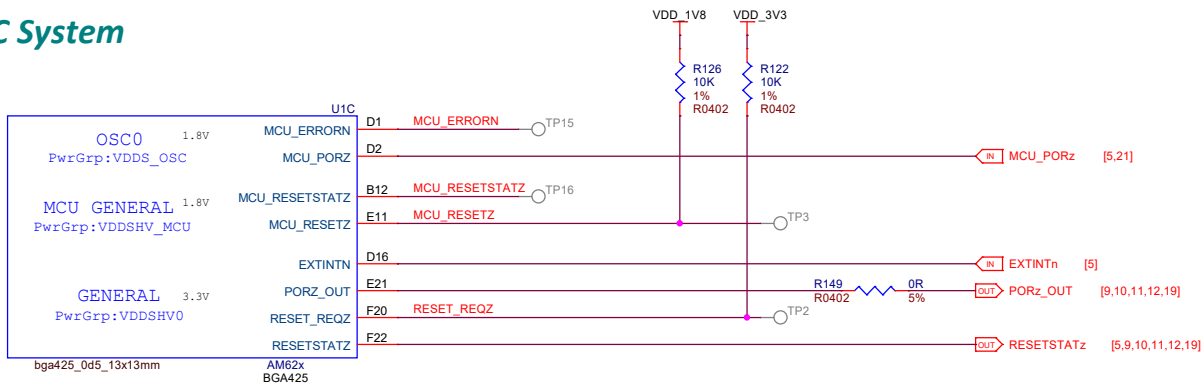
Main

		<a href="https://www.seeedstudio.com">https://www.seeedstudio.com</a>	
		Title: <b>BeaglePlay</b>	
Size: A3	Document Number: 014_SoC GPIO 1.8V & Bootstrap	Rev: v1.0	
Draw By: qxn	Date: Tuesday, December 27, 2022	Sheet: 14 of 22	

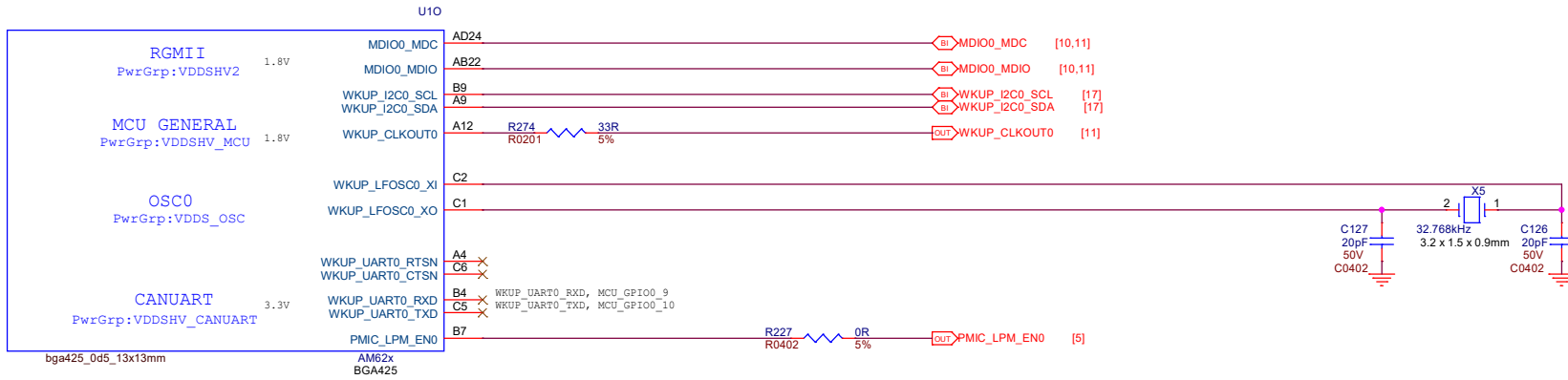
# USB\_A & USB\_C



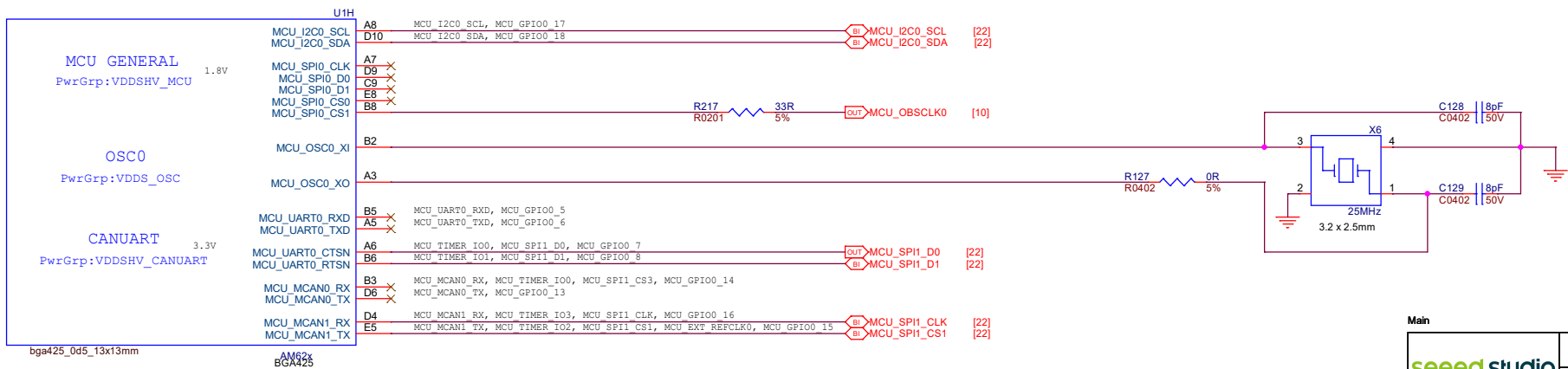
# SoC System



# WKUP Domain



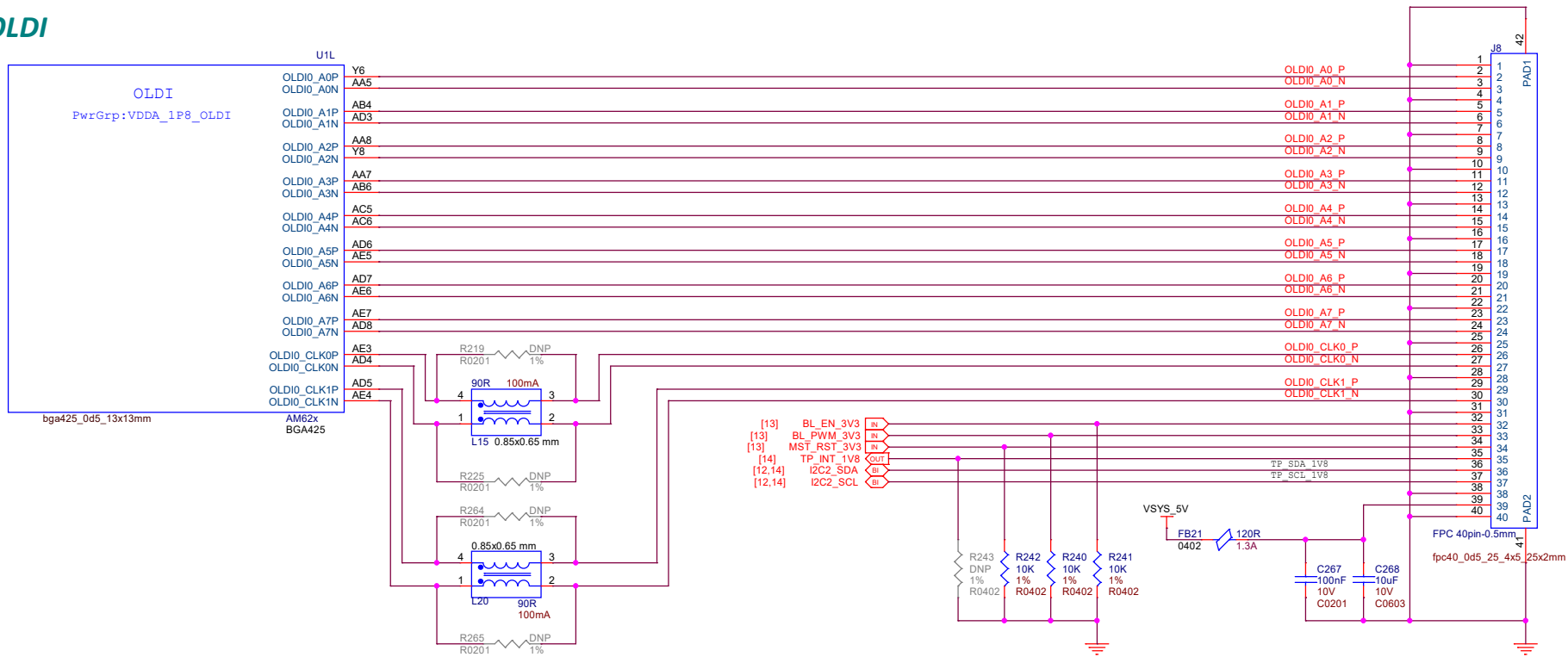
# MCU Domain



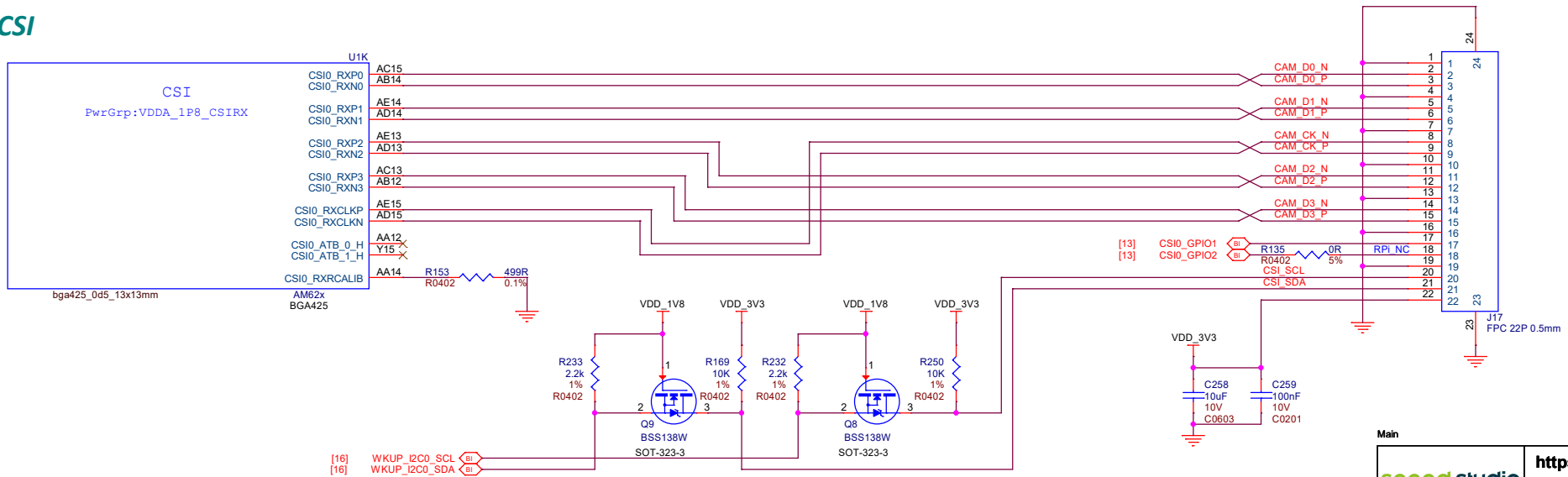
		<a href="https://www.seeedstudio.com">https://www.seeedstudio.com</a>	
		Title: <b>BeaglePlay</b>	
Size: <b>A3</b>	Document Number: <b>016_SoC Reset &amp; MCU</b>	Rev: <b>v1.0</b>	
Draw By: <b>qxn</b>	Date: <b>Tuesday, December 27, 2022</b>	Sheet: <b>16 of 22</b>	



# OLDI



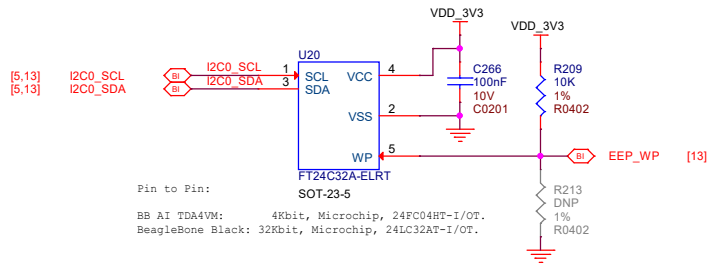
# CSI



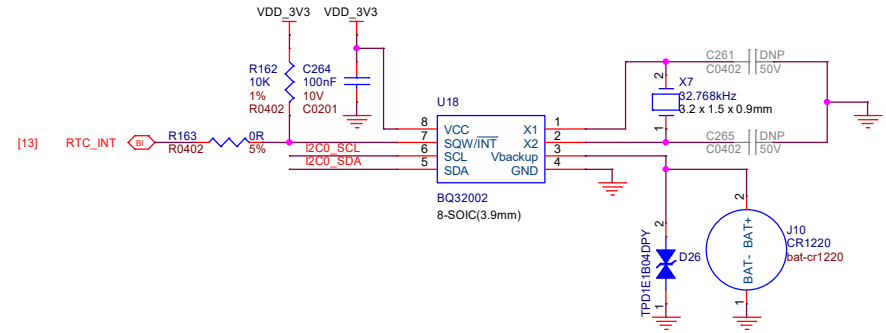
Main

<b>seeed studio</b>		<a href="https://www.seeedstudio.com">https://www.seeedstudio.com</a>	
		Title: <b>BeaglePlay</b>	
Size: A3	Document Number: 017_SoC CSI & OLDI	Rev: v1.0	
Draw By: qxn	Date: Tuesday, December 27, 2022	Sheet: 17 of 22	

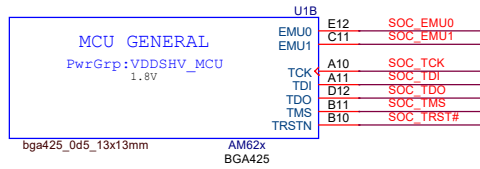
# BOARD ID EEPROM 4Kbit



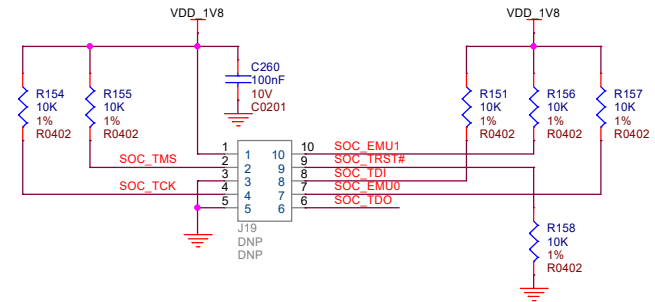
# RTC



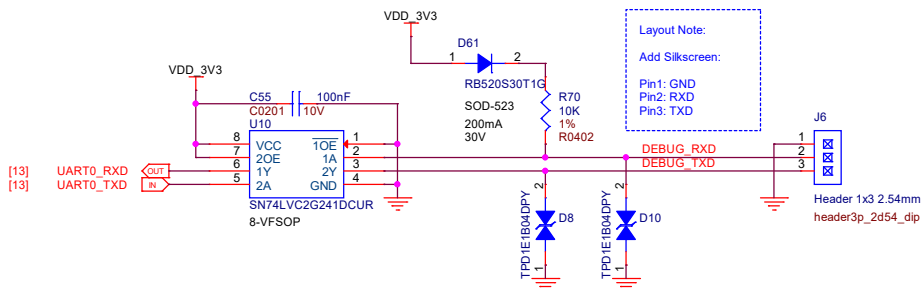
# JTAG



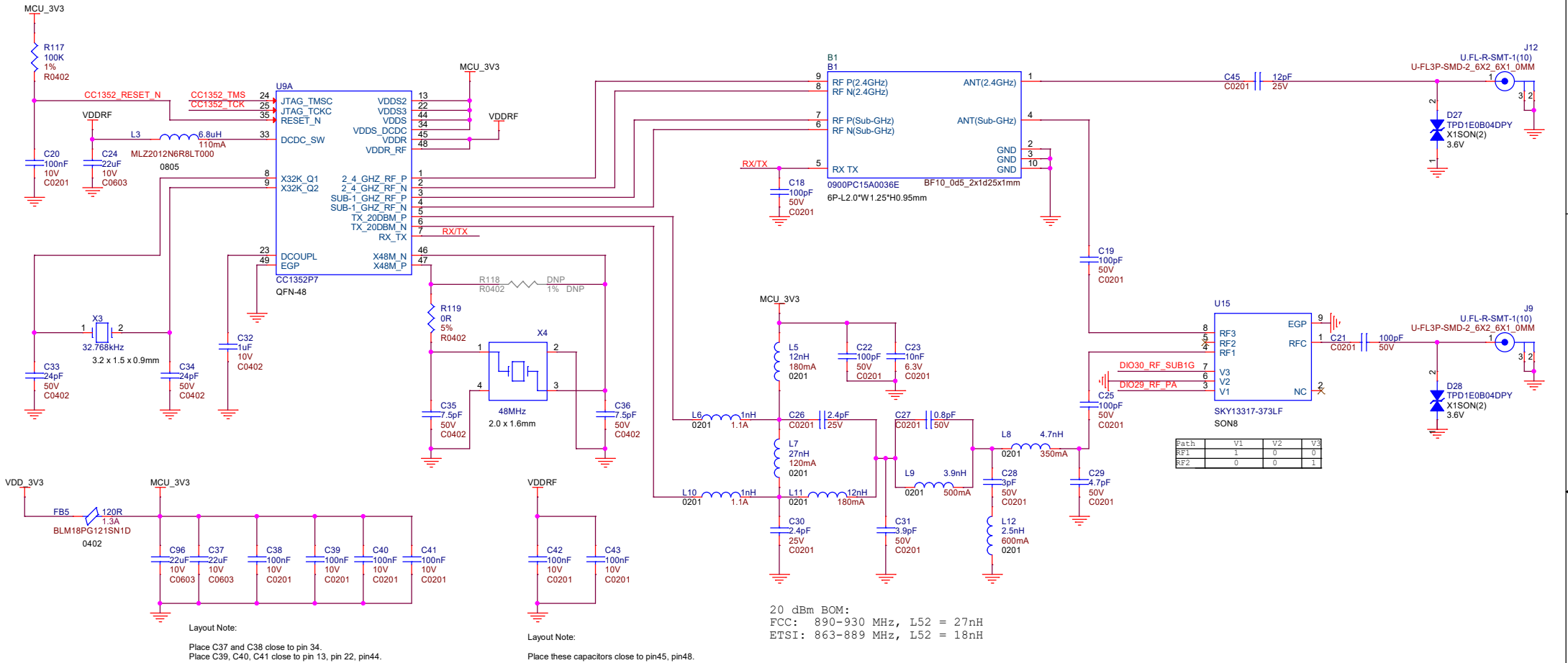
# Tag-Connect



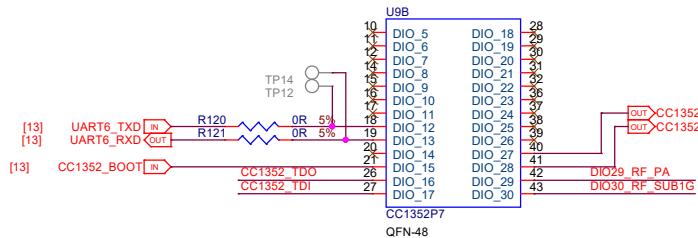
# Debug



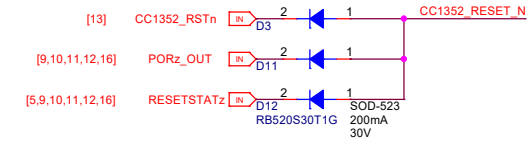
# CC1352P RF



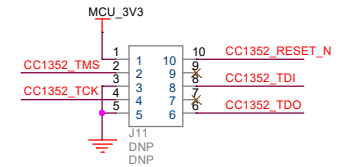
# CC1352P GPIO



# RESET



# CC1352P JTAG Tag-Connect



Main

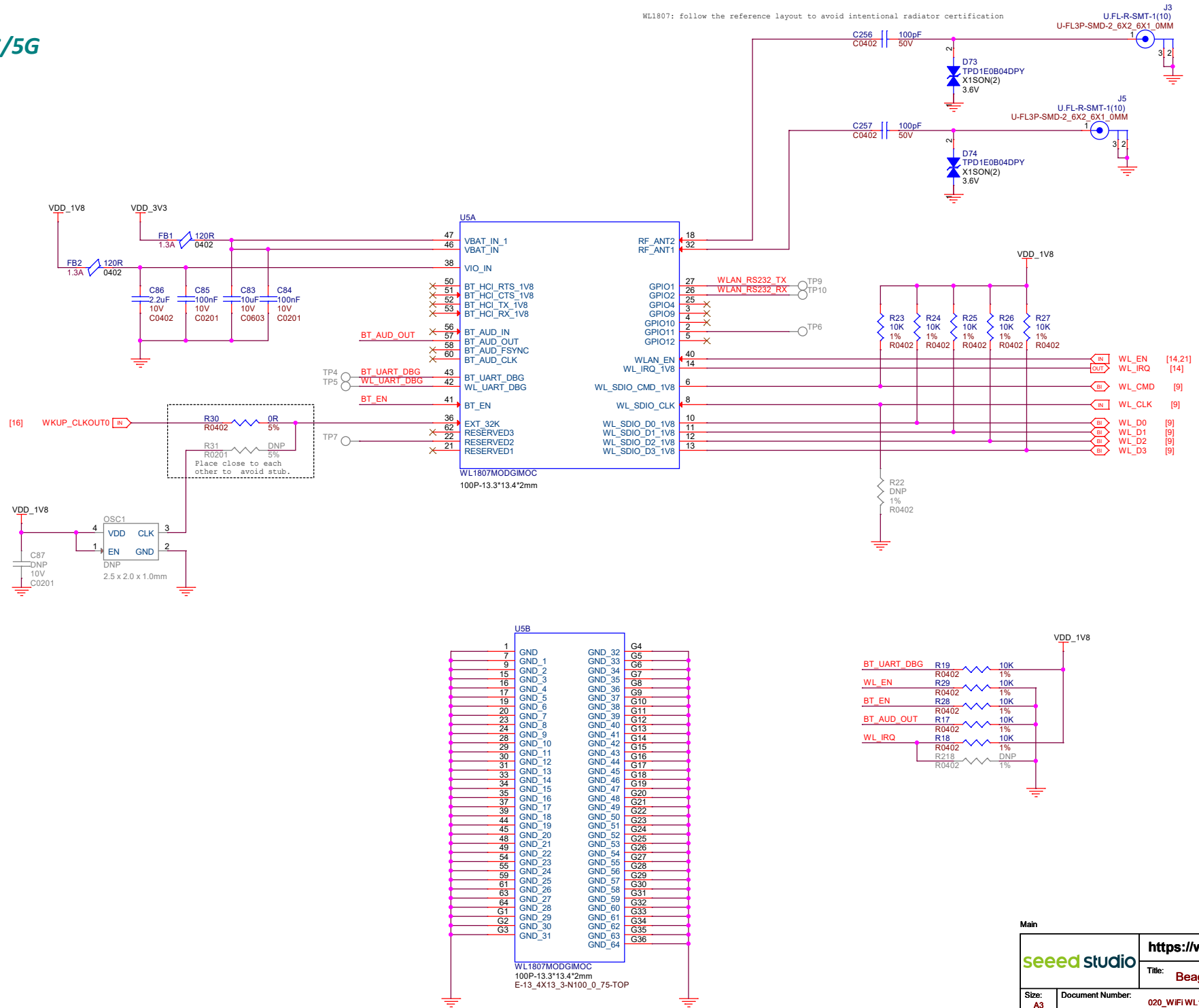
**seed studio** <https://www.seeedstudio.com>

Title: **BeaglePlay**

Size: A3	Document Number: 019_CC1352P	Rev: v1.0
Draw By: qxm	Date: Tuesday, December 27, 2022	Sheet: 19 of 22

# WiFi 2.4G/5G

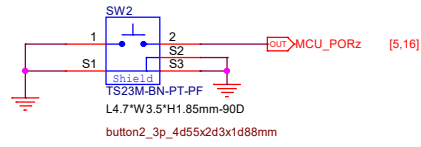
WL1807: follow the reference layout to avoid intentional radiator certification



Main

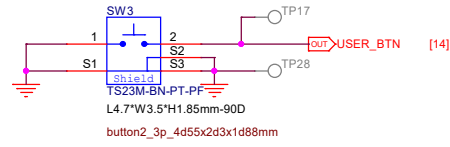
<b>seeed studio</b>		<a href="https://www.seeedstudio.com">https://www.seeedstudio.com</a>	
		Title: <b>BeaglePlay</b>	
Size: <b>A3</b>	Document Number: <b>020_WIFI WL1807MOD</b>	Rev: <b>v1.0</b>	
Draw By: <b>qxm</b>	Date: <b>Tuesday, December 27, 2022</b>	Sheet: <b>20 of 22</b>	

## Reset Button

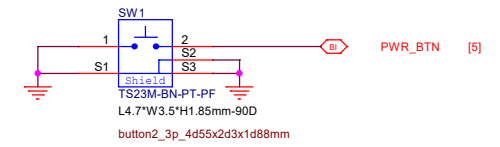


## User Button

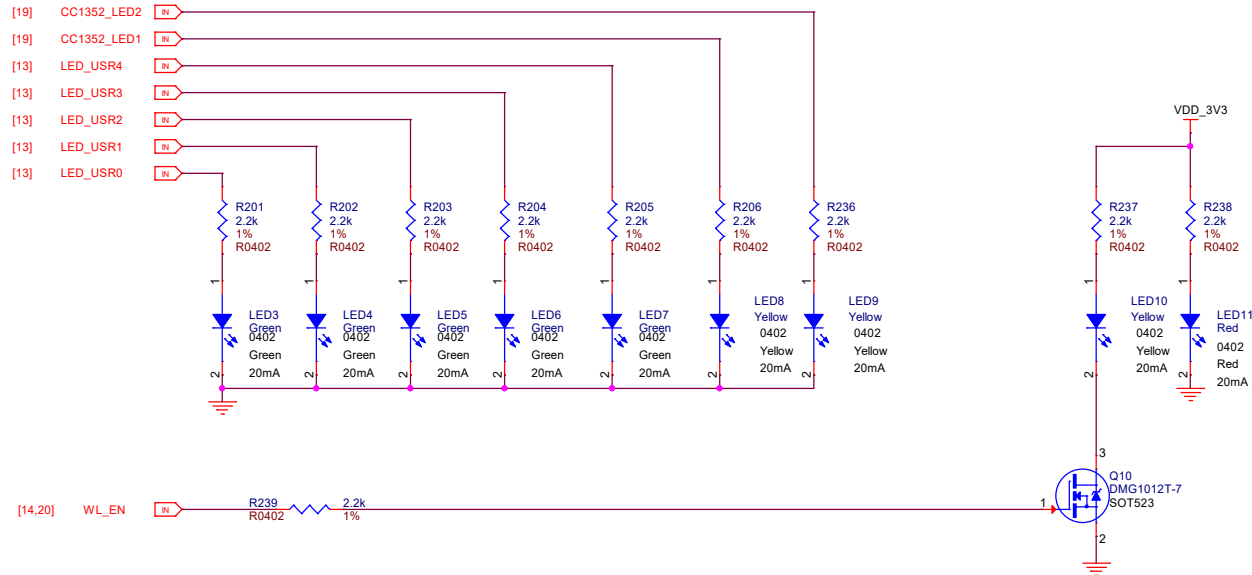
Layout Note:  
Place TP17 and TP28 close to each other, keep 2.54mm spacing.



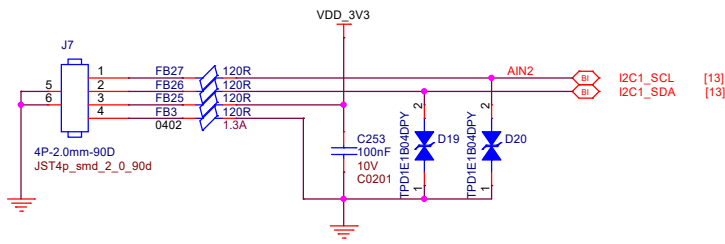
## Power Button



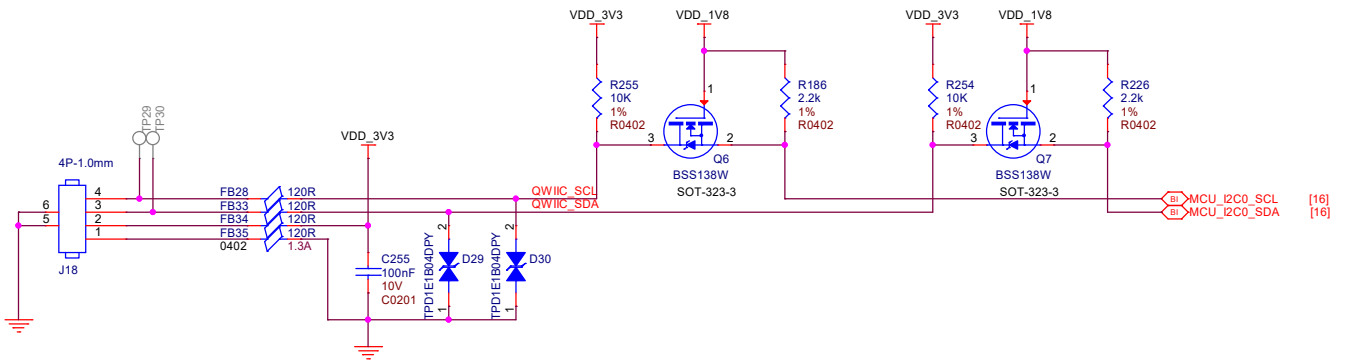
## LEDs



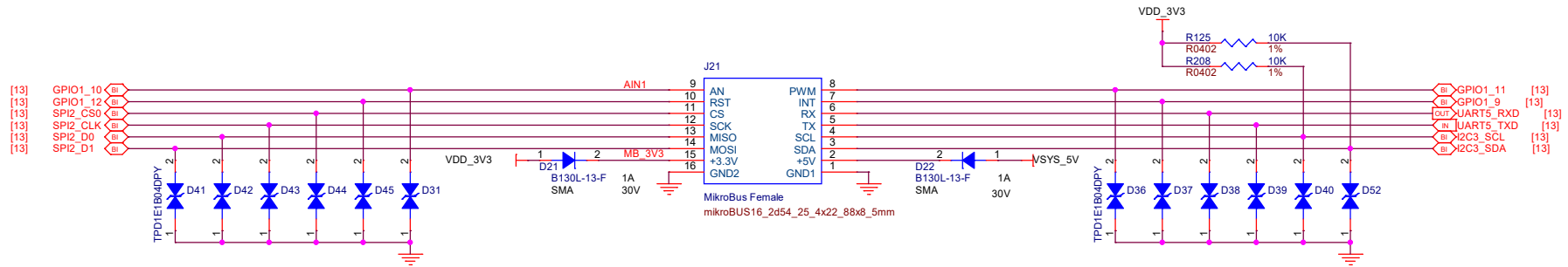
## Grove Connector



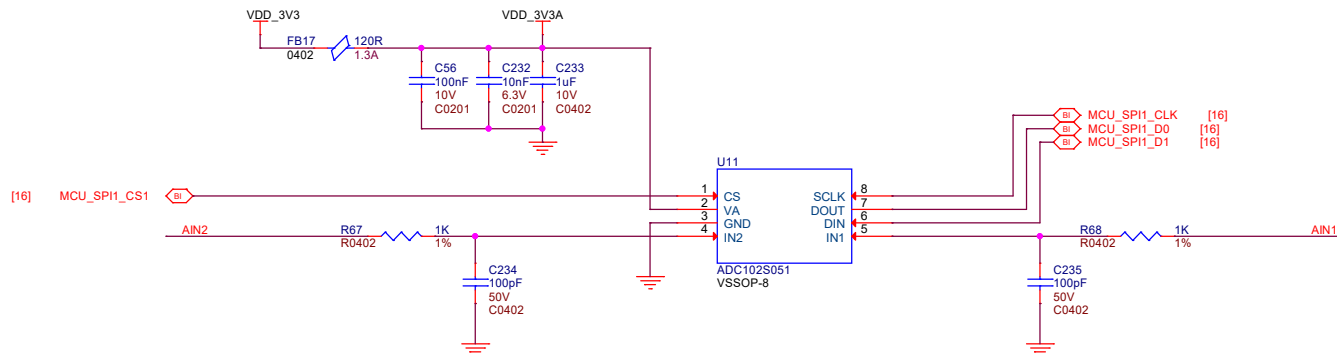
## QWIIC Connector



## MikroBus



## ADC



Main

		<a href="https://www.seeedstudio.com">https://www.seeedstudio.com</a>	
		Title: <b>BeaglePlay</b>	
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