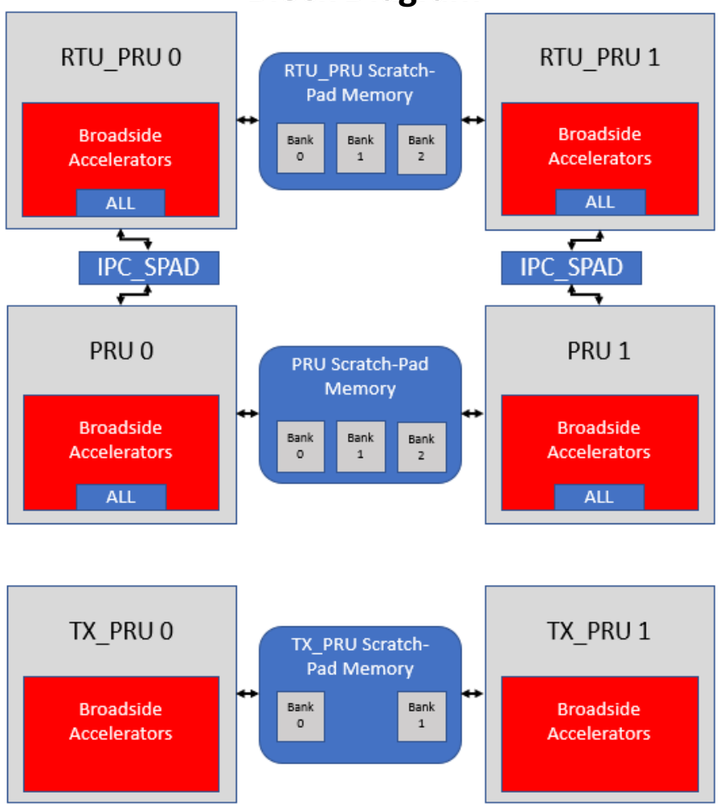
ICSS_G Broadside functions – 1024-bit data bus

Block Diagram



General Information

- PRU_ICSSG consists of 6 cores: **PRU 0/1, RTU_PRU 0/1** and **TX_PRU 0/1**
- Broadside Interface uses the **X_{IN}, X_{OUT},** or **X_{CHG} instruction** to transfer the contents
- This interface enables **up to 31 registers** (**R0-R30**, or 124 bytes) to be transferred in a single instruction
- Register **R30 (read only) = GPI / R31 (read/write) = GPO**

Registers

Accelerators	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	R17	R18	R19	R20	R21	R22	R23	R24	R25	R26	R27	R28	R29	R30	R31
MAC																										R/W	R				W	
CRC16/32			W																							W		R		R/W		
SUM32			W																											R		
BSWAP	Enables any of the internal PRU registers (R0 to R29) to swap byte (Little-Endian to Big Endian and vice versa)																															
Spinlock		R/W																														
FDB											R/W																					
xfr2vbus DMA			R/W (32 byte)								R/W (64 byte)								R/W													
xfr2psi DMA		R/W																														
BS_RAM			R/W																													
xfr2tr DMA			W				R/W																									
Scratch Pad	Has access to all registers of the Cores																															
IPC scratch pad			R/W																													
MII_RT			R/W																											W	R/W	

BS Accelerators

Processing

Accelerator	Function	ID	Core
MAC	Multiplies 32-bit operands and gives a 64-bit result with 2 modes (Multiply only or Multiply Accumulate)	00	ALL
CRC16/32	Cyclic redundancy check. Supports three polynomials → CRC32, CRC16, CRC16-CCITT	01	ALL
SUM32	Continuously monitors the Broadside (BS) RAM and facilitates SW to detect a UDP Checksum	47/39 49/38	PRU RTU
Byte Swap (BSWAP)	Allows any of the internal Registers (R0 – R29) to swap byte order	160-162	ALL
Task Manager	Real-time Task Managers with three priority levels and preemption support. 152 HW triggers	252	ALL
Spinlock	64 channel real-time arbitration to allow fast signaling and resource sharing. Can be used to trigger task manager	144-146	ALL
Filter Data Base (FDB)	Performs HW Lookup and provides port mapping to firmware. Helps ensure efficient using of Ethernet	32-35	PRU RTU

Data Transfer

Accelerator	Function	ID	Core
xfr2vbus DMA 64-byte	Single cycle read and write transfers with up to 64 bytes. 3x read widgets and 2x write widgets	96 - 100	ALL
xfr2psi DMA	PSI = Packet Streaming Interface, used to transfer words of packet data and control info between 2 entities in the system	80 -83	PRU RTU
BS_RAM	Dedicated 2 kB Broadside RAM that connects with internal registers R2-R9, 256 x 32 bytes	30/48 38/49	PRU RTU
xfr2tr DMA	Used for accelerating system dma transfer	112/ 113	ALL
SPAD Register	Temporary storage for register content of the cores. XIN/XOUT shift functionality to remap content	10 - 12	ALL
IPC scratch pad	32-byte Scratch pad connecting PRU and RTU within a Slice	15	ALL
MII_RT → RX_L2 / TX_L2	Real-time Media Interface as I/O interface for PRU to access and control up to 2 MII-ports	20/21 40	PRU RTU