

TI TMS320C6678 EVM Board Rev. 3A

DSPM-8301E

PCB PN : 19C2830103

PCB Rev. A104-1

Project Code :

**PCB Thickness : 62 mils(1.6mm)
12 Layers**

TOP	1.0 oz	3.6mils	p.p
L2_GND	1.0 oz	4mils	core
L3	0.5 oz	4.8mils	p.p
L4_PWR	1.0 oz	5mils	core
L5	0.5 oz	4.5mils	p.p
L6_GND	1.0 oz	4mils	core
L7_GND	1.0 oz	4.5mils	p.p
L8	0.5 oz	5mils	core
L9_PWR	1.0 oz	4.8mils	p.p
L10	0.5 oz	4mils	core
L11_GND	1.0 oz	3.6mils	p.p
BOT	1.0 oz		

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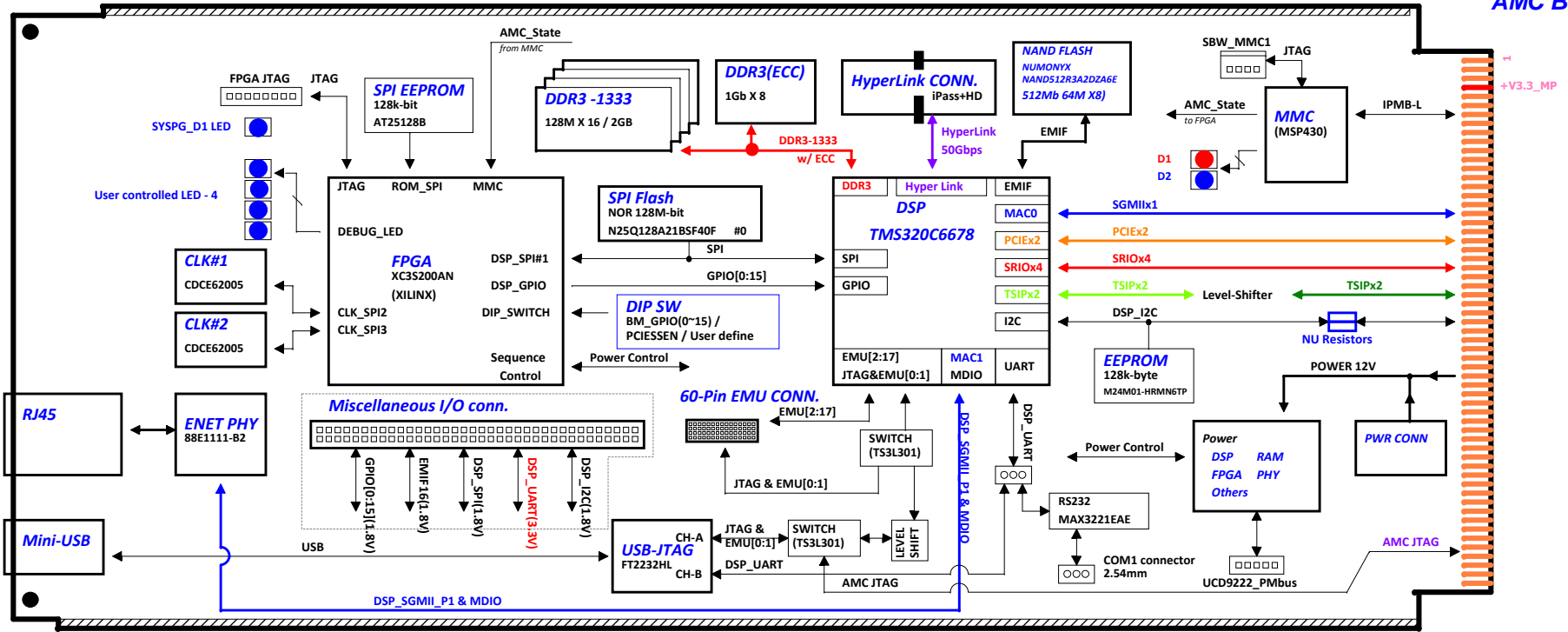
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BLOCK DIAGRAM_AMC

AMC Board



Miscellaneous I/O 80 Pin conn. Signal

PIN	Port mapping	PIN	Port mapping	PIN	Port mapping
02	EMIFA00	42	EMIFA20	01	GND
04	EMIFA01	44	EMIFA21	03	SDA
06	EMIFA02	46	EMIFA22	05	SCL
08	EMIFA03	48	EMIFA23	07	EMIFD0
10	EMIFA04	50	GPI00	09	EMIFD1
12	EMIFA05	52	GPI01	11	EMIFD2
14	EMIFA06	54	GPI02	13	EMIFD3
16	EMIFA07	56	GPI03	15	EMIFD4
18	EMIFA08	58	GPI04	17	EMIFD5
20	EMIFA09	60	GPI05	19	EMIFD6
22	EMIFA10	62	GPI06	21	EMIFD7
24	EMIFA11	64	GPI07	23	EMIFD8
26	EMIFA12	66	GPI08	25	EMIFD9
28	EMIFA13	68	GPI09	27	EMIFD10
30	EMIFA14	70	GPI010	29	EMIFD11
32	EMIFA15	72	GPI011	31	EMIFD12
34	EMIFA16	74	GPI012	33	EMIFD13
36	EMIFA17	76	GPI013	35	EMIFD14
38	EMIFA18	78	GPI014	37	EMIFD15
40	EMIFA19	80	GPI015	39	EMIFCE1Z

AMC Port mapping

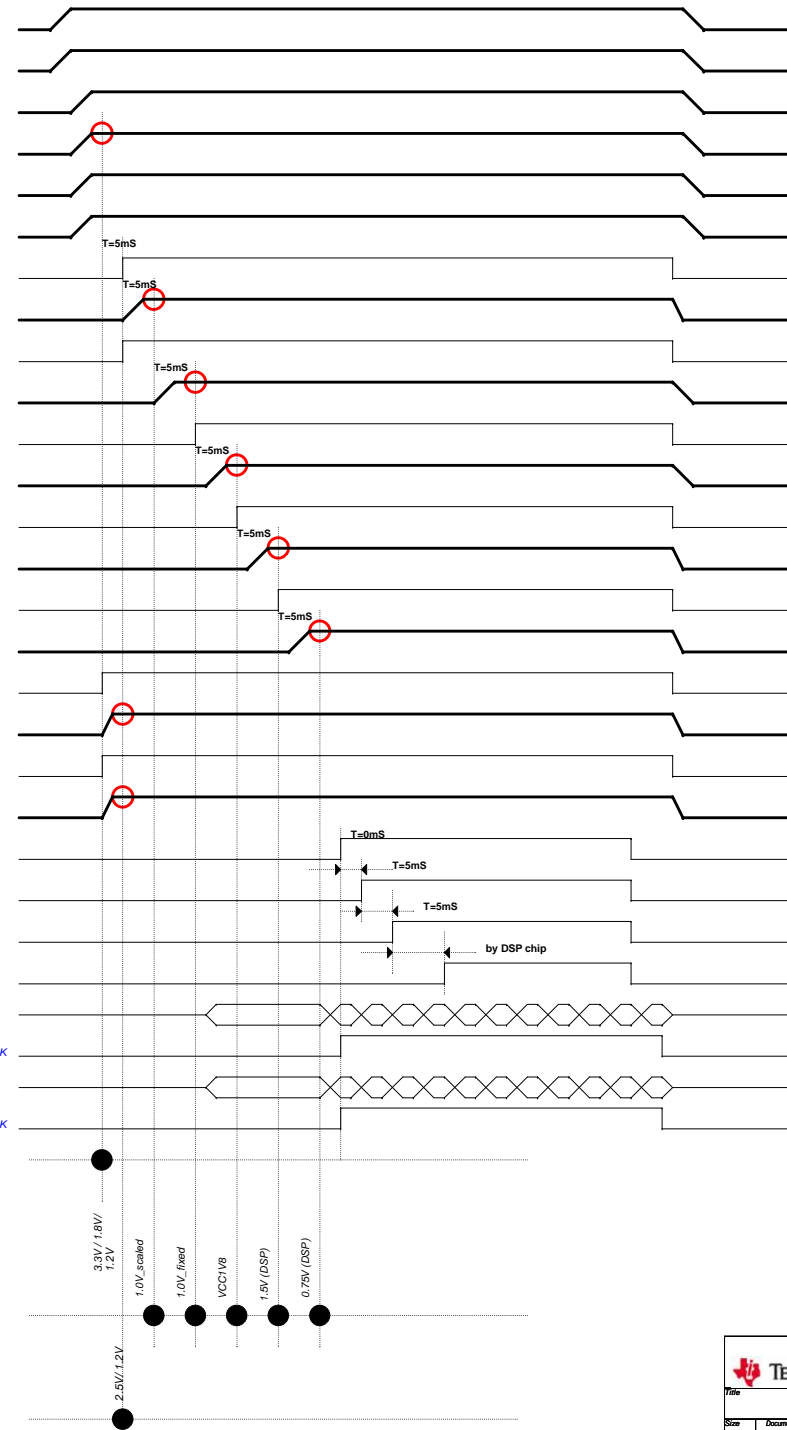
PIN	Port mapping	PIN	Port mapping
TCLKA	TSIP_CLK0	11	SRIO_4
TCLKB	TSIP_CLK1	12	TSIPO [0..3]
FCLKA	100MHz	13	TSIP1 [0..3]
00	SGMII	14	Alternate I2C link
01		15	
02		16	
03		TCLKC	TSIP_FS0
04	PCI-E_1	TCLKD	TSIP_FS1
05	PCI-E_2	17	
06		18	
07		19	
08	SRIO_1	20	AMC_JTAG
09	SRIO_2		
10	SRIO_3		

Power Sequence

Label	Time	Description
T0	1ms	S2 plane power stable to S3 enable signal assertion

VCC3V3_MP_AMC			
S0	MMC	VCC3V3_MP	
S1		VCC12	
S2	Other FT2232H XC3S200AN	VCC3V3_AUX	
S3	XC3S200AN	VCC1V8_AUX	
S4	88E1111 XC3S200AN	VCC1V2	
S5		PMBUS & UCD9222_ENA1	
S6	DSP TMS320C6678	CVDD	
S7		UCD9222_VID2 & UCD9222_ENA2	
S8	DSP TMS320C6678	VCC1V0	
S9		VCC1V8_EN	
S10	DSP TMS320C6678	VCC1V8	
S11		VCC1V5_EN	
S12	DDR3 DSP TMS320C6678	DDR3 SDRAM VCC1V5	
S13		VCC0V75_EN	
S14	DDR3 DSP TMS320C6678	DDR3 Vref VCC0V75	
S15		VCC2V5_EV	
S16	88E1111	VCC2V5	
S17		VCC5_EN	
S18	XDS560V2 Mazzenine Board	VCC5	

RESET# including peripherals.
 POR#
 RESETFULL#
 RESETSTAT#
 REFCLKP&N by REFCLK_PD#
 CLOCK2_PLL_LOCK
 DDRCLKP&N by REFCLK3_PD#
 CLOCK3_PLL_LOCK

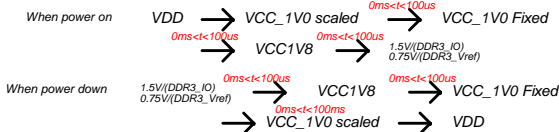


Power Sequence

Reset Sequence

CLK Sequence

There is no specific power-up nor power-down sequence.



There is no specific power-up nor power-down sequence.

XILINX_XC3S200AN
 1.2V_AUX (VCCINT)
 1.8V_AUX (VCC1V8_AUX)
 3.3V_AUX (VCCAUX)

XILINX_XC3S200AN

DSP TMS320C6678
 VCC1V0 Scaled (CVDD)
 VCC1V0 Fixed (CVDD1)
 VCC1V8 (DVDD18)
 1.5V/(DDR3_IO)
 0.75V/(DDR3_Vref)

DSP TMS320C6678

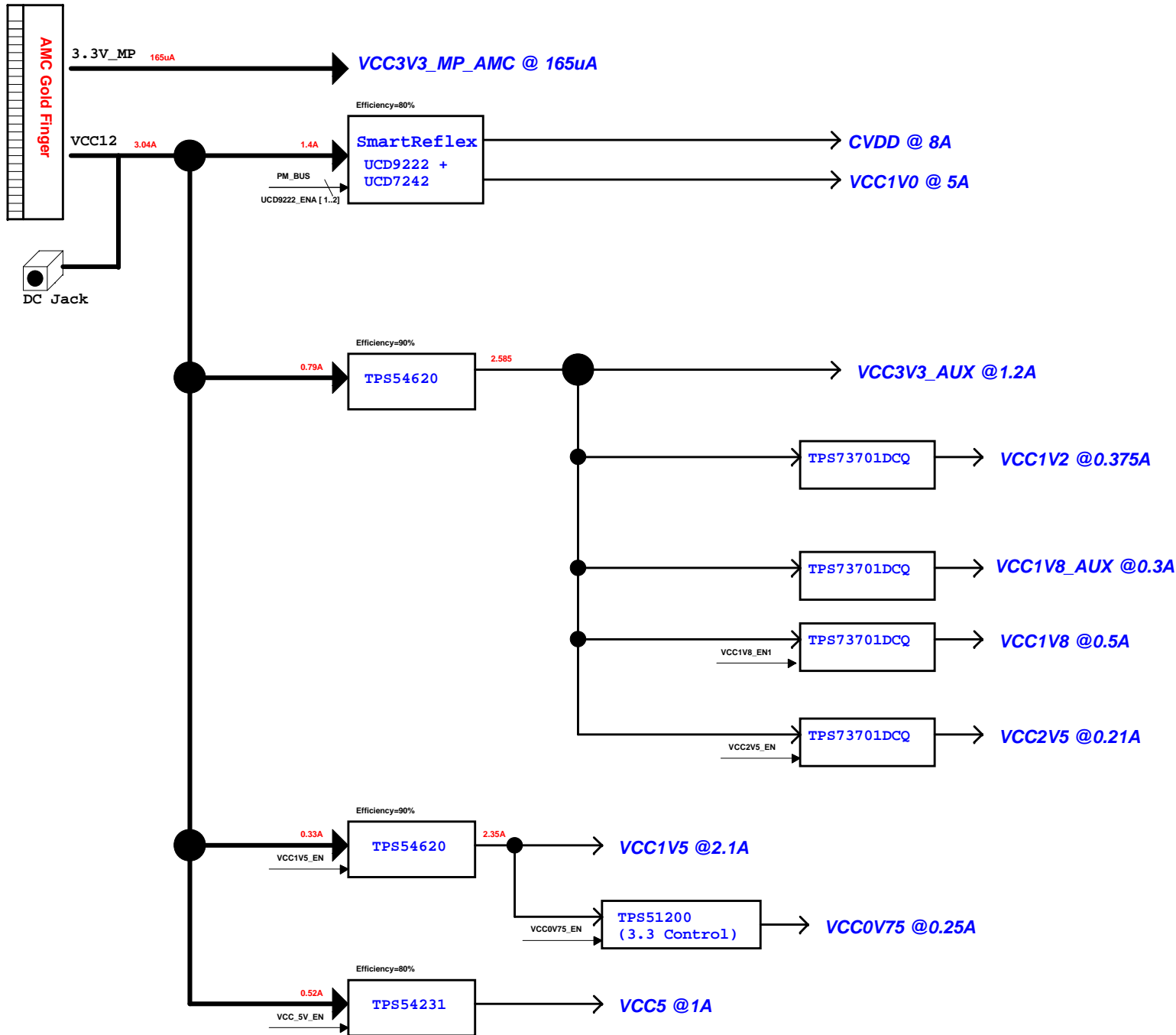
88E1111 (PHY)
 2.5V
 1.2V

88E1111

POWER CONSUMPTION

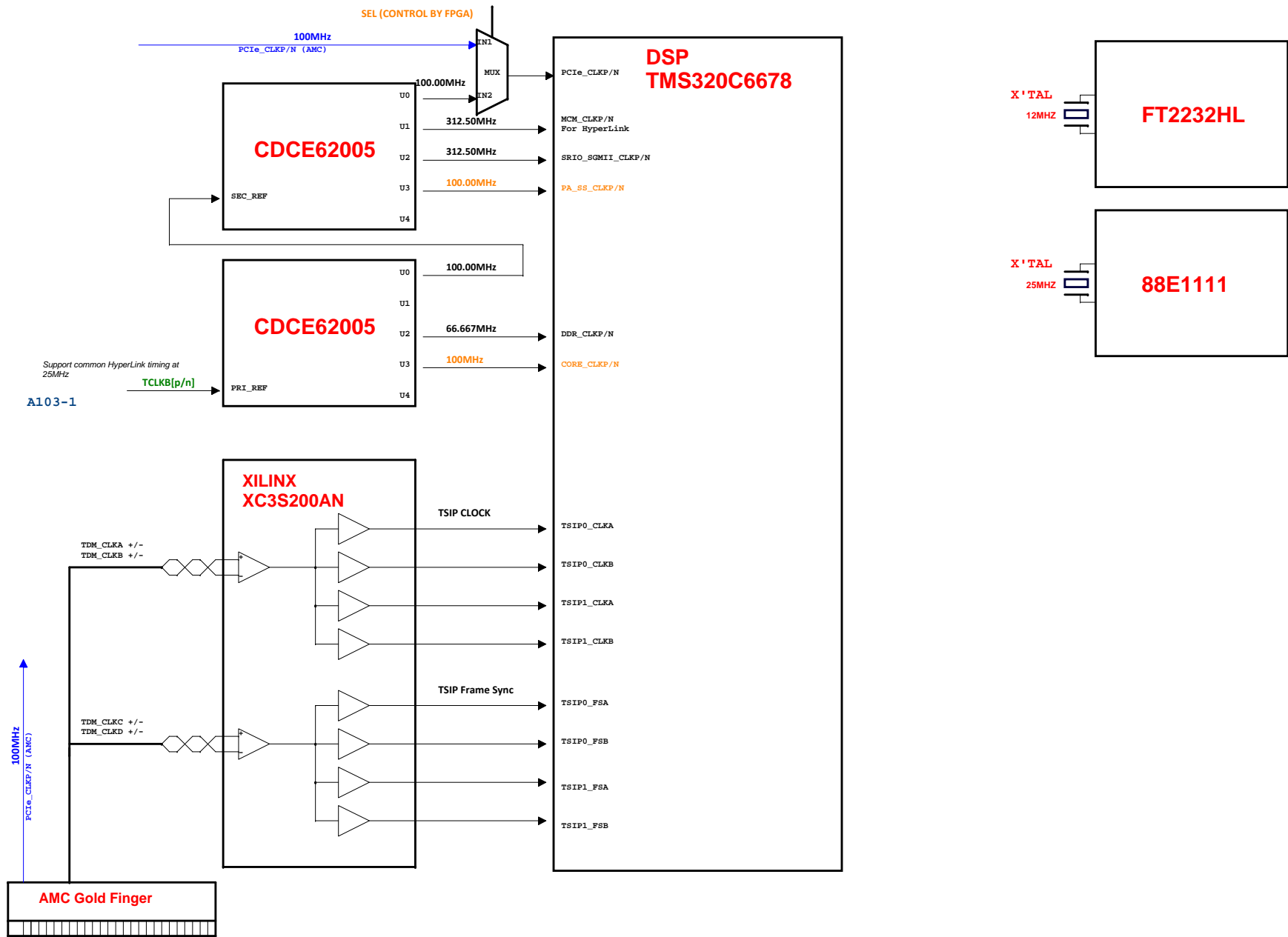
	V	I	Qty	Isub.	Efficiency	Max. Power Design			Operating (for Thermal)		Note
						Pd (W)	I12V	I3vsb	Utilization	Pd (W)	
CVDD (12V-->1.0V)				8.000			0.741				UCD9222 + UCD7242
TMS320C6678	1.00	8.000	1	8.000	90%	8.889	0.741	x	70%	6.222	
VCC1V0 (12V-->1.0V)				5.000			0.463				
TMS320C6678	1.00	5.000	1	5.000	90%	5.556	0.463	x	70%	3.889	
VCC1V5 (12V-->1.5V)				2.300			0.319				TPS54620
TMS320C6678	1.50	0.850	1	0.850	90%	1.417	0.118	x	70%	0.992	
DDR3	1.50	0.240	5	1.200	90%	2.000	0.167	x	100%	2.000	
VCC0V75 (VTT for DDR3) 1.5V-->0.75V							x				TPS51200
DDR3	0.75	0.050	5	0.250	45%	0.417	0.035	x	70%	0.292	
VCC3V3_AUX (12V-->3.3V_AUX)				2.484			0.748				TPS54620
FPGA	3.30	0.024	1	0.024	85%	0.093	0.008	x	70%	0.065	
XDS560V2 Mazzenine Board	3.30	0.300	1	0.300	85%	1.165	0.097	x	70%	0.815	
FT2232H	3.30	0.210	1	0.210	85%	0.815	0.068	x	70%	0.571	
Others	3.30	0.660	1	0.660	85%	2.562	0.214	x	70%	1.794	
VCC1V8_AUX (3.3V_AUX-->1.8V_AUX)							x				TPS73701DCQ
FPGA	1.80	0.200	1	0.200	46%	0.783	0.065	x	70%	0.548	
Others	1.80	0.100	1	0.100	46%	0.391	0.033	x	70%	0.274	
VCC1V8 (3.3V_AUX-->1.8V)							x				TPS73701DCQ
TMS320C6678	1.80	0.330	1	0.330	46%	1.291	0.108	x	70%	0.904	
FT2232H	1.80	0.075	1	0.075	46%	0.293	0.024	x	70%	0.205	
VCC1V2_AUX (3.3V_AUX-->1.2V_AUX)							x				TPS73701DCQ
FPGA	1.20	0.125	1	0.125	30%	0.500	0.042	x	70%	0.350	
88E1111	1.00	0.250	1	0.250	90%	0.278	0.023	x	70%	0.194	
VCC2V5 (3.3V_AUX-->2.5V)							x				TPS73701DCQ
88E1111	2.50	0.210	1	0.210	65%	0.808	0.067	x	70%	0.565	
VCC5 (12V-->5V)				1.000			0.490				TPS54231
XDS560V2 Mazzenine Board	5.00	1.000	1	1.000	85%	5.882	0.490	x	70%	4.118	
VCC3V3_MP_AMC (150mA)				0.048			x	0.048			
MMC_MSP430	3.30	0.048	1	0.048	100%	0.158	x	0.048	70%	0.111	
Total power consumption						P_{max}	I_{12V}	I_{3VSB}		P_{op}	
						33.298	2.762	0.096		23.909	

POWER DISTRIBUTION



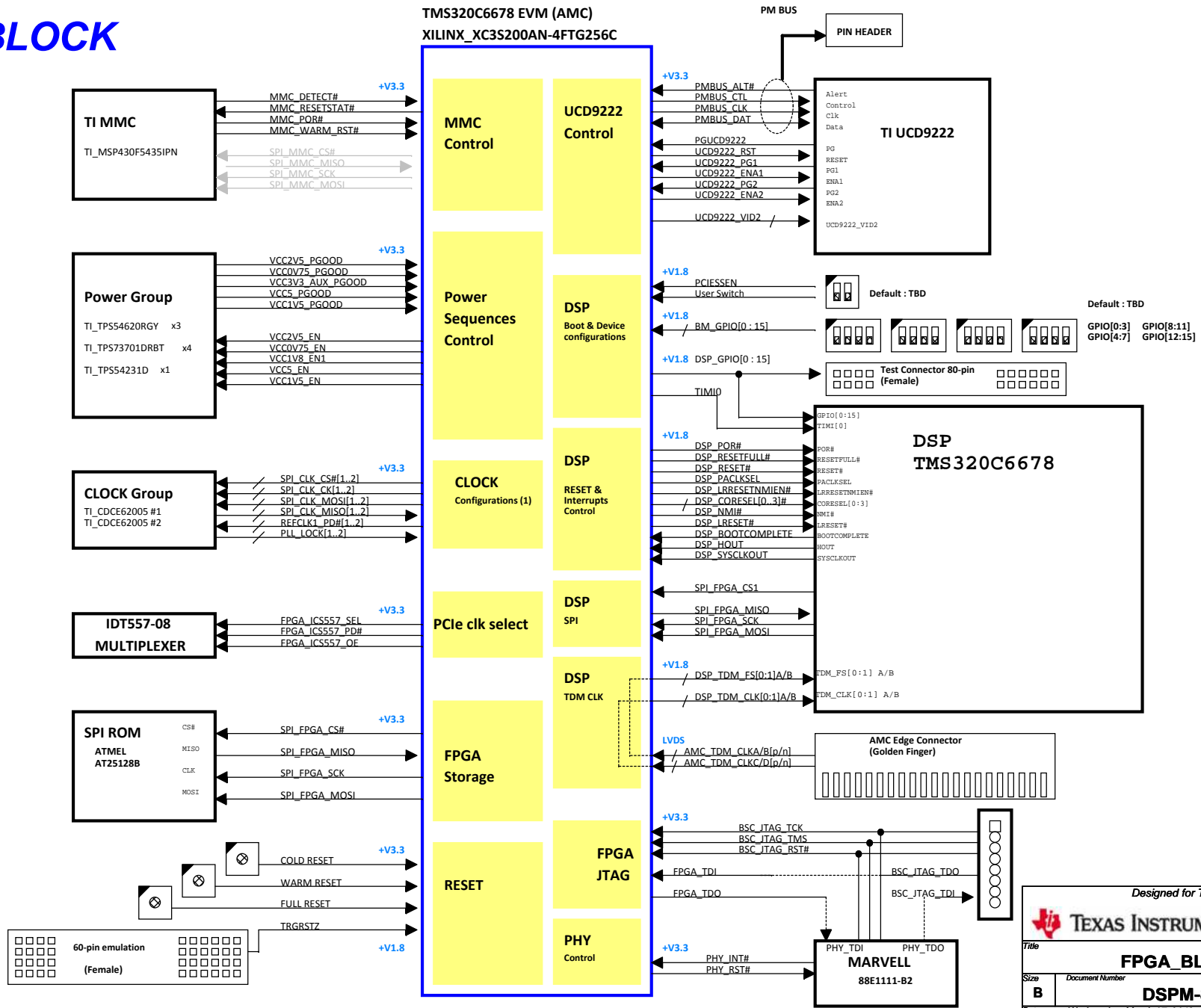
- XILINX_XC3S200AN**
1.2V_AUX/ 0.125A (VCCINT)
3.3V_AUX/ 0.024A (VCCAUX)
- DSP TMS320C6678**
VCC1V0 / 8A Scaled/(CVDD)
VCC1V0 / 5A Fixed/(CVDD1)
VCC1V8 / 0.33A (VDD18)
1.5V / 0.85A (DDR3_IO)
0.75V/(DDR3_Vref)
- DDR3**
1.5V / 1.2A (DDR3_VDD)
0.75V / 0.25A (DDR3_Vref)
- 88E1111 (PHY)**
2.5V / 0.21A
1.2V / 0.25A
- FT2232H(USB-JTAG)**
3.3V / 0.21A
- RS232**
3.3V
- FLASH**
1.8V
- SPI NOR FLASH**
1.8V
- XDS560V2 Mazzerine Board**
5.0V / 1A
3.3V / 0.3A

CLOCK DIAGRAM



FPGA_BLOCK

TMS320C6678 EVM (AMC)
XILINX_XC3S200AN-4FTG256C



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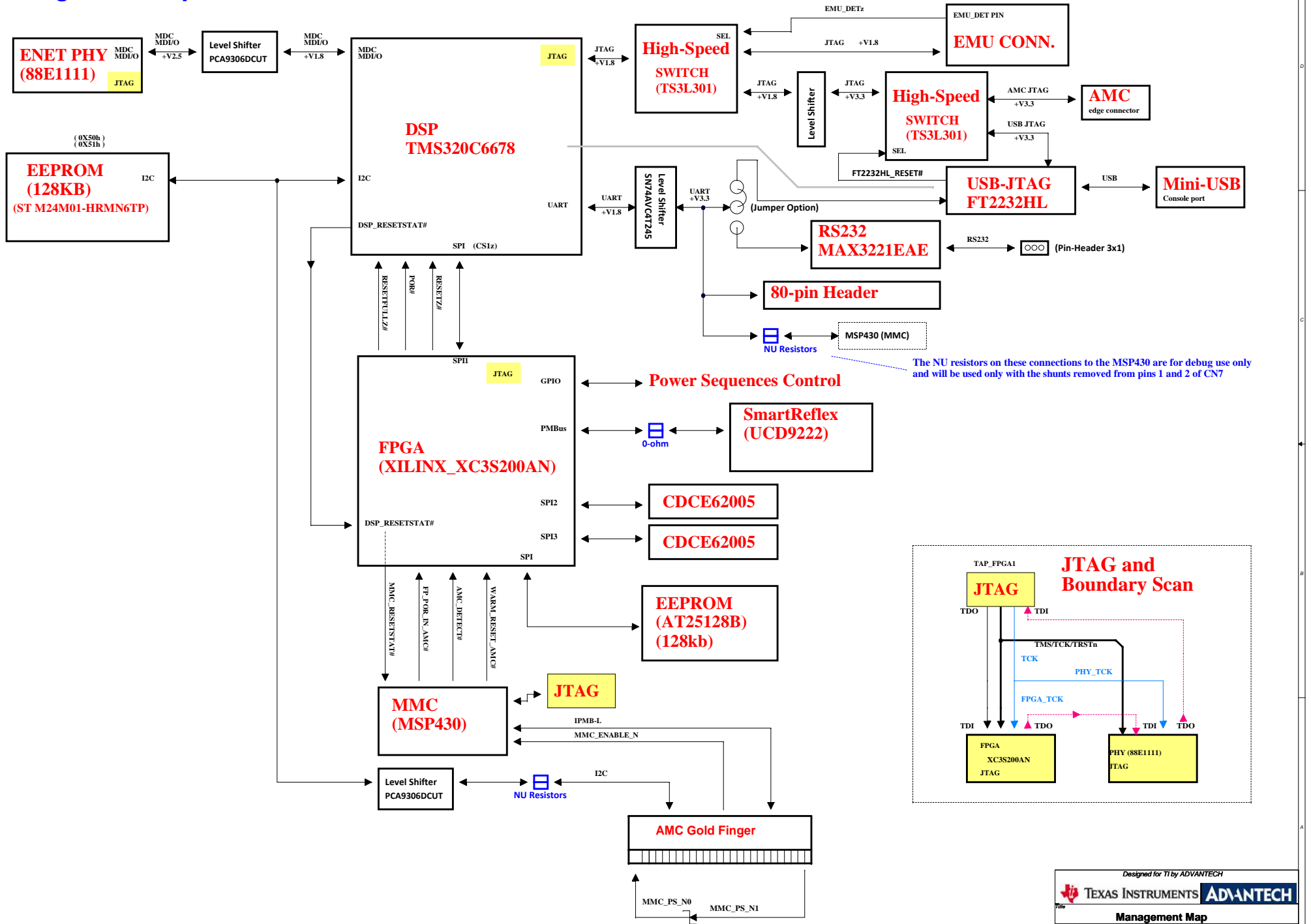
TEXAS INSTRUMENTS ADVANTECH

Title: **FPGA_BLOCK**

Size: **B** Document Number: **DSPM-8301E** Rev: **A104-1**

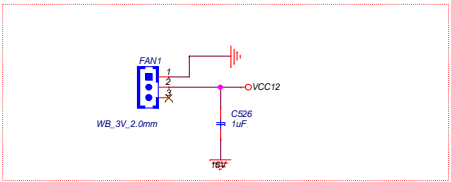
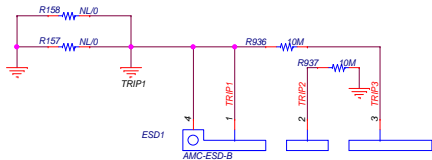
Date: **Wednesday, March 07, 2012** Sheet: **8** of **40**

Management Map

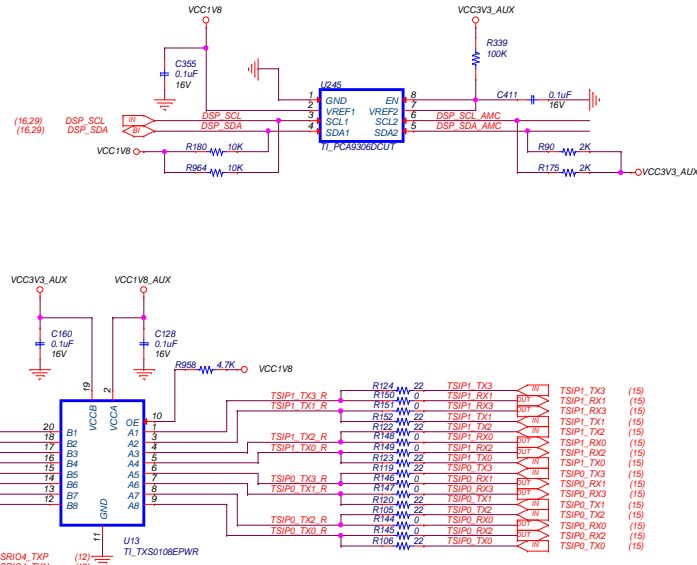
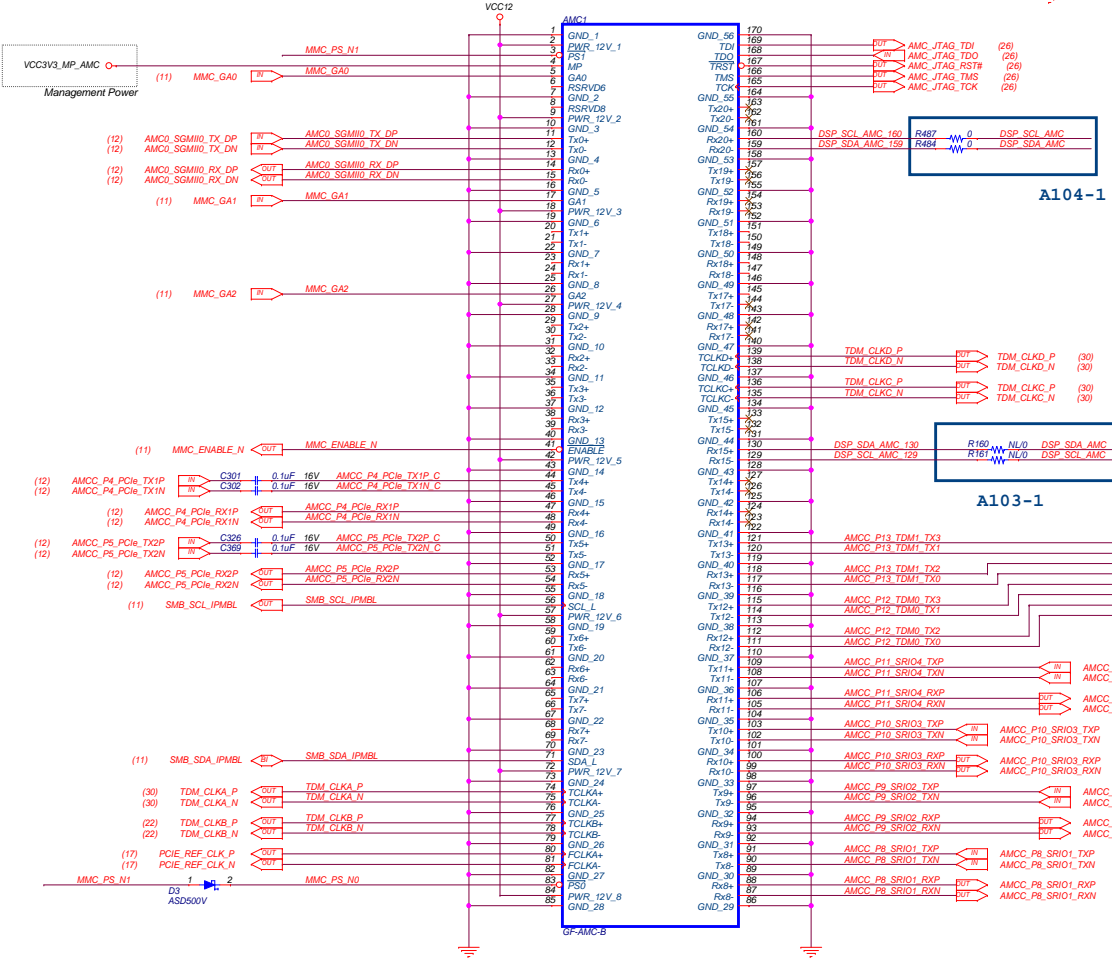
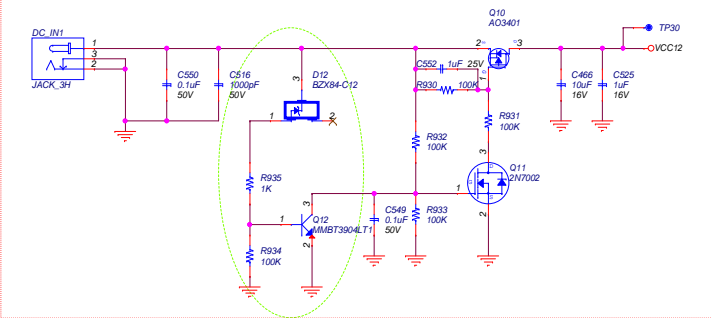


The NU resistors on these connections to the MSP430 are for debug use only and will be used only with the shunts removed from pins 1 and 2 of CN7

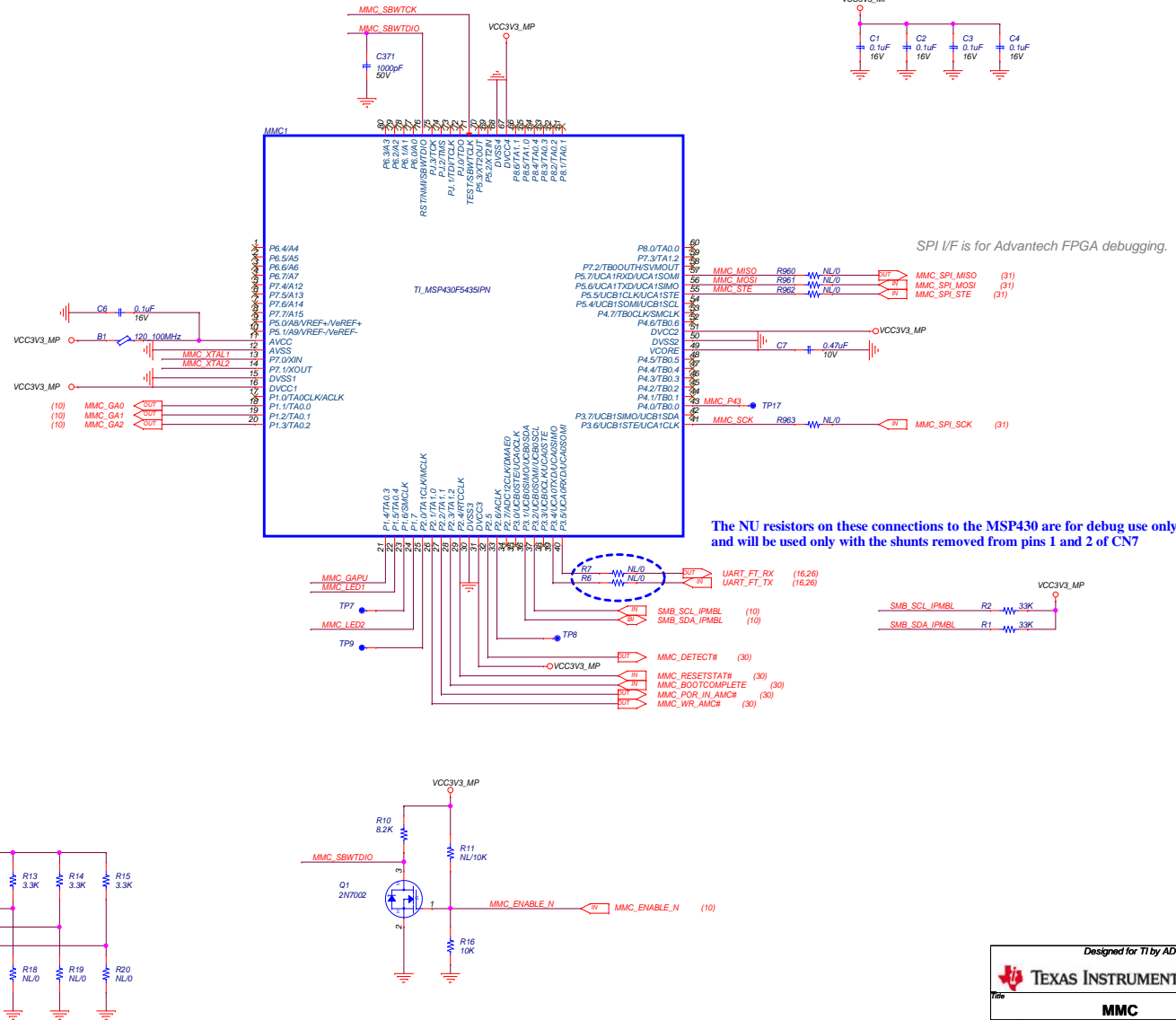
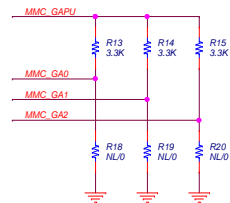
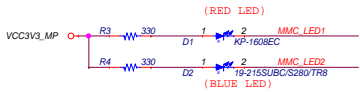
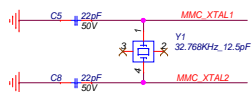
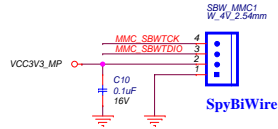
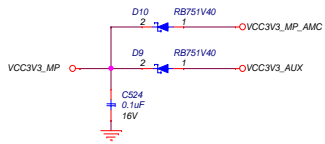
Front panel and ESD Strip



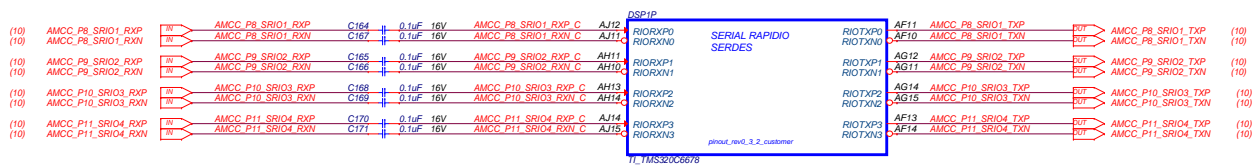
OVP: ~12.7V+0.6V = ~13.3V



Power for MSP430



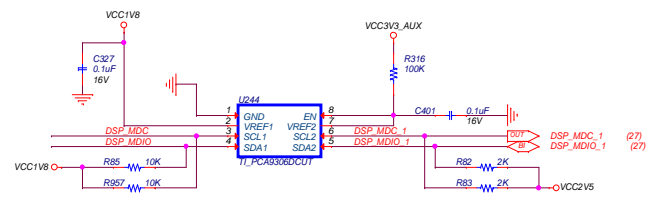
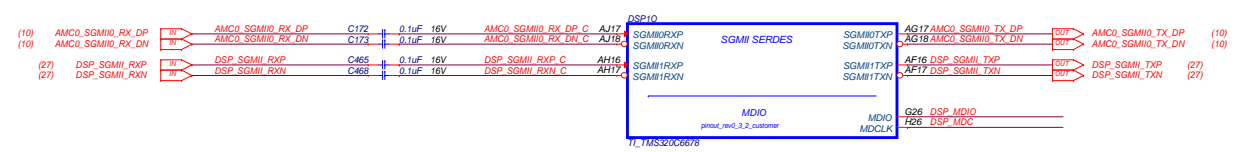
SRIO



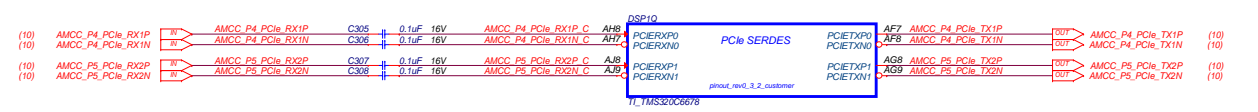
Caution!

"Place ALL SERDES DC-blocking caps on top layer adjacent to the DSP's RX pins so that there are no additional vias"

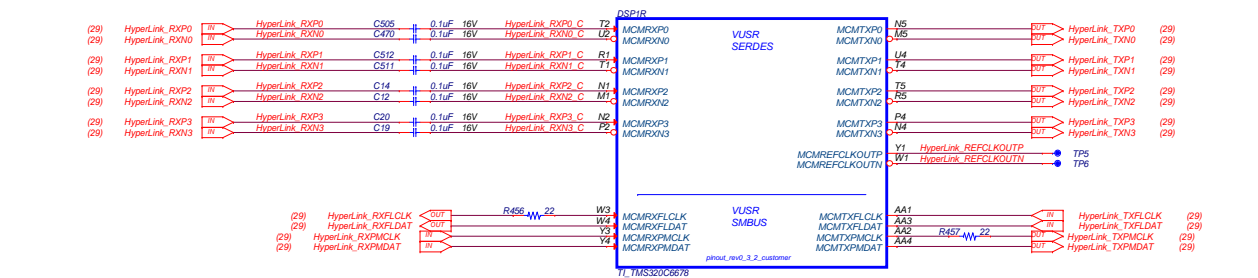
SGMII



PCIE



HyperLink



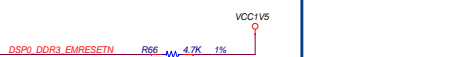
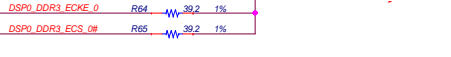
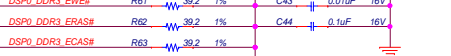
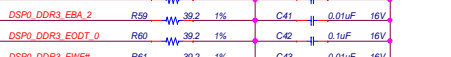
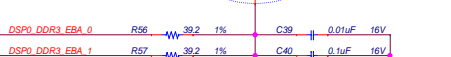
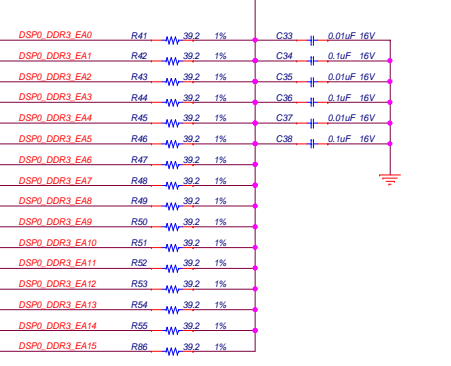
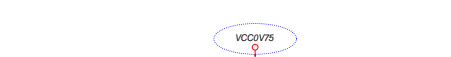
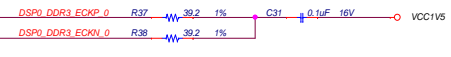
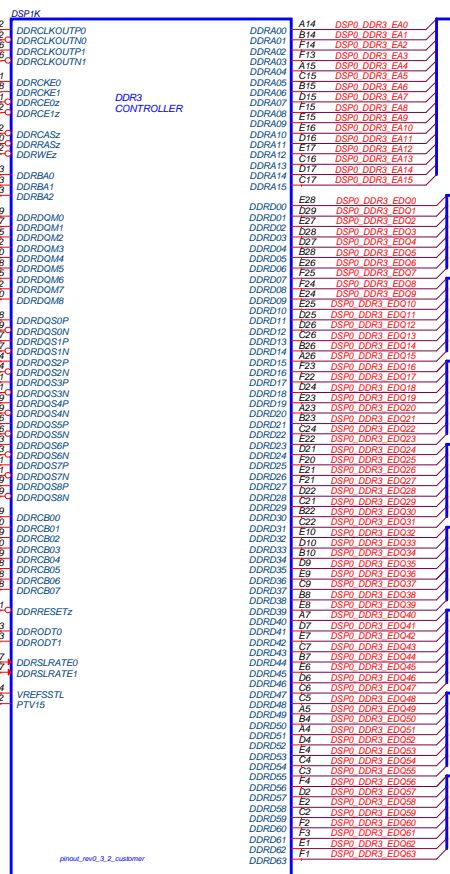
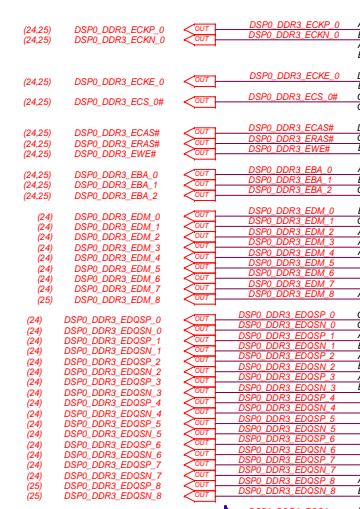
"The HyperLink routes must have a maximum of 2 vias and no via stubs – top layer routing recommended"

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DSP_SERDES_PORTS

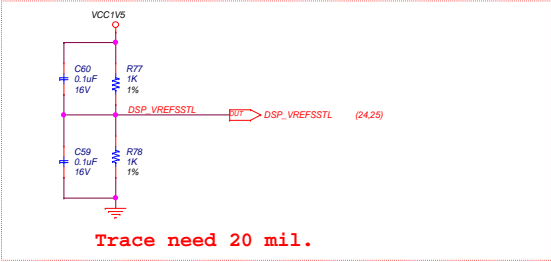
Size: C Document Number: **DSPM-8301E** Rev: **A104-1**

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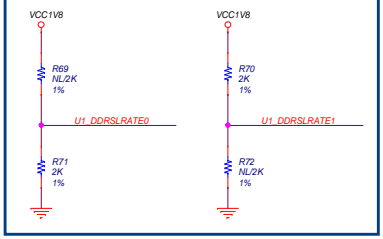
Place these resistors at the end of the trace.

A103-1



Trace need 20 mil.

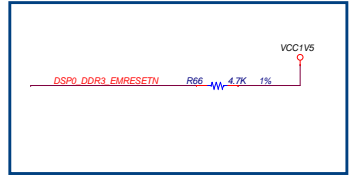
A103-1

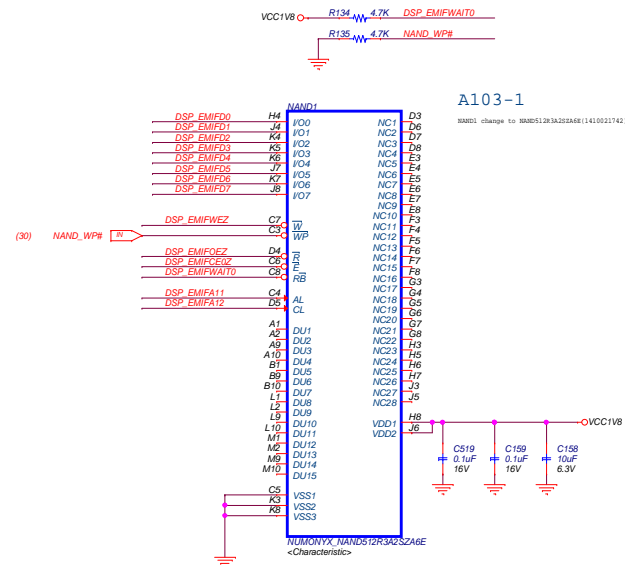
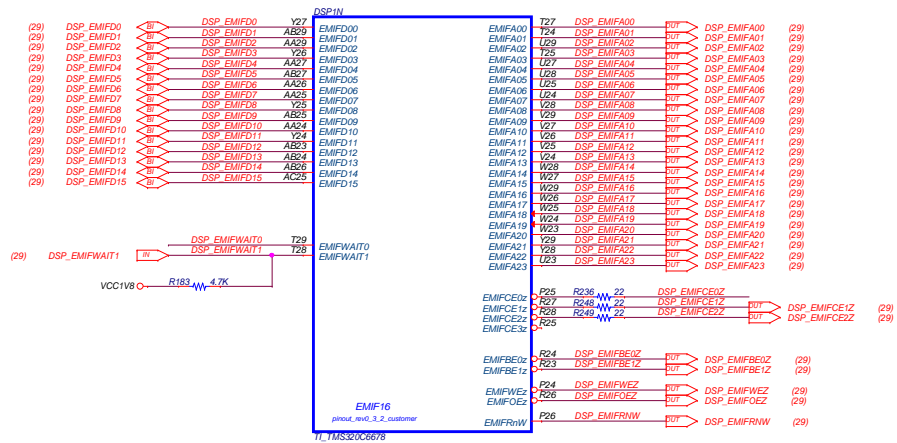


DDR3 Slew-Rate Setting (DDRSLRATE[1:0]):

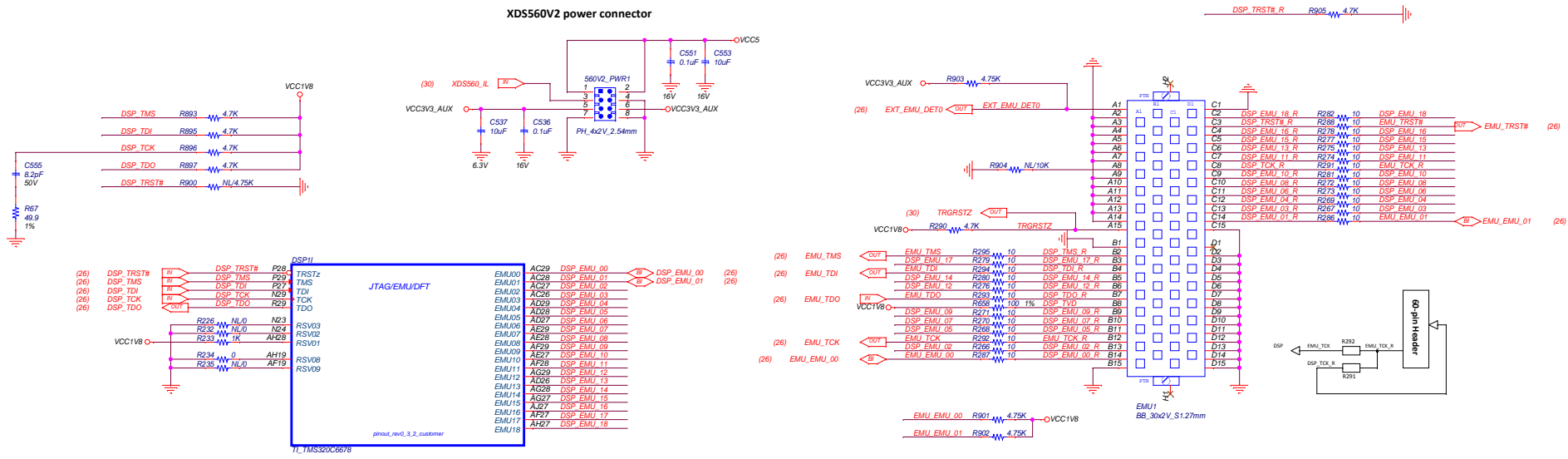
- 00 Fastest
- 10 Fast
- 01 Slow
- 11 Slowest

A103-1

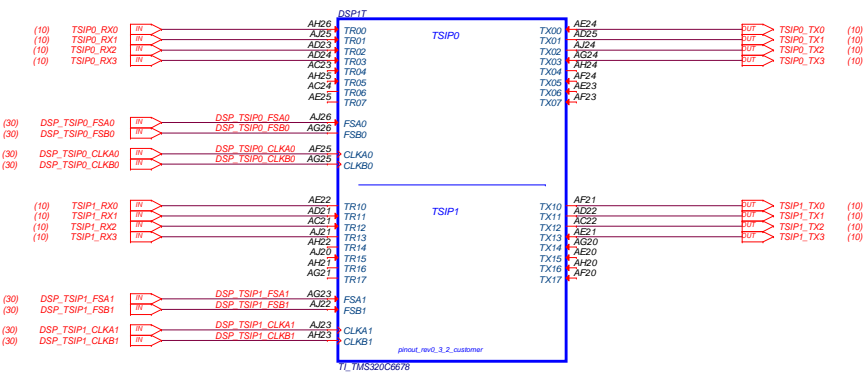




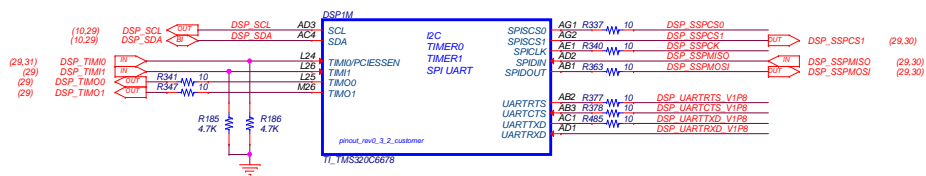
JTAG & EMU



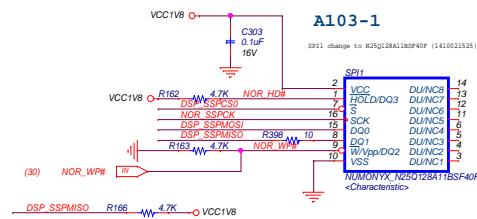
TSIP0, 1



I2C, TIMER0,1, SPI, UART

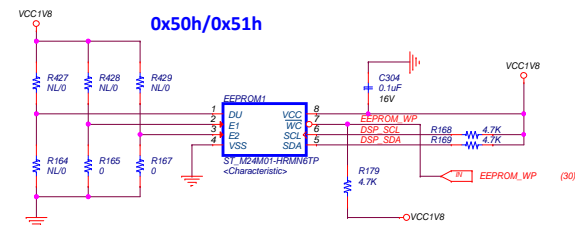


16M SPI NOR Flash

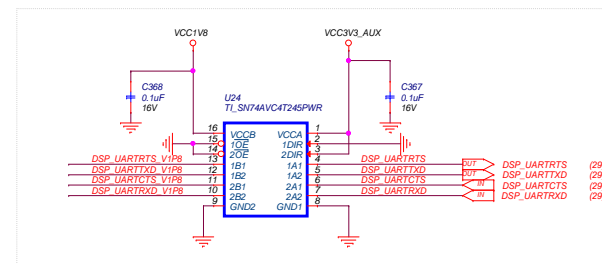
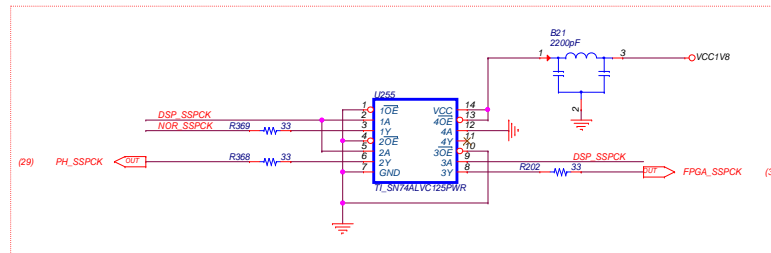


1M-bit I2C EEPROM

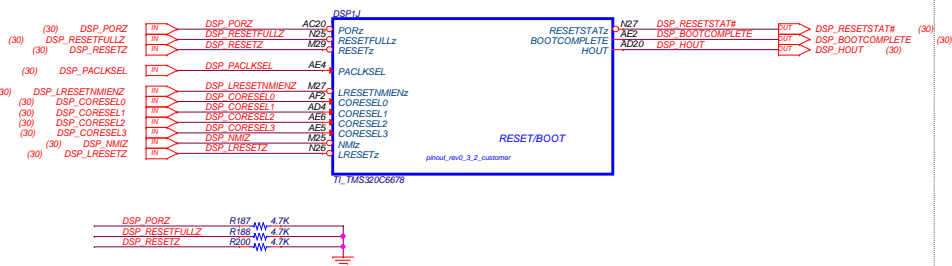
Ox50h/Ox51h



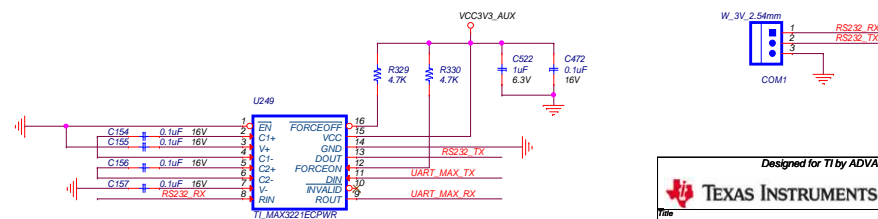
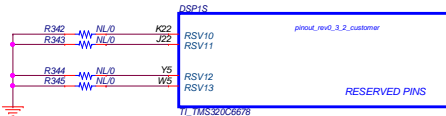
GPIO



Reset Control



Reserved



Designed for TI by ADVANTECH

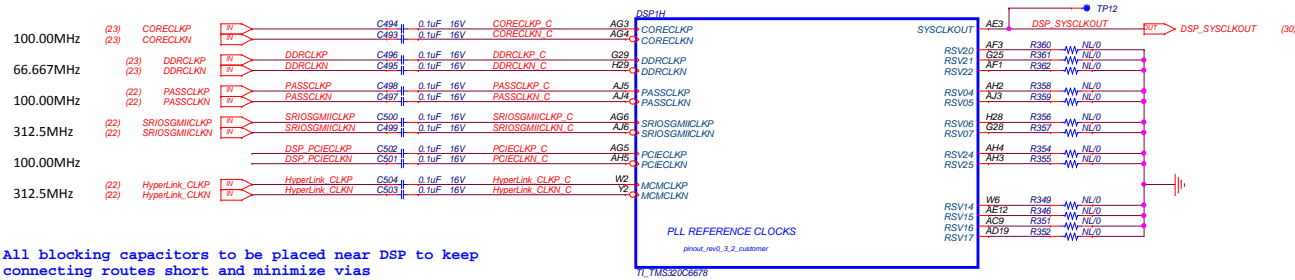
TEXAS INSTRUMENTS **ADVANTECH**

File: **DSP_MISC**

Size: **C** Document Number: **DSPM-8301E** Rev: **A104-1**

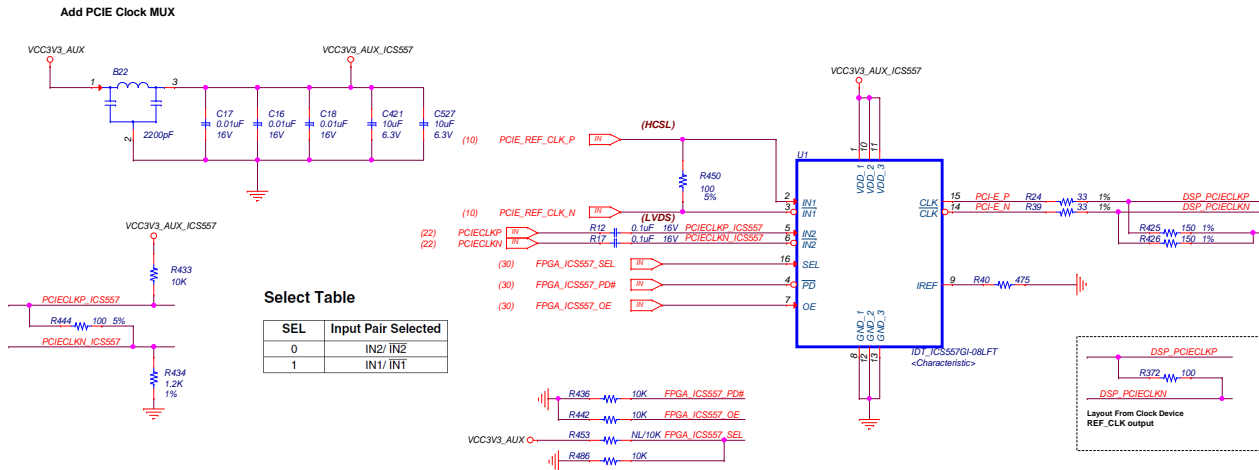
Date: Wednesday, March 07, 2012 Sheet: 16 of 40

DSP CLOCK

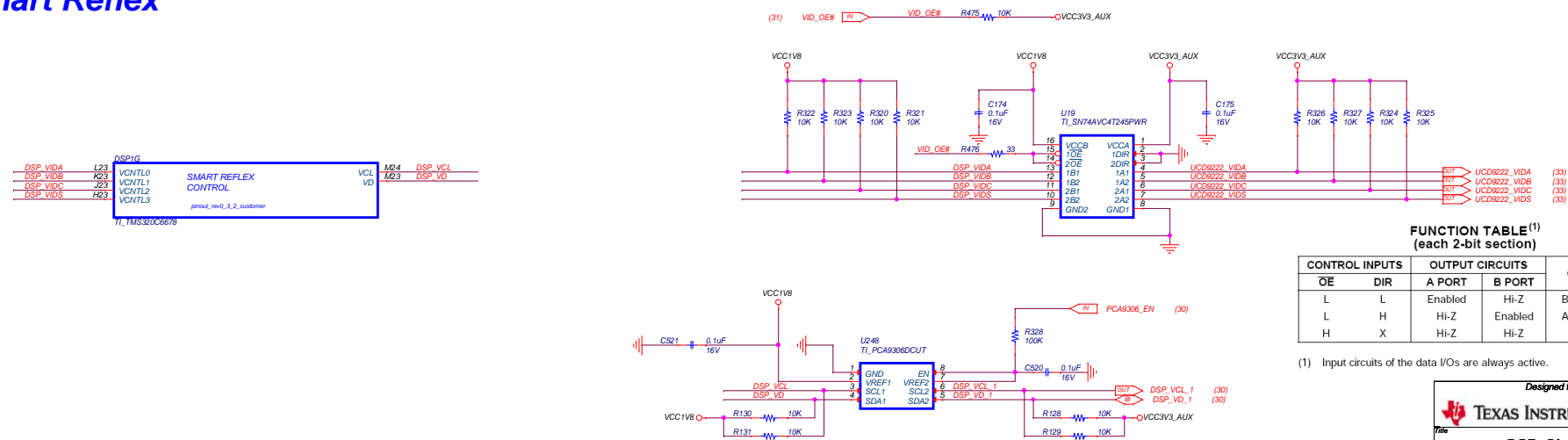


All blocking capacitors to be placed near DSP to keep connecting routes short and minimize vias

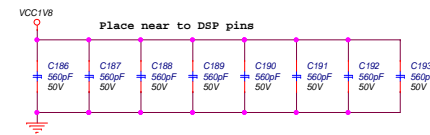
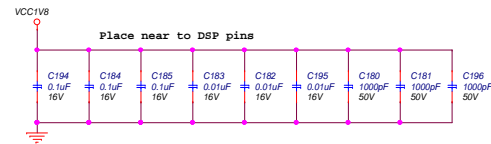
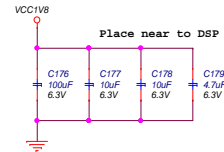
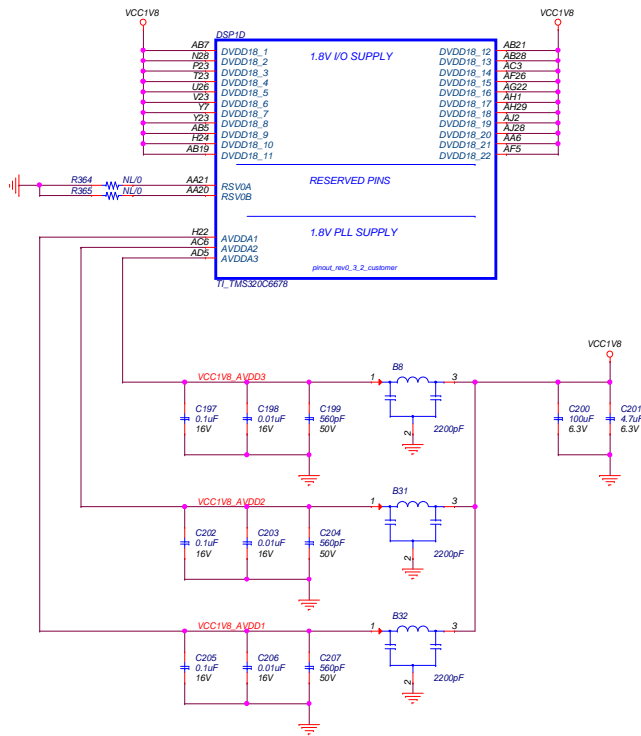
"All DC-blocking capacitors to be placed near DSP to keep connecting routes short and minimize vias"



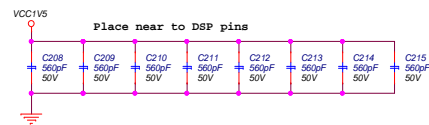
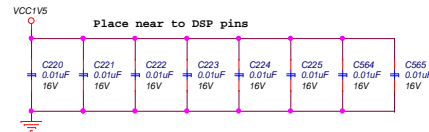
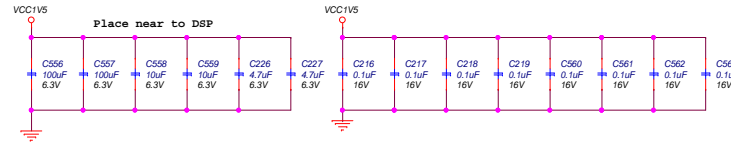
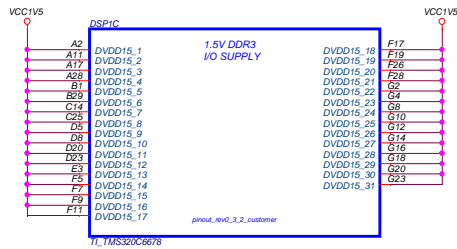
Smart Reflex



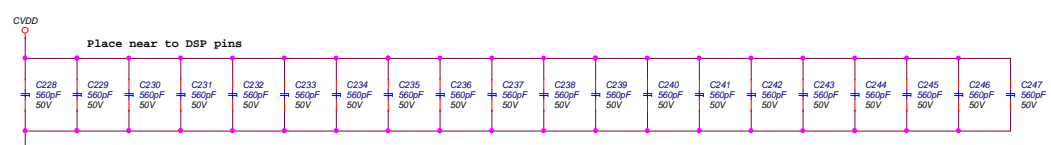
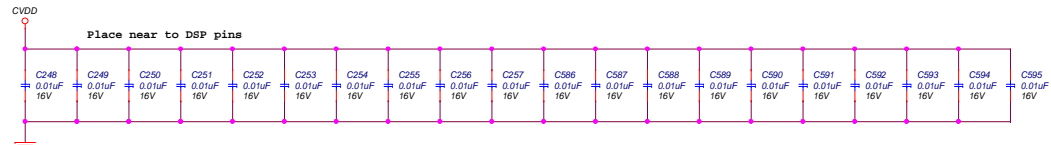
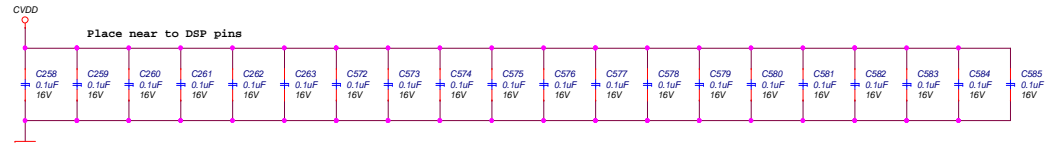
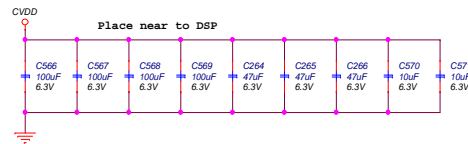
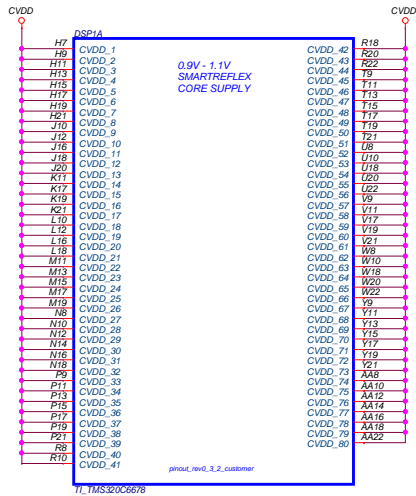
1.8V



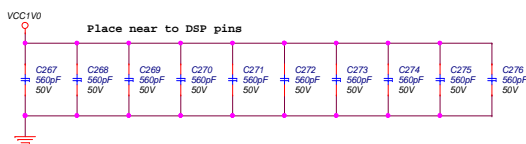
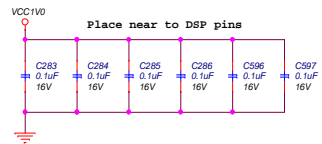
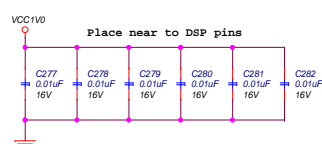
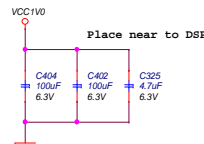
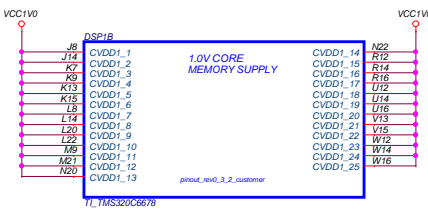
1.5V



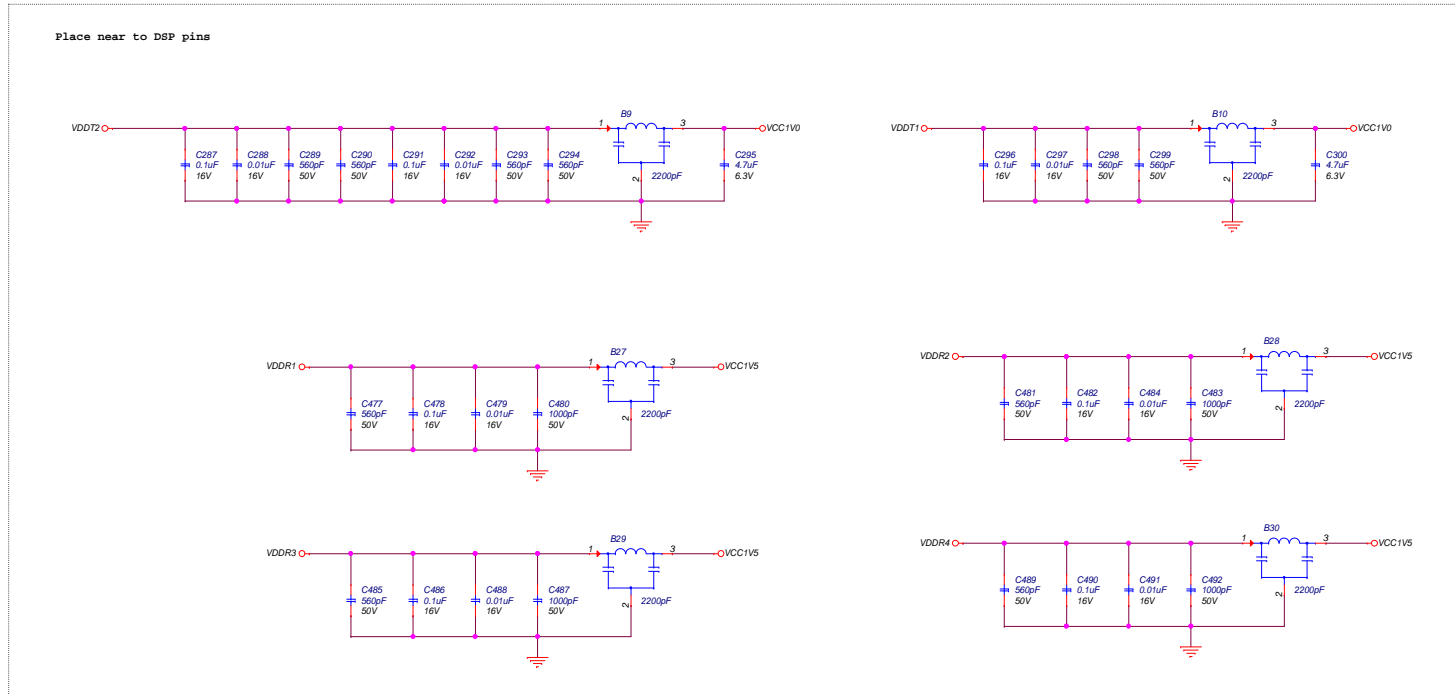
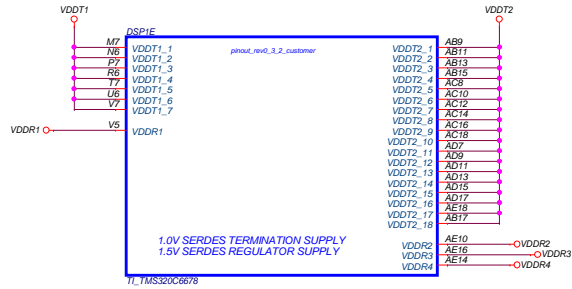
0.9V - 1.1V (Smart Reflex)

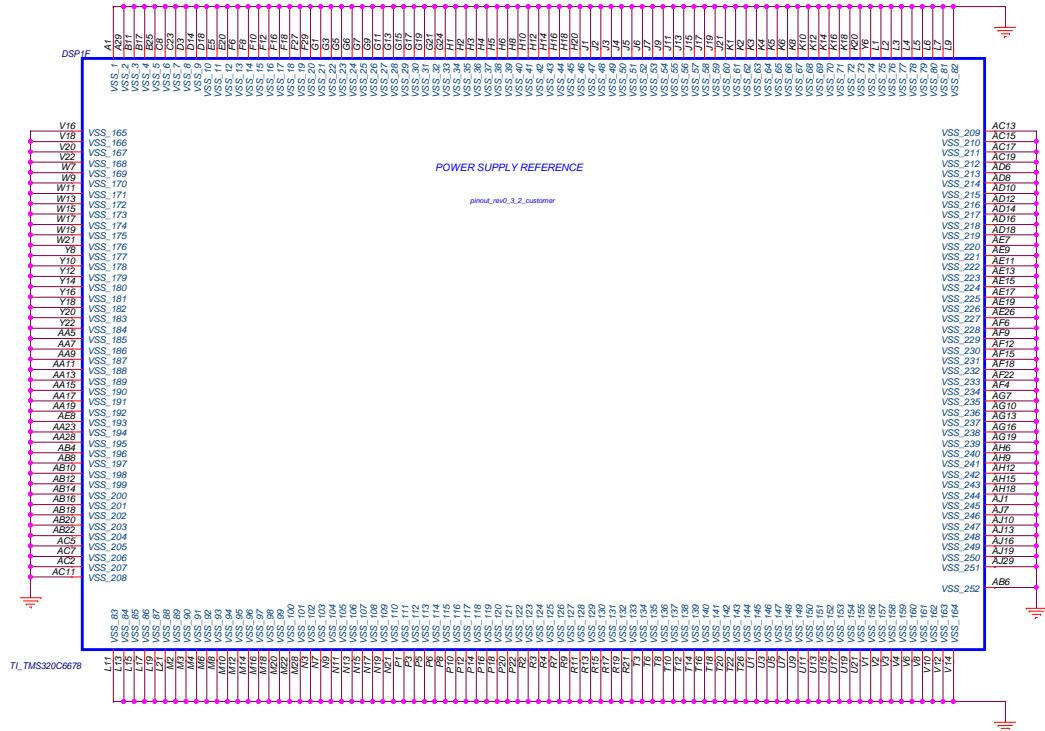


VCC1V0



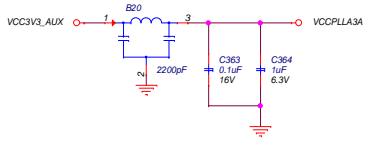
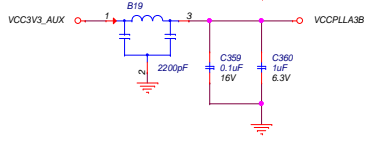
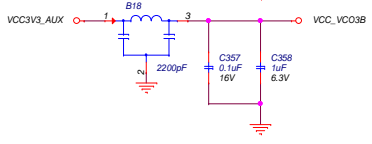
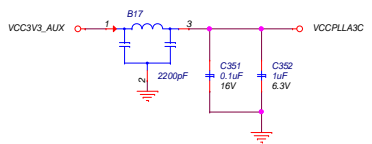
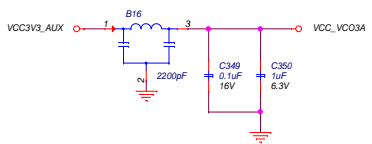
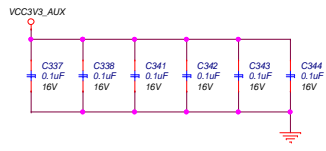
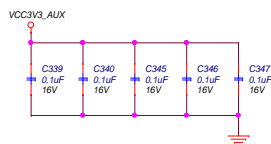
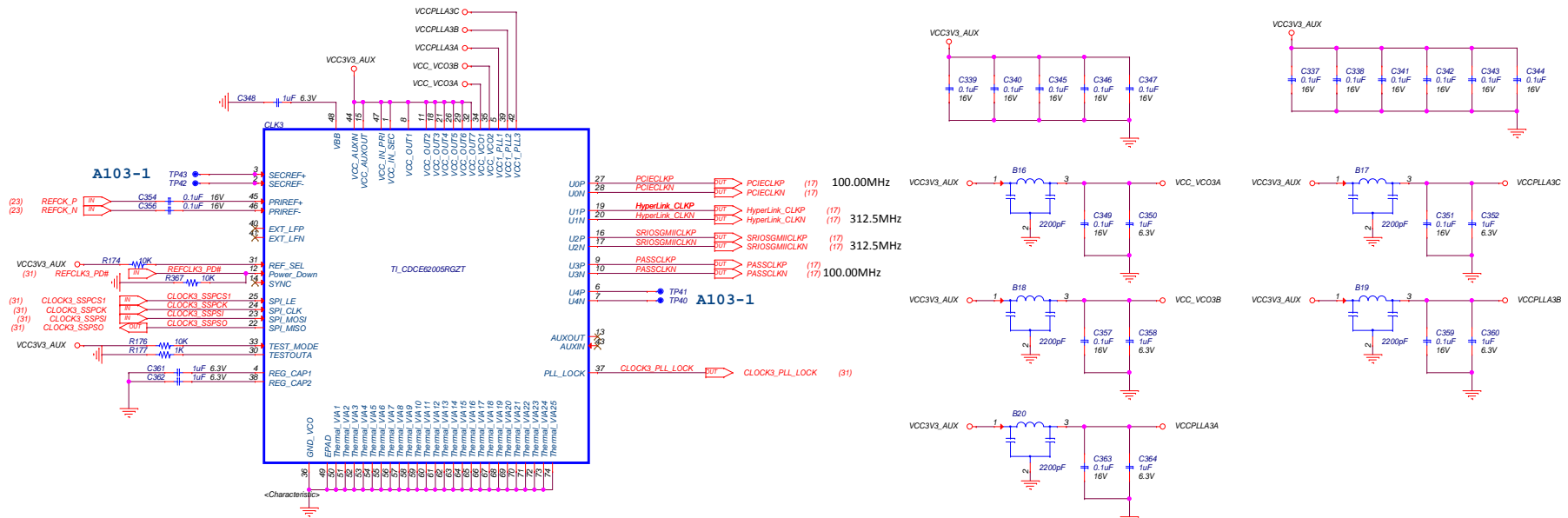
1.0V & 1.5V for Serdes



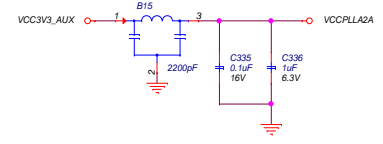
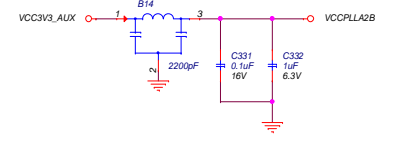
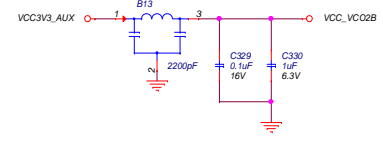
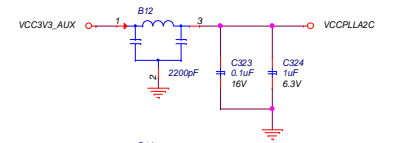
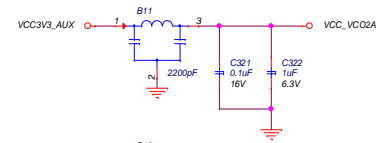
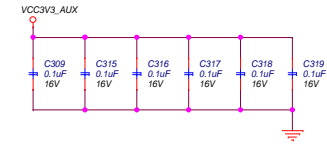
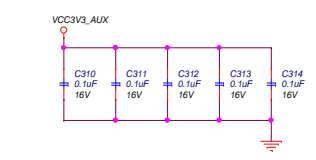
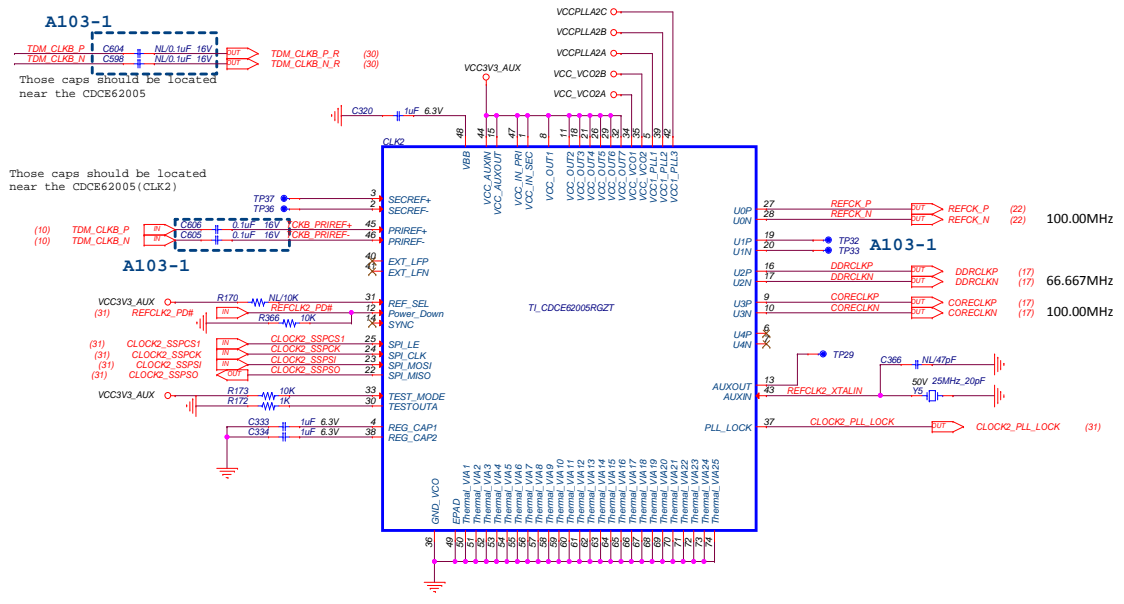


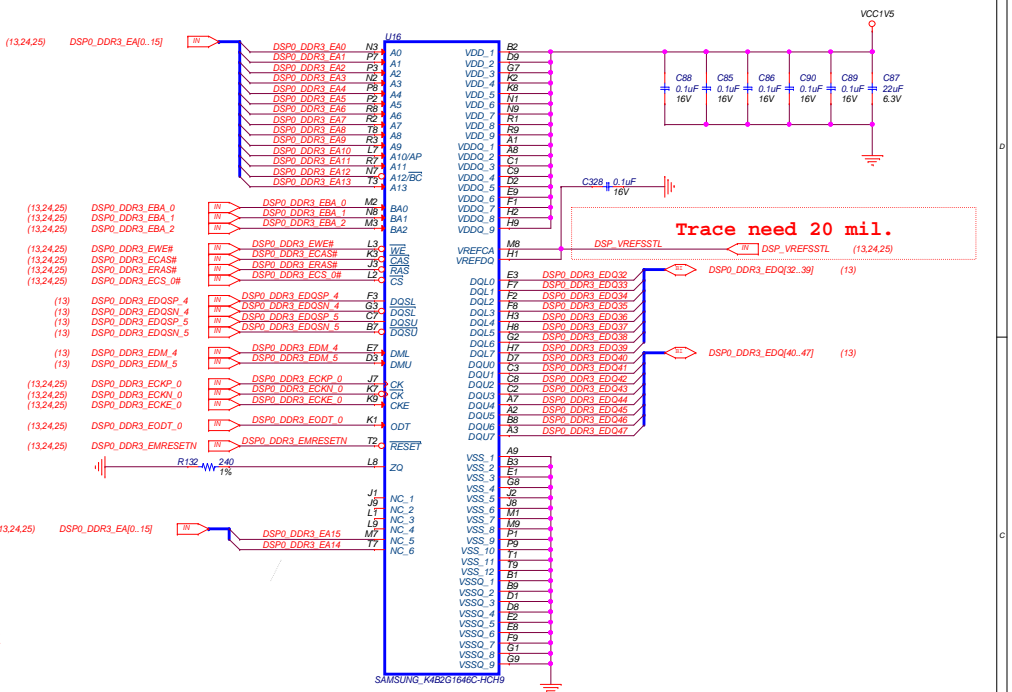
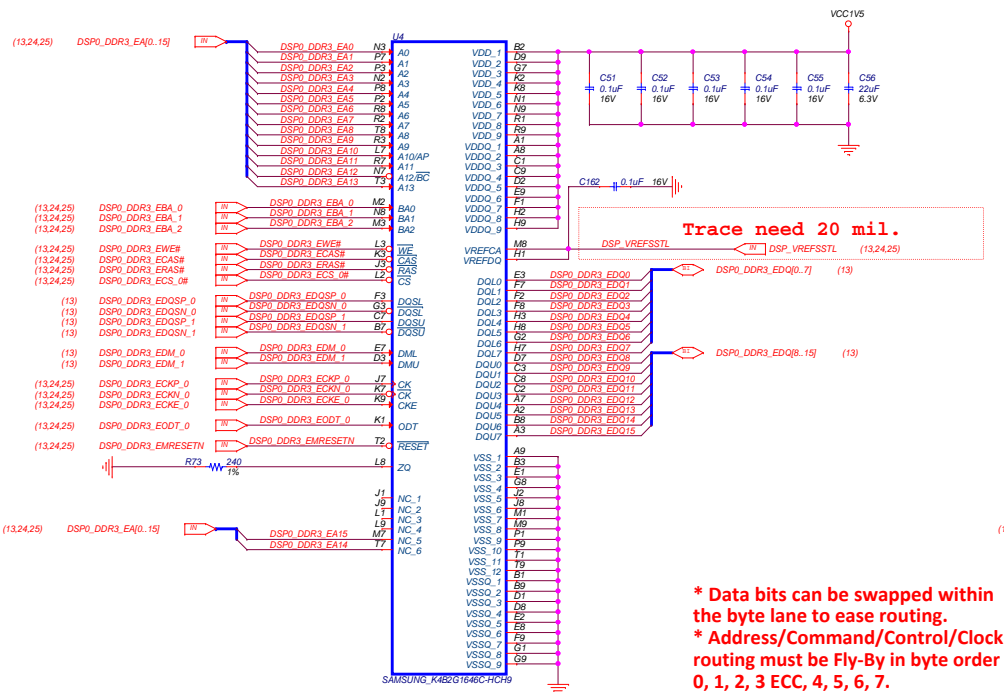
TI TMS320C6678

CLOCK GEN3

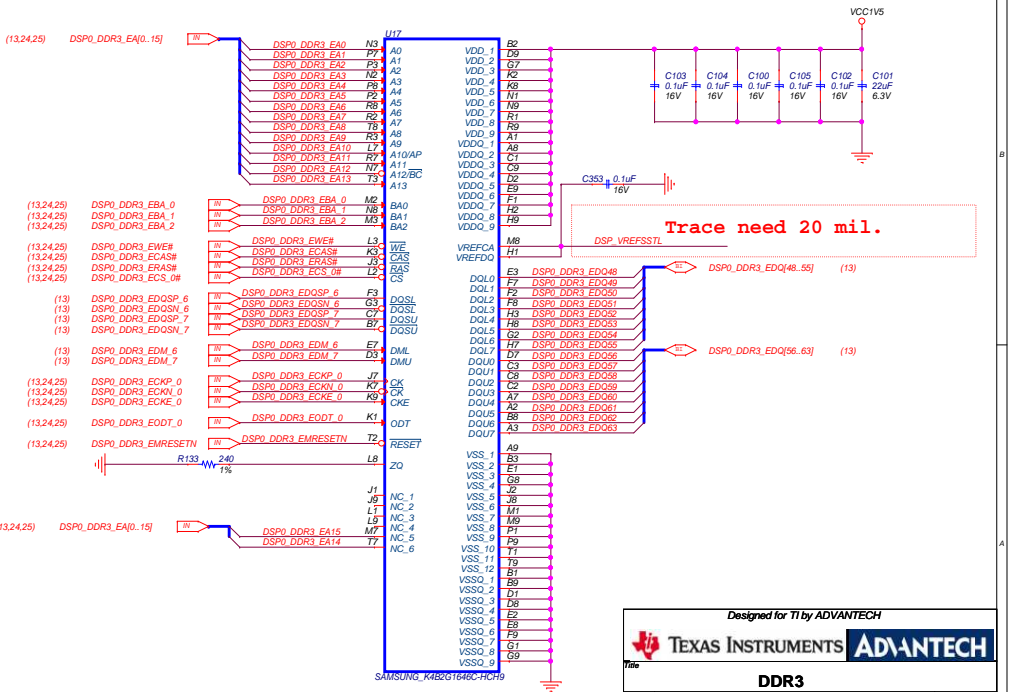
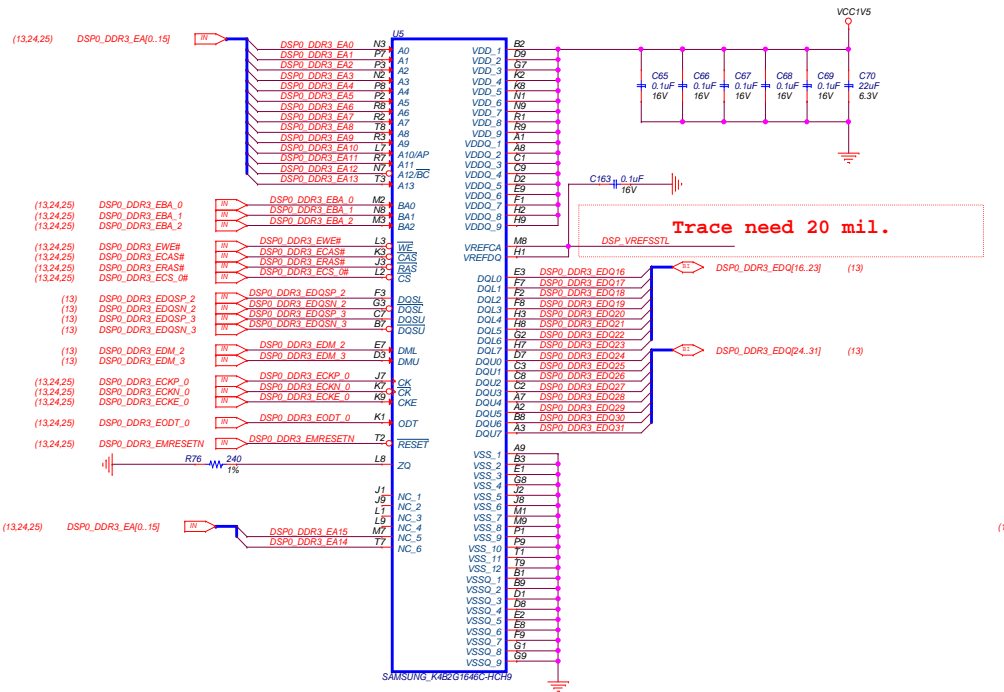


CLOCK GEN2



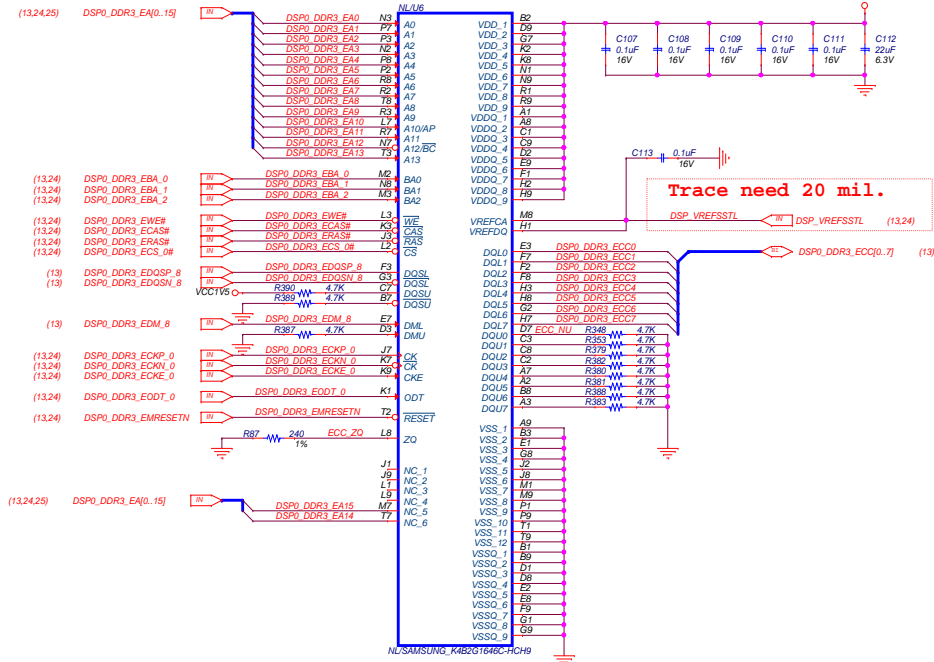
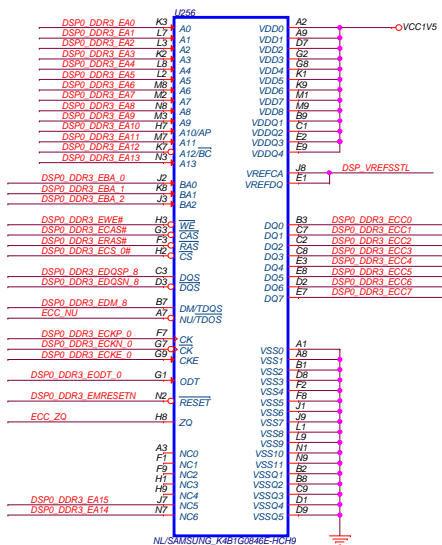


* Data bits can be swapped within the byte lane to ease routing.
 * Address/Command/Control/Clock routing must be Fly-By in byte order 0, 1, 2, 3 ECC, 4, 5, 6, 7.



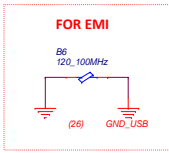
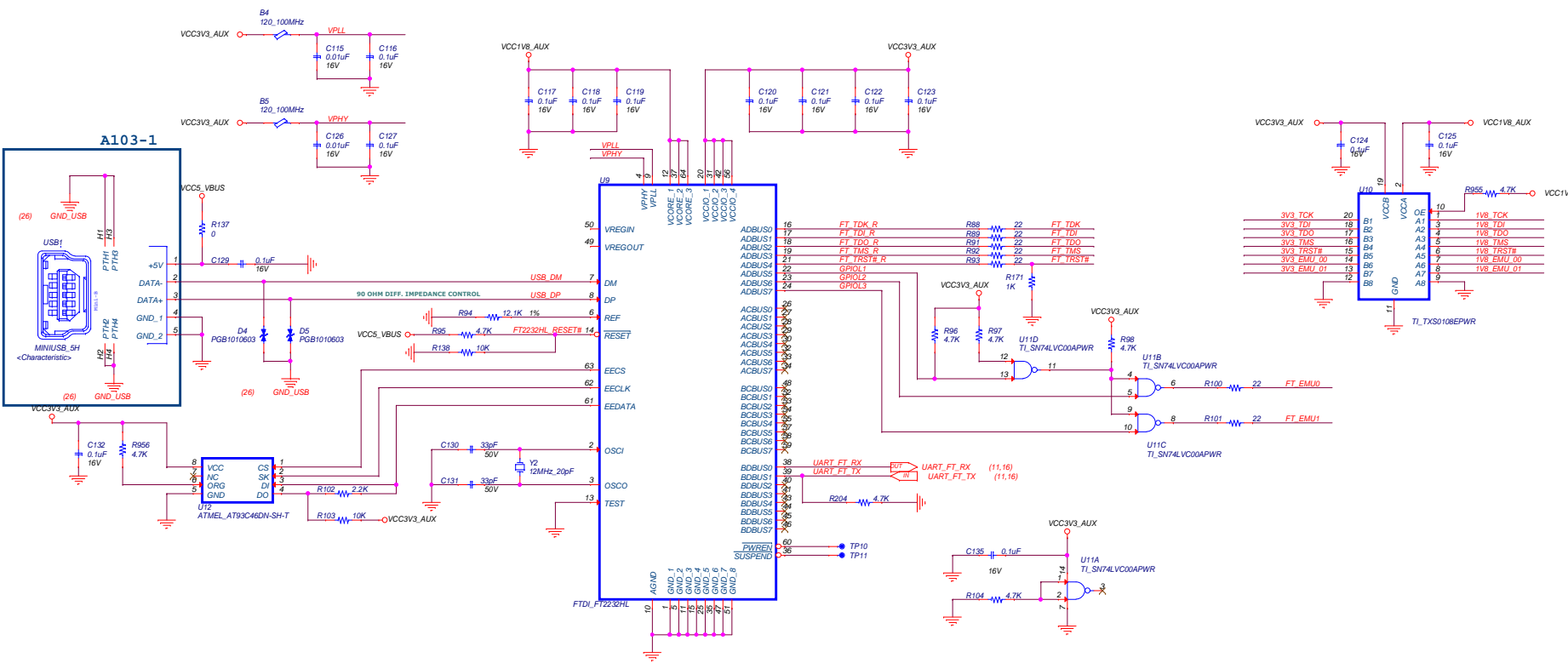
CO-LAYOUT

U4, U5, U16, U17, U8 change SAMSUNG_K4B2G1646C-HCH9



Trace need 20 mil.
DSP_VREFSSTL

1024MB: (2Gb, X16) 4pcs & (1Gb X8, ECC) 1pcs

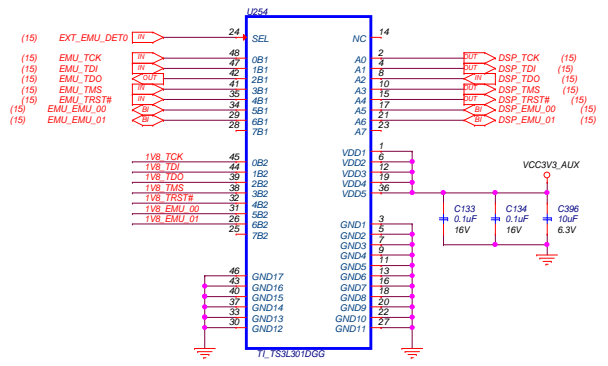
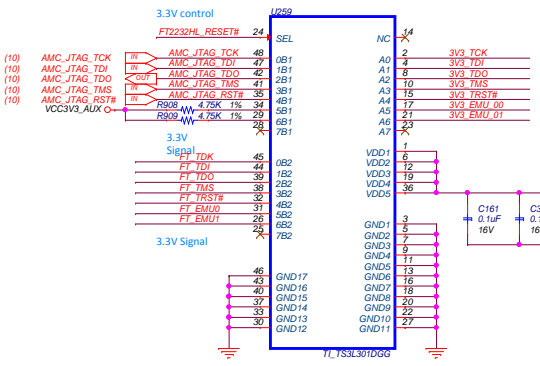


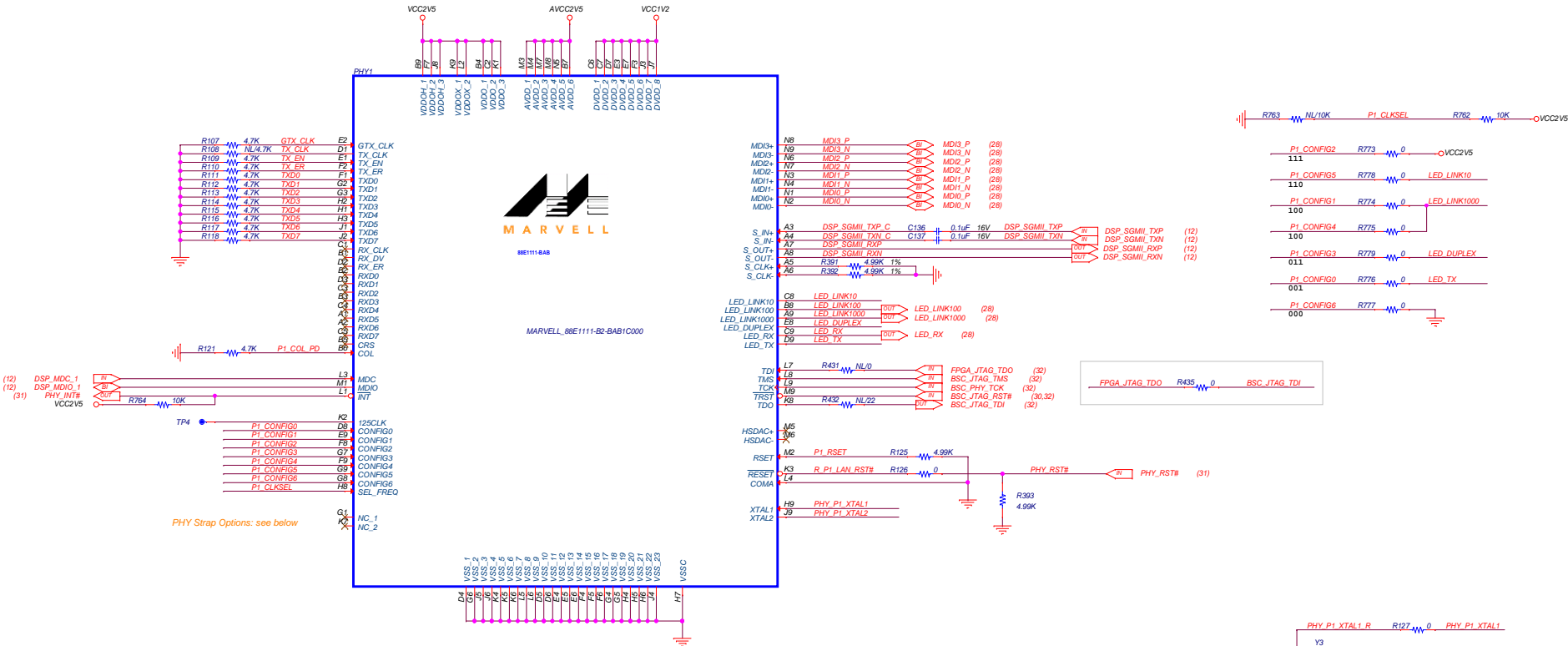
FUNCTION TABLE

INPUT SEL	INPUT/OUTPUT A _n	FUNCTION
L	nB ₁	A _n = nB ₁
H	nB ₂	A _n = nB ₂

Switch for JTAG emulation
 FT2232HL_RESET# = 0 --> AMC
 FT2232HL_RESET# = 1 --> Mini USB

Switch for JTAG emulation
 EXT_EMU_DET = 0 --> External / Mezzanine Emulator
 EXT_EMU_DET = 1 --> On board emulation





88E1111 Device Pin to Configuration Bit Mapping

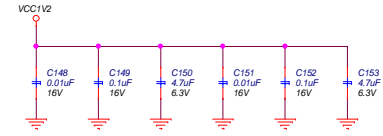
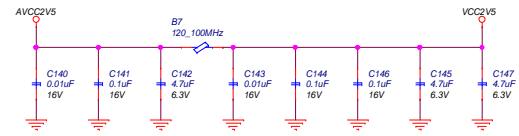
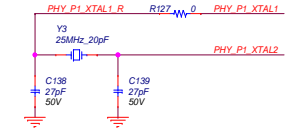
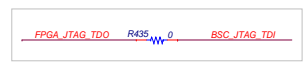
Pin	Bit[2]	Bit[1]	Bit[0]
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM

Pin to Constant Mapping

Pin	Bit[2:0]
VDDO	111
LED_LINK10	110
LED_LINK1000	101
LED_LINK10000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG Pin Connection

Pin	LED Pin Connection	Hardware Configuration Bit Setting	PHY Configuration
CONFIG0	001	LED_TX	PHY Address bit[2:0] 001
CONFIG1	100	LED_LINK1000	Enable Pause ,PHY Address bit[4:3] = 00
CONFIG2	111	VDDO	Auto-Neg advertise all capabilities, prefer Master
CONFIG3	011	LED_DUPLEX	Enable MDI crossover, disable 125CLK
CONFIG4	100	LED_LINK1000	SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	110	LED_LINK10	Disable fiber /copper Auto-detect, Disable sleep
CONFIG6	000	VSS	Select MDIO interface, INT signal active high, 50 ohm SERDES



Designed for TI by ADVANTECH

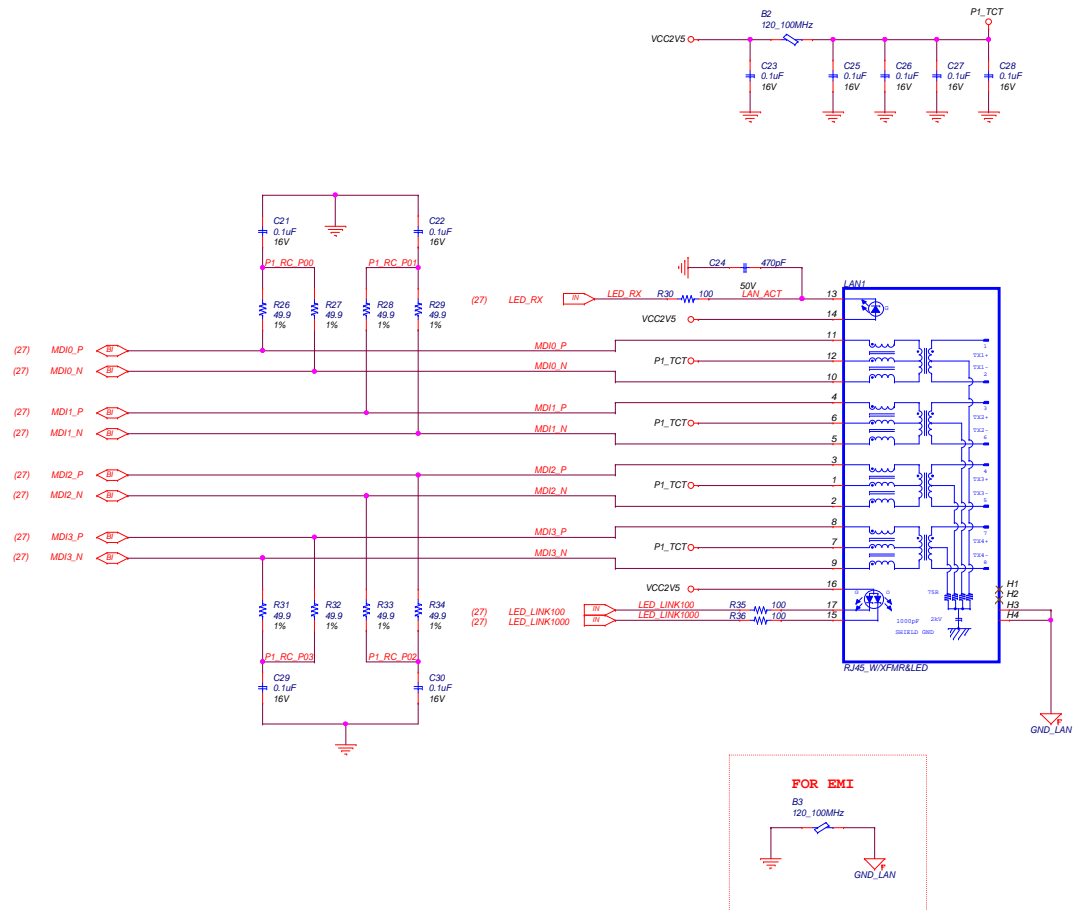
TEXAS INSTRUMENTS ADVANTECH

Gigabit Ethernet PHY

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Date: Wednesday, March 07, 2012 Sheet 27 of 40

RJ-45

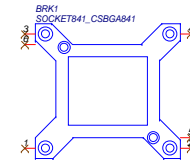
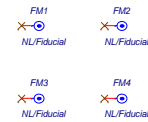


Heatsink Holes

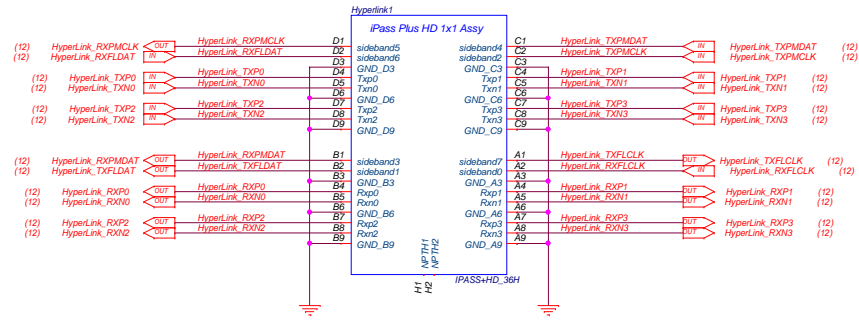


AMC Hole

On board

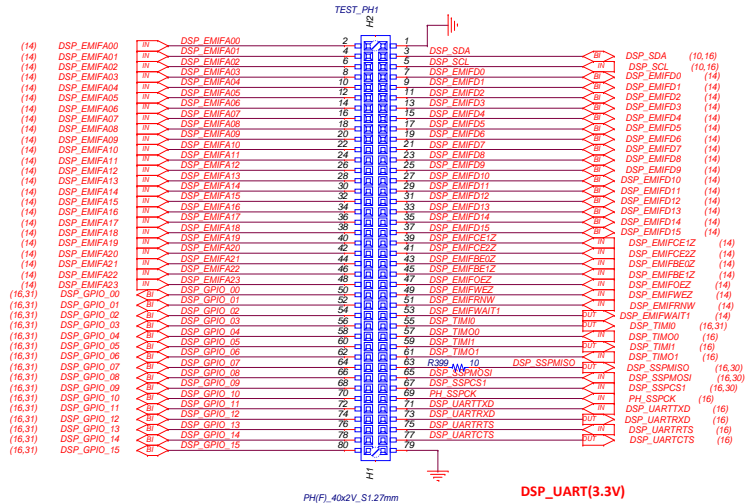


IPASS+HD for HyperLink Bus connection



Pin Header for debug

the interfaces on the 80-pin header are all 1.8V LVCMOS except for the UART which is 3.3V LVCMOS

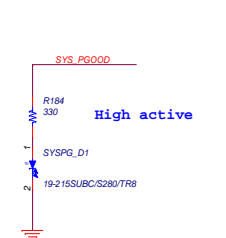
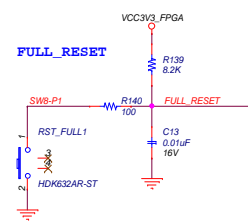
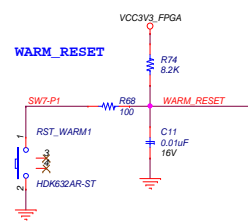
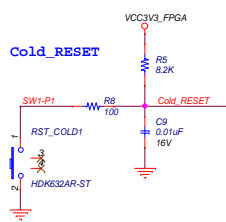
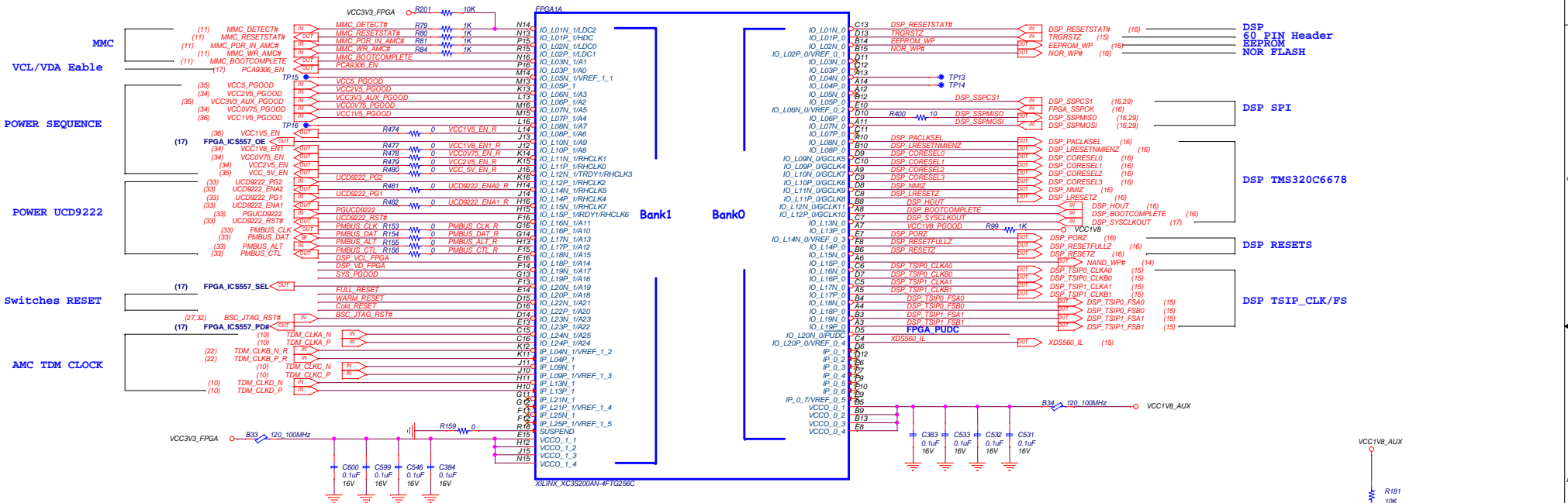


TDM_CLKA_P	R228	100	TDM_CLKA_N
TDM_CLKB_P_R	R317	100	TDM_CLKB_N_R
TDM_CLKC_P	R318	100	TDM_CLKC_N
TDM_CLKD_P	R319	100	TDM_CLKD_N

Place near to FPGA

Add three pins for the PCIECLK source selection on the MUX.

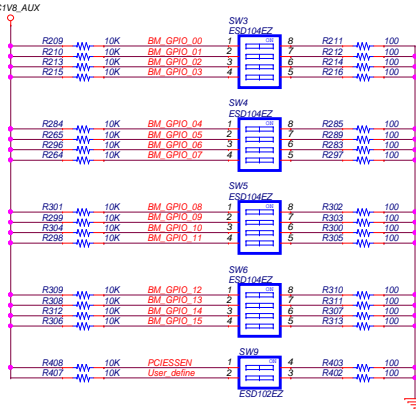
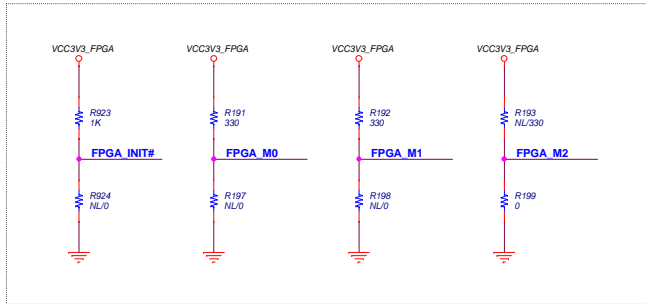
- a. FPGA_IC557_OE, pin.J13
- b. FPGA_IC557_PD#, pin.E13
- c. FPGA_IC557_SEL, pin.F13



FUDC:
User I/O Pull-Up Control. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank VCC0 input.
0: Pull-ups during configuration
1: No pull-ups

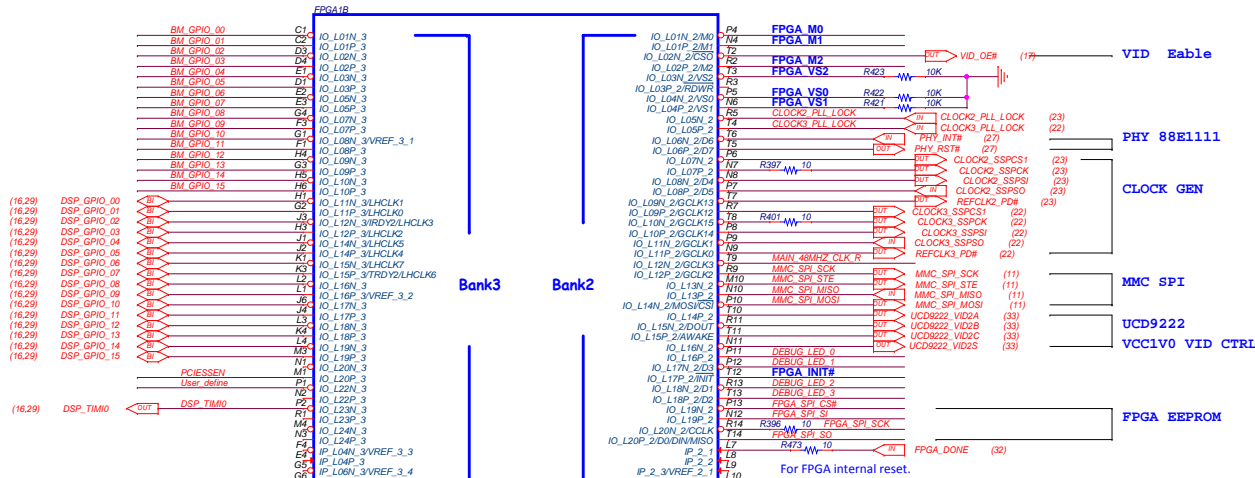
BOOT STRAP CONFIGURATION

default value : TBD

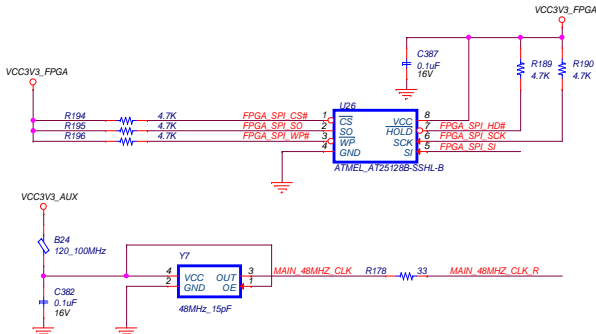
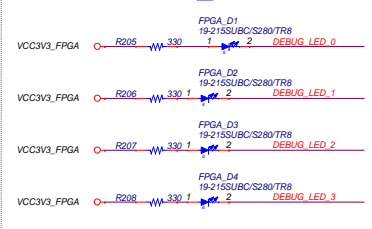


For BOOT MODE SWITCH

DSP GPIO TO FPGA



DEBUG_LED



Boot Configuration

DIP Switch	DSP	Boot Mode	Primary Function	
			Pull Up	Pull Down
BM_GPIO0	GPIO0	LENDIAN	Little Endian	Big Endian
BM_GPIO1	GPIO1	BOOTMODE00	Boot Device	
BM_GPIO2	GPIO2	BOOTMODE01	Boot Device	
BM_GPIO3	GPIO3	BOOTMODE02	Boot Device	
BM_GPIO4	GPIO4	BOOTMODE03	Device Cfg	
BM_GPIO5	GPIO5	BOOTMODE04	Device Cfg	
BM_GPIO6	GPIO6	BOOTMODE05	Device Cfg	
BM_GPIO7	GPIO7	BOOTMODE06	Device Cfg	
BM_GPIO8	GPIO8	BOOTMODE07	Device Cfg	
BM_GPIO9	GPIO9	BOOTMODE08	Device Cfg	
BM_GPIO10	GPIO10	BOOTMODE09	Device Cfg	
BM_GPIO11	GPIO11	BOOTMODE10	PLL Multiplier/I2C	
BM_GPIO12	GPIO12	BOOTMODE11	PLL Multiplier/I2C	
BM_GPIO13	GPIO13	BOOTMODE12	PLL Multiplier/I2C	
BM_GPIO14	GPIO14	PCIESSMODE0	Endpt/RootComplex	
BM_GPIO15	GPIO15	PCIESSMODE1	Endpt/RootComplex	

Boot Device

BM_GPIO	BOOT	Device	NOTE
3 2 1	0	EMIF16	
0 0 1	0	sRIO	
0 1 0	0	SMGII	PA driven from core clk
0 1 1	0	SGMII	PA driver from PA clk
1 0 1	0	I2C	
1 1 0	0	SPI	
1 1 1	0	HyperLink	

Device Configuration

BM_GPIO	Device Configuration Field	The device configuration fields GPIO[10:4] are used to configure the boot peripheral and, therefore, the bit definitions depend on the boot mode.
[10:4]		

PLL Settings

BM_GPIO	INPUT	CLK (MHz)	CorePac System PLL Configuration
13 12 11	0	50.00	
0 0 0	0	66.67	
0 1 0	0	80.00	PA driven from core clk
0 1 1	0	100.00	PA driver from PA clk
1 0 0	0	156.25	
1 0 1	0	250.00	
1 1 0	0	312.50	
1 1 1	0	122.88	

PCIe Mode selection (PCIESSMODE[1:0])

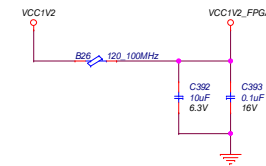
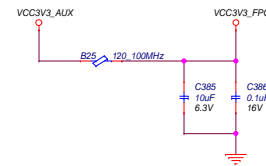
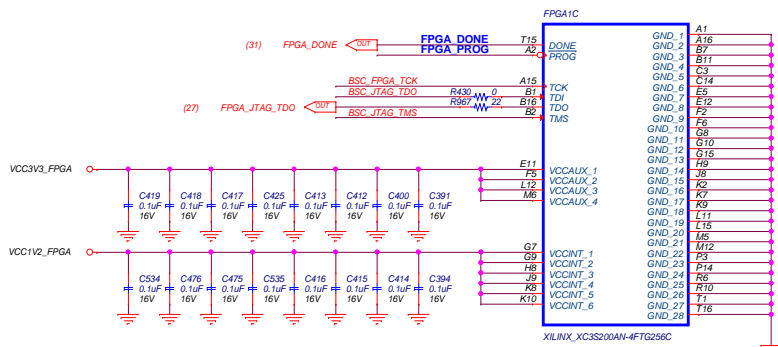
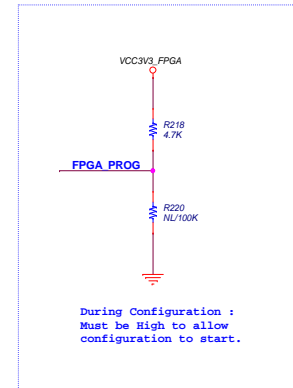
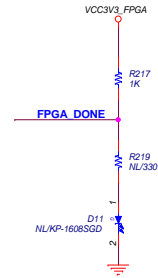
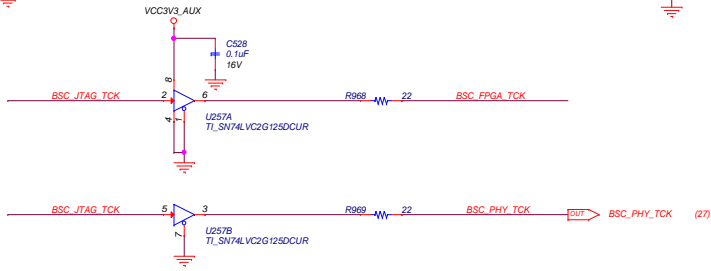
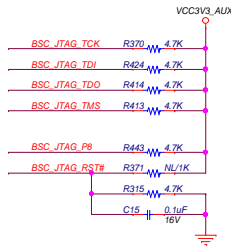
BM_GPIO [15:14]	INPUT	Description
00b		PCIe in End-point mode
01b		PCIe in Legacy End-point mode(no support for MSI)
10b		PCIe in Legacy Root complex mode

PCIESSSEN

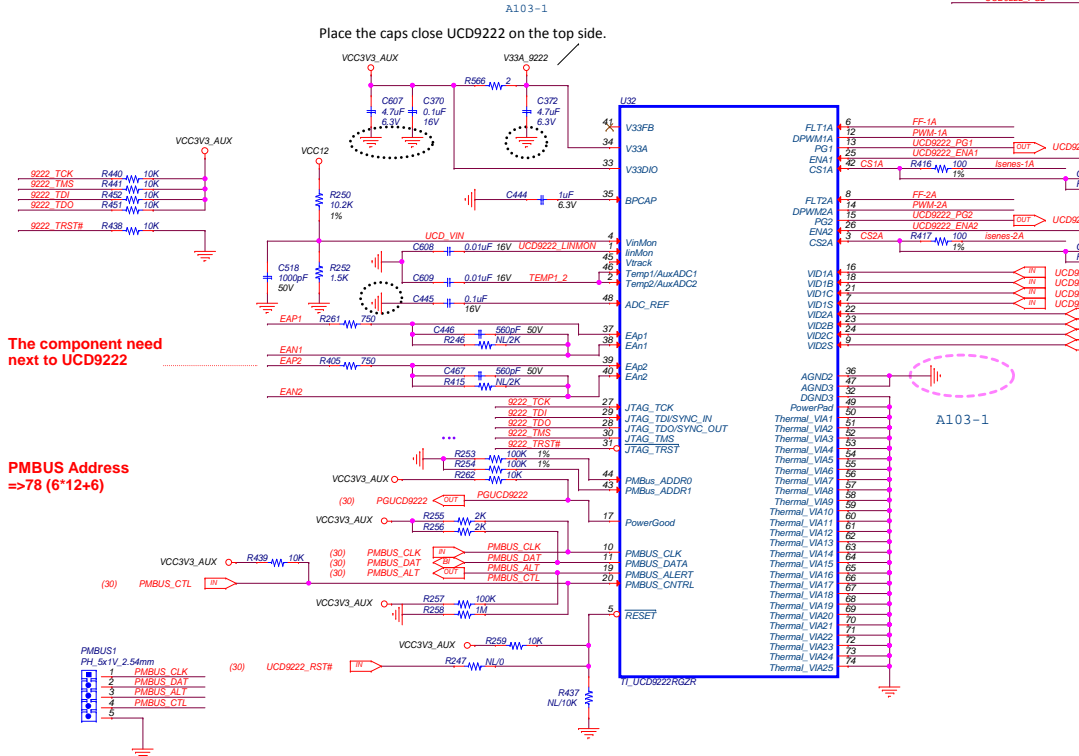
Input	Description
0	Initial state of the power domain and the clock domain for PCIe subsystem is disabled
1	Initial state of the power domain and the clock domain for PCIe subsystem is enabled

- a. Remove the boundary scan chain from UCD9222.
- b. Remove bus switch and loop in the FPGA and PHY .

TAP_FPGA1
PH_8x1V,2.54mm



CVDD / VCC1V0



The component need next to UCD9222

PMBUS Address =>78 (6*12+6)

+++output capacitor Calculation for VCC1V0+++

$$V_{PPQ} \approx \frac{\Delta I}{8 \times C \times f_s}$$

(VPPQ=10mV)

$$C = 5 / (10m \times 8 \times 750k)$$

$$C = 83.3\mu F$$

1.0V@ 5A

+++Inductor Calculation for VCC1V0+++

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \frac{D}{f_s}$$

$$L = (12 - 1) / 5 * (1/12) / 750k$$

$$L = (11 / 5) * (0.083 / 750k)$$

$$L = 0.243 \mu H$$

DSP Vcore @8A

+++Inductor Calculation for CVDD+++

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \frac{D}{f_s}$$

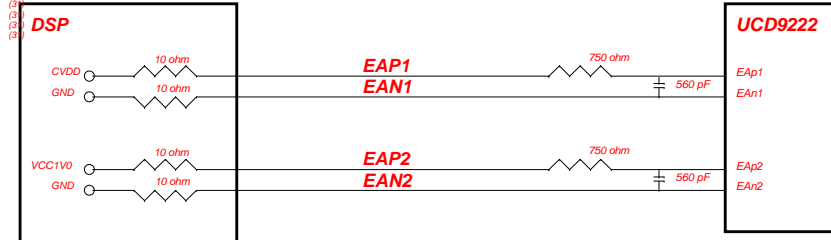
$$L = (12 - 1) / (8) * (1/12) / 750k$$

$$L = (11 / 8) * (0.083 / 750k)$$

$$L = 0.152 \mu H$$

PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	205
10	178
9	154
8	133
7	115
6	100
5	86.6
4	75
3	64.9
2	56.2
1	48.7
0	42.2
SHORT	--



Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

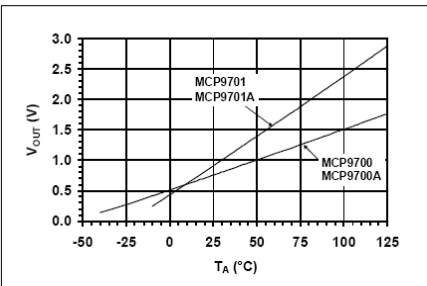
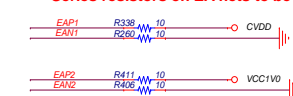


FIGURE 2-16: Output Voltage vs. Ambient Temperature.

+++output capacitor Calculation for VCC1V0+++

$$V_{PPQ} \approx \frac{\Delta I}{8 \times C \times f_s}$$

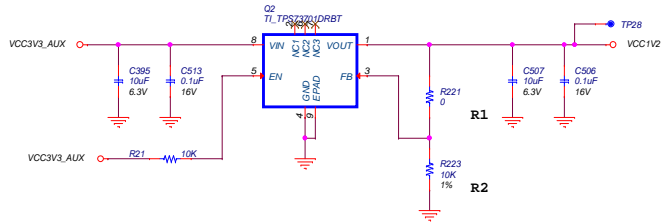
(VPPQ=10mV)

$$C = 8 / (10m \times 8 \times 750k)$$

$$C = 133.3\mu F$$

VCC1V2

1.2V @0.38A

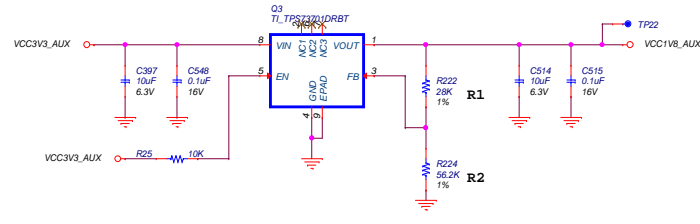


$$V_{out} = (R1+R2) / R2 * 1.204$$

$$1.204V = (0+10k) / 10k * 1.204$$

VCC1V8_AUX

1.8V_AUX @0.3A

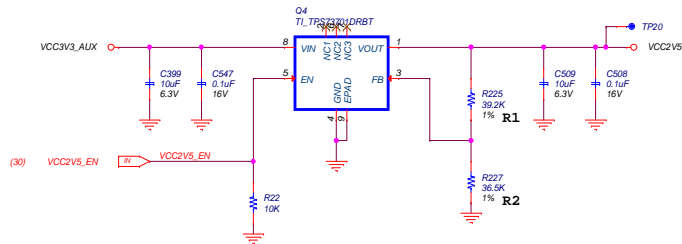


$$V_{out} = (R1+R2) / R2 * 1.204$$

$$1.805V = (28k+56.2k) / 56.2k * 1.205$$

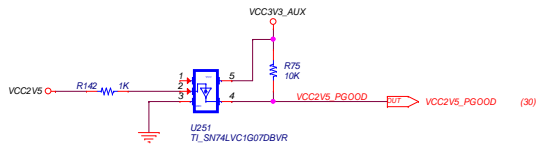
VCC2V5

2.5V @0.21A



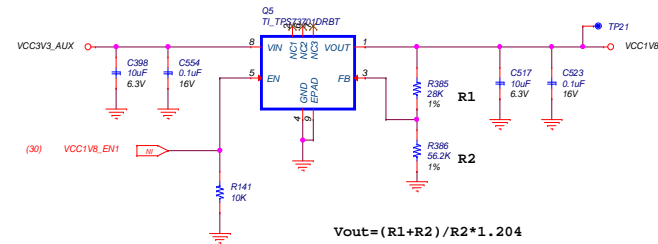
$$V_{out} = (R1+R2) / R2 * 1.204$$

$$2.50V = (39.2k+36.5k) / 36.5k * 1.204$$



VCC1V8

1.8V@0.5A

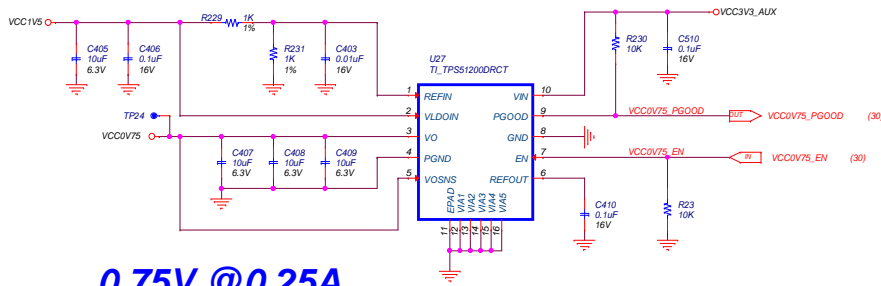


$$V_{out} = (R1+R2) / R2 * 1.204$$

$$1.805V = (28k+56.2k) / 56.2k * 1.205$$

VCC0V75

0.75V @0.25A

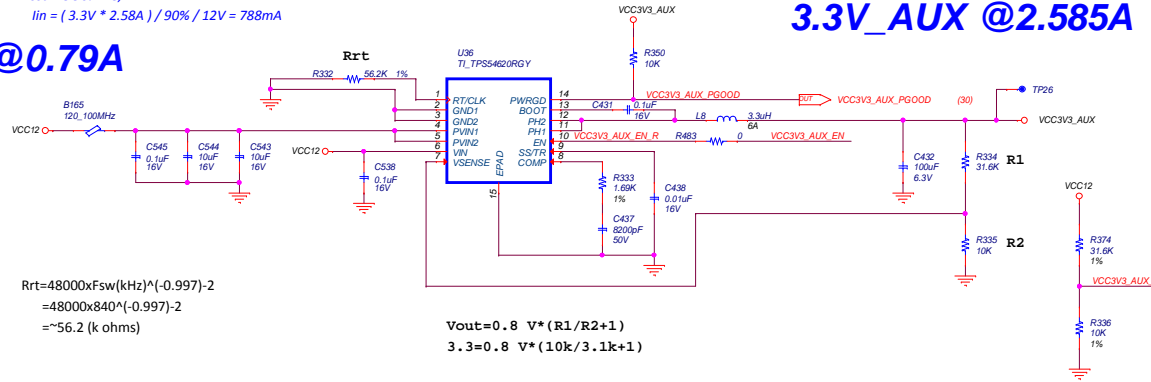


VCC3V3_AUX

Assume 90% Pe,
 $I_{in} = (3.3V * 2.58A) / 90\% / 12V = 788mA$

12V@0.79A

3.3V_AUX @2.585A



$$R_{rt} = 48000 \times F_{sw}(\text{kHz})^{(-0.997)-2}$$

$$= 48000 \times 840^{(-0.997)-2}$$

$$= \sim 56.2 \text{ (k ohms)}$$

$$V_{out} = 0.8 \text{ V} * (R1/R2 + 1)$$

$$3.3 = 0.8 \text{ V} * (10k / 3.1k + 1)$$

(Over all tolerance is 5%, DC tolerance is 2.5%)

+++output capacitor Calculation+++
 $C_{out} > (2 * \Delta I_{out}) / (F_{sw} * \Delta V_{out})$
 $C_{out} > (2 * 3) / (840kHz * 0.0825)$
 $C_{out} > \sim 87\mu F$

Reference Capacitor=100uF

(KIND=0.3)

+++Inductor Calculation+++
 $L = (V_{in} - V_{out}) / (I_{out} * Kind) * (V_{out} / (V_{in} * F_{sw}))$
 $L = ((12 - 3.3) / (3A * 0.3)) * (3.3 / (12 * 840kHz))$
 $L = 9.67 * 0.33\mu$
 $L = \sim 3.2 \text{ uH}$

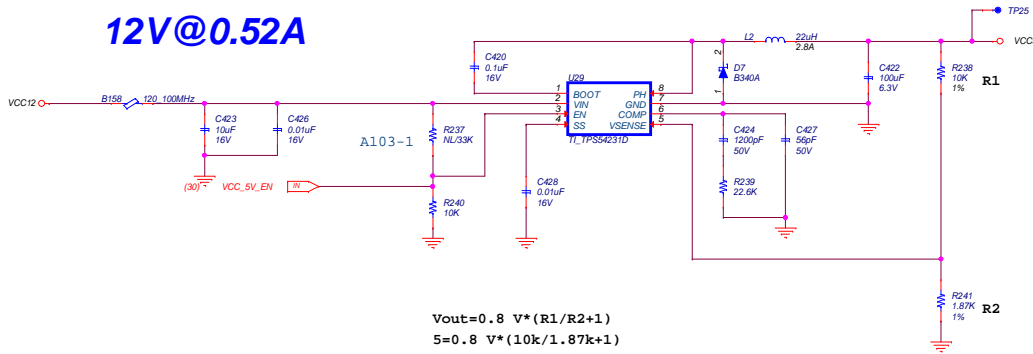
Reference Inductor 3.3uH

VCC5

Assume 80% Pe,
 $I_{in} = (5V * 1A) / 80\% / 12V = 520mA$

12V@0.52A

5V @1A



$$V_{out} = 0.8 \text{ V} * (R1/R2 + 1)$$

$$5 = 0.8 \text{ V} * (10k / 1.87k + 1)$$

+++output capacitor Calculation+++

$$C_{o_min} = 1 / (2 * \pi * R_o * F_{CO_max})$$

$$C_{out} = 1 / (2 * 3.14 * 5 * 25K)$$

$$C_{out} = 1.3 \text{ uF}$$

Reference Capacitor=100uF

+++Inductor Calculation+++

(KIND=0.3)

$$L = ((V_{in(max)} - V_{out}) / I_{out} * Kind) * (V_{out} / (V_{in(max)} * F_{sw}))$$

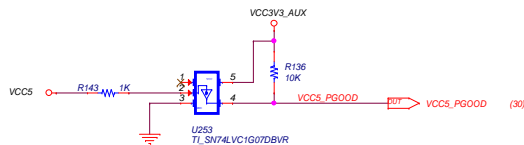
$$L = ((12.6 - 5) / 1 * Kind) * (5 / (12.7 * 570K))$$

$$L = ((7.6 / 0.3)) * (5 / (7239K))$$

$$L = (25.3) * (0.69M)$$

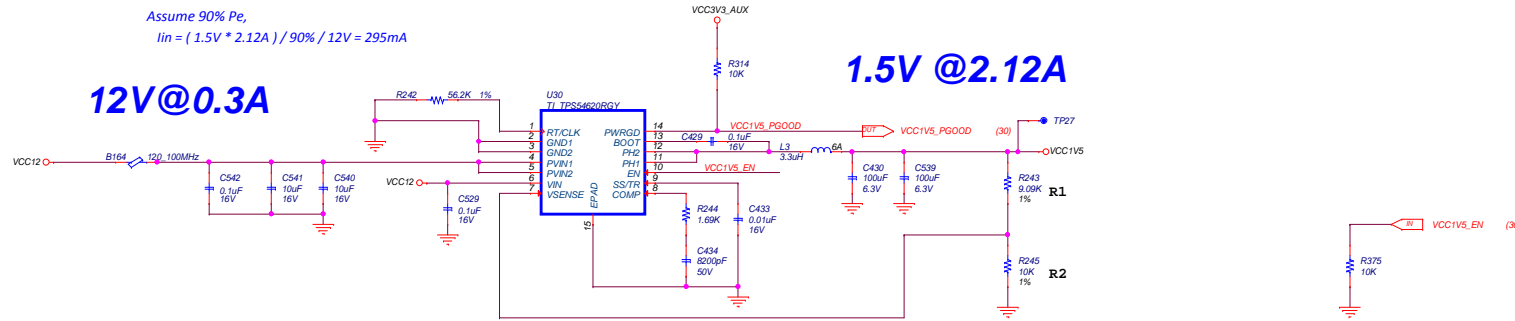
$$L = 17.5\mu H$$

Reference Inductor 22uH



VCC1V5

Assume 90% Pe,
 $I_{in} = (1.5V * 2.12A) / 90\% / 12V = 295mA$



$$V_{out} = 0.8 V * (R1/R2 + 1)$$

$$1.52 = 0.8 V * (9.09k/10k + 1)$$

(Over all tolerance is 5% ,DC tolerance is 2.5%)

(KIND=0.3)

+++output capacitor Calculation+++

$$C_{out} = (2 * \Delta I_{out}) / (F_{sw} * \Delta V_{out})$$

$$C_{out} = (2 * 2.5A) / (840kHz * 0.0375)$$

$$C_{out} \sim 159\mu F$$

Reference Capacitor=200uF

+++Inductor Calculation+++

$$L = (V_{in} - V_{out}) / (I_{out} * Kind) * V_{out} / (V_{in} * F_{sw})$$

$$L = (12 - 1.5) / (2.5A * 0.3) * 1.5 / (12 * 840kHz)$$

$$L \sim 2.08\mu H$$

Reference Inductor 3.3uH

History

DSPM-8301 A101-1 / 19C2830100

Jan.24.2011:

1. BOM change list: (ECOP-078102)

- a. MMC enable pin: remove R11, populate R16.
- b. DDR3 slew rate setting: remove R72, populate R70.
- c. VCC5_AUX enabled by FPGA: remove R237.
- d. Change I2C serial EEPROM for the 50h & 51h of address.
 - d.1 Change I2C EEPROM to STMicro_M24M01-HRMN6TP.
 - d.2. remove R164.
- e. Change COM1 pin header to the connector with lock.

2. Schematics change list:

- a. Update Block, Sequences, Clock diagrams.
- b. Correct the MCMRX sideband pins to output and the MCMTX sideband pins to input.
- c. Change the note 'NL/' on R235 (RSVD09), populating R234 (RSVD08).

3. FPGA code change list:

- a.1 De-assert PORz first and de-assert RESETFULLz after for DSP reset sequence.
- b. Change DSP clockings: CORECLK = PASSCLK = 100MHz, PCIECLK = 100MHz
- b. Boot mode change to I2C EEPROM and none-boot mode.
- d. All reset behaviours on the board are defined.

DSPM-8301 A102-1 / 19C2830101

1. Add the JTAG connection on AMC edge connector .
2. Remove the SW2, R9, C10, R12, R17 for LEDs re-placement.
3. Change I2C EEPROM (128kB) to M24M01-HRMN6TP and its footprint.
4. Change COM_SEL1 to DIP type and COM1 with lock.
5. Add a clock MUX to select the DSP PCIECLK source from the AMC FCLK or CDCE62005.
6. Change DDR3 1333 to 1600 by the Micron 1G X16.
7. Modify the boundary scan loop and remove the JTAG connections from the UCD9222 portion.
8. Change the PMBUS1 to 5Pin/2.54mm connector
9. UCD9222 changes:
 - a. Add a 10k pull-up resistor on the PMBUS_CTL and DNI it.
 - b. Add a 10k pull-down resistor on the JTAG_TSRT.
 - c. Remove the JTAG pins on the UCD9222 from the boundary scan chain.
 - d. Add a 10k pull-down resistor on the UCD9222_RST# and DNI it.
 - e. Separate analog GND to digital GND.
10. Add test points on all power rails.
11. Remove R443 on the PCIECLK to the DSP, put all terminations next by PCIECLK MUX.
12. Install R440 on 9222_TCK, install R439 on PMBUS_CTL, might have a new firmware loading into the UCD9222 for the Beta2 and production units.
13. Pull down the BSC_JTAG_RST# for normal operation of phy.
14. Add H5 for AMC spec
15. Add pull up resistor (R908, R909) to the inputs to the switch so that these signals are held high when the AMC JTAG interface is selected.

16. Add 22-ohm series termination resistors at the outputs MCMTXPMCLK and MCMRXFLCLK which are HyperLink sideband signal clock outputs.

17. Add a temperature monitor to the unused TEMP2 input to the UCD9222

18. Add 4.7K pull-down resistors on the GPIO[15:1] pins and a 4.7K pull-up resistor on GPIO[0] so that these pins are not floating after FPGA release.

19. Replace the 14-pin JTAG with the Spy-Bi-Wire interface .

20. Add 0 Ohm resistors on all power enable signals.

21.ADD R485 for DSP UARTTXD termination

22.DSP_PCIECLOCK was set from IN2.

23.Change R425 and R426 package from 0603 to 0402.

24.Change R58 package from 0603 to 0402.

25. To modify the title from CLOCK GEN1 to CLOCK GEN3

26. Change net name from Isenes-2A to isenes-2A

27. U4, U5, U16, U17 U8 change to SAMSUNG_K4B1G1646G

28. NL/U8

29. NL/R431, NL/R432, Add R435

DSPM-8301 A103-1 / 19C2830102

1. Page26: Change mini-USB to through-hole type

2. Page13: Change the registers value to 2k ohms and the pull-up voltage to IO 1.8V on the DDR3 slew rate pins

3. Page22,23: Add the test points on unused clock inputs and outputs of CDCE62005s

4. Page10: Enable the expansion I2C by default, populate the registers of R160 and R161 for I2C connections between C6678 and AMC finger

5. Page23: Modify the CLK2 (CDCE62005) inputs for the common HyperLink timing,TCLKB will be the PRI_REF input and branch another one to the FPGA by two pairs. The 100MHz input from CLK3 CDCE62005 will be changed to its SEC_REF input.

6. AGND change to GND

7. Leave R160 and R161 as NL and add 2 more resistors on these nets connecting to AMC connector pins 159 and 160. Install 0 ohms in these new resistors

DSPM-8301 A104-1 / 19C2830103

1. Remove R484 and R487 and cross-wire these signals to make the connections functionally match the C6670 EVMs

2. Change R433 to 10k, change R434 to 1.2k, change R12 and R17 from 0 ohm to 0.1uF

Designed for TI by ADVANTECH



TEXAS INSTRUMENTS

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Title

History_0

Size

Document Number

B

DSPM-8301E

Rev

A104-1

Date:

Tuesday, March 13, 2012

Sheet

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