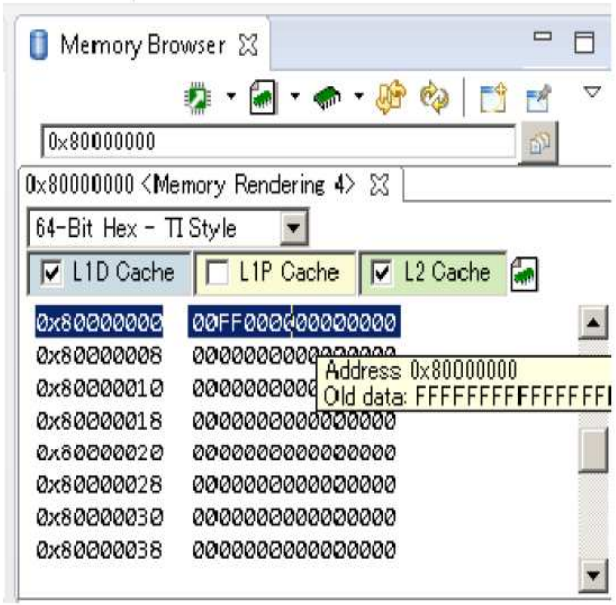
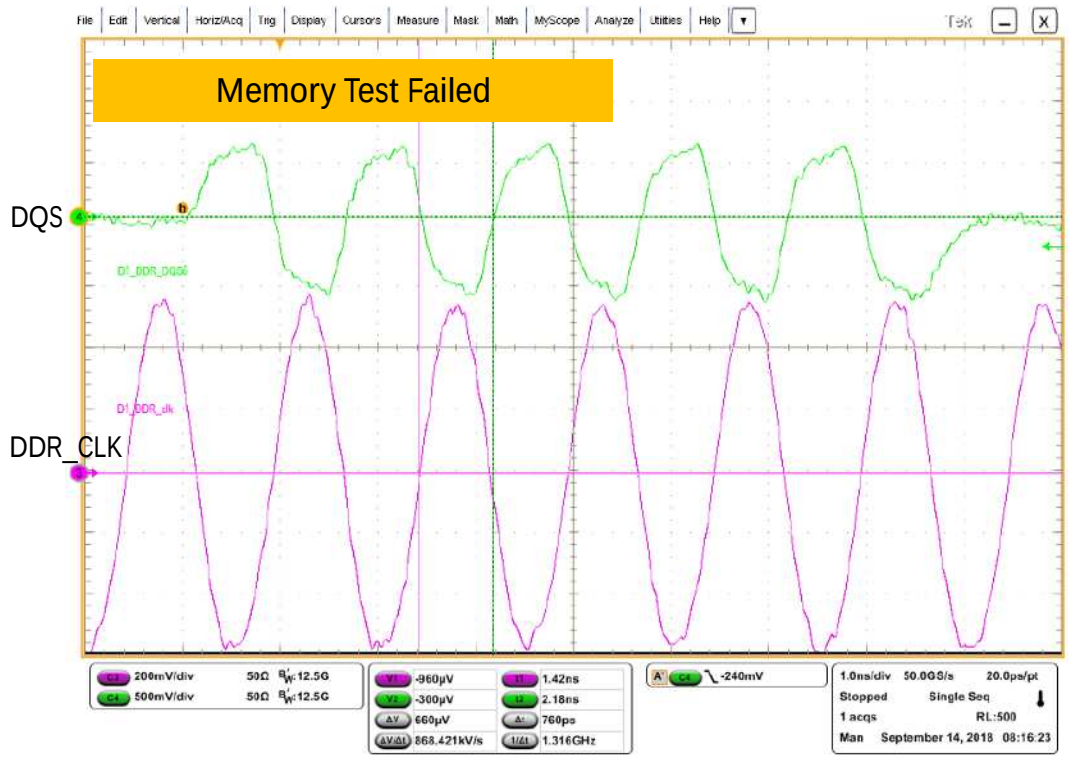


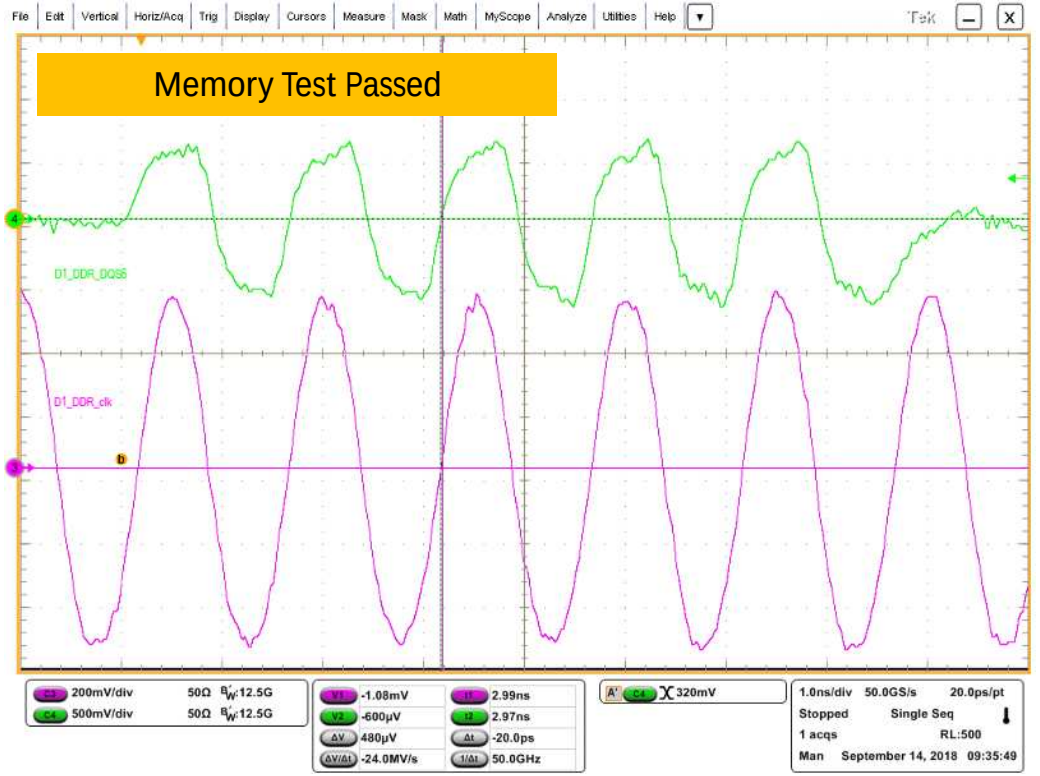
Question:
When memory test failed, they connect to CCS and tried memory write via memory browser and the following signal diagram was captured when writing to the memory.
The phase of clock and DQS was 180 degree out of phase compared against the signal which passed the memory test.

But what kind of cause can be considered?
(My customer are considering that write leveling have failed.)

DQS6-DQS6# vs CLKp-CLKn (Byte lane where bit corruption occurs)



DQS6-DQS6# vs CLKp-CLKn



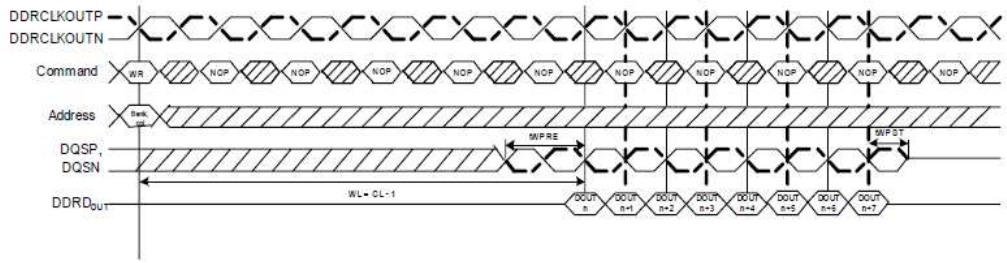
[C6678 DDR3 specification]

2.4.6 Write (WR) Command

Prior to a WRT command, the desired bank and row are activated by the ACT command. Following the WRT command, a write latency is incurred. Write latency is equal to CAS latency minus 1. All writes have a burst length of 8. Figure 2-3 shows the timing for a write on the DDR3 memory controller. If the transfer request is for less than 8 words, depending on the scheduling result and the pending commands, the DDR3 memory controller can:

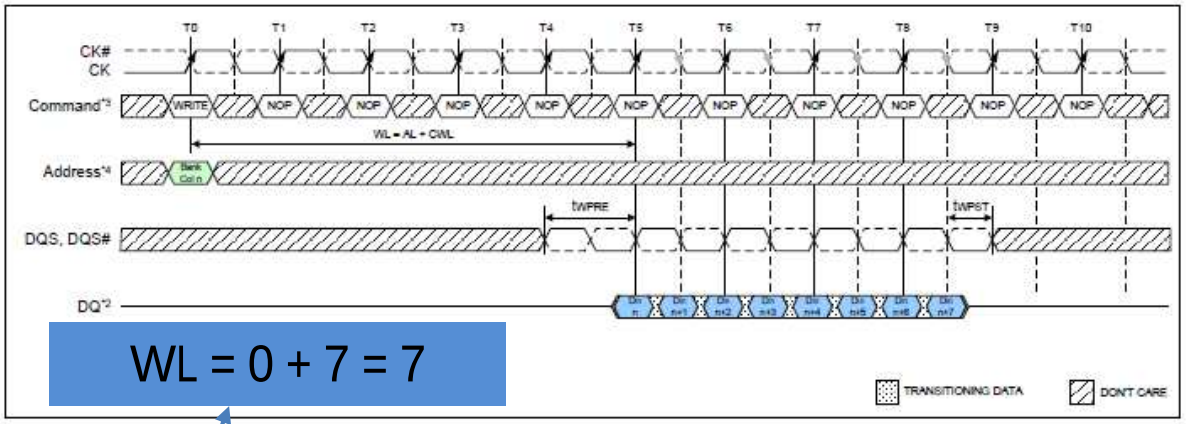
- Mask out the additional data using DDRDQM outputs
- Terminate the write burst and start a new write burst

Figure 2-3 WRITE Command



WL = 9 – 1 = 8

[customer's DDR3 memory specification]



WL = 0 + 7 = 7

Notes:

1. BL8, WL = 5; AL = 0, CWL = 5.
2. Din n = data-in from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0 A[1:0] = 00 or MR0 A[1:0] = 01 and A12 = 1 during WRITE command at T0.

Figure 43 – WRITE Burst Operation WL = 5 (AL = 0, CWL = 5, BL8)

DDR3 Memory Controller Register setting value:
CL = 9, CWL = 7, AL = 0

Question:

With current setting, do you think data timing between DSP and memory are not matching?