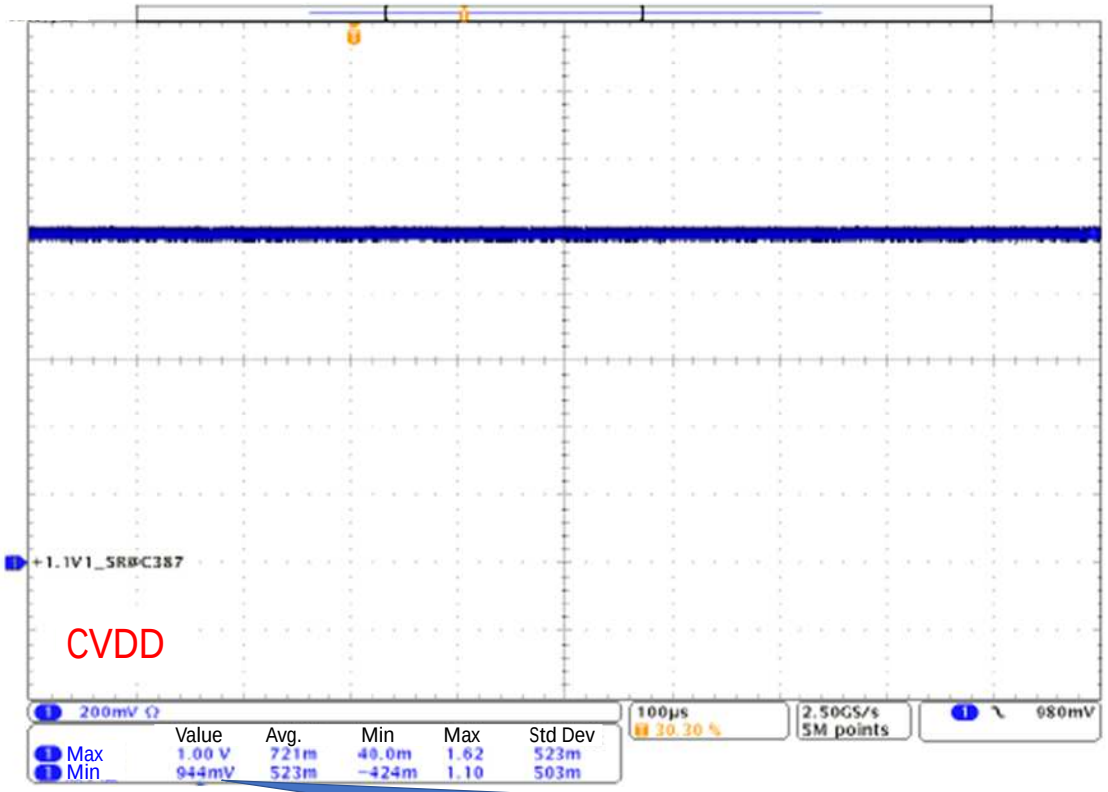
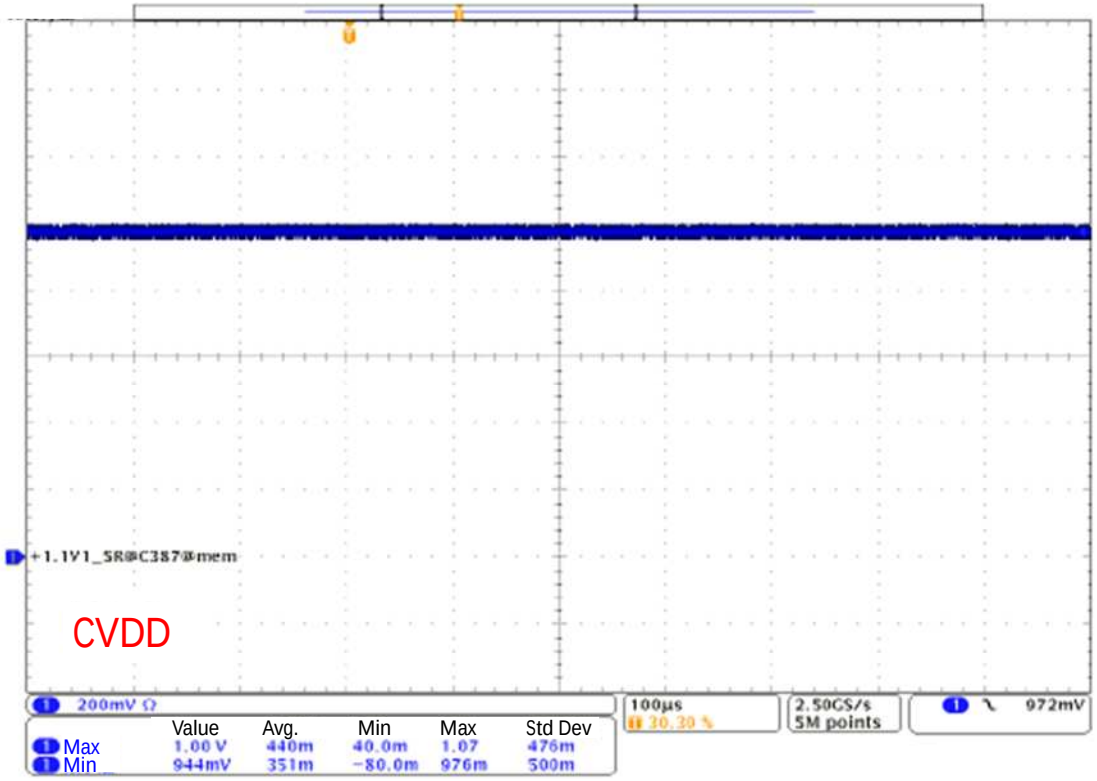
Date : March 14th, 2023
Target : Customer Board [DSP Lot No : 1CZCP19 (Genuine)]
Method : DSP power waveforms are observed with an oscilloscope
during DSP normal operation and memory test.
Active probe (1.5GHz) was used to probe through-holes near the DSP pins.
Result : No ripple, so we think the power rail is normal.

- DSP 1 (Memory Access Failure DSP), Power Supply:CVDD

<Usual Operation>



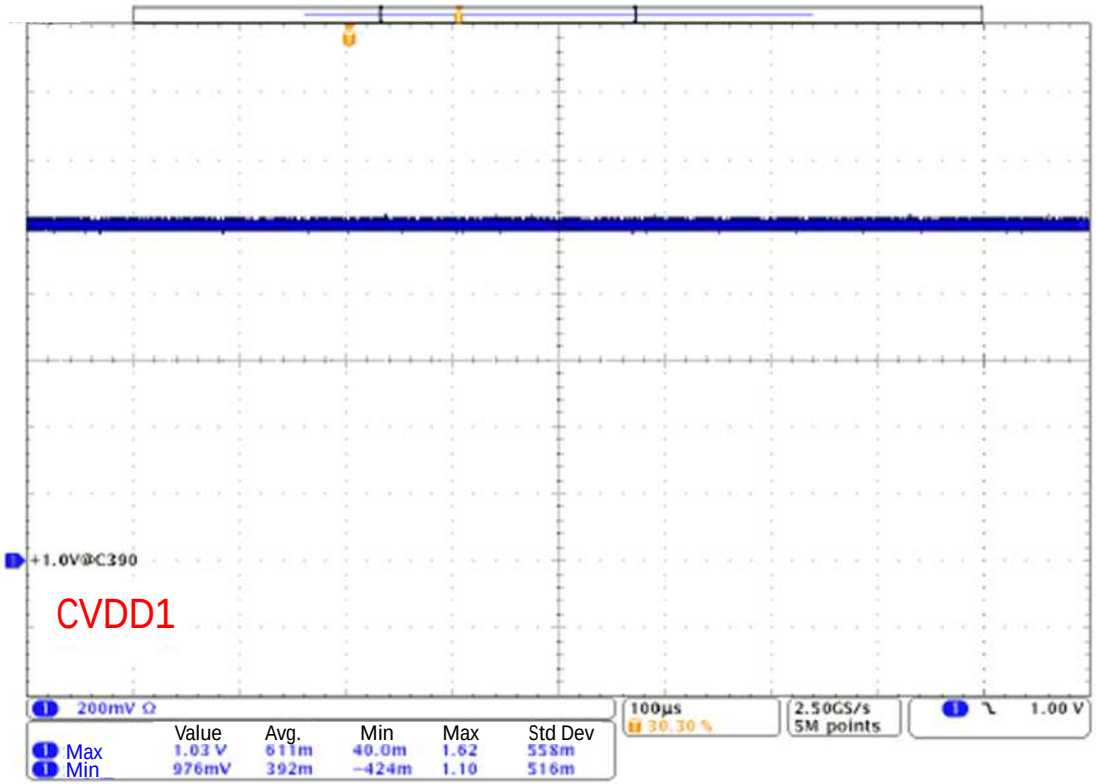
<Durning Memory Access>



Compared to normal DSP2, the voltage level of DSP1 is about 0.1[v] lower when Smart Reflex is enabled (1.1V when disabled).
Since this was suspected to be the cause, we conducted similar measurements(see next page) on other boards and found DSPs that were abnormal even at 1.1[v].

• DSP 1 (Memory Access Failure DSP) , Power Supply: CVDD1

<Usual Operation>



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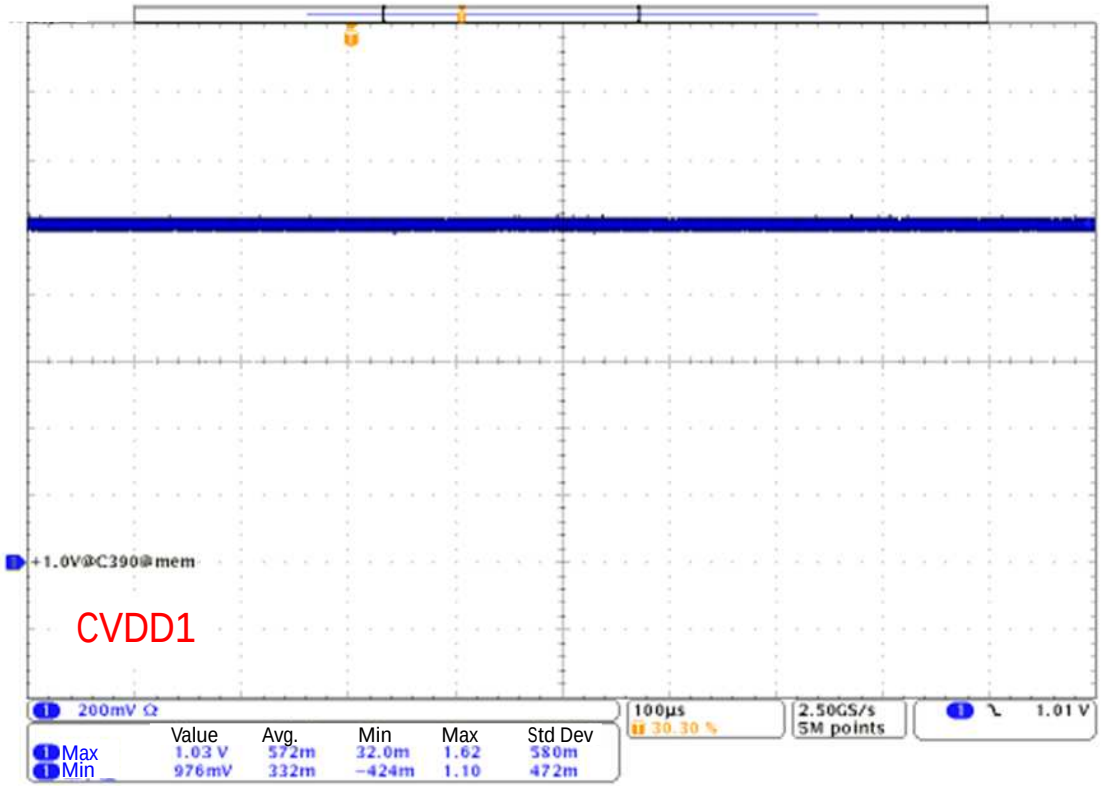
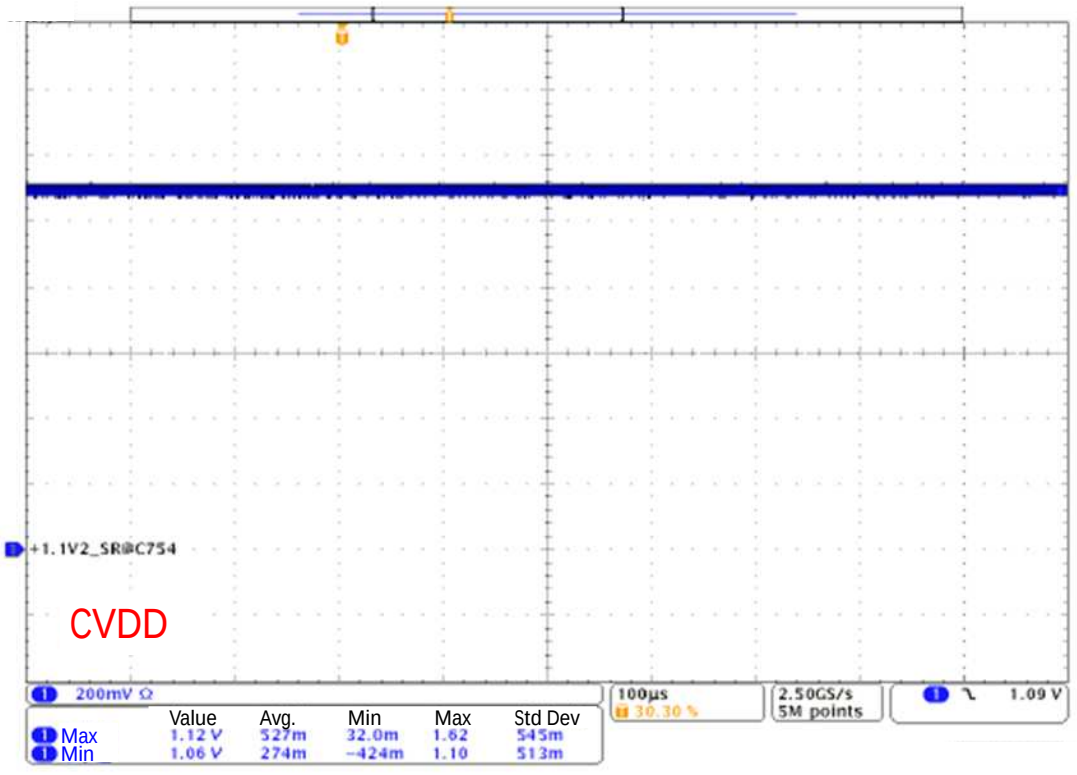
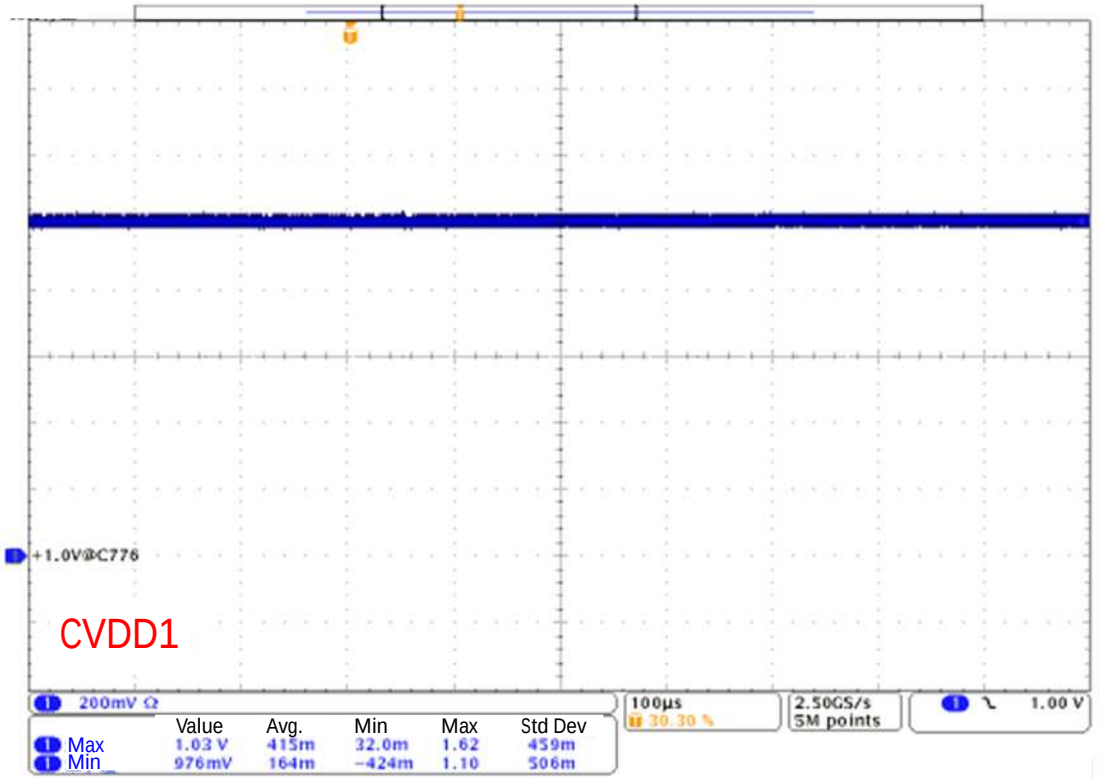


- DSP 2 (Memory Access Normal DSP), Power Supply CVDD and CVDD1





Reference Result
(C6678 which is marketed product)

Excerpts from C6678 datasheet. (All customer boards using 1000MHz-Device)

6.2 Recommended Operating Conditions

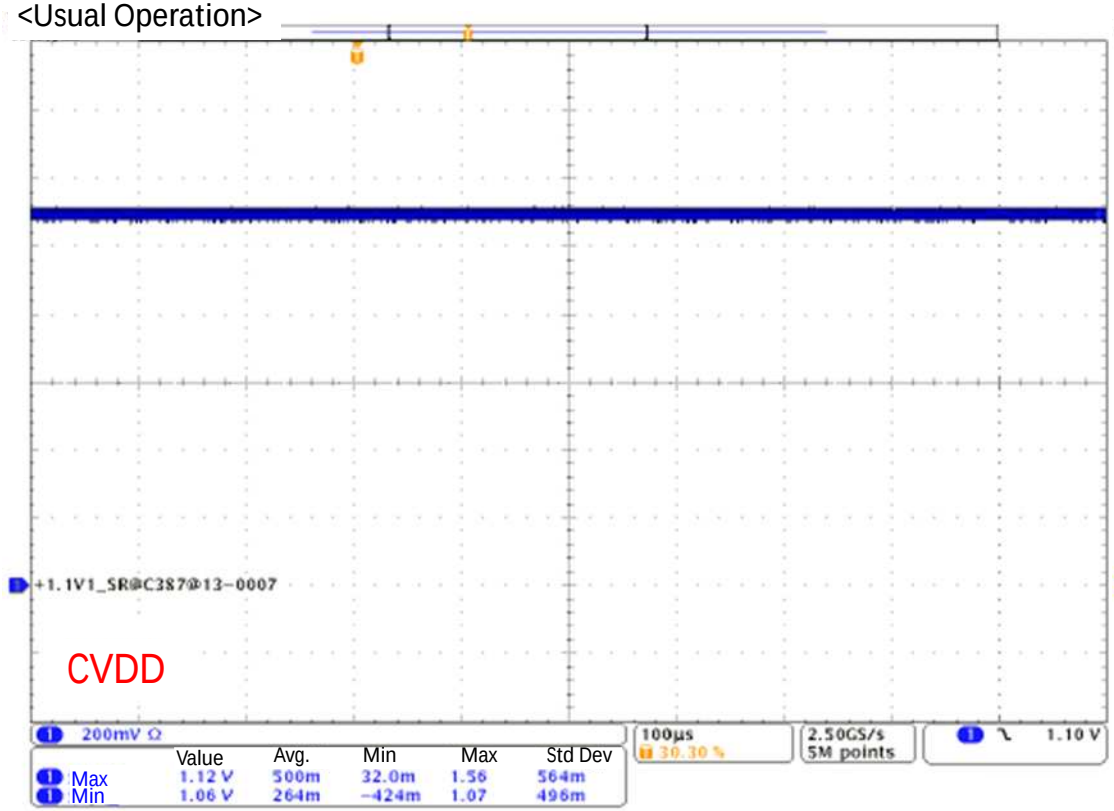
Table 6-2 Recommended Operating Conditions [1] [2]

			Min	Nom	Max	Unit
CVDD	SR Core Supply	Initial Startup	VINITnom × 0.95	1.1or 1.15 [3]	VINITnom × 1.05	V
		1000MHz - Device	SRVnom [4] × 0.95	0.85-1.1	SRVnom × 1.05	
		1250MHz - Device	SRVnom × 0.95	0.9-1.1	SRVnom × 1.05	
		1400MHz - Device	SRVnom × 0.95	0.95-1.15	SRVnom × 1.05	
CVDD1	Core supply voltage for memory array		0.95	1	1.05	V

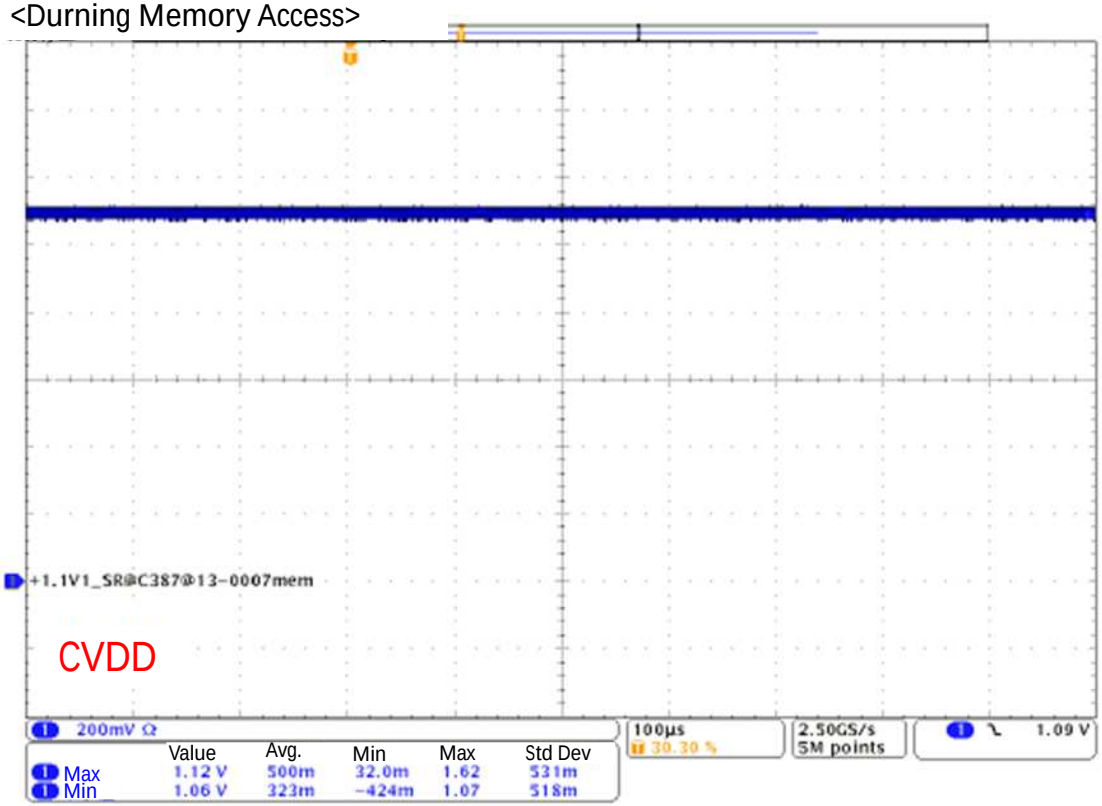
<Reference>

The result of DSP(marketed product) with memory access anomaly, although CVDD is 1.1[v] when Smartreflex is enabled.

<Usual Operation>

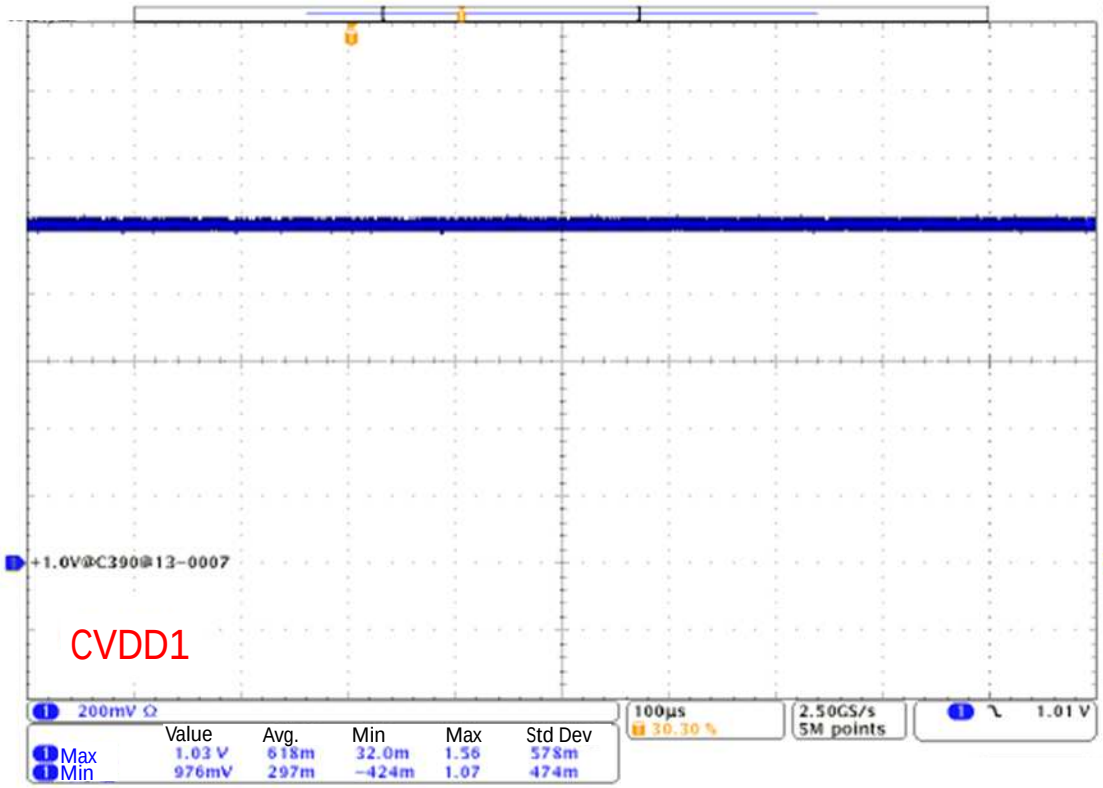


<Durning Memory Access>



<Reference>
The result of DSP(marketed product) with memory access anomaly, although CVDD is 1.1[v] when Smartreflex is enabled.

<Usual Operation>



<Durning Memory Access>