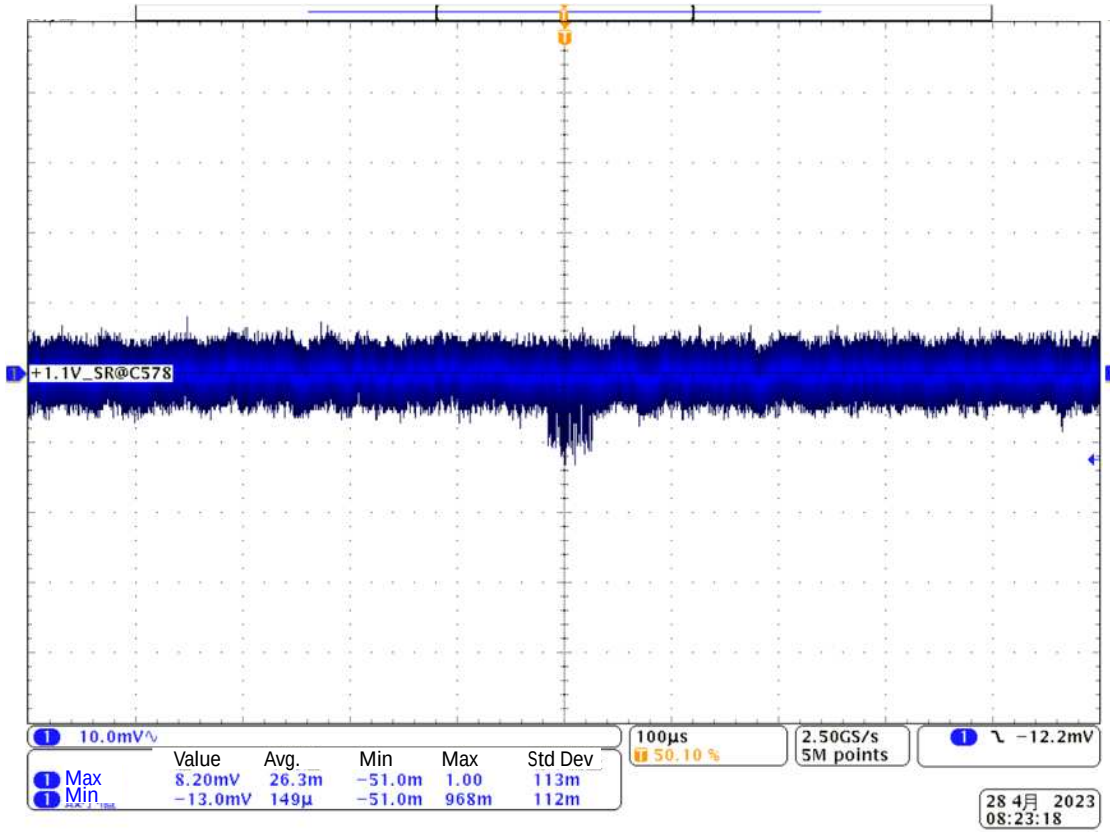
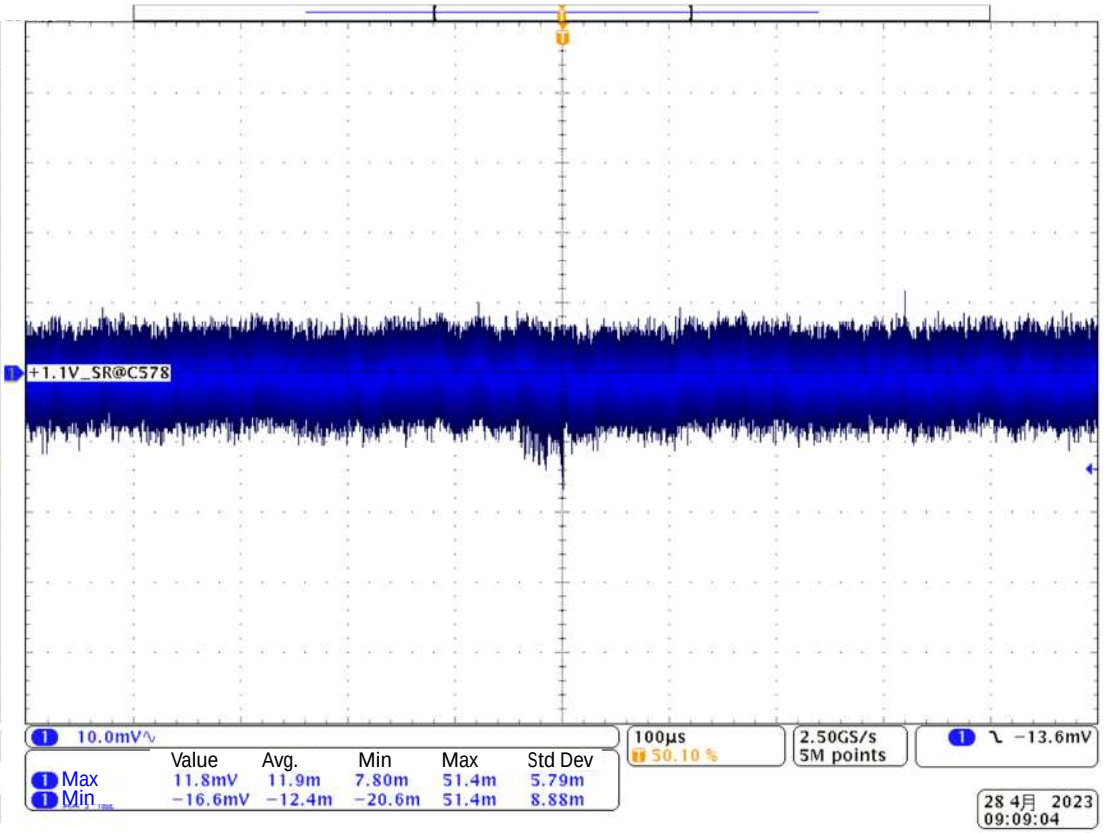
Date : April 28th, 2023
Target : Customer Board [ DSP Lot No : 1CZCP19 (Genuine) ]
Method : DSP power waveforms are observed with an oscilloscope during
DSP normal operation and memory test.
Passive probe (500MHz) was connected to the through-holes near the DSP pins and
the DC component was removed in the AC coupling setting.
Result : In DSP1 with abnormal memory access, the amplitude of fluctuation was -13.0 to 8.2 mV
during normal operation. And during memory access, it was -16.6 to 11.8 mV.
This satisfied the power supply specifications of the C6678 and did not differ from the
normal DSP2 results.

- DSP 1 (Memory Access Failure DSP) , Power Supply: CVDD

<Usual Operation>

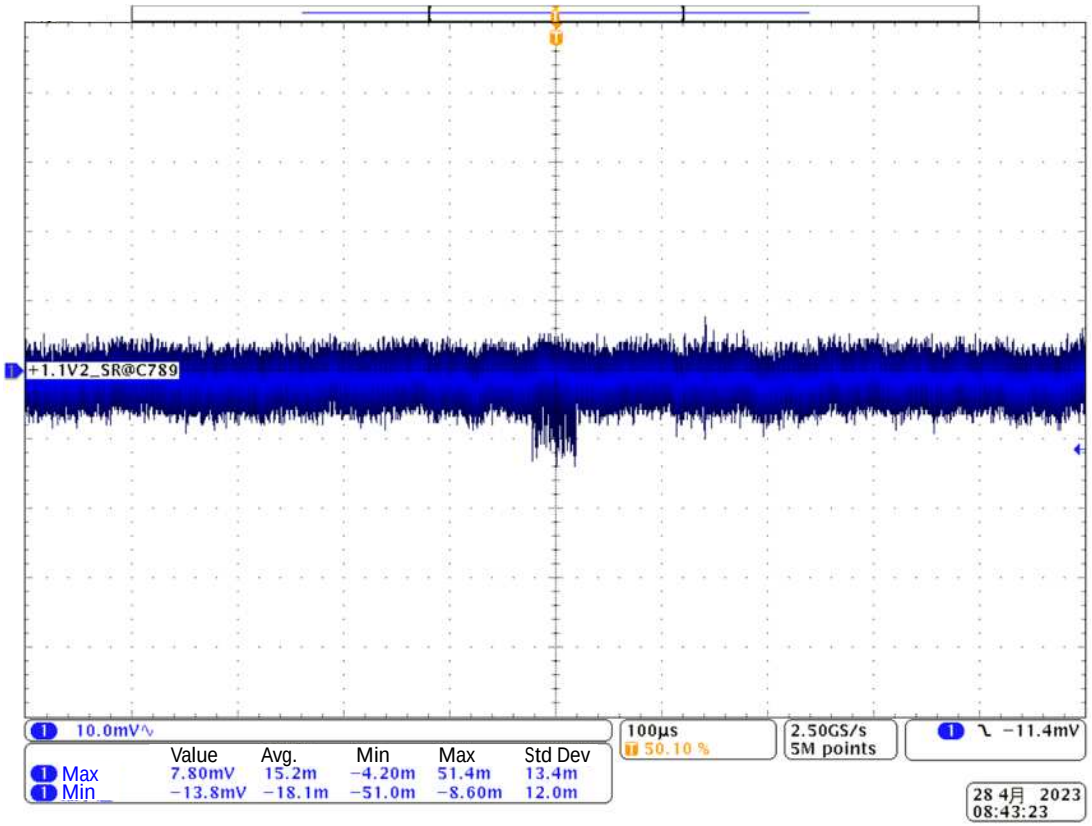



<During Memory Test>

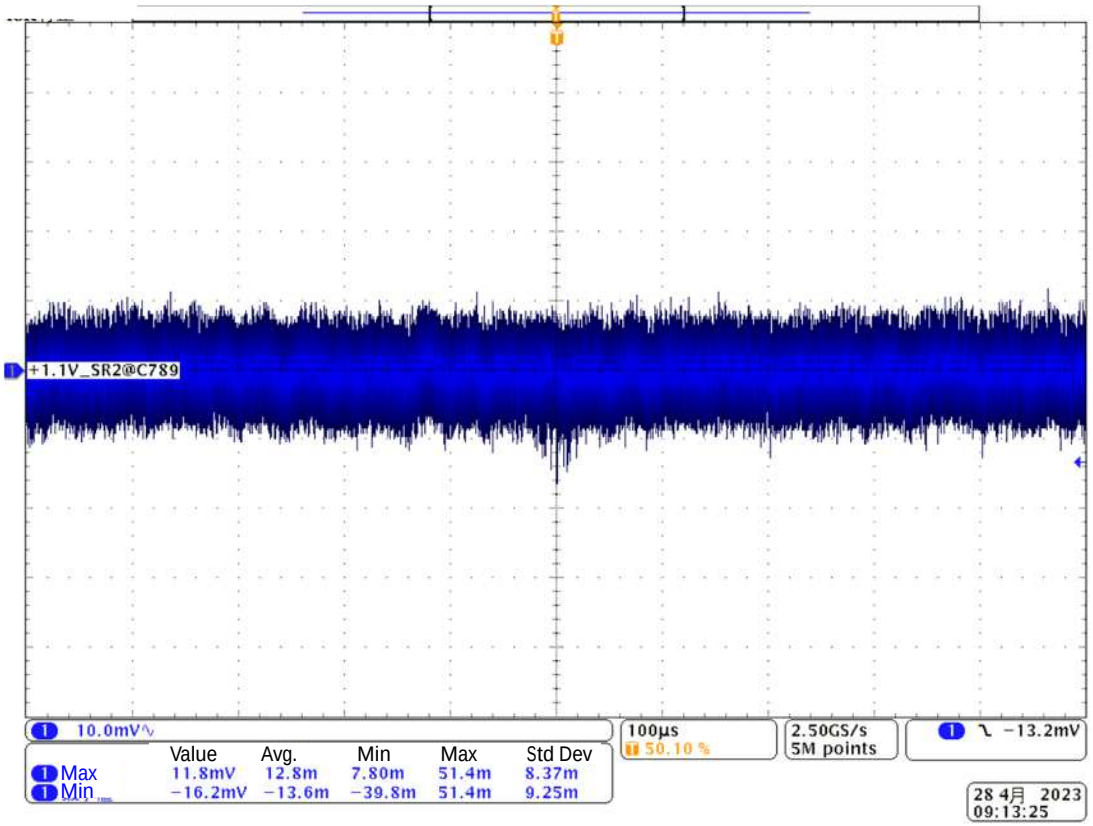


- DSP 2 (Memory Access Normal DSP) , Power Supply: CVDD

<Usual Operation>




<During Memory Test>



| | Genuine DSP | |
|---|---|---|
| | Smart Reflex Enable | Smart Reflex Disable |
| CVDD(1) | 1.094 | 0.973 |
| CVDD(2) | 1.094 | 1.094 |

<Consideration>

The CVDD voltage(DC component) measured by digital meter previously was 0.973 V (SRVnom).

The CVDD voltage (AC component) observed by the oscilloscope this time was -16.6mV max, and this is within the C6678 specification (SRVnom ±5% (48mV)).

Excerpts from C6678 datasheet. ( All customer boards using 1000MHz-Device)

## 6.2 Recommended Operating Conditions

**Table 6-2 Recommended Operating Conditions (1) (2)**

| | | | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| CVDD | SR Core Supply | Initial Startup | VINITnom × 0.95 | 1.1or 1.15 (3) | VINITnom × 1.05 | V |
| | | 1000MHz - Device | SRVnom (4) × 0.95 | 0.85-1.1 | SRVnom × 1.05 | |
| | | 1250MHz - Device | SRVnom × 0.95 | 0.9-1.1 | SRVnom × 1.05 | |
| | | 1400MHz - Device | SRVnom × 0.95 | 0.95-1.15 | SRVnom × 1.05 | |
| CVDD1 | Core supply voltage for memory array | | 0.95 | 1 | 1.05 | V |