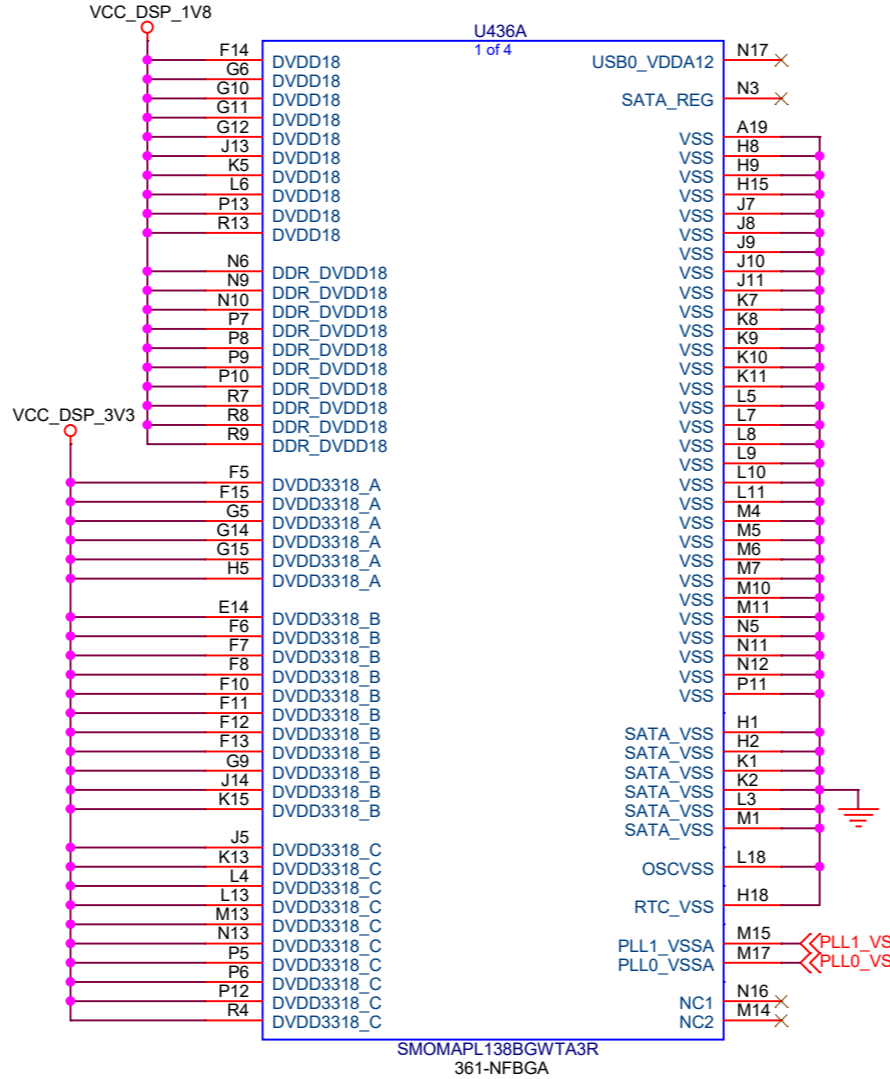
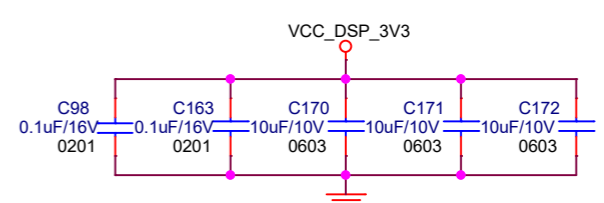
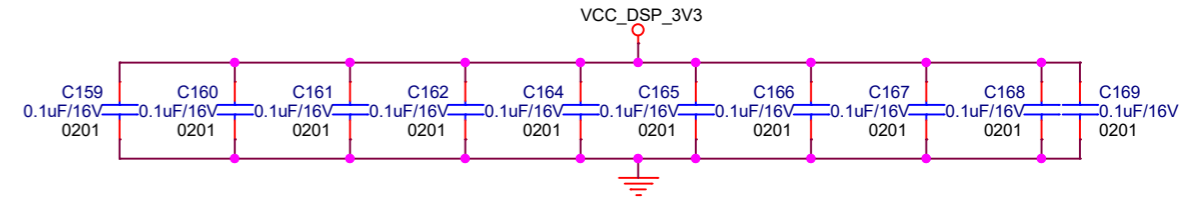
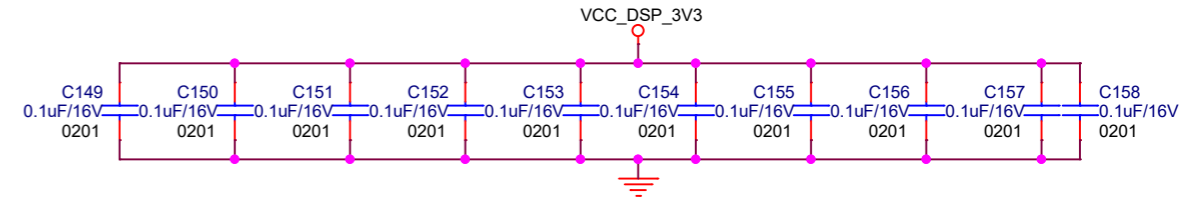
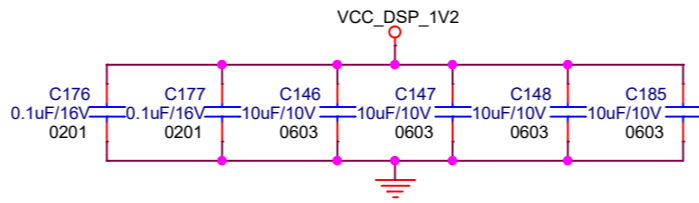
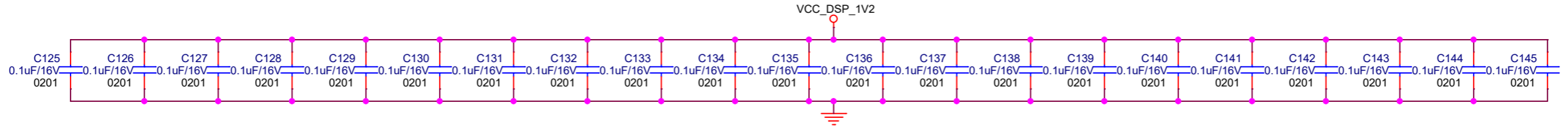
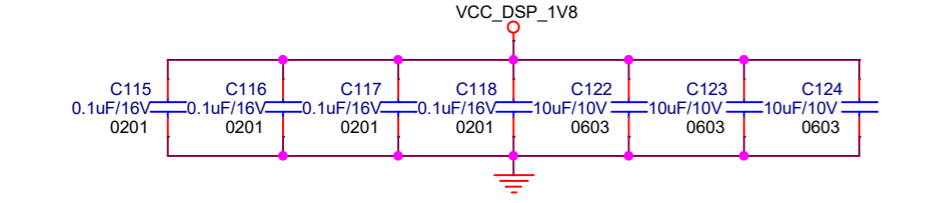
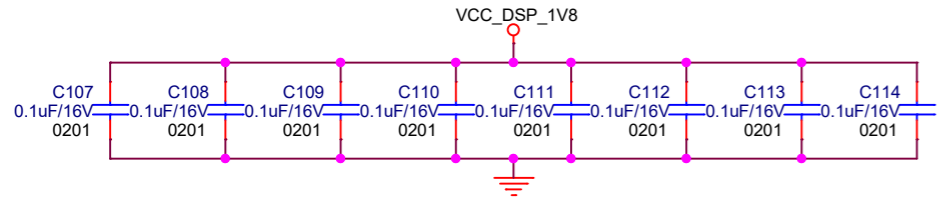
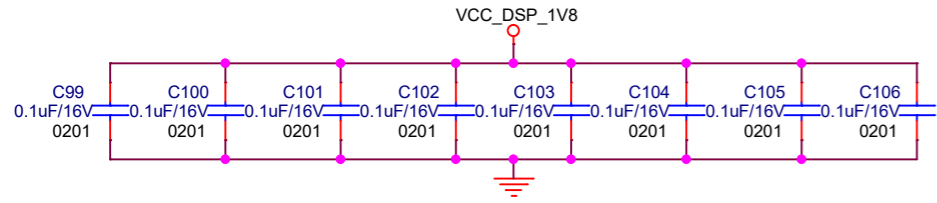


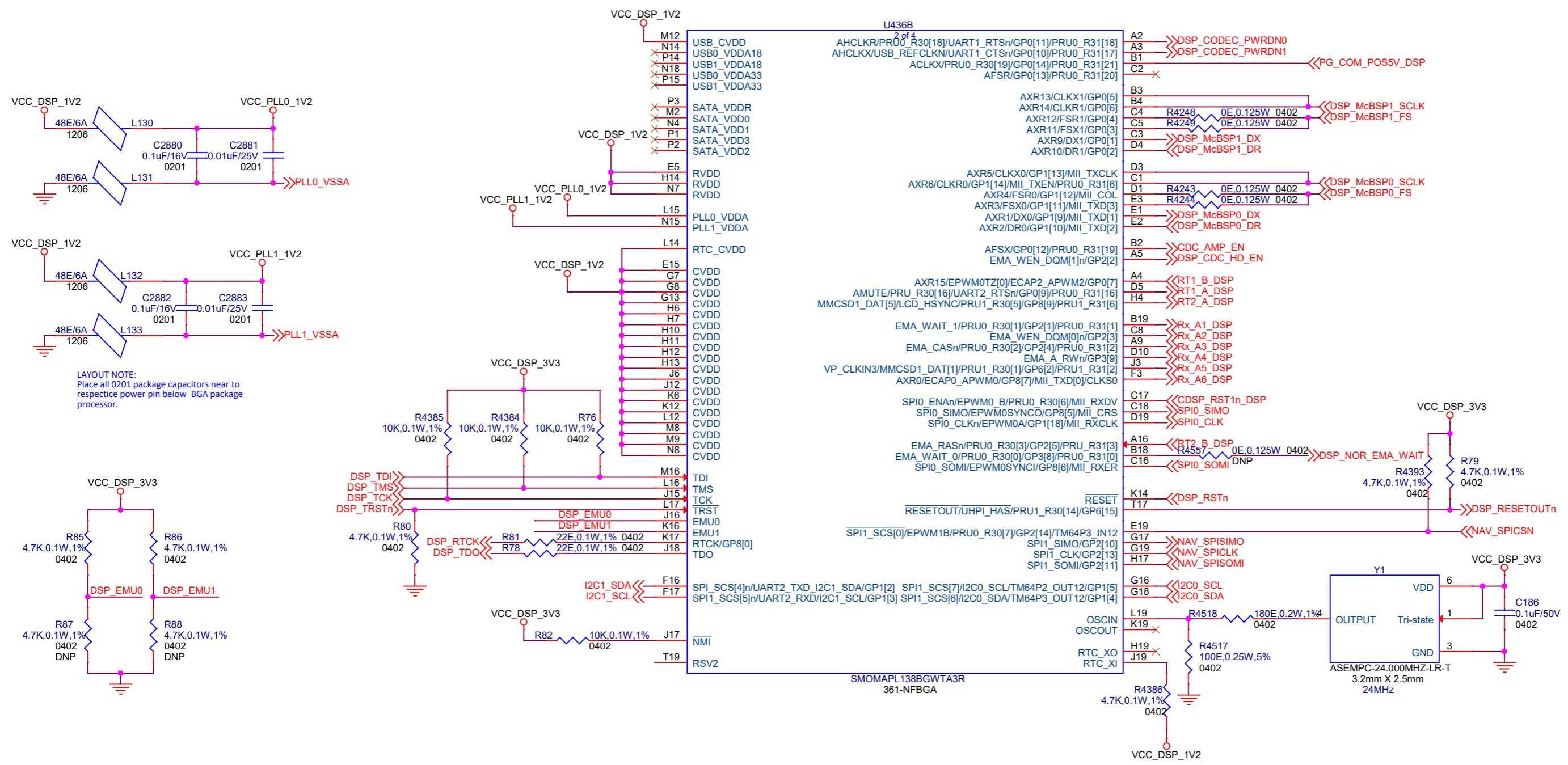
Power ON Sequence

1. RTC_CVDD --> CVDD OR RTC_CVDD = CVDD
2. CVDD, RVDD, PLL0_VDDA, PLL1_VDDA, USB_CVDD, SATA_VDD
3. All static 1.8V IO supplies: DVDD18, DDR_DVDD18, USB0_VDDA18, USB1_VDDA18, SATA_VDDR, DVDD3318_A, DVDD3318_B, DVDD3318_C
4. All analog 3.3V PHY supplies: USB0_VDDA33, USB1_VDDA33, DVDD3318_A, DVDD3318_B, DVDD3318_C
VCC_DSP_1V2 --> VCC_DSP_1V8 --> VCC_DSP_3V3

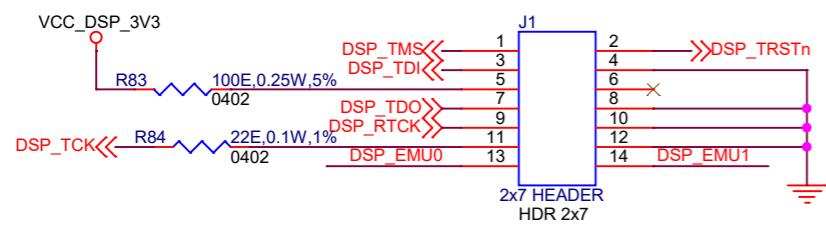


LAYOUT NOTE:
Place all 0201 package capacitors near to respective power pin below BGA package processor.

CONFIGURATION BOARD	NAME	SIGNATURE	DATE	CSIR - NAL PB 1779, Old Airport Road, Bengaluru Karnataka 560 017		
DRAWN:	Vighnesh					
DESIGNED:	Vighnesh			DRAWING TITLE COM BASE CARD DSP COM POWER		
PEER REVIEWER:	Karthik			SIZE	DRAWING NUMBER	REV
QA REVIEWER:				A3	DR-2007	-
CHECKED BY:				THIRD ANGLE PROJ	SCALE	SHEET No
APPROVED BY:					1:1	3
						of SHEETS 25



LAYOUT NOTE:
Place all 0201 package capacitors near to respectice power pin below BGA package processor.



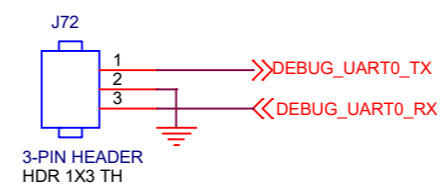
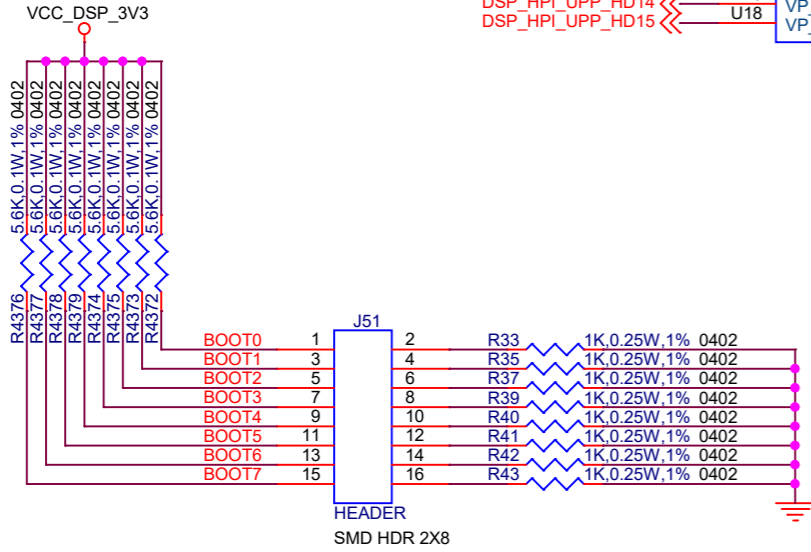
CONFIGURATION BOARD	NAME	SIGNATURE	DATE	CSIR - NAL		
DRAWN:	Vighnesh			PB 1779, Old Airport Road, Bengaluru Karnataka 560 017		
DESIGNED:	Vighnesh			DRAWING TITLE COM BASE CARD		
PEER REVIEWER:	Karthik			DRAWING NUMBER DSP CLOCK AND JTAG		
QA REVIEWER:				SIZE	DRAWING NUMBER	REV
CHECKED BY:				A3	DR-2007	-
APPROVED BY:				THIRD ANGLE PROJ	SCALE 1:1	SHEET No 4 of SHEETS 25



LAYOUT NOTE:
ROUTE THIS PAIR OF SIGNALS (DDR_DQGATE0 & DDR_DQGATE1) PHYSICALLY CLOSE TO THE DATA BUS. KEEP BOTH SIGNALS CLOSE TO EACH OTHER. THERE IS NO IMPEDANCE REQUIREMENT FOR THESE SIGNALS.

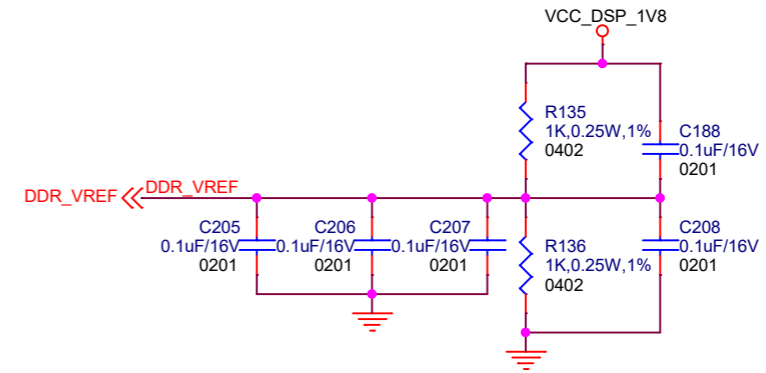
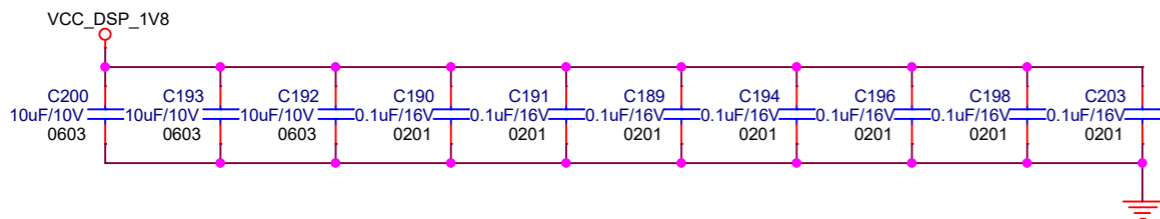
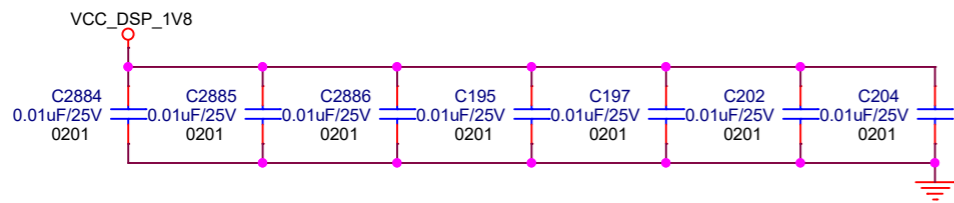
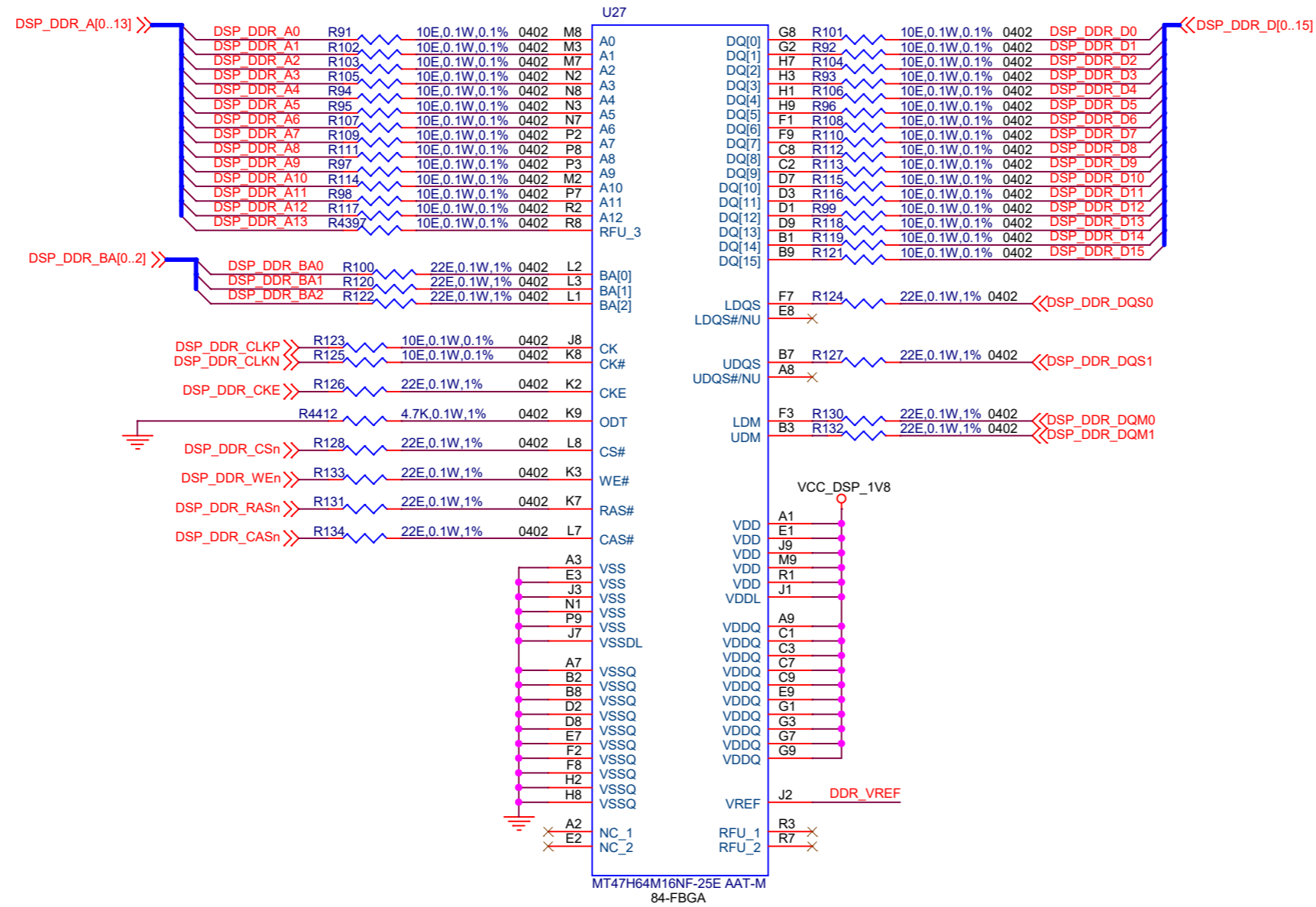
ROUTE THE SIGNAL DDR_DQGATE0, DDR_DQGATE1 INCLUDING R89,R90 TOWARDS THE DDR2 DEVICE AS TWICE THE DISTANCE AS THAT OF DDR_DQ.

CONFIGURATION BOARD	NAME	SIGNATURE	DATE	CSIR - NAL PB 1779, Old Airport Road, Bengaluru Kamataka 560 017
DRAWN:	Vighnesh			
DESIGNED:	Vighnesh			DRAWING TITLE COM BASE CARD DSP NOR DDR2 BLOCK
PEER REVIEWER:	Karthik			SIZE A3 DRAWING NUMBER DR-2007 REV -
QA REVIEWER:				THIRD ANGLE PROJ SCALE 1:1 SHEET No 5
CHECKED BY:				of SHEETS 25
APPROVED BY:				

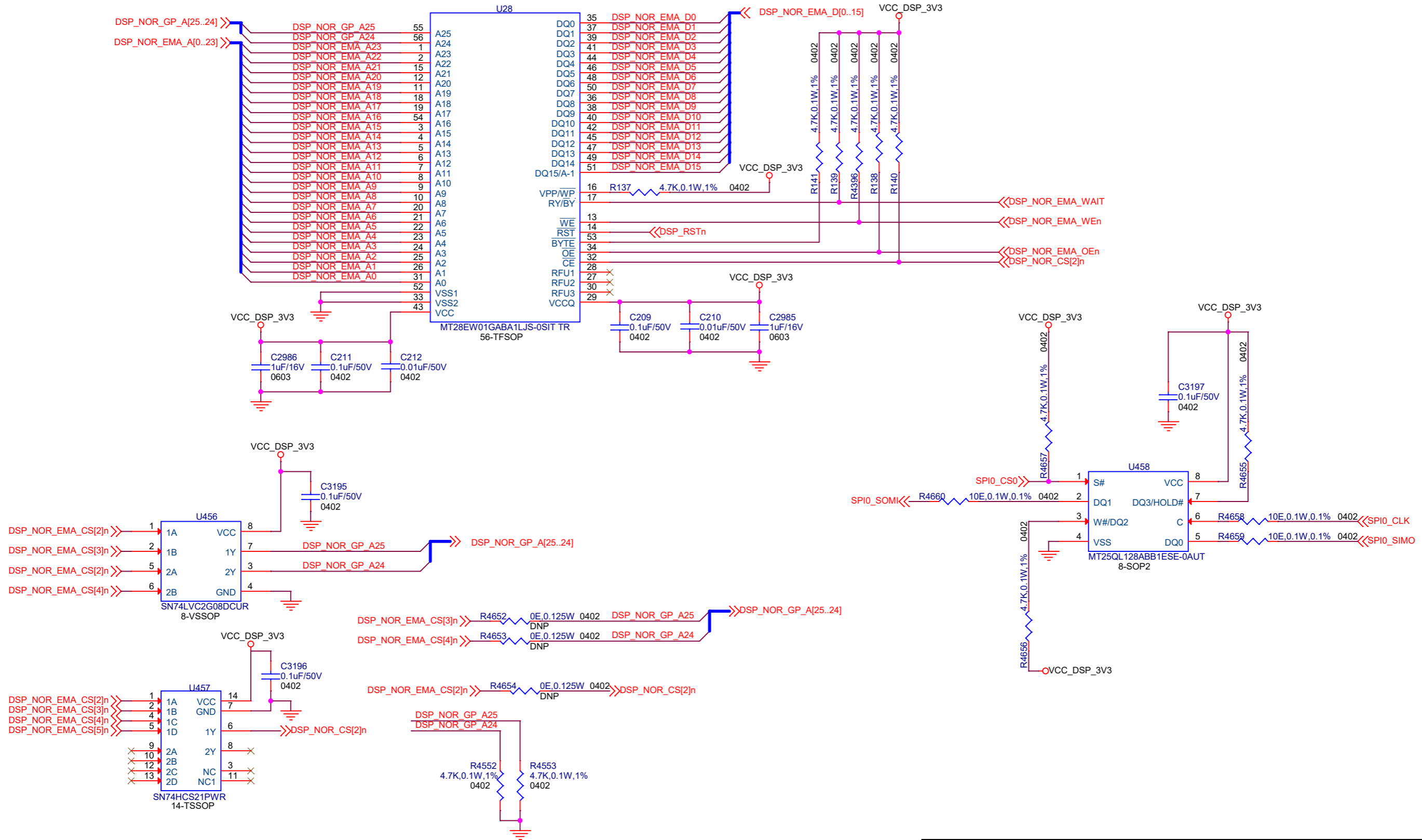


Use below mentioned jumper for shorting connector pin to set BOOT mode
Part number : QFC02SXGN-RC

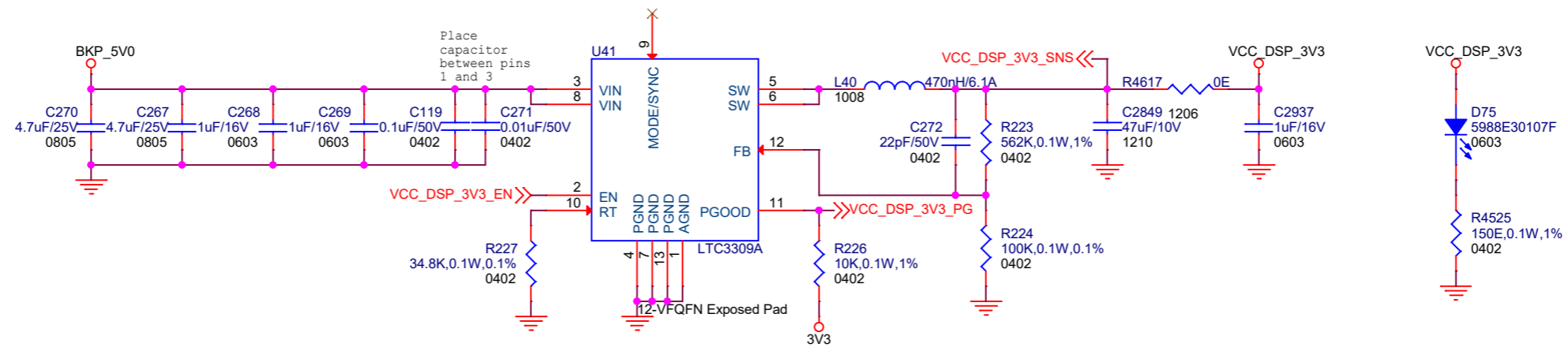
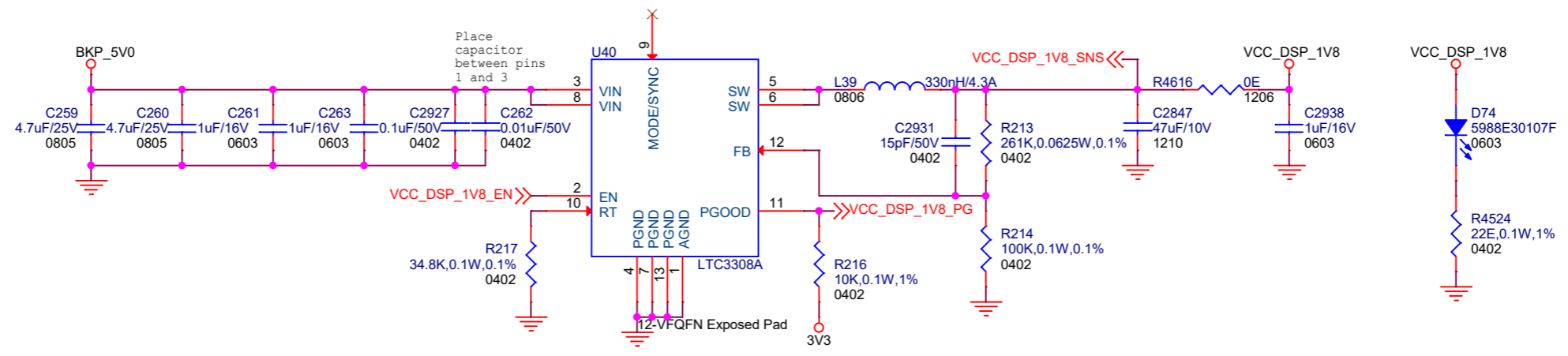
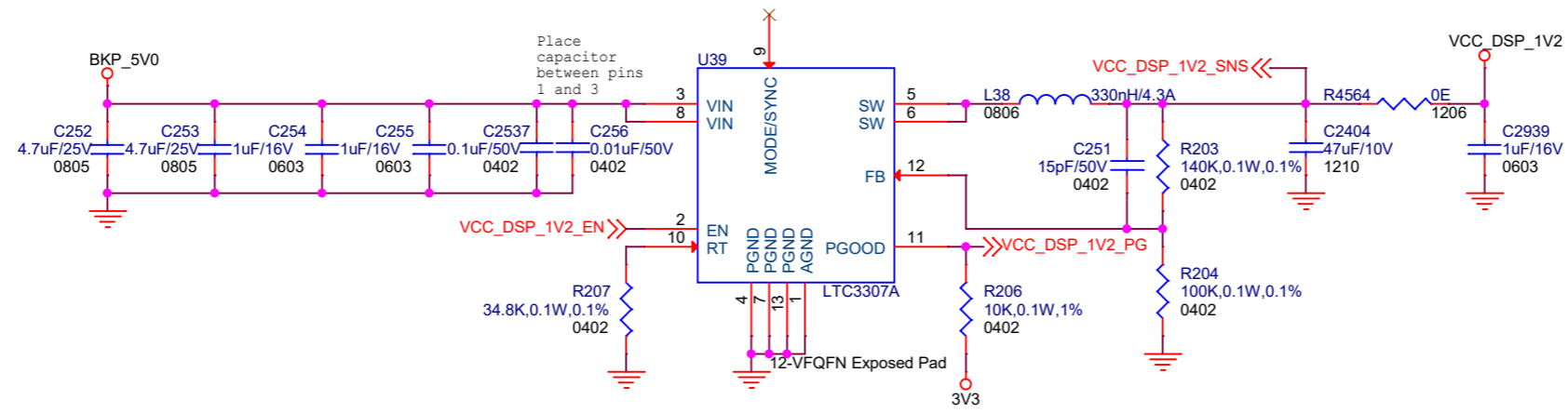
CONFIGURATION BOARD	NAME	SIGNATURE	DATE	CSIR - NAL		
DRAWN:	Vighnesh			PB 1779, Old Airport Road, Bengaluru Karnataka 560 017		
DESIGNED:	Vighnesh			DRAWING TITLE COM BASE CARD		
PEER REVIEWER:	Karthik			DSP HPI UPP BOOT		
QA REVIEWER:				SIZE	DRAWING NUMBER	REV
CHECKED BY:				A3	DR-2007	-
APPROVED BY:				THIRD ANGLE PROJ	SCALE 1:1	SHEET No 6 of SHEETS 25



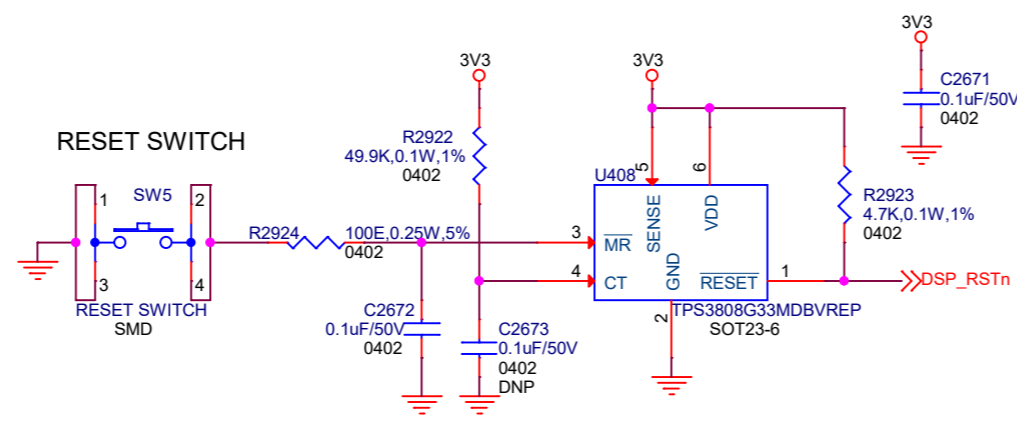
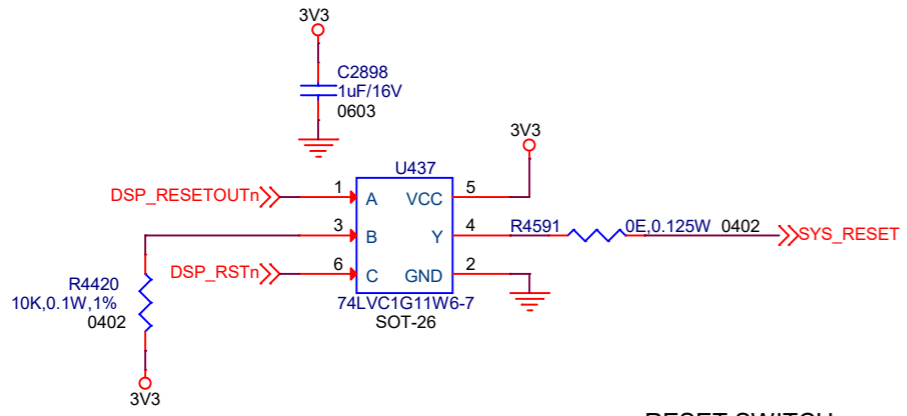
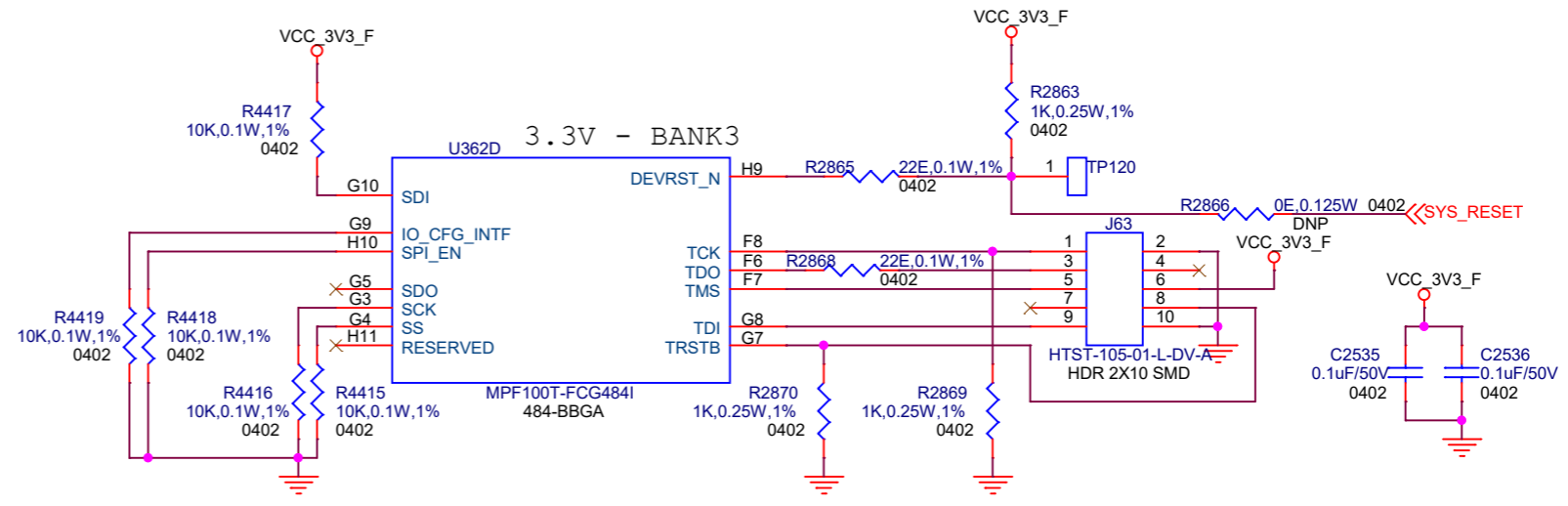
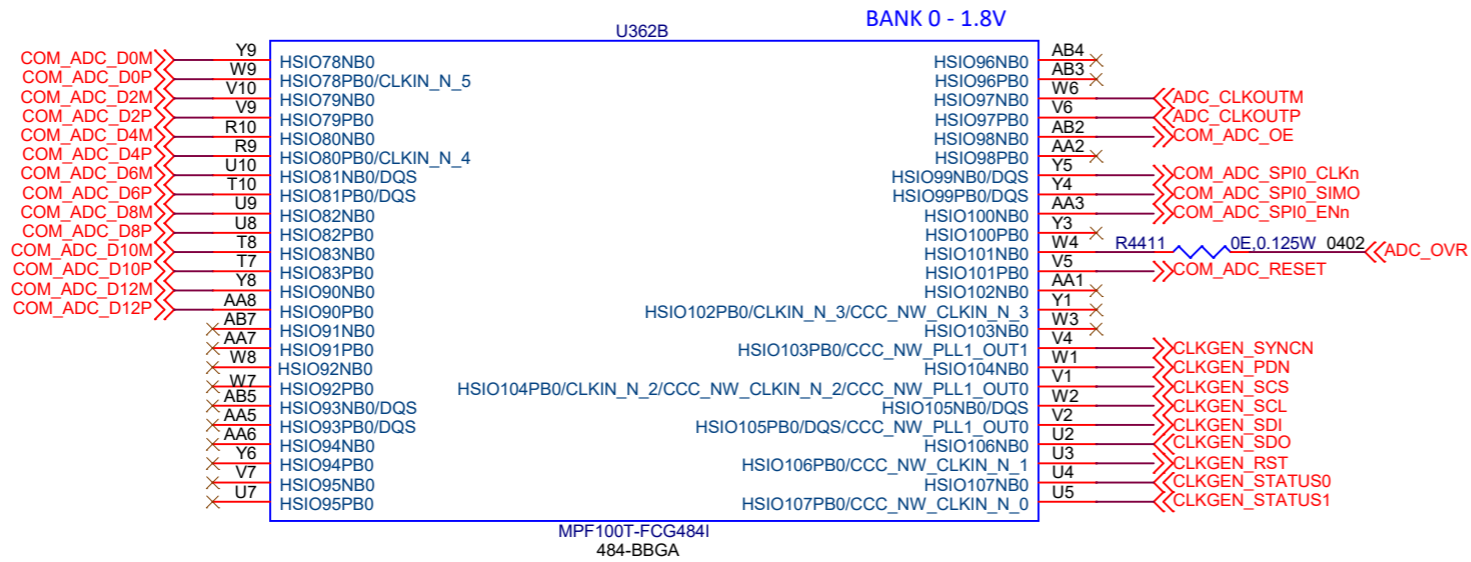
CONFIGURATION BOARD	NAME	SIGNATURE	DATE	CSIR - NAL		
DRAWN:	Vighnesh			PB 1779, Old Airport Road, Bengaluru Karnataka 560 017		
DESIGNED:	Vighnesh			DRAWING TITLE COM BASE CARD		
PEER REVIEWER:	Karthik			DDR2 INTERFACE		
QA REVIEWER:				SIZE	DRAWING NUMBER	REV
CHECKED BY:				A3	DR-2007	-
APPROVED BY:				THIRD ANGLE PROJ	SCALE 1:1	SHEET No 7 of SHEETS 25



CONFIGURATION BOARD	NAME	SIGNATURE	DATE	CSIR - NAL		
DRAWN:	Vighnesh			PB 1779, Old Airport Road, Bengaluru Karnataka 560 017		
DESIGNED:	Vighnesh			DRAWING TITLE COM BASE CARD		
PEER REVIEWER:	Karthik			NOR FLASH INTERFACE		
QA REVIEWER:				SIZE	DRAWING NUMBER	REV
CHECKED BY:				A3	DR-2007	-
APPROVED BY:				THIRD ANGLE PROJ	SCALE 1:1	SHEET No 8 of SHEETS 25



CONFIGURATION BOARD	NAME	SIGNATURE	DATE	CSIR - NAL PB 1779, Old Airport Road, Bengaluru Karnataka 560 017		
DRAWN:	Vighnesh					
DESIGNED:	Vighnesh			DRAWING TITLE COM BASE CARD DSP POWER SUPPLY		
PEER REVIEWER:	Karthik			SIZE	DRAWING NUMBER	REV
QA REVIEWER:				A3	DR-2007	-
CHECKED BY:				THIRD ANGLE PROJ	SCALE	SHEET No
APPROVED BY:					1:1	13
						of SHEETS 25



CONFIGURATION BOARD	NAME	SIGNATURE	DATE	CSIR - NAL		
DRAWN:	Vighnesh			PB 1779, Old Airport Road, Bengaluru Karnataka 560 017		
DESIGNED:	Vighnesh			DRAWING TITLE COM BASE CARD		
PEER REVIEWER:	Karthik			FPGA BANK 0 AND 3		
QA REVIEWER:				SIZE	DRAWING NUMBER	REV
CHECKED BY:				A3	DR-2007	-
APPROVED BY:				THIRD ANGLE PROJ	SCALE 1:1	SHEET No 20 of SHEETS 25