J7X COMMON PROCESSOR BOARD

TABLE OF CONTENTS

REV	E3B
VER	0.1

Project : J7 EVM	TEXAS INSTRUMENTS	Title: TABLE OF CONTENTS
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 1 of 68

REVISION HISTORY #1

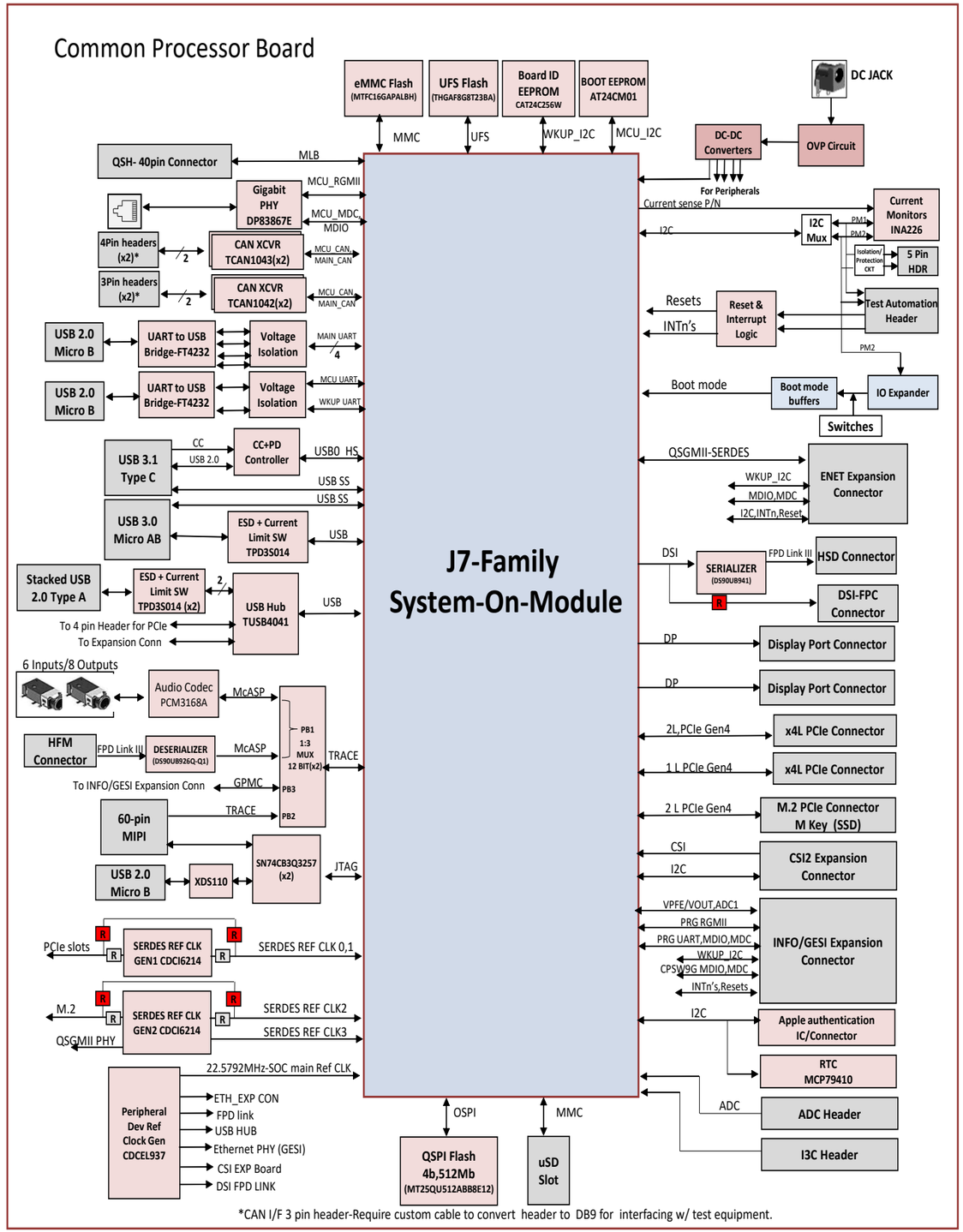
VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	21st NOV 2019	Drafted from "PROC079E3A_SCH, VER: 2.0" Released on 23rd OCT 2019 TP145 moved to DNI list Hardware Schematic Page Updated	Mistral Design Team		

REVISION HISTORY #2

BLANK

Project : J7 EVM	TEXAS INSTRUMENTS	Title: REVISION HISTORY	
		Size: C	PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 3 of 68

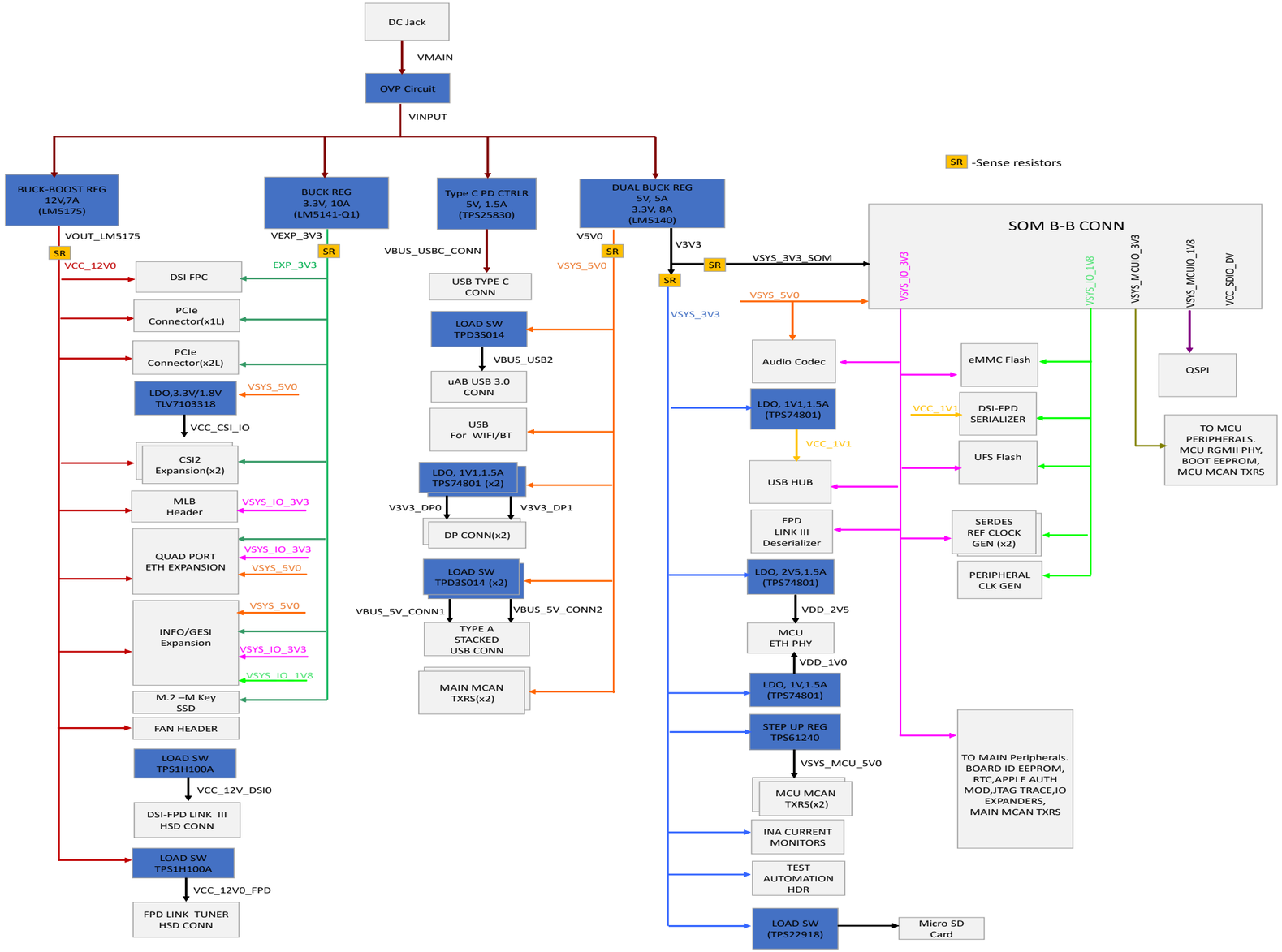
BLOCK DIAGRAM



*CAN I/F 3 pin header-Require custom cable to convert header to DB9 for interfacing w/ test equipment.

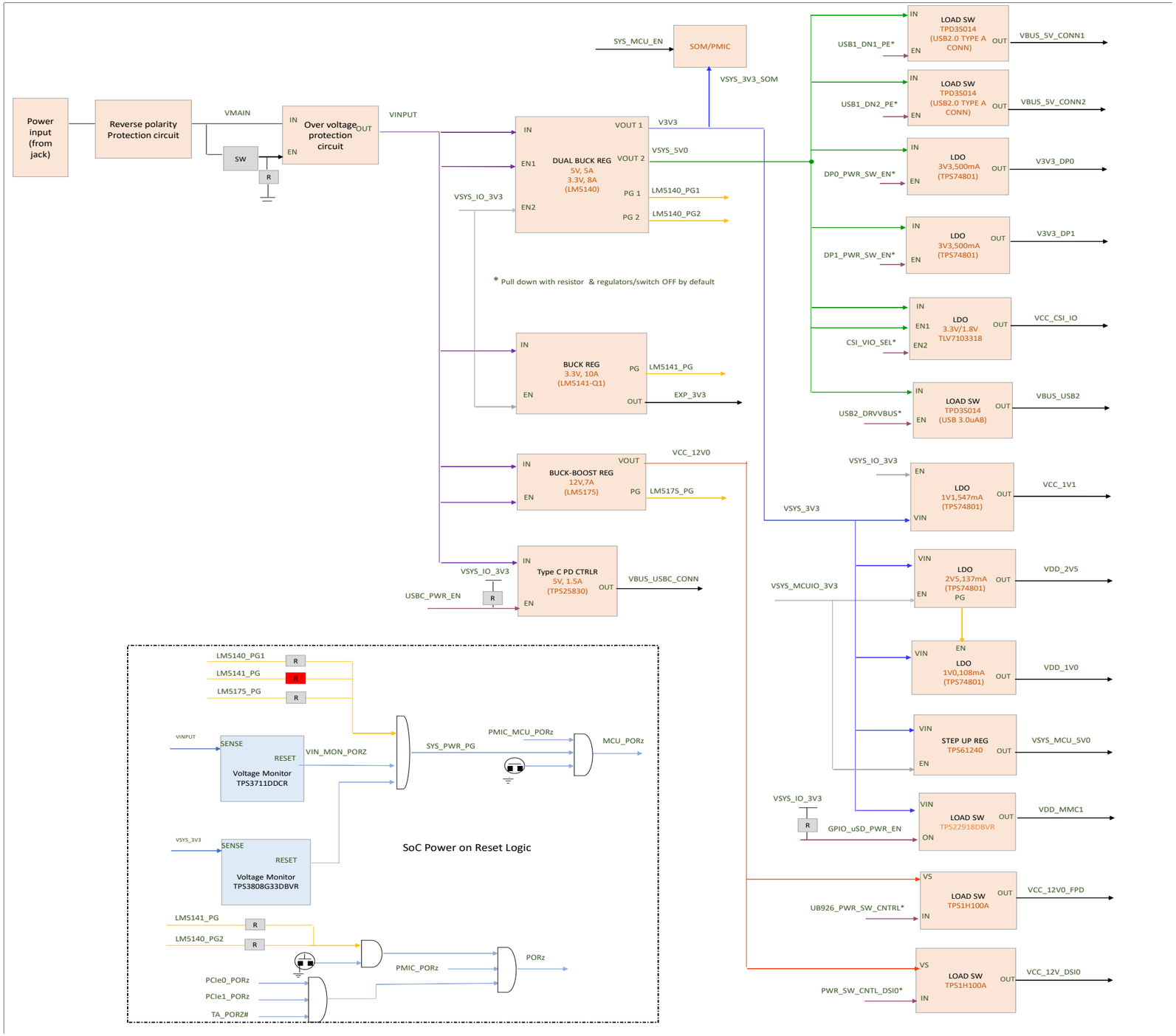
Project : J7 EVM	TEXAS INSTRUMENTS	Title: BLOCK DIAGRAM
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 4 of 68

POWER FLOW DIAGRAM



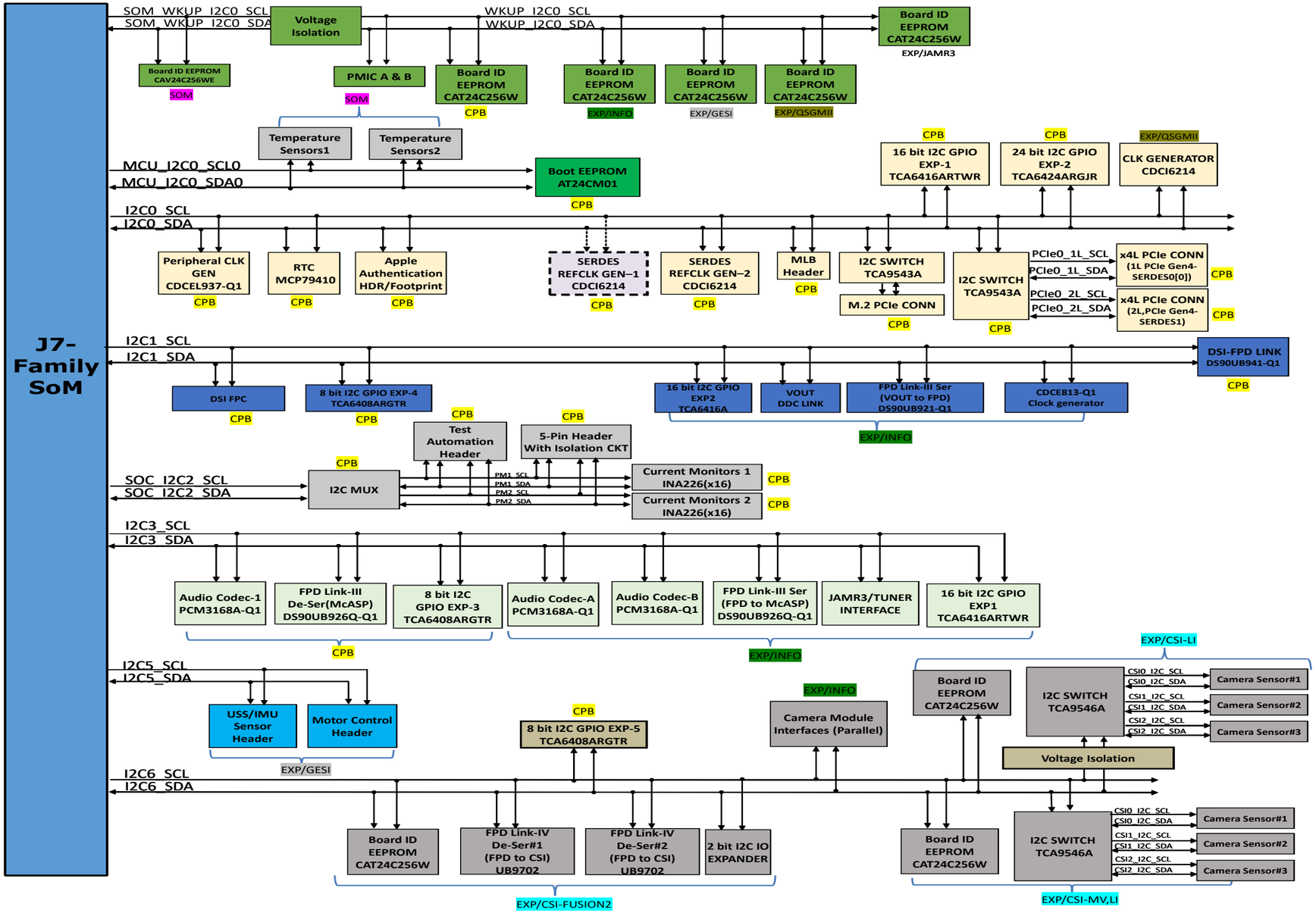
Project : J7 EVM	TEXAS INSTRUMENTS	Title: POWER FLOW DIAGRAM
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 5 of 68

POWER SEQUENCE



Project : J7 EVM	TEXAS INSTRUMENTS	Title: POWER SEQUENCE
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 6 of 68

I2C TREE



Project : J7 EVM	TEXAS INSTRUMENTS	Title: I2C TREE
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 7 of 68

GPIO EXPANDER MAP/TABLE

I2C Bus/Address	GPIO Port	Net name	Direction WRT CTRL	Default state	Active state	Remarks
GPIO Expander - 1 Part# TCA6416ARTWR						
I2C0/0x20	P00	PCIE_2L_MODE_SEL	Input	DIP_SEL	NA	PCIe 2-Lane Mode Select ('0' - Root Complex, '1' - End Point)
	P01	PCIE_2L_PERSTZ	Input	PD	Active low	PCIe 2-Lane Bus Reset ('0' - device reset, '1' - normal operation)
	P02	PCIE_2L_RC_RSTZ	Output	PD	Active low	PCIe 2-Lane RC Reset Control ('0' - device reset, '1' - normal operation)
	P03	PCIE_2L_EP_RST_EN	Output	PD	Active low	PCIe 2-Lane EP Reset Enable ('0' - PERSTz isolated from PORz, '1' PERSTz connected to PORz)
	P04	PCIE_1L_MODE_SEL	Input	DIP_SEL	NA	PCIe 1-Lane Mode Select ('0' - Root Complex, '1' - End Point)
	P05	PCIE_1L_PERSTZ	Input	PD	Active low	PCIe 1-Lane Bus Reset ('0' - device reset, '1' - normal operation)
	P06	PCIE_1L_RC_RSTZ	Output	PD	Active low	PCIe 1-Lane RC Reset Control ('0' - device reset, '1' - normal operation)
	P07	PCIE_1L_EP_RST_EN	Output	PD	Active low	PCIe 1-Lane EP Reset Enable ('0' - PERSTz isolated from PORz, '1' PERSTz connected to PORz)
	P10	PCIE_2L_PRSNT#	Input	PU	Active High	PCIE 2-Lane Hot Plug/Card Detect ('0' - PCIe Card Detected, '1' - no card detected)
	P11	PCIE_1L_PRSNT#	Input	PU	Active High	PCIE 1-Lane Hot Plug/Card Detect ('0' - PCIe Card Detected, '1' - no card detected)
	P12	CDCI1_OE1/OE4	Output	PU	Active High	PCIE 2L Reference Clock Enable ('0 - clock disabled, '1' - clock enabled)
	P13	CDCI1_OE2/OE3	Output	PU	Active High	PCIE 1L Reference Clock Enable ('0 - clock disabled, '1' - clock enabled)
	P14	EXP_MUX1	Output	NA	NA	Expansion Board Mux control1
	P15	EXP_MUX2	Output	NA	NA	Expansion Board Mux control2
	P16	EXP_MUX3	Output	NA	NA	Expansion Board Mux control3
	P17	GESI_EXP_PHY_RSTz	Output	PU	Active High	GESI expansion PHY Reset ('0' - device reset, '1' - normal operation)
GPIO Expander - 2 Part# TCA6424ARGJR						
I2C0/0x21	P00	APPLE_AUTH_RSTZ	Output	PD	Active low	Apple Authentication Chip Reset ('0' - device reset, '1' - normal operation)
	P01	MLB_RSTZ	Output	PD	Active low	MLB Interface Board Reset ('0' - board reset, '1' - normal operation)
	P02	GPIO_USD_PWR_EN	Output	PU	Active High	MicroSD Card Power Enable ('0' - power off, '1' - power on)
	P03	USBC_PWR_EN	Output	PU	Active High	USB-TypeC VBUS Controller Power Enable ('0' - power off, '1' - power on)
	P04	USBC_MODE_SEL1	Output	DIP_SEL	NA	USB-Type C Mode Select
	P05	USBC_MODE_SEL0	Output	DIP_SEL	NA	USBC_MODE_SEL[1:0]: '00' = DFP, '01' = DRP, '1x' = UFP
	P06	MCAN0_EN	Output	PD	Active High	MCAN0 PHY Enable ('0' - device disabled, '1' normal operation)
	P07	MCAN0_STB#	Output	PD	Active low	MCAN0 PHY Standby ('0' - device standby, '1' - normal operation)
	P10	MUX_SPARE	Output	NA	Test Point	Signal Mux Control ('0' - Not Used, '1' - Not Used)
	P11	MCASP/TRACE_MUX_S0	Output	PU	PU / DIP_SEL	Signal Mux Control, DIP switch allow default to either Trace or GPMC. · TRACE with MIPI-60 Interface (set to '1 / 1') · Expansion for GPMC Support (set to '1 / 0') Audio Codec/Tuner Support (set to '0 / 1')
	P12	MCASP/TRACE_MUX_S1	Output	PU		
	P13	MLB_MUX_SEL	Output	PD	NA	Signal Mux Control ('0' - MCAN2/Expansion, '1' - 3 Wire MLB)
	P14	MCAN_MUX_SEL	Output	PD	NA	Signal Mux Control ('0' - MCAN2/GPIO, '1' - Expansion/EQEP)
	P15	MCASP2/SPI3_MUX_SEL	Output	PD	NA	Signal Mux Control ('0' - Expansion/SPI3, '1' - Tuner I2S/MCASP2)
	P16	PCIe_CLKREQn_MUX_SEL	Output	PD	NA	Signal Mux Control ('0' - PCIe CLKREQn/I3C, '1' - Expansion GPIO)
	P17	CDCI2_RSTZ	Output	PU	Active low	Peripheral Clock Generator ('0' - device reset, '1' - normal operation)
	P20	ENET_EXP_PWRDN	Output	PD	Active High	Ethernet Expansion PHY Powerdown ('0' - normal operation, '1' - device power down)
	P21	ENET_EXP_RESETZ	Output	PU	Active low	Ethernet Expansion Reset ('0' - device reset, '1' - normal operation)
	P22	ENET_I2CMUX_SEL	Input	PD	NA	Signal Mux Control ('0' - No Connect , '1' - I2C0)
	P23	ENET_EXP_SPARE2	Input	NA	NA	Ethernet Expansion Spare2 ('0' - not defined, '1' - not defined)
	P24	M2PCIE_RTSZ	Output	PD	Active High	PCIe M.2 Reset ('0' - device reset, '1' - normal operation)
	P25	USER_INPUT1	Input	DIP_SEL	NA	User Dip Switch Input1 ('0' - User Define, '1' - User Define)
	P26	USER_LED1	Output	PD	Active High	User LED1 Enable ('1' - LED Off, '0' - LED On)
	P27	USER_LED2	Output	PD	Active High	User LED2 Enable ('1' - LED Off, '0' - LED On)
GPIO Expander - 3 Part# TCA6408ARGTR						
I2C3/0x20	P0	CODEC_RSTZ	Output	PD	Active low	Audio Codec Reset ('0' - device reset, '1' - normal operation)
	P1	CODEC_SPARE1	NA	UNUSED	NA	Not used (test point)
	P2	UB926_RESETN	Output	PD	Active low	Tuner Deserializer Reset ('0' - device reset, '1' - normal operation)
	P3	UB926_LOCK	Input	NA	NA	Tuner Deserializer Lock Status ('0' - Lock status, '1' - Lock status)
	P4	UB926_PWR_SW_CNTRL	Output	PD	NA	Tuner Board Power Enable ('0' - power off, '1' - power on)
	P5	UB926_TUNER_RESET	Output	PD	Active low	Tuner Device Reset ('0' - device reset, '1' - normal operation)
	P6	UB926_GPIO_SPARE	Output	PD	NA	Tuner Device Spare ('0' - TBD, '1' - TBD)
	P7	UNUSED	NA	NA	NA	No Connect
GPIO Expander - 4 Part# TCA6408ARGTR						
I2C1/0x20	P0	DP0_PWR_SW_EN	Output	PD	Active High	DisplayPort0 Power Enable ('0' - power off, '1' - power on)
	P1	DP1_PWR_SW_EN	Output	PD	Active High	DisplayPort1 Power Enable ('0' - power off, '1' - power on)
	P2	UB981_PDB	Output	PD	Active low	DSI Display Power Down/Reset ('0' - device powerdown/reset, '1' - normal operation) Note: Resistor option to DSI_DISP_RST#
	P3	UB981_GPIO0	Output	NA	NA	Display Dependent. Backlight Enable ('0' - power off, '1' - power on)
	P4	UB981_GPIO1	Output	NA	NA	Display Dependent. Spare
	P5	UB981_GPIO2	Input	NA	NA	Display Dependent. Spare
	P6	UB981_GPIO3	Input	NA	NA	Display Dependent. Interrupt ('0' - interrupt pending, '1' - no interrupt)
	P7	PWR_SW_CNTL_DSI0	Output	PD	Active High	Display Panel Power Enable ('0' - power off, '1' - power on)
GPIO Expander - 5 Part# TCA6408ARGTR						
I2C6/0x20	P0	CSI2_EXP_RSTZ	Output	PD	Active low	CSI2 Expansion Interface Reset ('0' - device reset, '1' - normal operation)
	P1	CSI2_EXP_A_GPIO0	IO	NA	NA	CSI2 Expansion Spare GPIO1
	P2	CSI2_EXP_A_GPIO1	IO	NA	NA	CSI2 Expansion Spare GPIO0
	P3	CSI2_EXP_A_GPIO3	IO	NA	NA	CSI2 Expansion Spare GPIO3
	P4	CSI2_EXP_B_GPIO1	IO	NA	NA	CSI2 Expansion Aux Spare GPIO1
	P5	CSI2_EXP_B_GPIO2	IO	NA	NA	CSI2 Expansion Aux Spare GPIO2
	P6	CSI2_EXP_B_GPIO3	IO	NA	NA	CSI2 Expansion Aux Spare GPIO3
	P7	CSI2_EXP_B_GPIO4	IO	NA	NA	CSI2 Expansion Aux Spare GPIO4

NOTE:EXP_ENET_RSTz Signal Default state changed to Pull down in REV E3

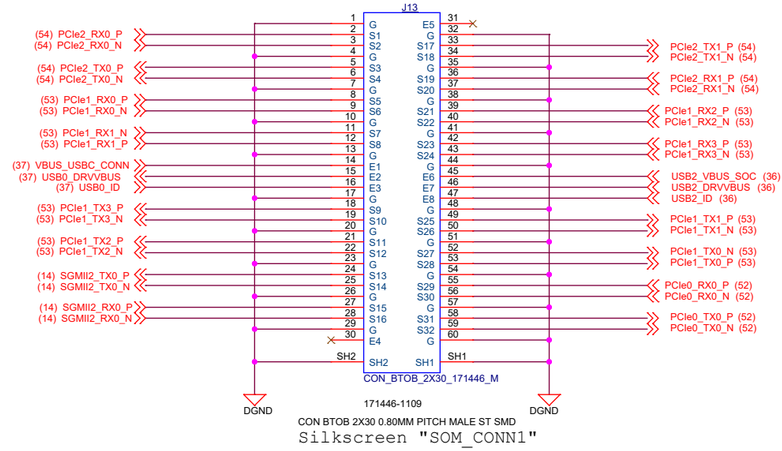
Project : J7 EVM	TEXAS INSTRUMENTS	Title: GPIO EXPANDER MAP/TABLE Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B Date: Thursday, November 21, 2019 — Sheet 8 of 68

SOM B-B MOLEX CONNECTORS

PCIe M.2

PCIe x4 Lane & USBC

SGMII



Silkscreen "SOM_CONN1"

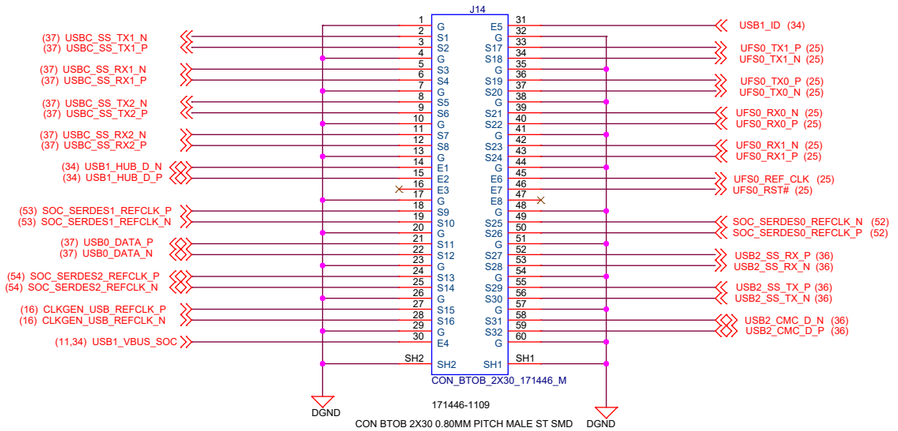
PCIe M.2

PCIe x4 Lane & USB2

PCIe x1 Lane

USB TYPE C

USB1 --> HUB



UFS

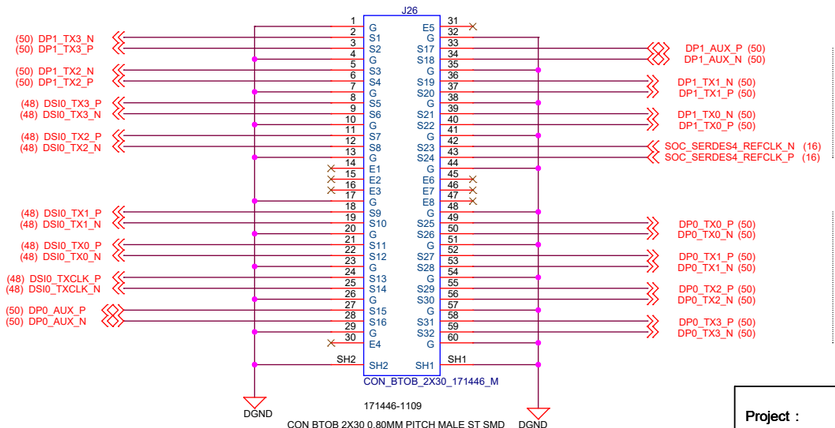
USB2 --> 3.0 uAB

Silkscreen "SOM_CONN2"

DP1

DSI0

DP0



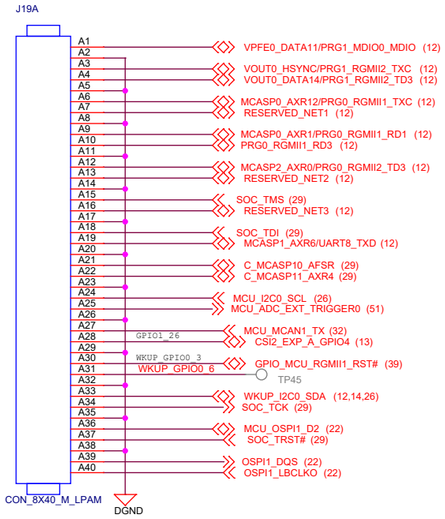
DP1

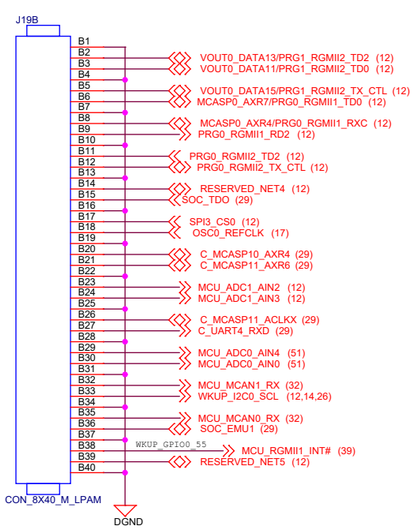
DP0

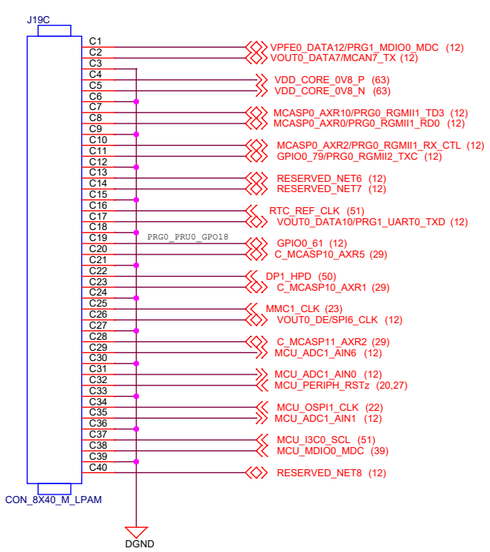
Silkscreen "SOM_CONN3"

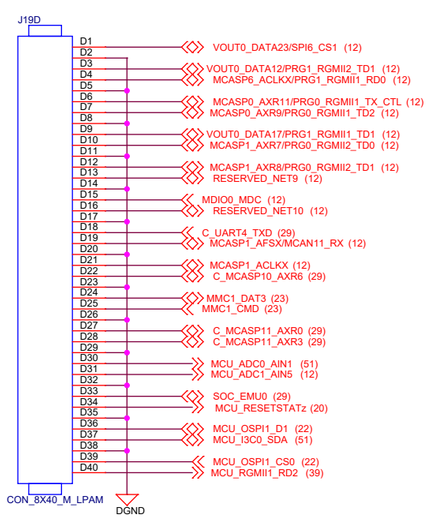
Project : J7 EVM	TEXAS INSTRUMENTS	Title: SOM B-B MOLEX CONNECTORS
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 9 of 68

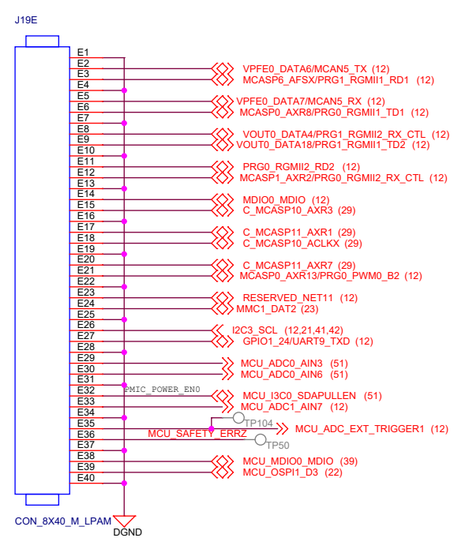
SOM B-B SAMTEC CONN#1

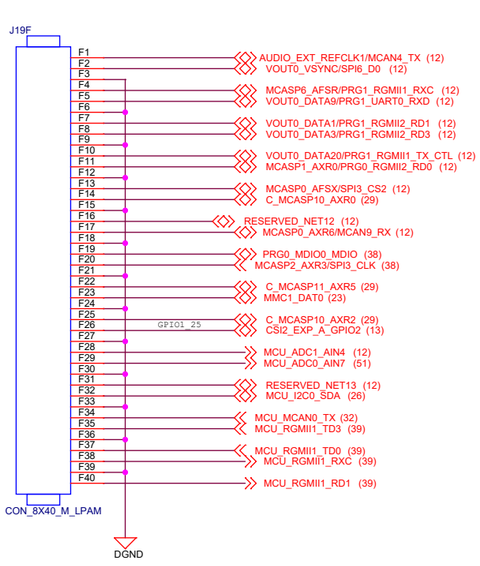


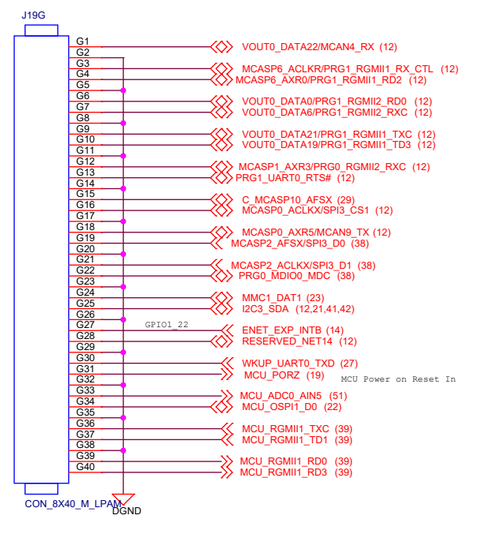


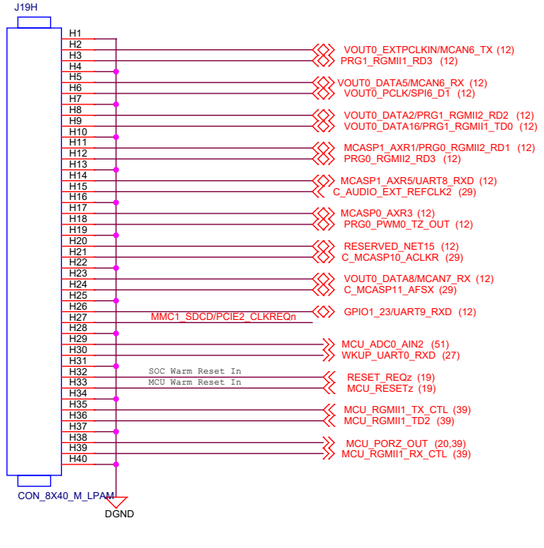


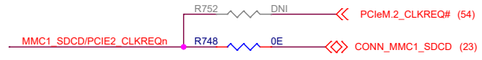






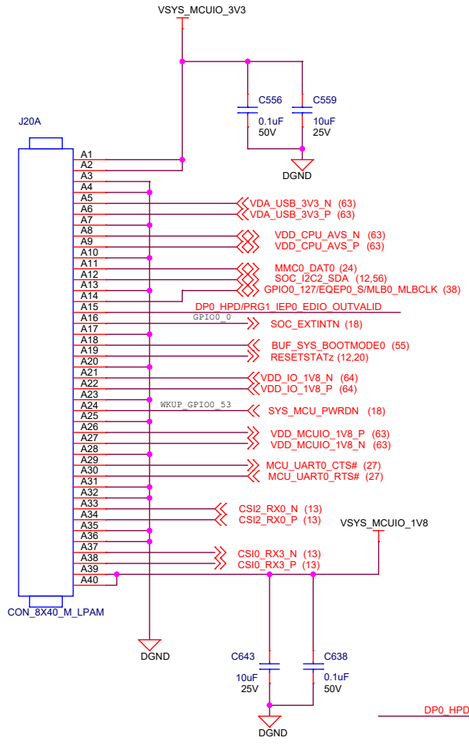


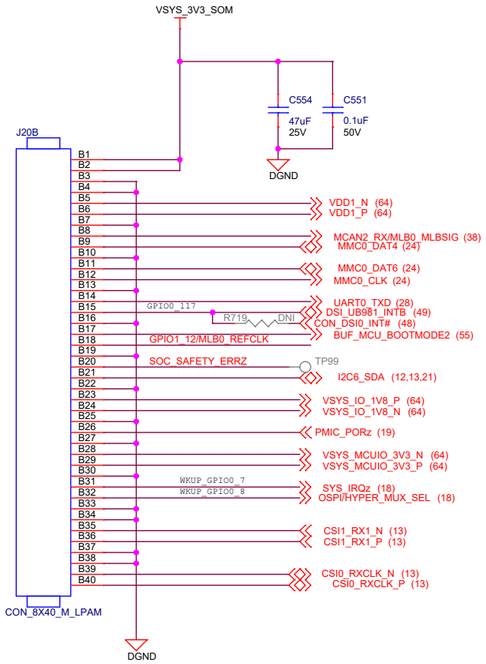


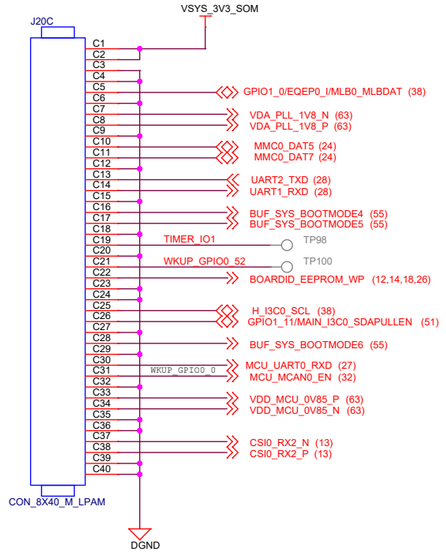


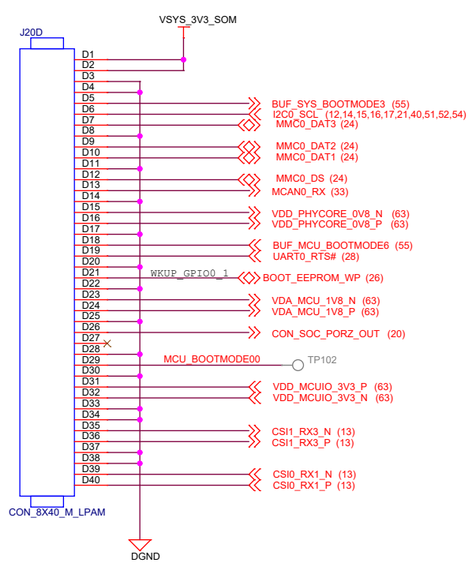
Project : J7 EVM		Title: SOM B-B SAMTEC CONN#1	
		Size: C	PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 10 of 68

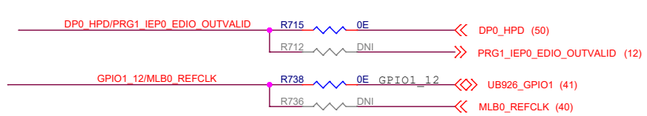
SOM B-B SAMTEC CONN#2

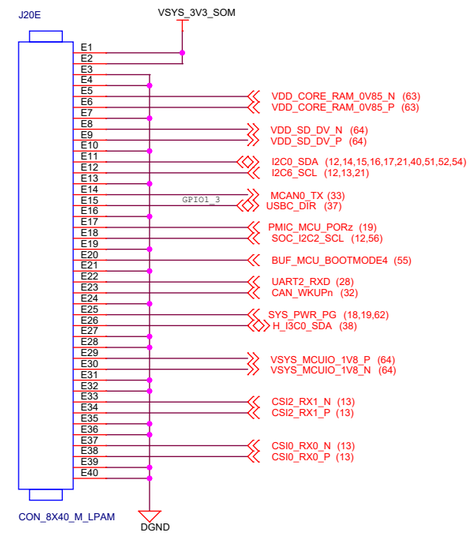


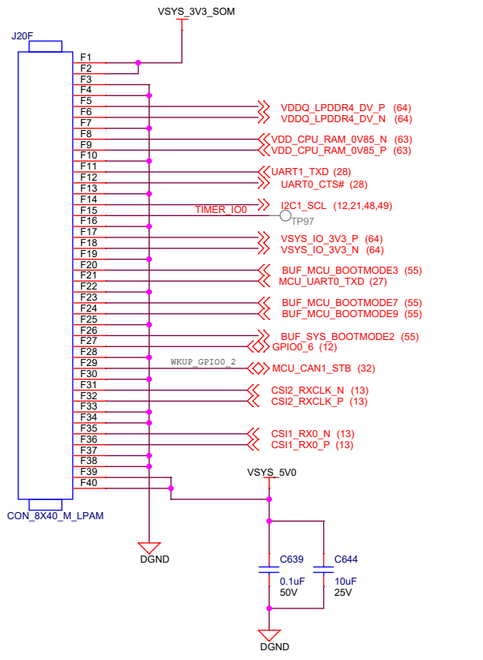


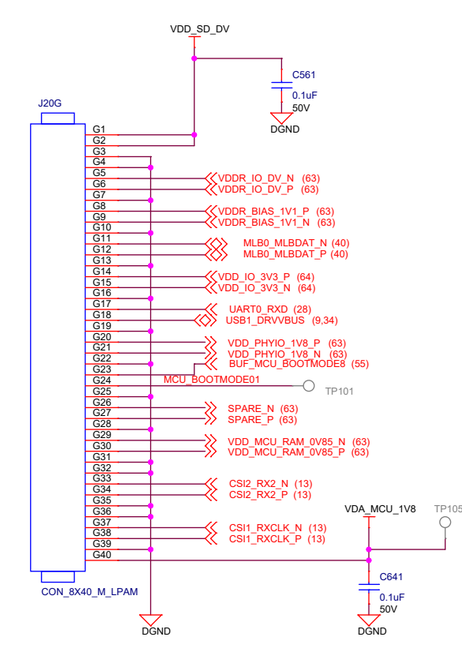


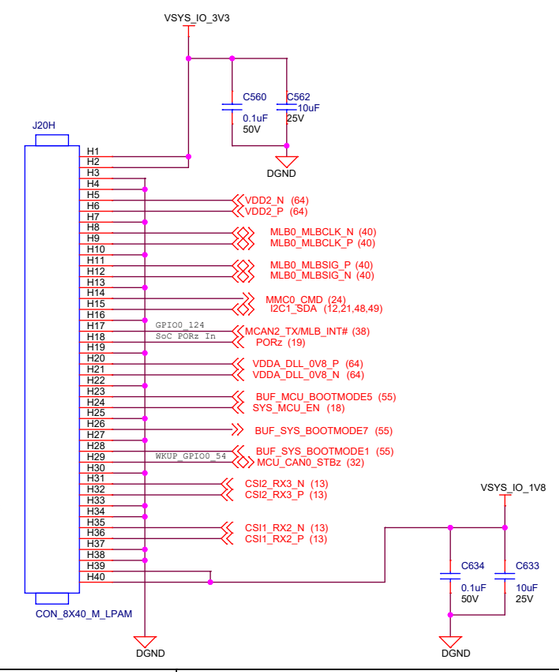






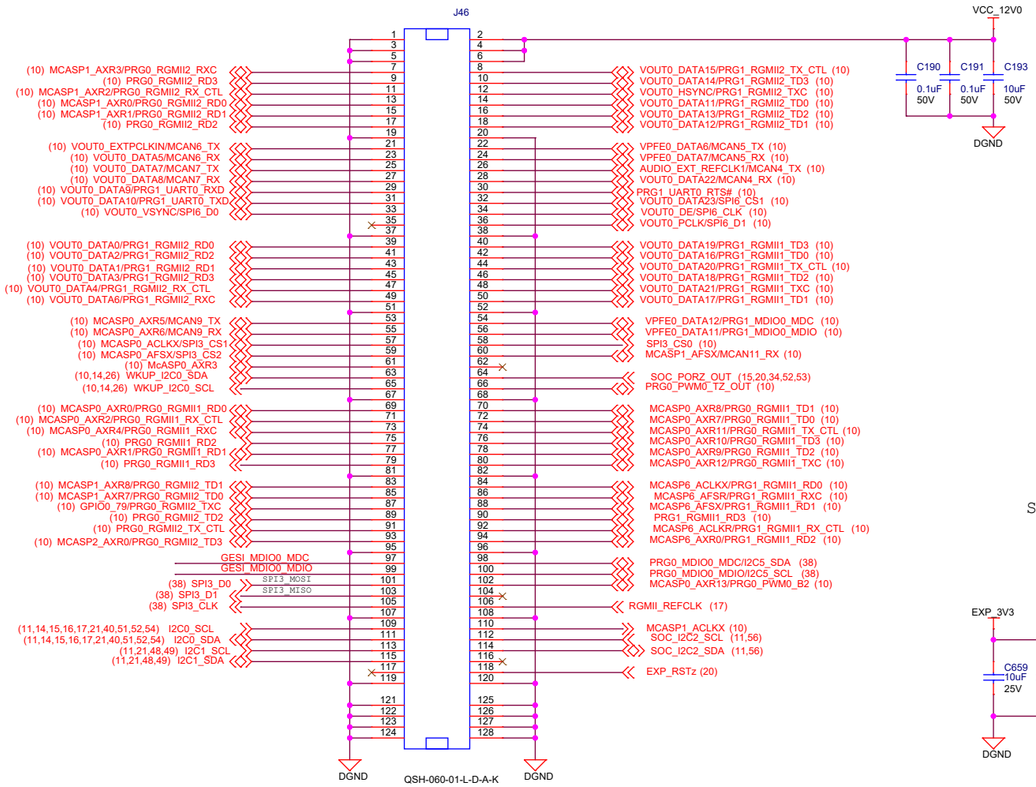




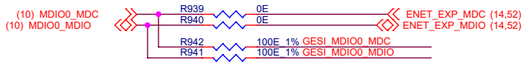


Project : J7 EVM	TEXAS INSTRUMENTS	Title: SOM B-B SAMTEC CONN#2
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 11 of 68

INFO/GESI_EXP_CONN



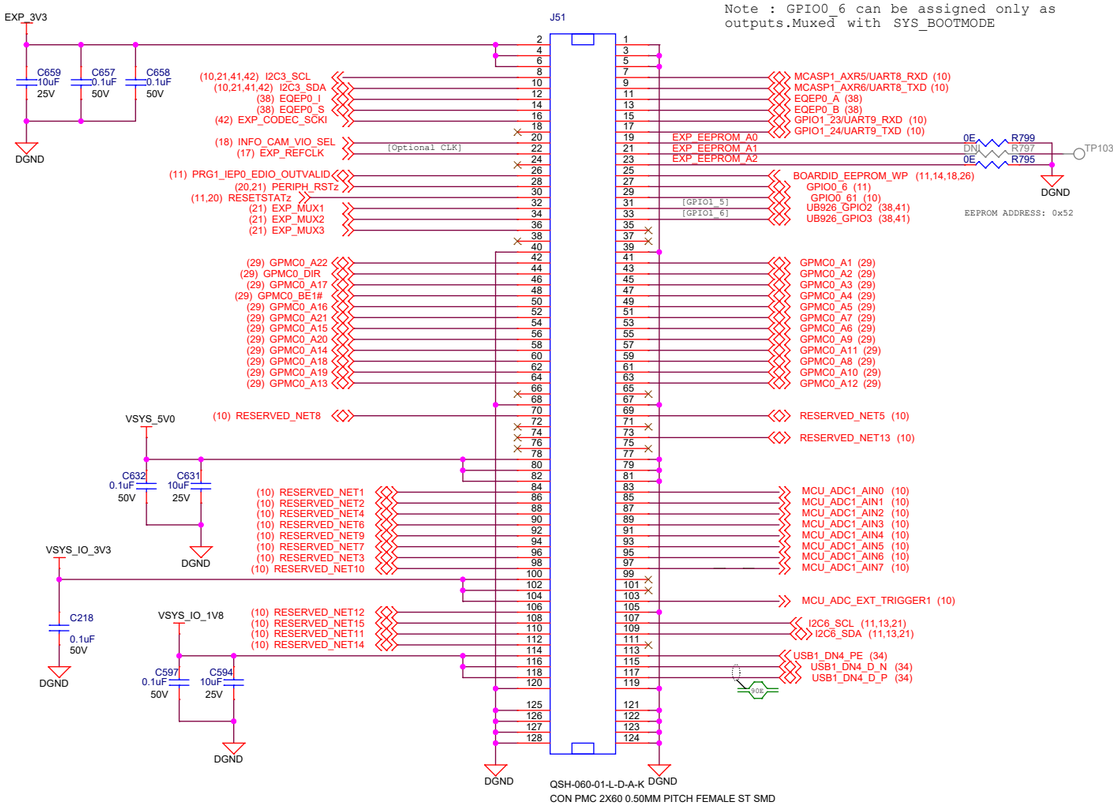
CON PMC 2X60 0.50MM PITCH FEMALE ST SMD



NOTE:Keep this Resistors close to J46

Silkscreen "EVM EXPANSION"

Note : GPIO0_6 can be assigned only as outputs.Muxed with SYS_BOOTMODE

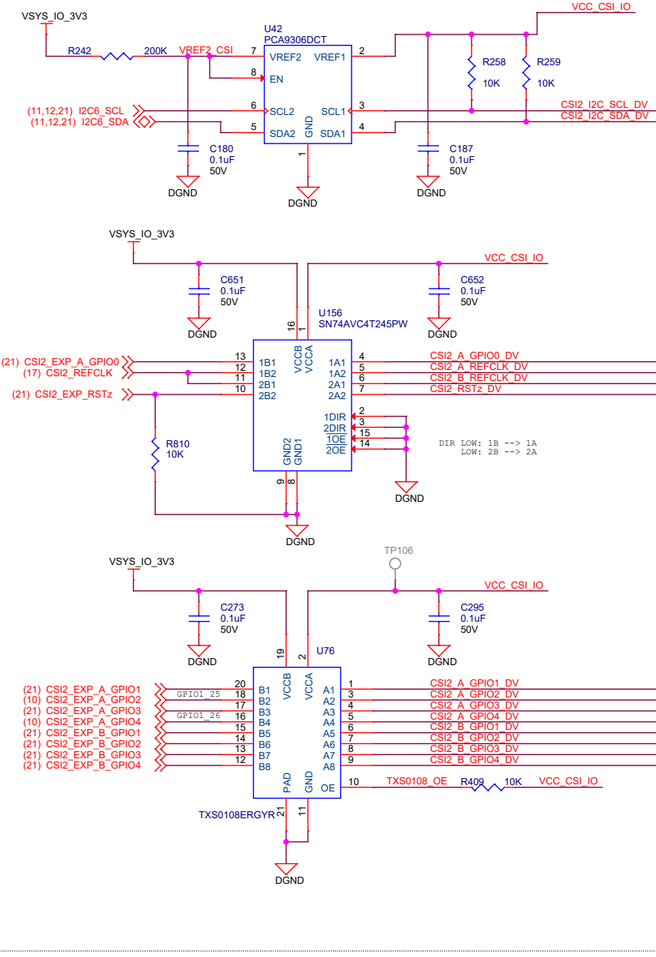


CON PMC 2X60 0.50MM PITCH FEMALE ST SMD

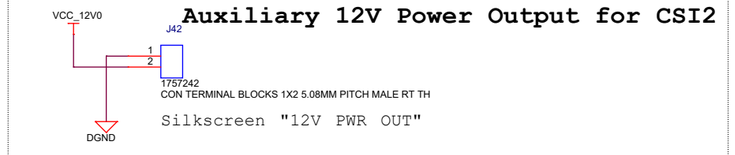
Project : J7 EVM	TEXAS INSTRUMENTS	Title: INFO/GESI_EXP_CONN
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 12 of 68

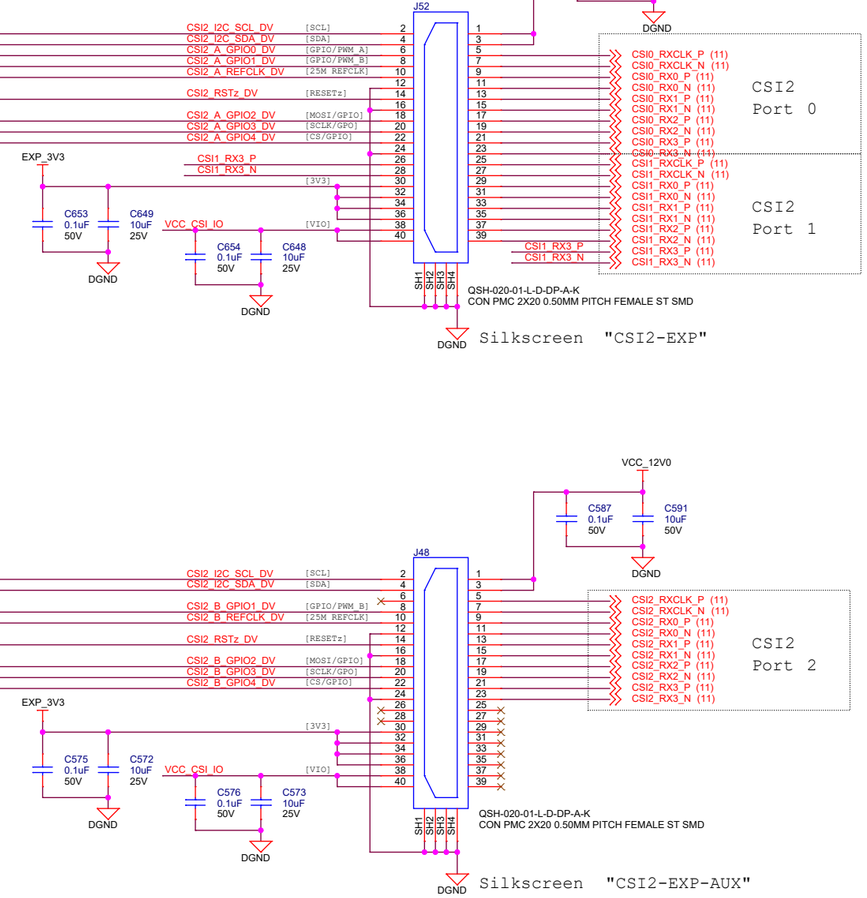
CSI2 EXPANSION CONNECTORS

Level Translation for LVCMOS

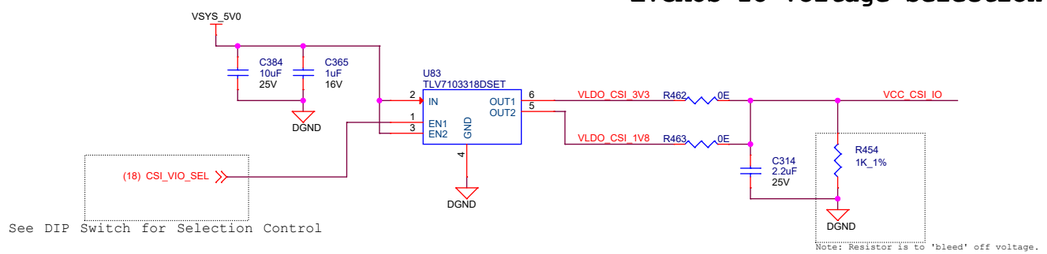


Auxiliary 12V Power Output for CSI2



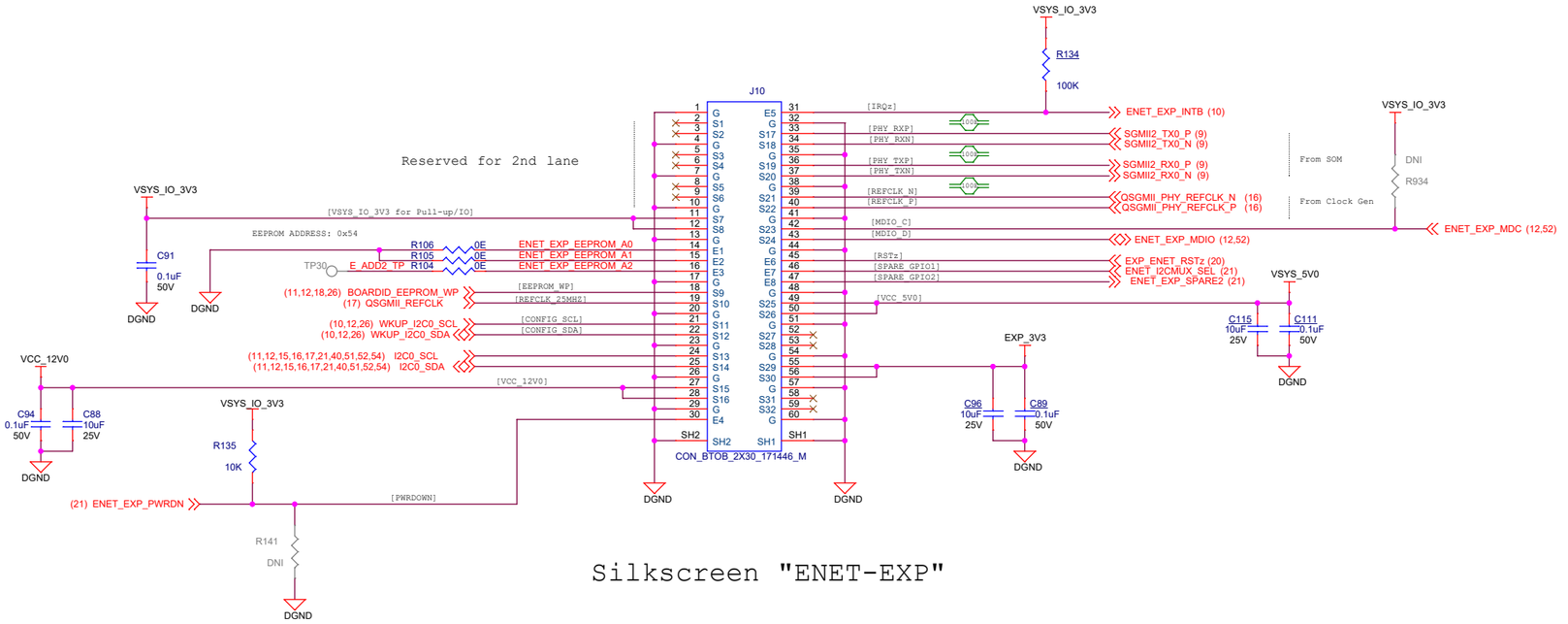


LVCMOS IO Voltage Selection



Project : J7 EVM	TEXAS INSTRUMENTS	Title: CSI2 EXPANSION CONNECTORS	
		Size: C	PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 13 of 68

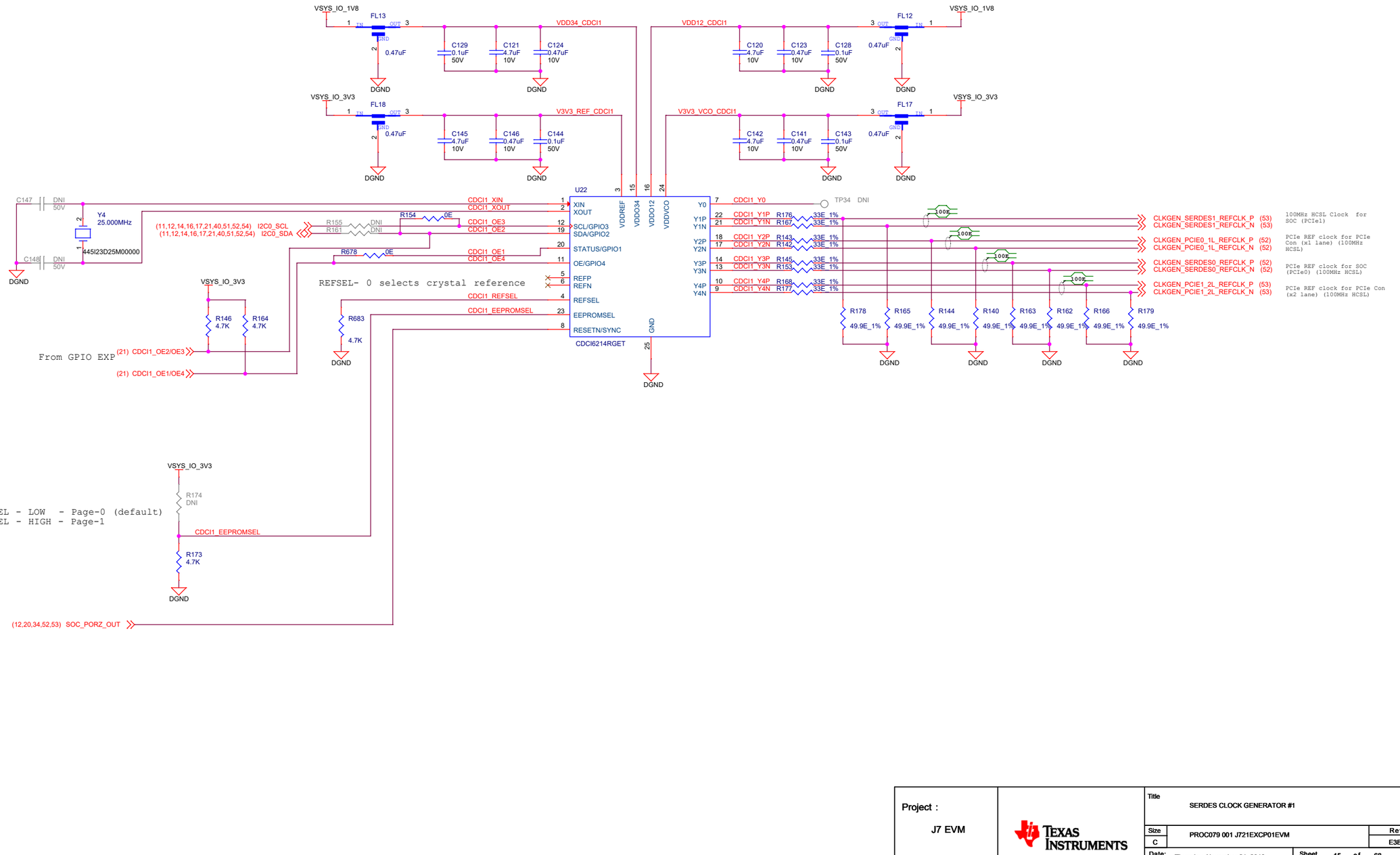
ENET EXPANSION CONNECTOR



Silkscreen "ENET-EXP"

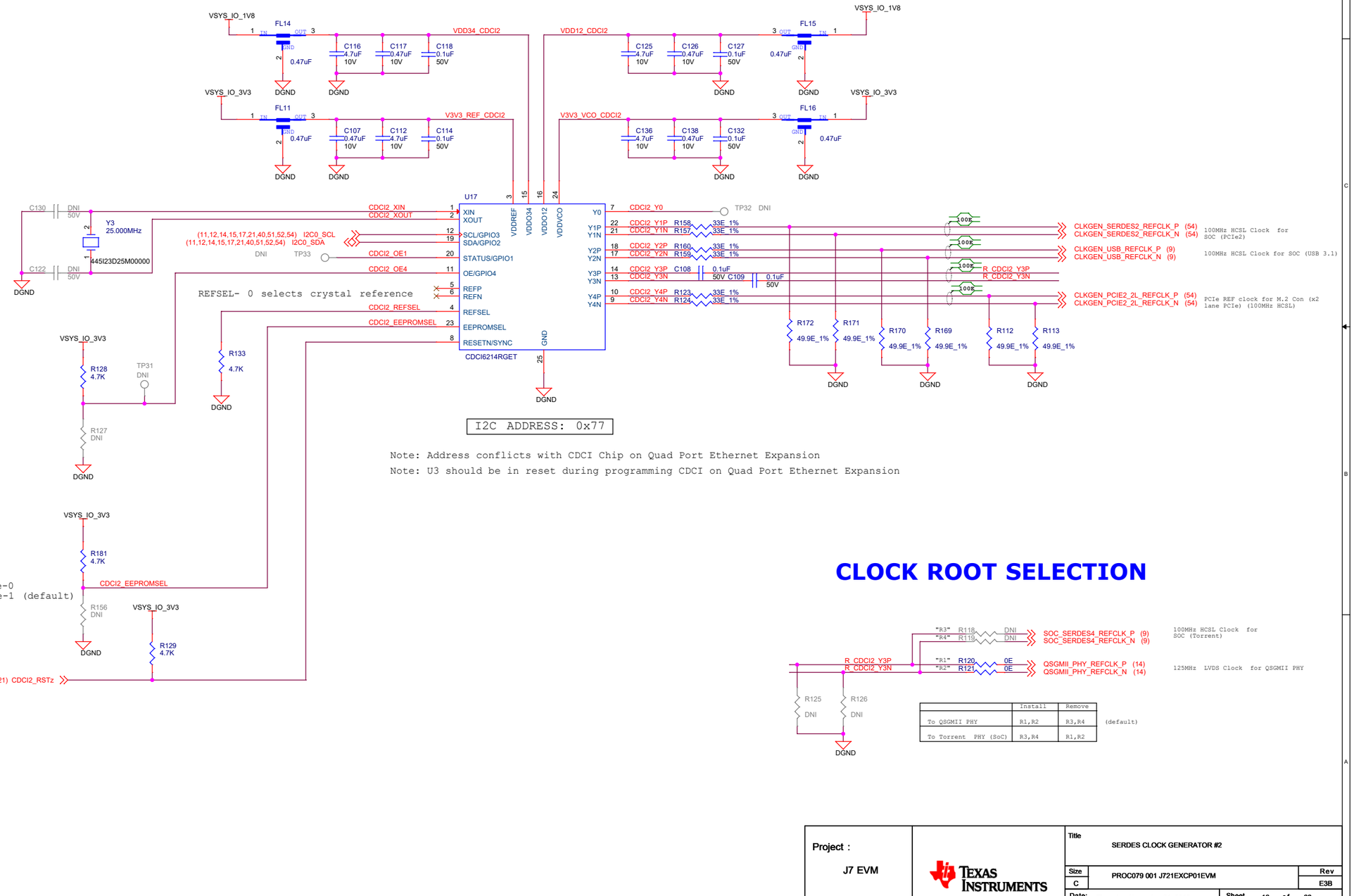
Project : J7 EVM	TEXAS INSTRUMENTS	Title: ENET EXPANSION CONNECTOR
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 14 of 68

SERDES CLOCK GENERATOR #1



Project : J7 EVM	TEXAS INSTRUMENTS	Title: SERDES CLOCK GENERATOR #1
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 15 of 68

SERDES CLOCK GENERATOR #2

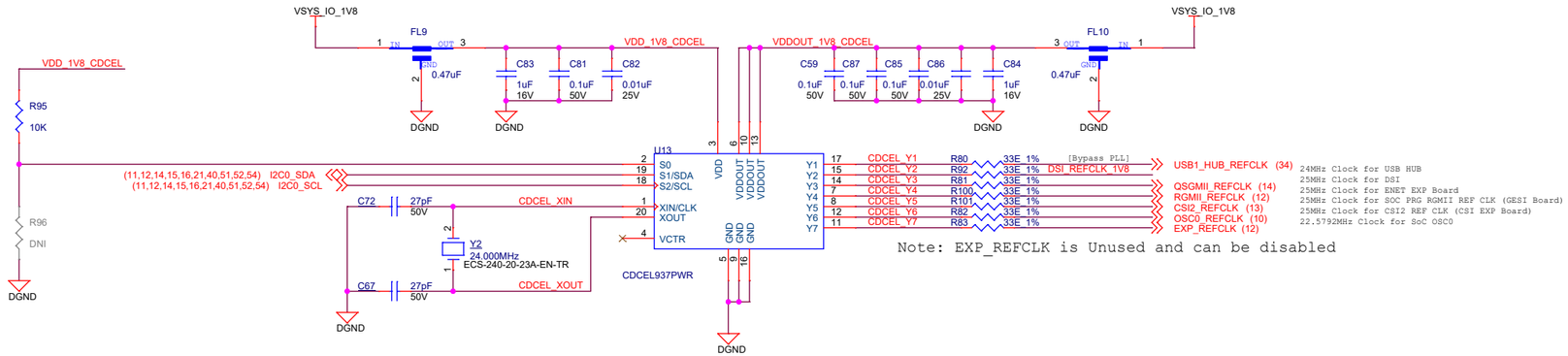


CLOCK ROOT SELECTION

	Install	Remove	
To QSGMII PHY	R1,R2	R3,R4	(default)
To Torrent PHY (SoC)	R3,R4	R1,R2	

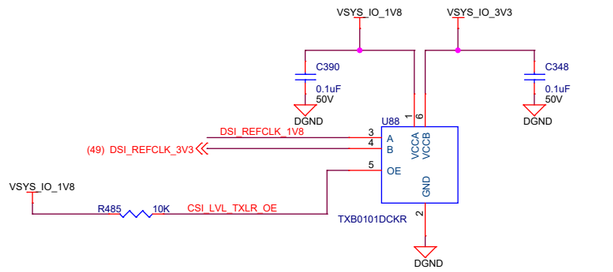
Project : J7 EVM	TEXAS INSTRUMENTS	Title: SERDES CLOCK GENERATOR #2	
		Size: C — PROC079 001 J721EXCP01EVM	Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 16 of 68

PERIPHERAL CLOCK GENERATOR



I2C ADDRESS: 0x6D

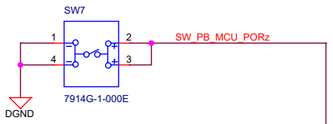
Level Translator for DSI REFCLK



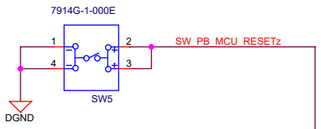
Project : J7 EVM	TEXAS INSTRUMENTS	Title: PERIPHERAL CLOCK GENERATOR	
		Size: C — PROC079 001 J721EXCP01EVM	Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 17 of 68

RESET BUTTONs

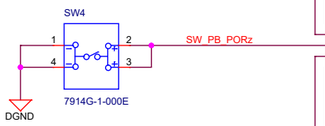
SILK: "MCU PORZ"



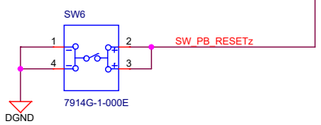
SILK: "MCU WARM RESET"



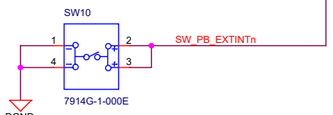
SILK: "MAIN PORZ"



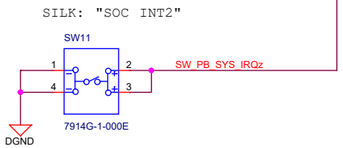
SILK: "MAIN WARM RESET"



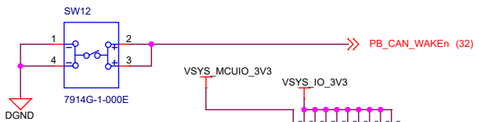
SILK: "SOC INT1"

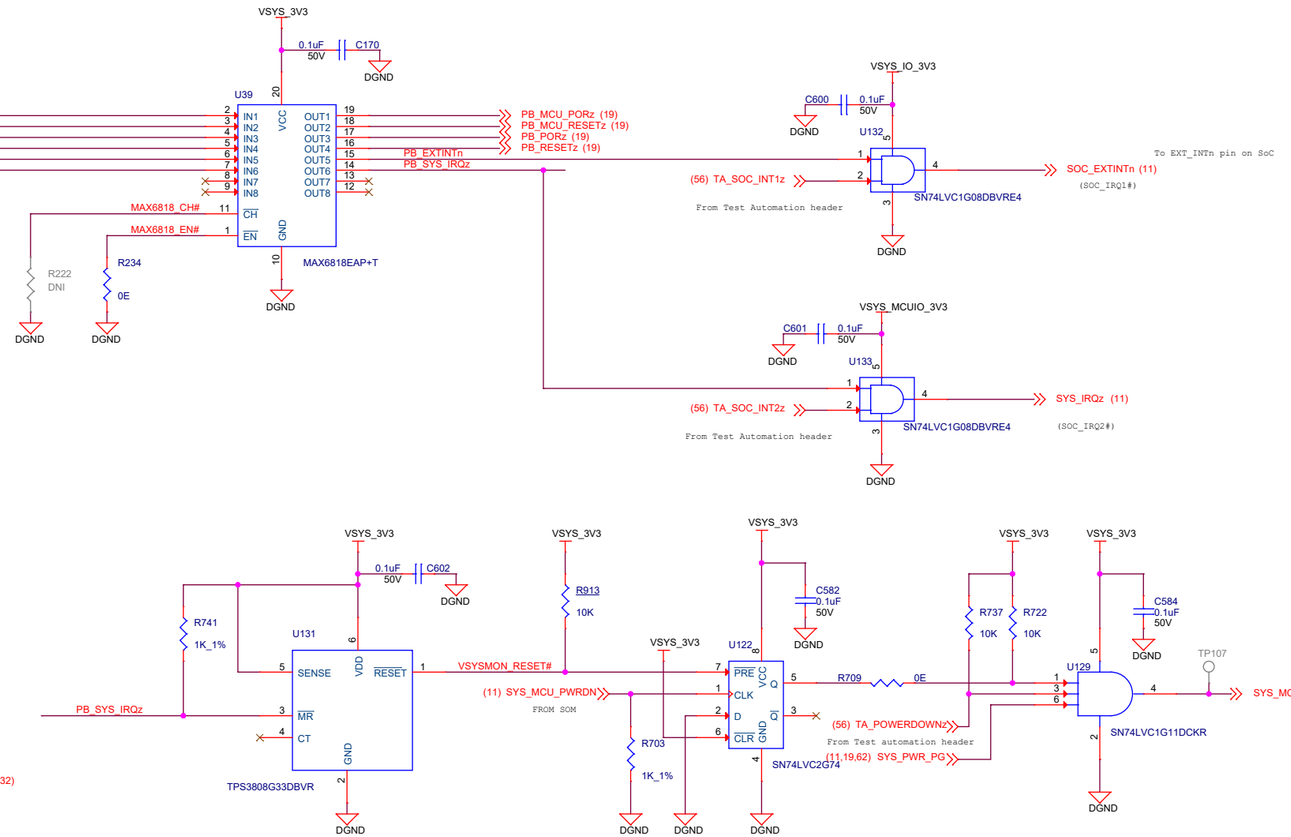


SILK: "SOC INT2"

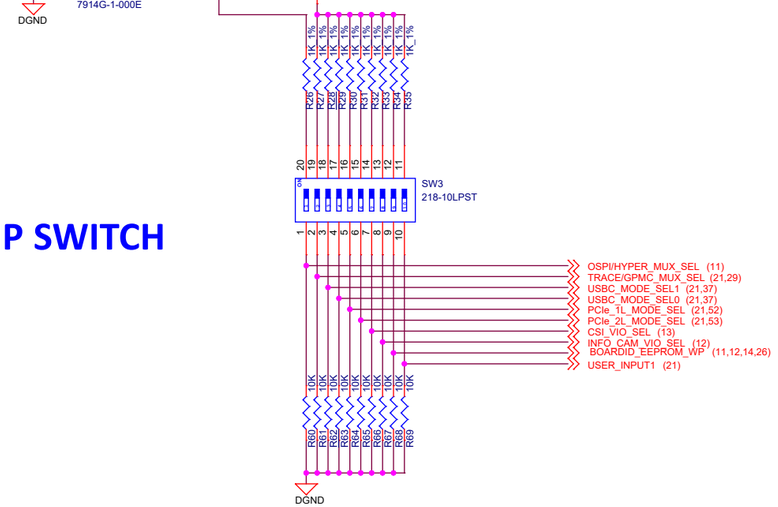


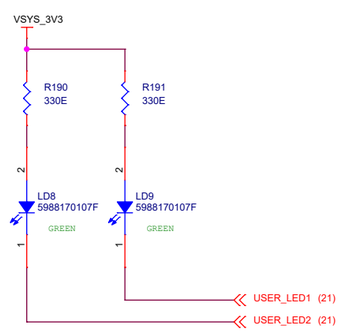
SILK: "CAN_WAKE"





CONFIG DIP SWITCH

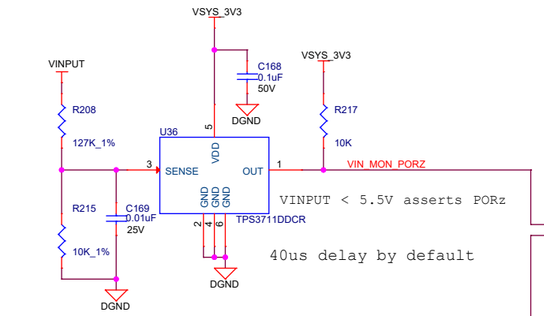




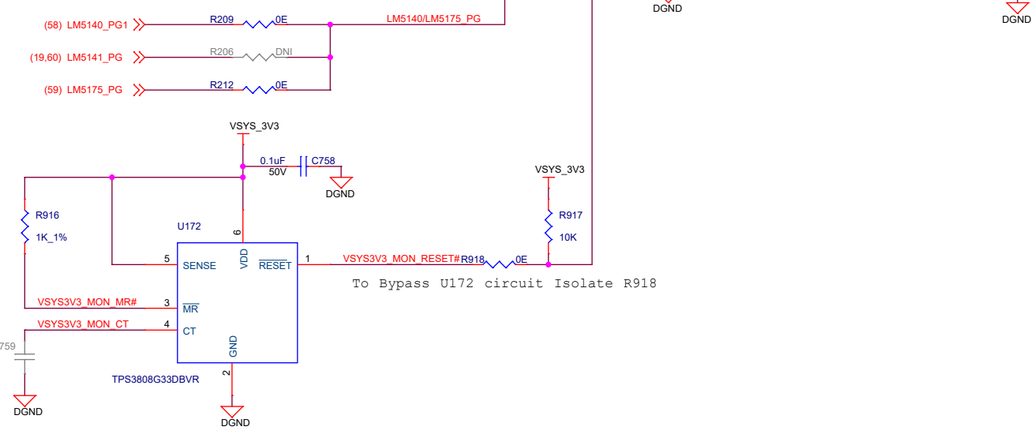
Project : J7 EVM	TEXAS INSTRUMENTS	Title: RESET BUTTONs
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 18 of 68

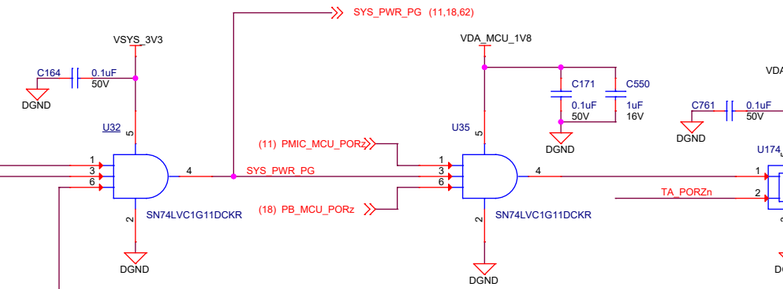
RESET INPUTS

Under Voltage Monitor (VINPUT)

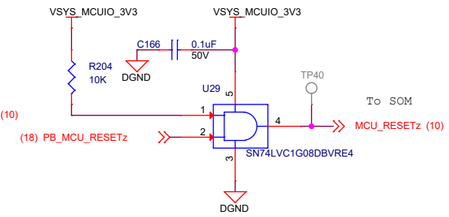


MCU PORZ

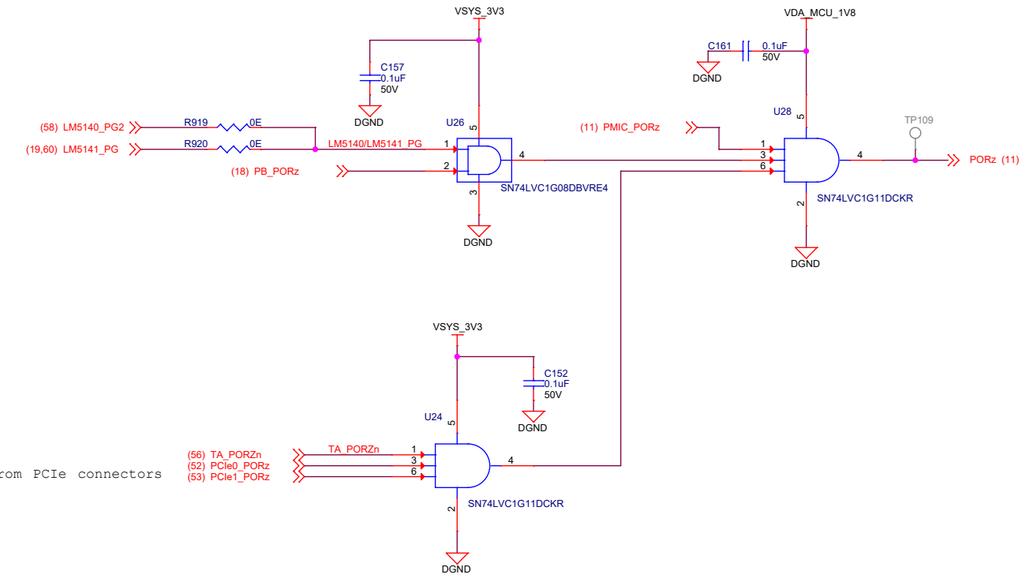




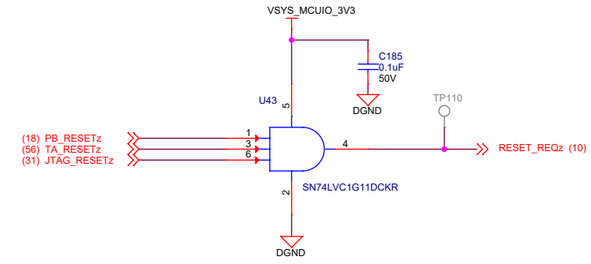
MCU_RESET



SOC PORZ

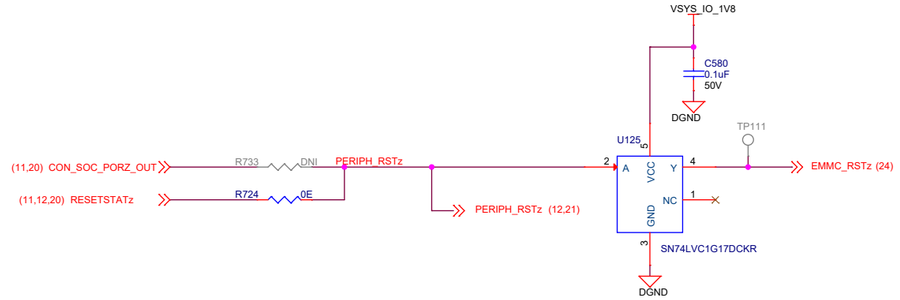


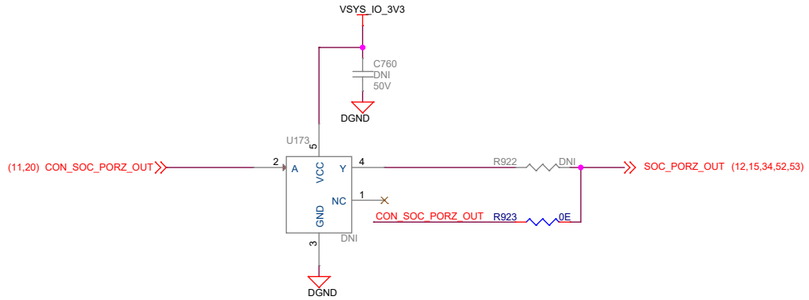
SOC RESET

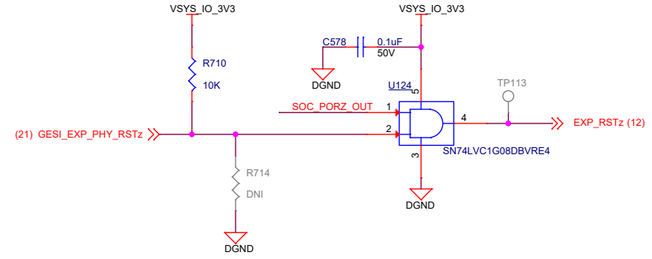


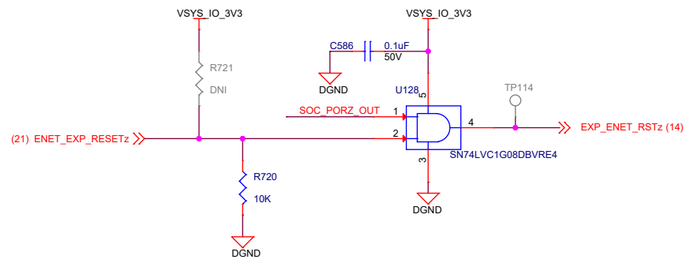
Project : J7 EVM	TEXAS INSTRUMENTS	Title: RESET INPUTS
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 19 of 68

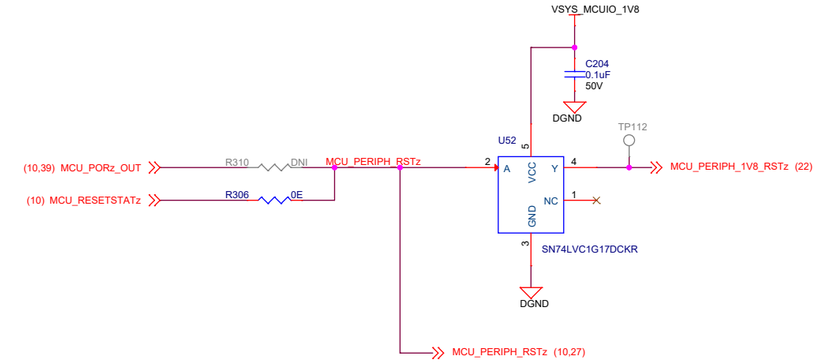
RESET OUTPUTS

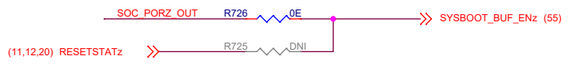








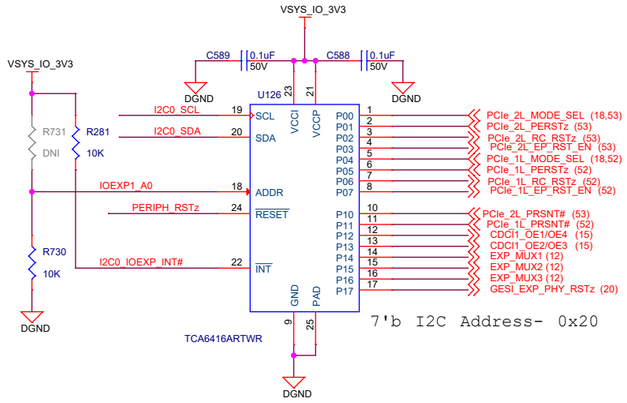




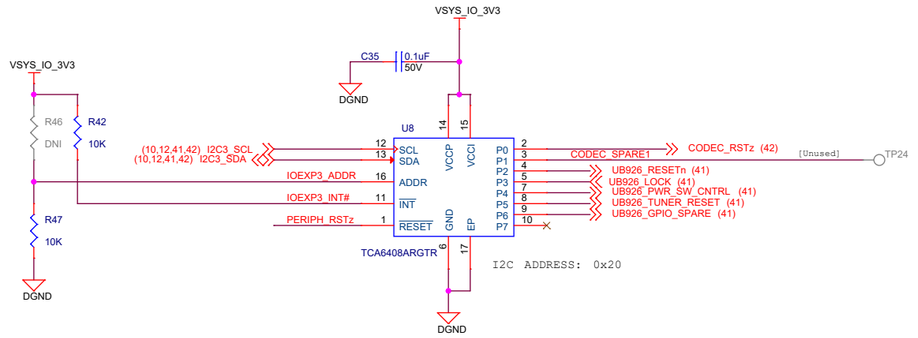
Project : J7 EVM	TEXAS INSTRUMENTS	Title: RESET OUTPUTS	
		Size: C — PROC079 001 J721EXCP01EVM	Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 20 of 68

GPIO EXPANDERS

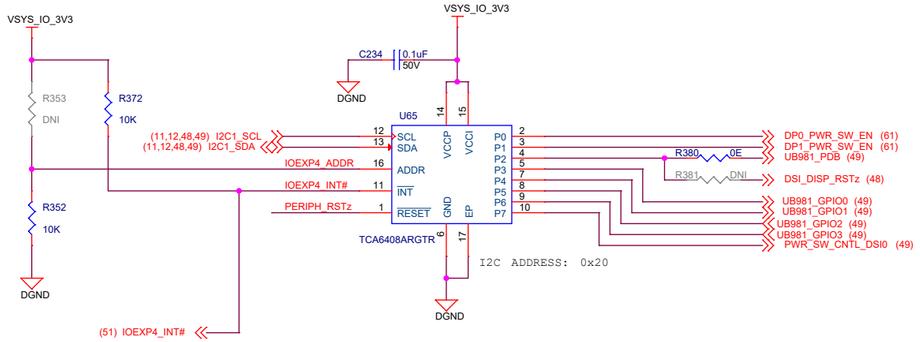
I2C GPIO EXPANDER1



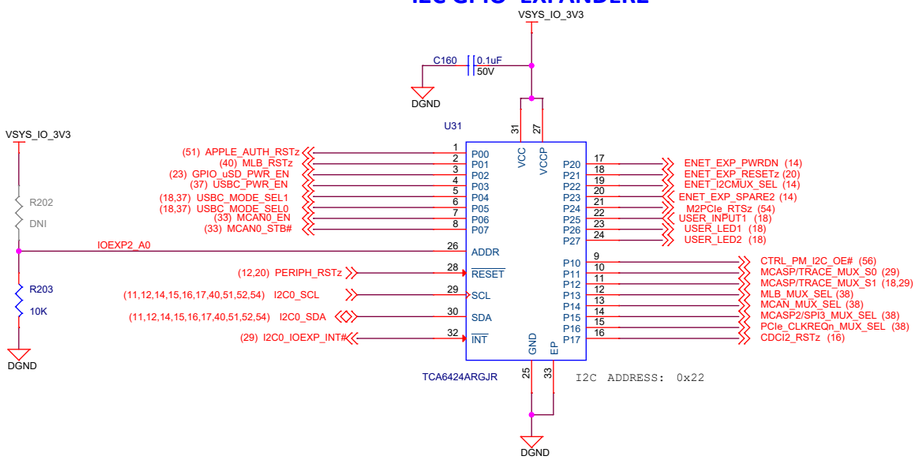
I2C GPIO EXPANDER3



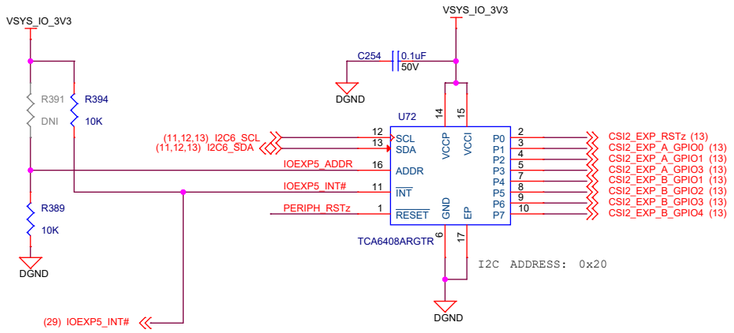
I2C GPIO EXPANDER4



I2C GPIO EXPANDER2

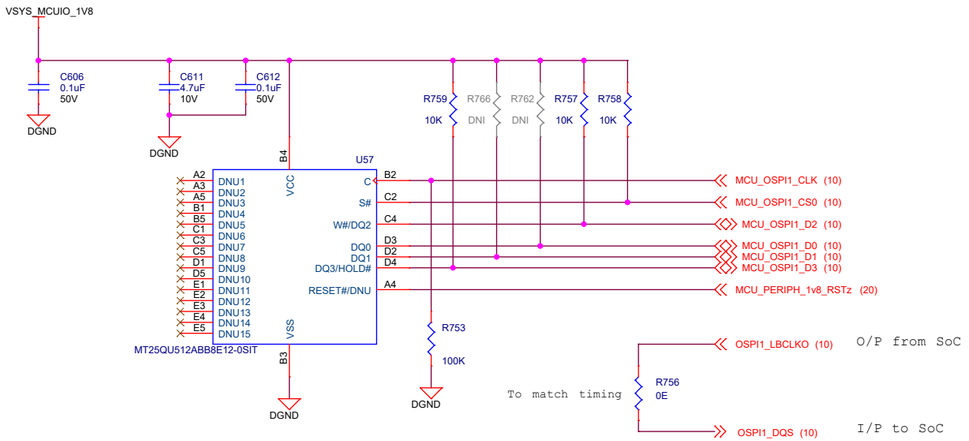


I2C GPIO EXPANDER5



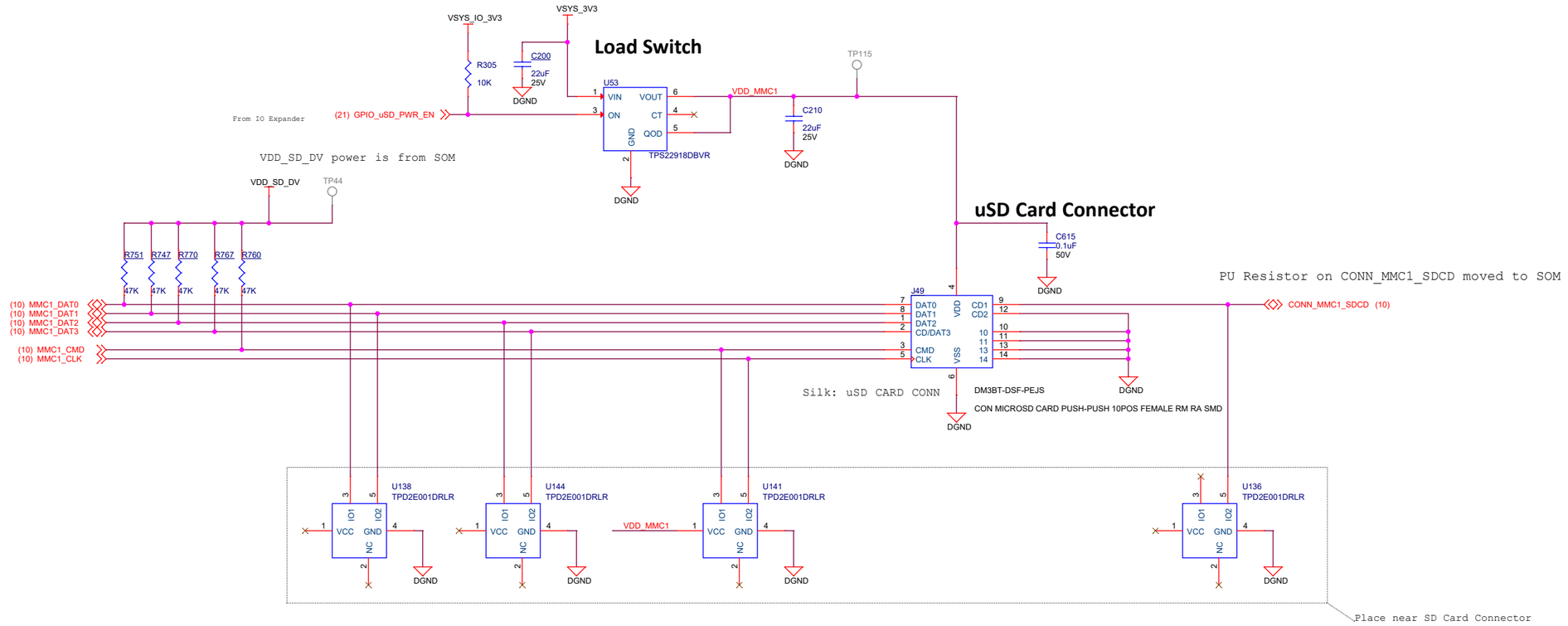
Project : J7 EVM	TEXAS INSTRUMENTS	Title: GPIO EXPANDERS	
		Size: C — PROC079 001 J721EXCP01EVM	Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 21 of 68

SPI NOR Flash



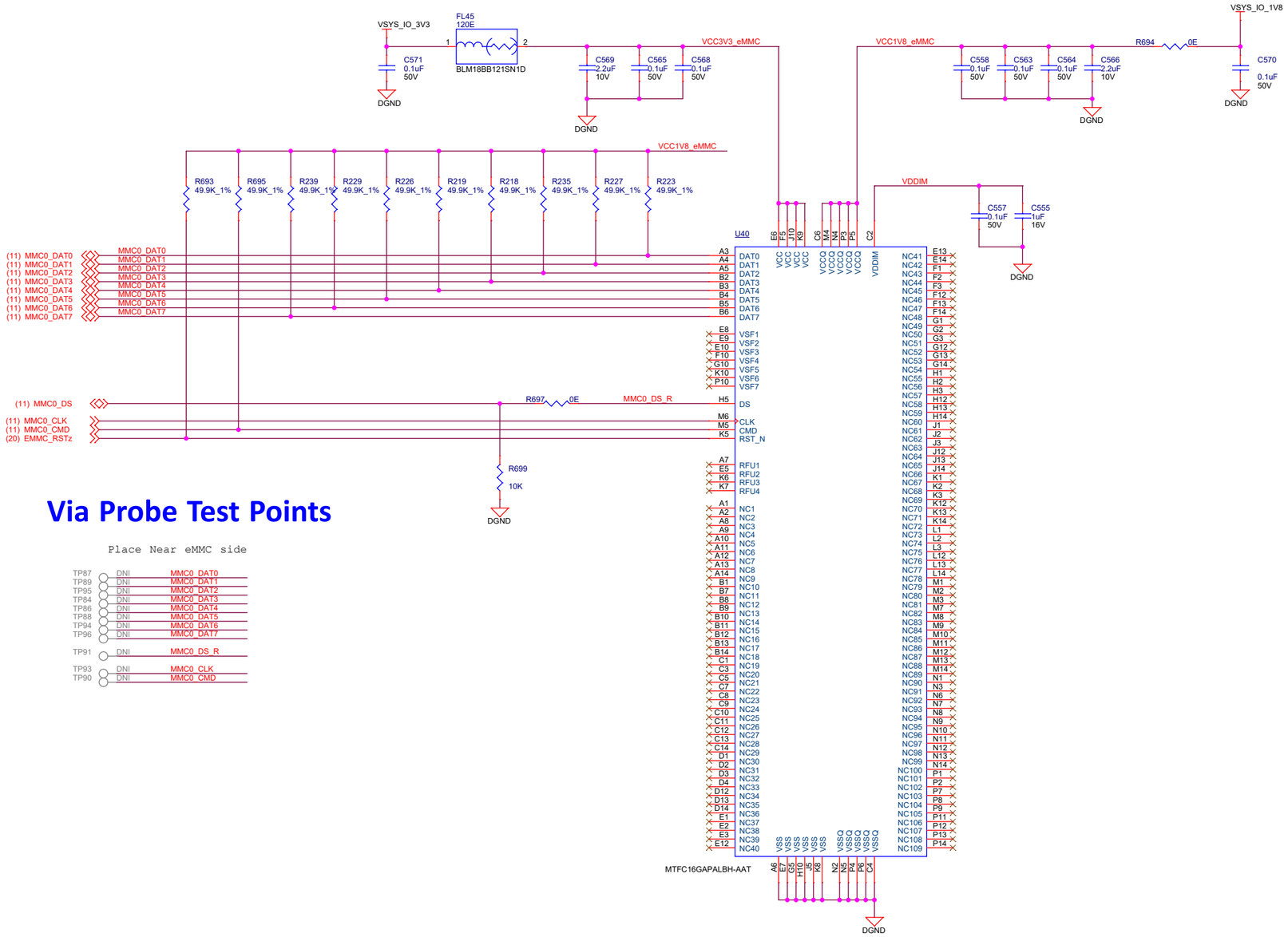
Project : J7 EVM	TEXAS INSTRUMENTS	Title: SPI NOR FLASH
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 22 of 68

Micro SD CARD INTERFACE



Project : J7 EVM	TEXAS INSTRUMENTS	Title: Micro SD CARD INTERFACE
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 23 of 68

eMMC FLASH



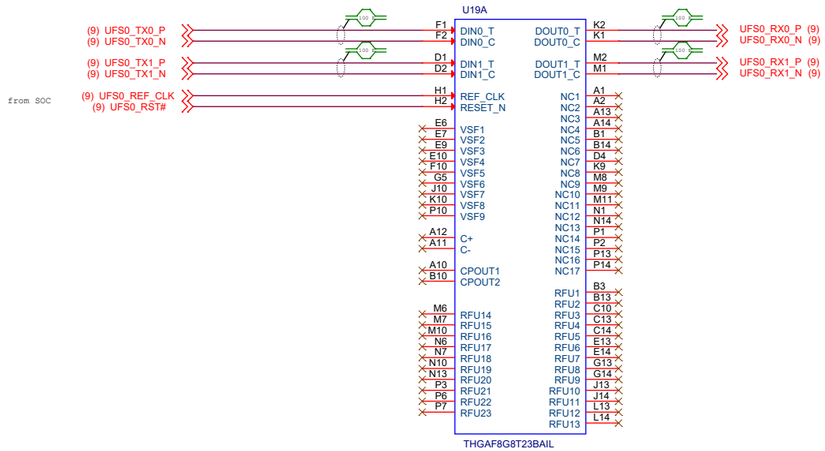
Via Probe Test Points

Place Near eMMC side

TP87	DNI	MMC0_DAT0
TP89	DNI	MMC0_DAT1
TP95	DNI	MMC0_DAT2
TP84	DNI	MMC0_DAT3
TP86	DNI	MMC0_DAT4
TP88	DNI	MMC0_DAT5
TP94	DNI	MMC0_DAT6
TP96	DNI	MMC0_DAT7
TP91	DNI	MMC0_DS_R
TP93	DNI	MMC0_CLK
TP90	DNI	MMC0_CMD

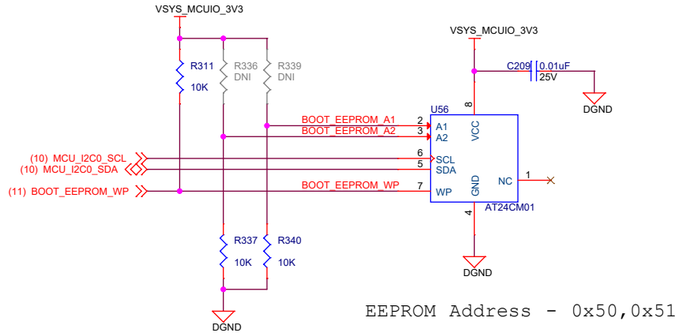
Project : J7 EVM	TEXAS INSTRUMENTS	Title: eMMC FLASH	
		Size: C	PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 24 of 68

UFS FLASH



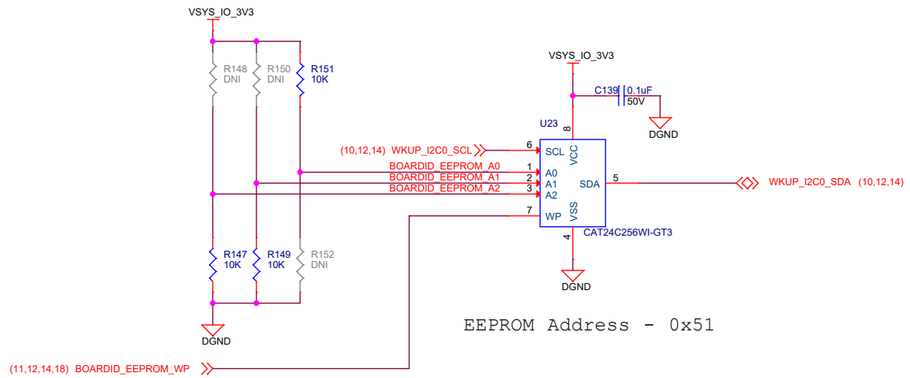
Project : J7 EVM	TEXAS INSTRUMENTS	Title: UFS FLASH	
		Size: C	PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 25 of 68

BOOT EEPROM



EEPROM Address - 0x50,0x51

BOARD ID EEPROM

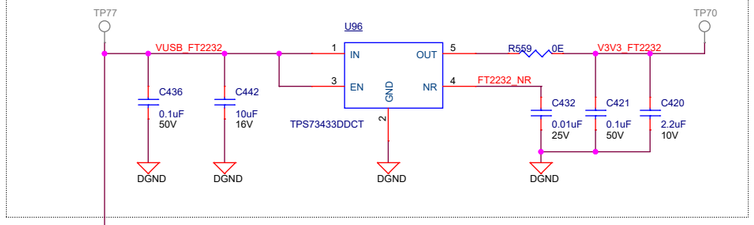


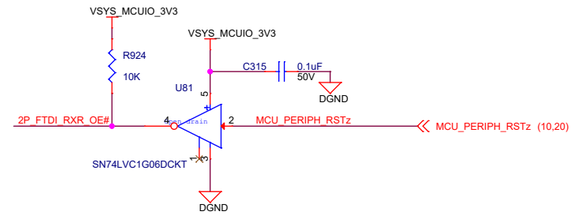
EEPROM Address - 0x51

Project : J7 EVM	TEXAS INSTRUMENTS	Title: EEPROM
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 26 of 68

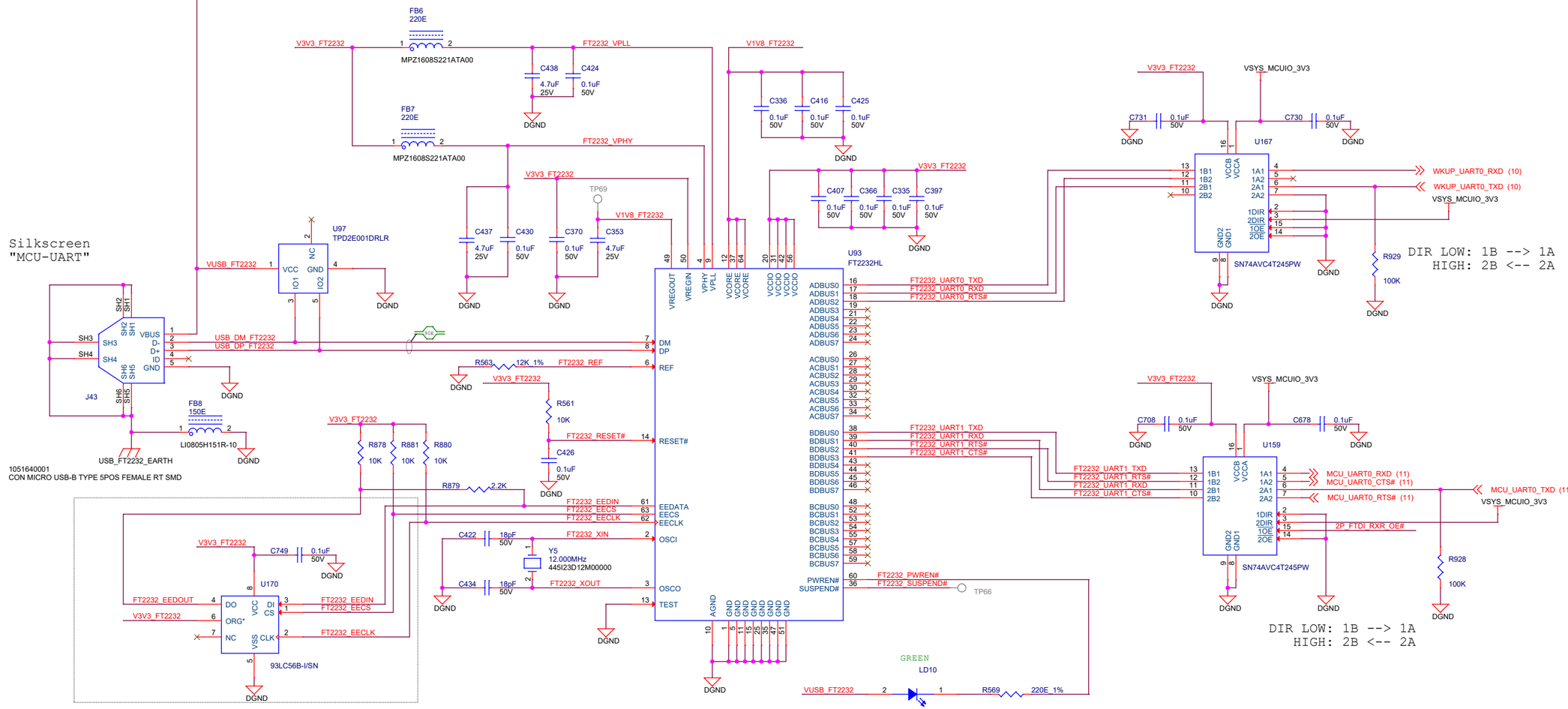
DUAL PORT FTDI

Note: FTDI Power sourced from USB.





Silkscreen "MCU-UART"



Note: FTDI EEPROM for storing manufacturing/configuration information.

Project : J7 EVM	TEXAS INSTRUMENTS	Title: DUAL PORT FTDI	
		Size: C	PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 27 of 68

QUAD PORT FTDI

Note: FTDI Power sourced from USB.

TP78 TP76

U171 TPS73433DDCT

VUSB_FT4232 → IN; OUT → R908 0E → V3V3_FT4232

EN → FT4232_NR

C755 0.1uF 50V DGND
C754 10uF 16V DGND
GND DGND
C750 0.01uF 25V DGND
C746 0.1uF 50V
C751 2.2uF 10V

FB4 220E — MPZ1608S221ATA00 — V3V3_FT4232 → FT4232_VPLL
C440 4.7uF 25V DGND
C427 0.1uF 50V

FB5 220E — MPZ1608S221ATA00 — FT4232_VPHY
C439 4.7uF 25V DGND
C431 0.1uF 50V

V1V8_FT4232
C337 0.1uF 50V
C417 0.1uF 50V
C428 0.1uF 50V DGND

V3V3_FT4232
C398 0.1uF 50V
C372 0.1uF 50V
C334 0.1uF 50V
C408 0.1uF 50V DGND

U98 TPD2E001DRLR
VUSB_FT4232 → VCC; NC; GND DGND; IO1; IO2

C371 0.1uF 50V DGND
TP71
V1V8_FT4232 → C354 4.7uF 25V DGND

Silkscreen "MAIN-UART"

J44
SH1 SH2 SH3 SH4 SH5 SH6
VBUS 1 — D- 2 — USB_DM_FT4232 — D+ 3 — USB_DP_FT4232 — ID 4 — GND 5 DGND

FB9 150E — LI0805H151R-10 — USB_FT4232_EARTH — DGND

1051640001
CON MICRO USB-B TYPE 5POS FEMALE RT SMD

U94 FT4232HL

VREGOUT	49	
VREGIN	50	
VPHY	4	
VPLL	9	
VCORE	12	
VCORE	37	
VCORE	64	
VCCIO	20	
VCCIO	31	
VCCIO	42	
VCCIO	55	
DM	7	
DP	8	
REF	6	R564 12K_1% DGND; V3V3_FT4232 → R562 10K
RESET	14	FT4232_RESET# → C429 0.1uF 50V DGND
EEDATA	61	FT4232_EEDIN
EECS	63	FT4232_EECS
EECLK	62	FT4232_EECLK
OSCI	2	FT4232_XIN
OSCO	3	FT4232_XOUT
TEST	13	
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8	1 5 11 15 25 35 47 51	
AGND	10	
PWREN	60	FT4232_PWREN#
SUSPEND	36	FT4232_SUSPEND# — TP67

V3V3_FT4232 → R874 10K; R877 10K; R876 10K
R875 2.2K

U169 93LC56B-I/SN
V3V3_FT4232 → C748 0.1uF 50V DGND
FT4232_EEDOUT ← DO; V3V3_FT4232 → ORG*; NC
VCC → DI ← FT4232_EEDIN; CS ← FT4232_EECS; CLK ← FT4232_EECLK; VSS DGND

C423 18pF 50V — Y6 12.000MHz 445I23D12M00000 — C435 18pF 50V DGND
FT4232_XIN; FT4232_XOUT

GREEN LD11
VUSB_FT4232 → 2 → 1 → R570 220E_1% — 5988170107F

Note: FTDI EEPROM for storing manufacturing/configuration information.

U168 SN74AVC4T245PW

FT4232_UART0_TXD	13	1B1
FT4232_UART0_RTS#	12	1B2
FT4232_UART0_RXD	11	2B1
FT4232_UART0_CTS#	10	2B2
UART0_RXD (11)	4	1A1
UART0_CTS# (11)	5	1A2
UART0_RTS# (11)	7	2A1
UART0_TXD (11)	6	2A2
VCCB	16	
VCCA	1	
1DIR	2	
2DIR	3	
1OE	15	
2OE	14	
GND2	9	
GND1	8	

V3V3_FT4232 → C734 0.1uF 50V DGND
VSYS_IO_3V3 → C733 0.1uF 50V DGND
R930 100K DGND

DIR LOW: 1B --> 1A
HIGH: 2B <-- 2A

U161 SN74AVC4T245PW

FT4232_UART1_TXD	13	1B1
FT4232_UART1_RXD	11	1B2
FT4232_UART2_TXD	12	2B1
FT4232_UART2_RXD	10	2B2
UART1_RXD (11)	4	1A1
UART2_RXD (11)	5	1A2
UART1_TXD (11)	6	2A1
UART2_TXD (11)	7	2A2
VCCB	16	
VCCA	1	
1DIR	2	
2DIR	3	
1OE	15	
2OE	14	
GND2	9	
GND1	8	

V3V3_FT4232 → C707 0.1uF 50V DGND
VSYS_IO_3V3 → C709 0.1uF 50V DGND
R931 100K DGND
R932 100K DGND

DIR LOW: 1B --> 1A
HIGH: 2B <-- 2A

U84 SN74AVC4T245PW

FT4232_UART3_TXD	13	1B1
FT4232_UART3_RXD	11	1B2
	12	2B1
	10	2B2
UART4_RXD (29)	4	1A1
	5	1A2
UART4_TXD (29)	6	2A1
	7	2A2
VCCB	16	
VCCA	1	
1DIR	2	
2DIR	3	
1OE	15	
2OE	14	
GND2	9	
GND1	8	

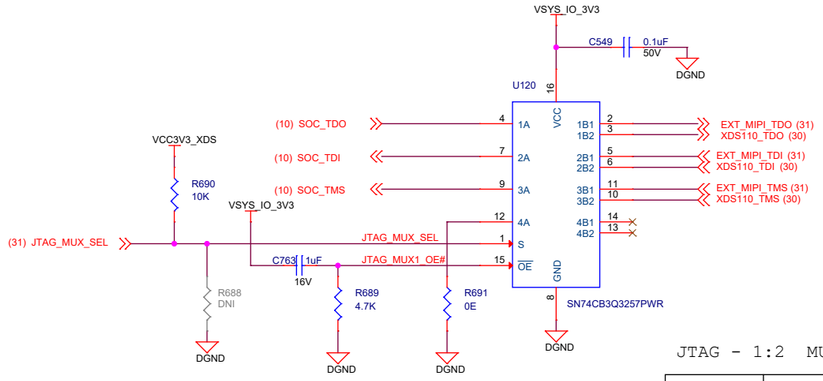
V3V3_FT4232 → C401 0.1uF 50V DGND
VSYS_IO_3V3 → C343 0.1uF 50V DGND
R933 100K DGND

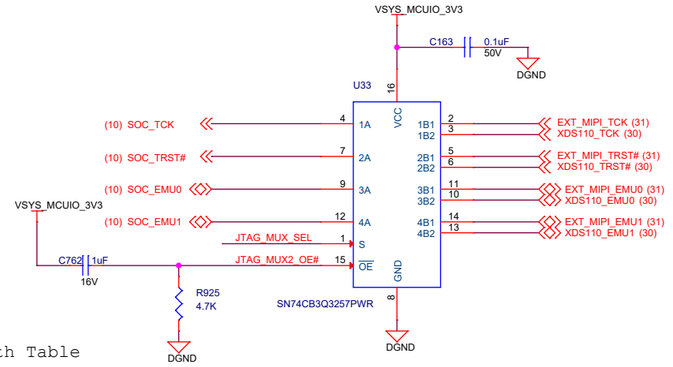
DIR LOW: 1B --> 1A
HIGH: 2B <-- 2A

Project :	J7 EVM
Title	USB HUB
Size	C
	PROC079 001 J721EXCP01EVM
Rev	E3B
Date:	Thursday, November 21, 2019
Sheet	28 of 68

TEXAS INSTRUMENTS

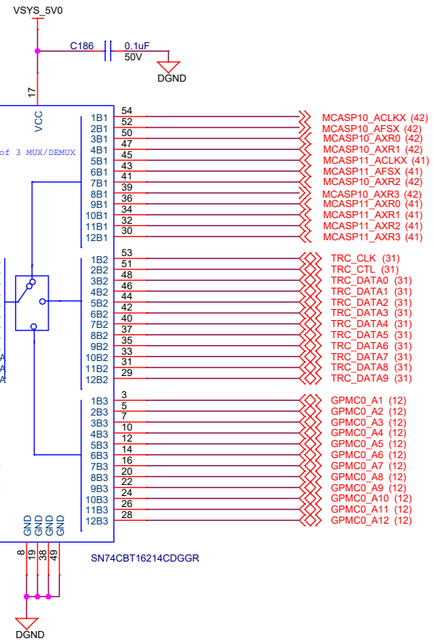
JTAG AND TRACE MUX

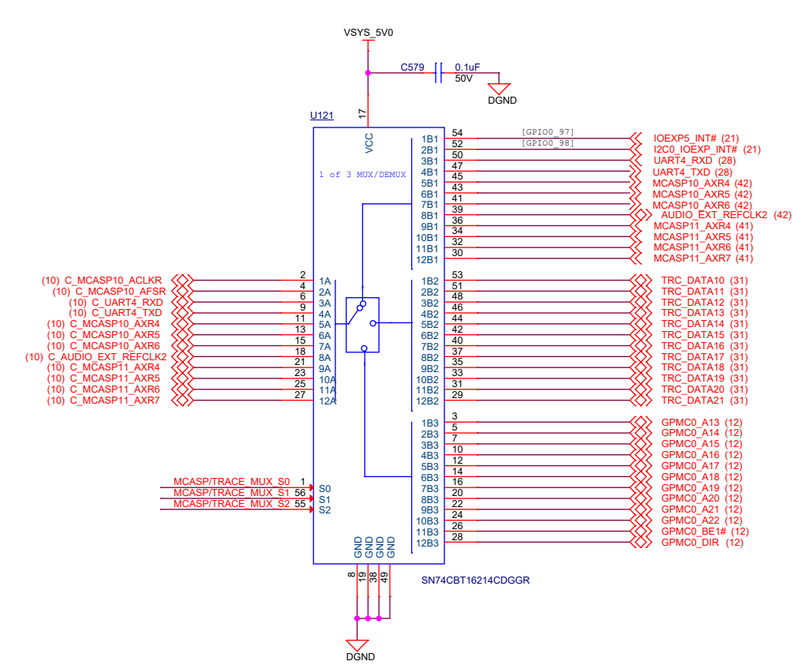




JTAG - 1:2 MUX : Truth Table

MUX_SEL	CONDITION	FUNCTION	
LOW	External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU]	(default)
HIGH	No External Emulator attached & XDS110 Powered via USB	A-->B2 port [ON Board EMU]	
LOW	External Emulator attached & XDS110 Powered via USB	A-->B1 port [EXTERNAL EMU]	
LOW	No External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU]	





MCASP/TRACE - 1:3 MUX : Truth Table

MUX_SEL2	MUX_SEL1	MUX_SEL0	FUNCTION	
HIGH	HIGH	LOW	A port = B1 port	
HIGH	HIGH	HIGH	A port = B2 port	(default)
HIGH	LOW	HIGH	A port = B3 port	

Project : J7 EVM	TEXAS INSTRUMENTS	Title: JTAG AND TRACE MUX	
		Size: C	PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 29 of 68

XDS110 DEBUGGER

Silkscreen "XDS110"

1051640001
CON MICRO USB-B TYPE 5POS FEMALE RT SMD

J3

FB1
150E
LI0805H151R-10

TPD4E004DRYR

U6
TPS79601DRBR

C18
2.2uF
10V

R43
51K

R40
30K

C28
15pF
50V

C17
1uF
16V

VCC3V3_XDS
V3V3_XDS_FB
VBUS_XDS_USB
XDS_USB_D_N
XDS_USB_D_P
XDS_USB_ID
XDS_SHIELD

TP6
TP116

C491 1uF 16V
C15 0.1uF 50V
C455 0.1uF 50V
C488 0.01uF 25V
C492 0.01uF 25V
C453 0.01uF 25V

U105B
TM4C1294NCPDTT3R

C27 1uF 16V
C490 0.01uF 25V
C13 2.2uF 10V
C14 1uF 16V
C32 0.01uF 25V
VDDC_1V2_XDS

R589 51E
VBAT_XDS
C452 0.1uF 50V

U105A
TM4C1294NCPDTT3R

(29) XDS110_TCK
(29) XDS110_TMS
(29) XDS110_TDO
(29) XDS110_TDI
(29) XDS110_TRST#

TP13 TM4C129_TCK
TP7 TM4C129_TMS
TP12 TM4C129_TDI
TP14 TM4C129_TDO

XDS_USB_D_P
XDS_USB_D_N

R588 DNI
R587 100E_1%
C454 0.1uF 50V
XDS_USB_ID
VBUS_XDS_USB

XDS110_VBUS_DET
XDS110_PROG_STAZ2
XDS110_PROG_STAZ1
XDS110_EMU0
XDS110_EMU1

R577 220E_1%
R572 180E
LD4 LP L296-J2L2-25 GREEN
LD1 LS Q976-NR-1 RED

R3 330K_1%
R4 220K_1%

VCC3V3_XDS
R23 R17 R12 R8 1K_1%
R22 R15 R5 R6 DNI

Set the unique ID
of the debugger

R581 10K
R585 DNI
TP4 TM4C129_RST# R586 100E_1%
XDS_RESET#

C457 12pF 50V
C456 12pF 50V
Y7
OSC0
OSC1
16.000MHZ
NX3225GA-16.000M-STD-CRG-1

R598 4.87K_1%
XDS_RBIAS

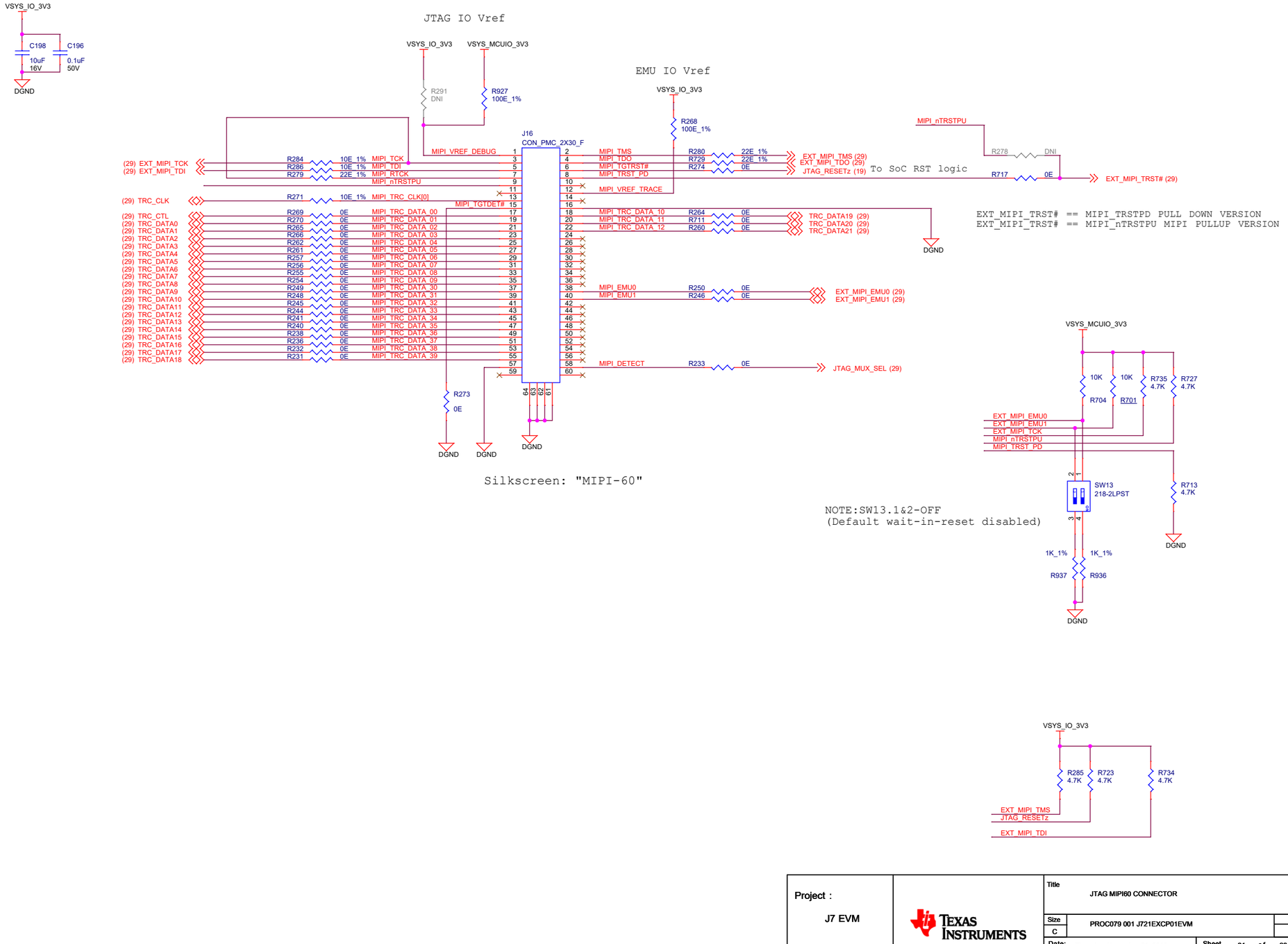
R41 4.7K
XDS_VREF

C30 0.01uF 25V
C29 0.1uF 50V
U7
LM4040B25IDCKR

R604 10K
R601 10K
XDS110_EMU0 (29)
XDS110_EMU1 (29)

Project : J7 EVM		Title: XDS110 DEBUGGER	
		Size: C	PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 30 of 68

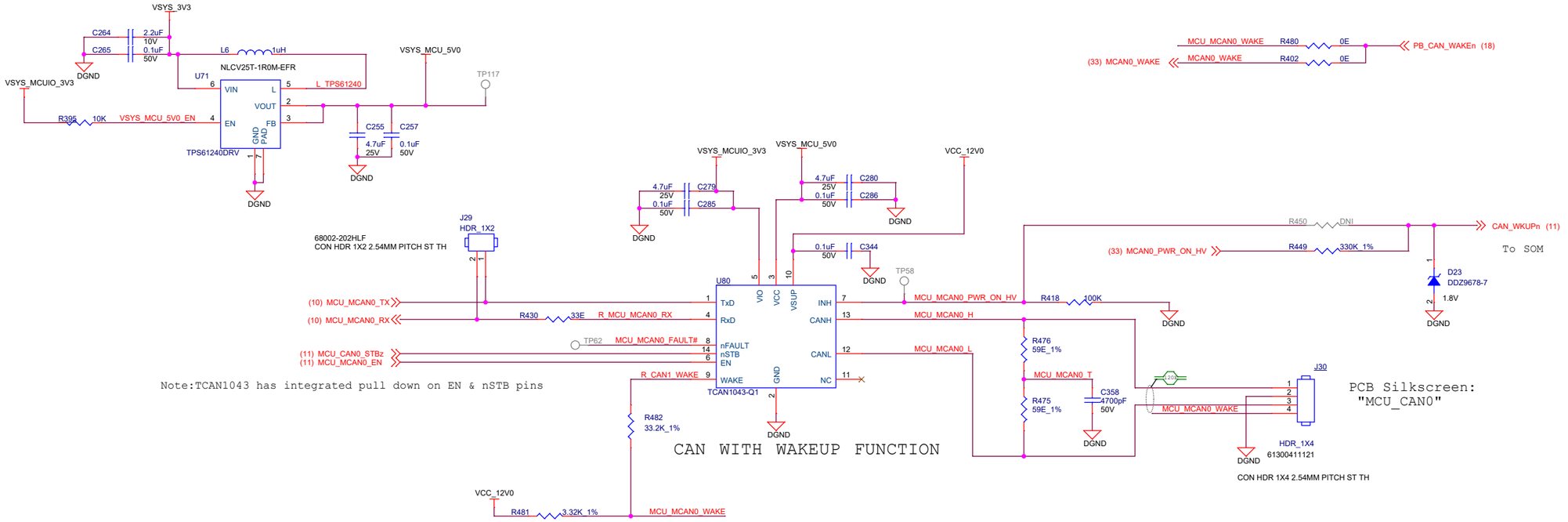
JTAG MIPI60 CONNECTOR

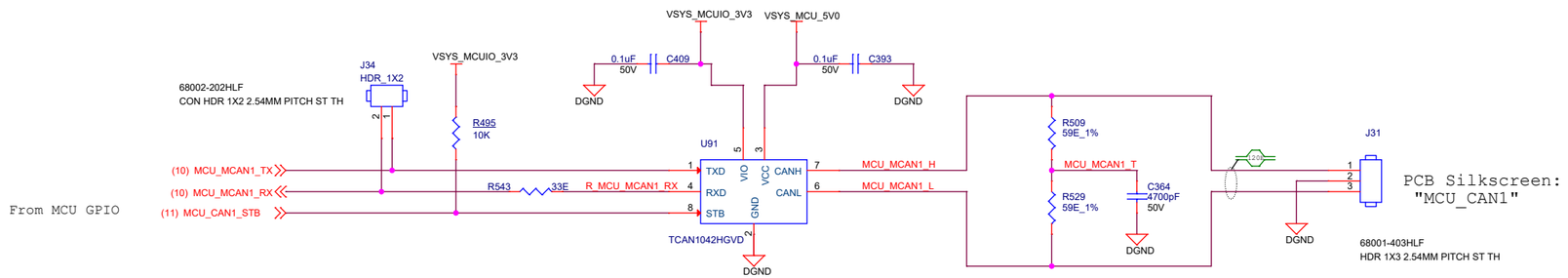


Project : J7 EVM	TEXAS INSTRUMENTS	Title: JTAG MIPI60 CONNECTOR
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 31 of 68

CAN TRANSCEIVERS #1-MCU DOMAIN

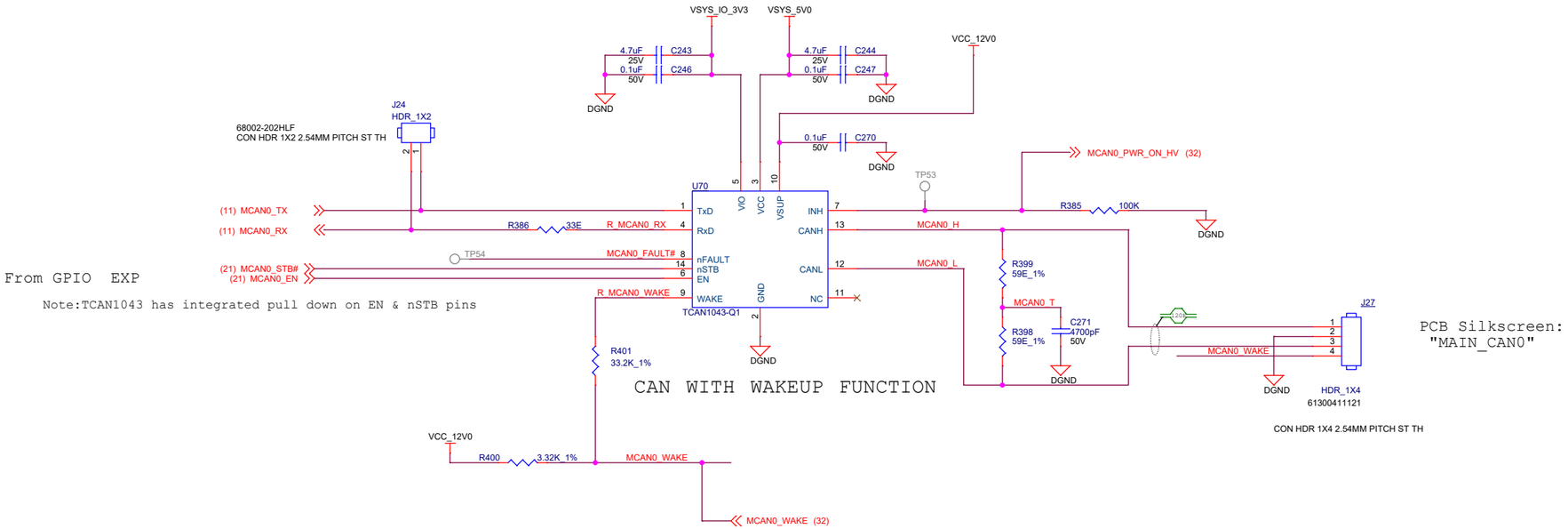
VSYS_MCU_5V0 GENERATION

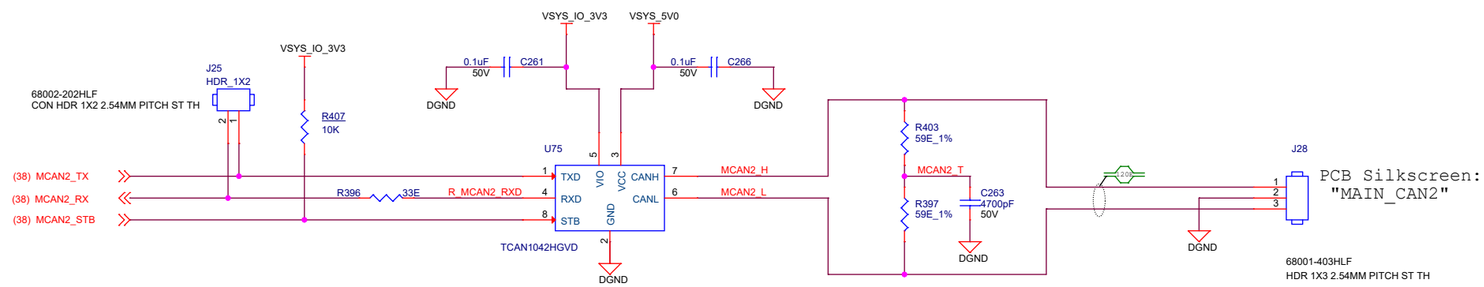




Project : J7 EVM	TEXAS INSTRUMENTS	Title: CAN TRANSCEIVERS #1
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 32 of 68

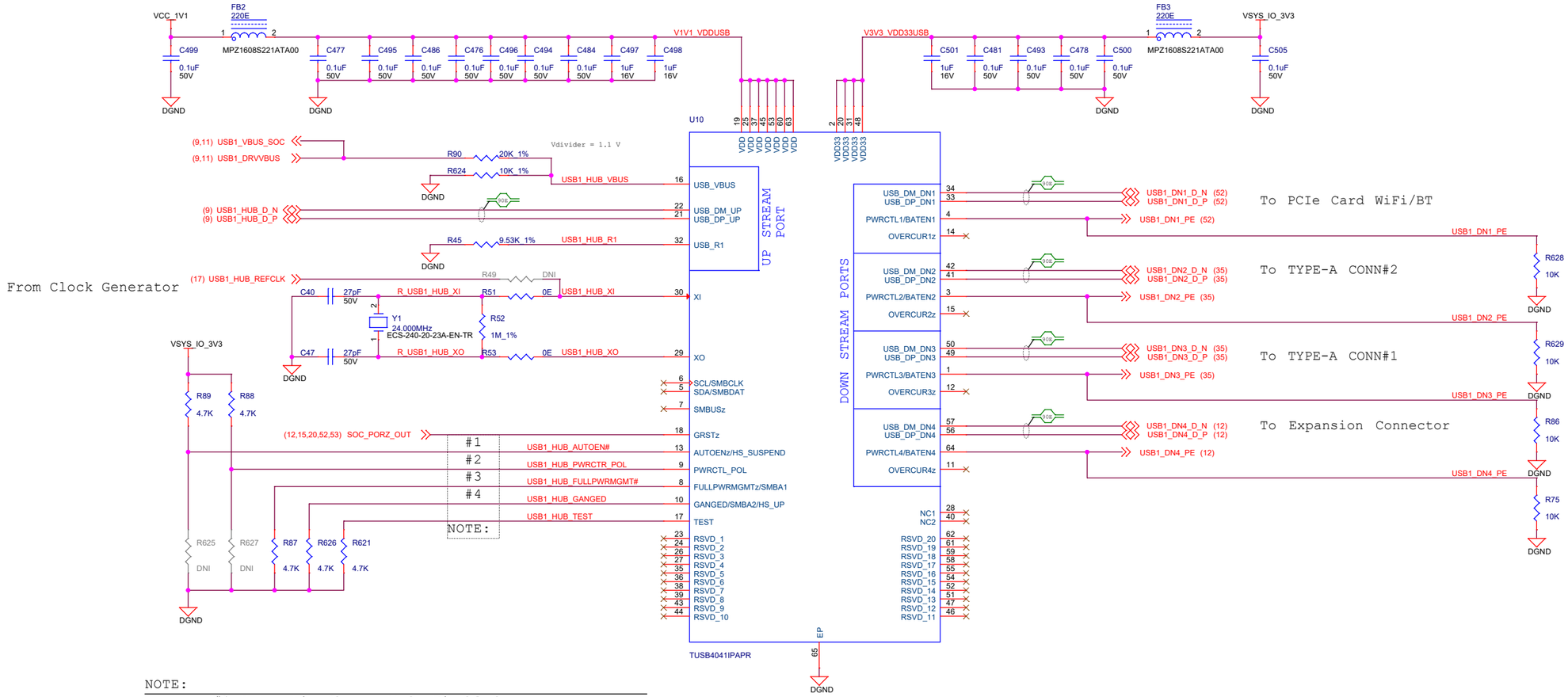
CAN TRANSCEIVERS #2-MAIN DOMAIN





Project : J7 EVM	TEXAS INSTRUMENTS	Title: CAN TRANSCEIVERS
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 33 of 68

USB HUB

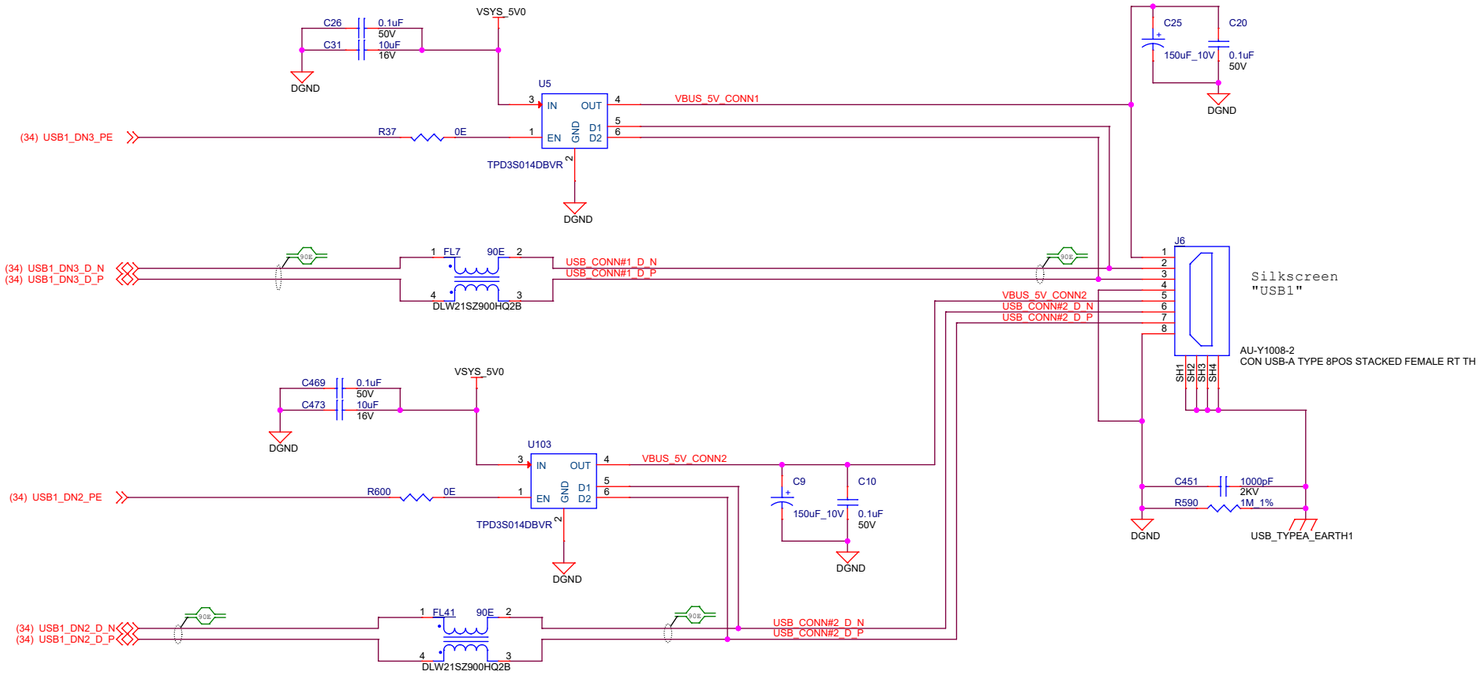


NOTE:

#1 Automatic Charge Mode Disabled
#2 PWRCTL Polarity is Active High
#3 Power Switching and Overcurrent Inputs Supported
#4 Individual Power Control Enabled

Project : J7 EVM	TEXAS INSTRUMENTS	Title: USB HUB
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 34 of 68

USB 2.0 TYPE-A CONNECTORS

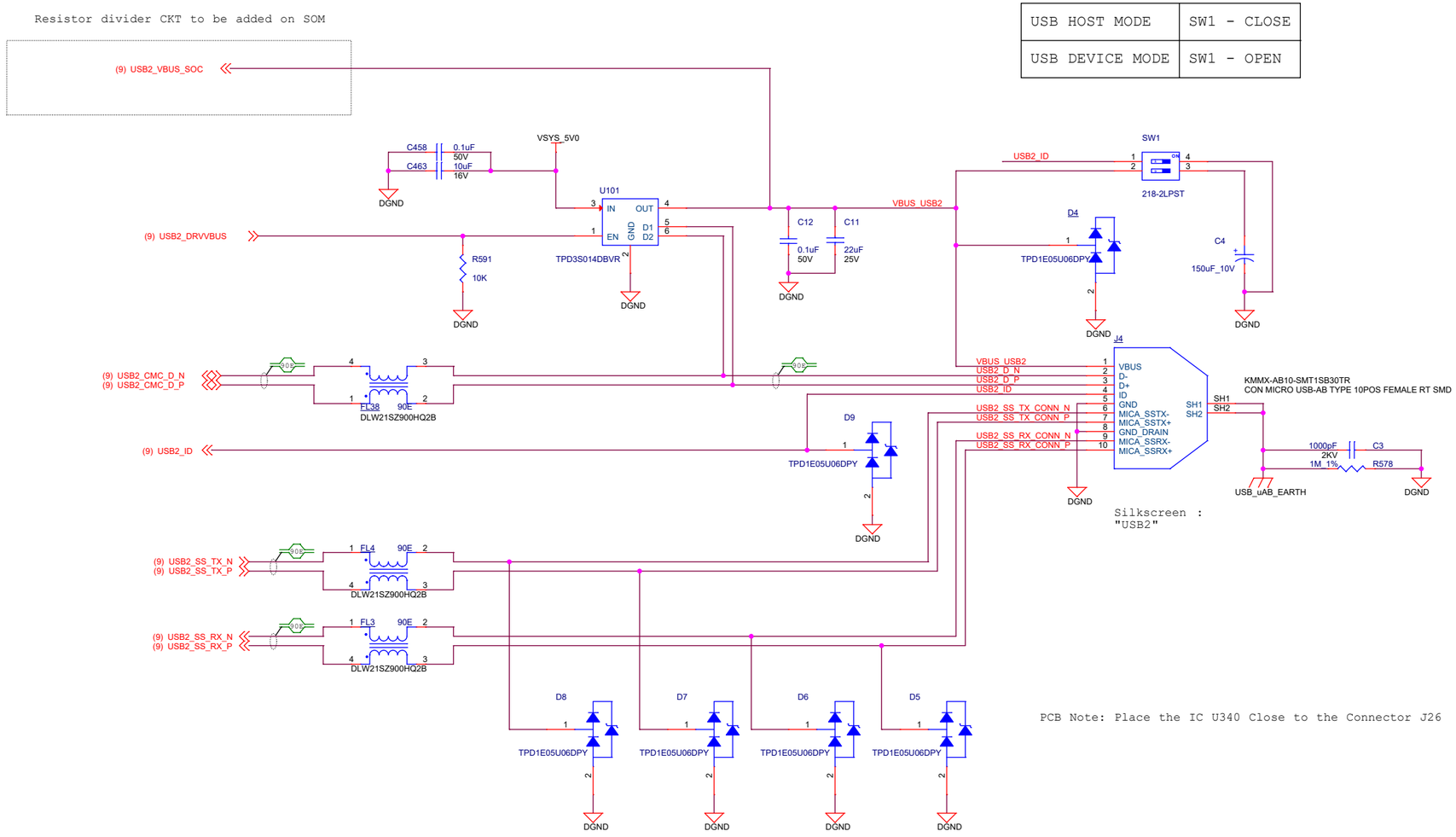


Project : J7 EVM	TEXAS INSTRUMENTS	Title: USB 2.0 TYPE-A CONNECTORS
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 35 of 68

USB 3.0 uAB

Resistor divider CKT to be added on SOM

USB HOST MODE	SW1 - CLOSE
USB DEVICE MODE	SW1 - OPEN



Project : J7 EVM	Title: USB 3.0 uAB	
	Size: C — PROC079 001 J721EXCP01EVM	Rev: E3B
	Date: Thursday, November 21, 2019	Sheet 36 of 68

USB 3.1 TYPE C INTERFACE

VCC_USBC_PD_5V
R614 100K
R613 100K
USBC_PD_FAULT#
USBC_PD_POL#

ILIMIT (max) = 1.5A

Note:VCC_USBC_PD_5V is Output of internal bias supply.

(21) USBC_PWR_EN
Note: Control to enable/powerdown circuit.
(9) USB0_DRVVBUS
Note: Control to enable/disable VBUS.
USBC_CTRL1_SW R9 0E
USB0_DRVVBUS
USBC_PD_CTRL1
SN74LVC1G08DBVRE4
Q13 BSS138-7-F
Q1 BSS138-7-F
Q2 BSS138-7-F
R20 10K
R596 10K
R19 0E
C19 0.1uF 50V
R24 100K
R612 DNI
(9) USB0_ID
USBC_PD_EN
USBC_PD_CTRL1
USBC_PD_CTRL2
USBC_PD_FAULT#
USBC_PD_LD_DET#
USBC_PD_POL#
EN/UVLO
CTRL1
CTRL2
FAULT
LD_DET
POL
DM_OUT
DP_OUT
A4 A3 A2 A1
TPS25830QWRHBTQ1
VINPUT
C22 15uF 50V
C24 10uF 50V
C23 0.1uF 100V
IN1 IN2 IN3
VCC
PGND PGND PGND EP AGND
C49 0.1uF 50V
C43 2.2uF 25V
BOOT
SW1 SW2 SW3 SW4
CSP
CSN/OUT
LS_GD
BUS
DM_IN DP_IN
CC1 CC2
RT/SYNC ILIMIT IMON
USBC_PD_BOOT C470 0.1uF 50V
L1 10uH
USBC_PD_SW
USBC_PD_CSP
R48 330E
USBC_PD_CSN/OUT
USBC_PD_LS_GD
VBUS_USBC_CONN
USBC_PD_CC1
USBC_PD_RT/SYNC
USBC_PD_ILIMIT
USBC_PD_IMON
R39 6.8K
R44 6.8K
R38 49.9K_1%
VCSP_USBC_PD
C45 0.1uF 50V
R76 0.033E_1% 1/2W
C54 C42 C41 C50 22uF 25V
C60 22uF 25V
C34 0.1uF 50V
PCB Note: Place Capacitor C close to the IC pin
U11 CSD85312Q3E
C65 1uF 16V
(for connecting to USB0_SOC_VBUS)
Resistor divider CKT to be added on SOM
TP5
VBUS_USBC_CONN
VBUS_USBC_CONN (9)
R652 910K
R635 5.1K_1%
R18 10K
U110 SI2301CDS-T1-GE3
C514 10uF 16V
C507 0.1uF 50V
C506 10uF 50V
D45 MBRS410LT3G
VDD_TUSB321
U111 TUSB321RWBR
Iout (max) = 1.5A
USBC_OUT1
USBC_OUT2
USBC_VCON_FAULT#
USBC_CURRENT_MODE
OUT1 OUT2 VCONN_FAULT CURRENT_MODE DIR
VDD GND
ID VBUS_DET PORT CC1 CC2
USBC_ID
USBC_VBUS_DET
USBC_PORT
USBC_CC1
USBC_CC2
TP82 TP81 TP83
R633 10K
R915 200K
R653 200K
R642 200K
R651 499K_1%
R648 DNI
(11) USBC_DIR
Note: Type C Cable Polarity Detection.
'0' - Position 1, '1' - Position 2
U176 SN74CBTLV1G125DBVR
USBC_ID
USBC_PD_LD_DET#
USBC_PORT_SW1 R16 0E
USBC_PORT_SW2 R7 10K_1% USBC_PORT
USBC_PORT
R609 10K
C764 0.1uF 50V
(18,21) USBC_MODE_SEL1
(18,21) USBC_MODE_SEL0
Note: DIP Switch/User Selectable.
USBC_MODE_SEL[1:0]: '00' = DFP
'01' = DRP
'1x' = UFP
R579 1M_1%
C2 1000pF 2KV
USBC_EARTH

J5 CON_USB-C_24_F
TYPE C CONN
VBUS1 VBUS2 VBUS3 VBUS4
D-_1 D+_1 D+_2 D-_2
CC1 CC2
SBU1 SBU2
TX1+ TX1- RX1+ RX1- TX2+ TX2- RX2+ RX2-
GND GND GND GND
SH1 SH2 SH3 SH4

USBC_DATA_CONN_N
USBC_DATA_CONN_P
(9) USB0_DATA_N
(9) USB0_DATA_P
FL8 90E DLW21SZ900HQ2B

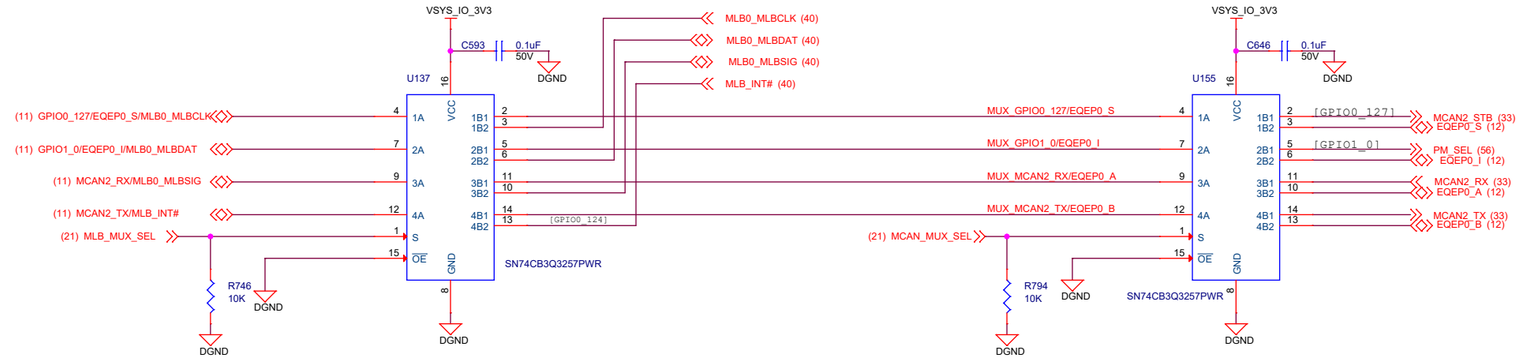
(9) USBC_SS_TX1_P
(9) USBC_SS_TX1_N
(9) USBC_SS_RX1_P
(9) USBC_SS_RX1_N
(9) USBC_SS_TX2_P
(9) USBC_SS_TX2_N
(9) USBC_SS_RX2_P
(9) USBC_SS_RX2_N
FL6 FL2 FL1 FL5 90E DLW21SZ900HQ2B
USBC_SS_TX1_CONN_P
USBC_SS_TX1_CONN_N
USBC_SS_RX1_CONN_P
USBC_SS_RX1_CONN_N
USBC_SS_TX2_CONN_P
USBC_SS_TX2_CONN_N
USBC_SS_RX2_CONN_P
USBC_SS_RX2_CONN_N
D15 D14 D10 D2 D3 D1 D12 D13 TPD1E05U06DPY

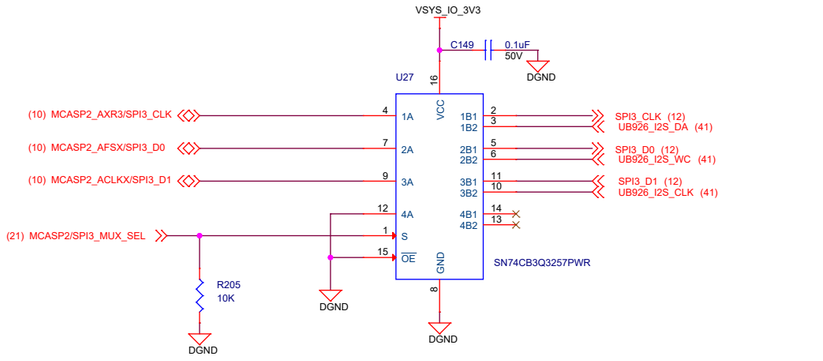
U2 TPD2E2U06-Q1
USBC_CC2
USBC_CC1
U175 TPD2E2U06-Q1
USBC_DATA_CONN1N
USBC_DATA_CONN_P

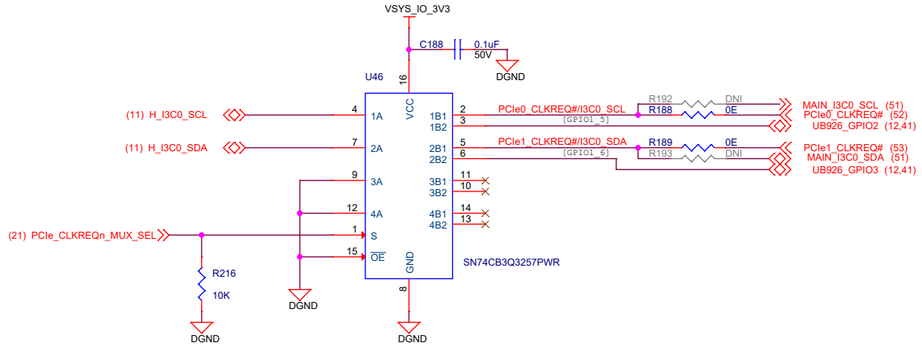
Silkscreen "USB 3.1 Type C"

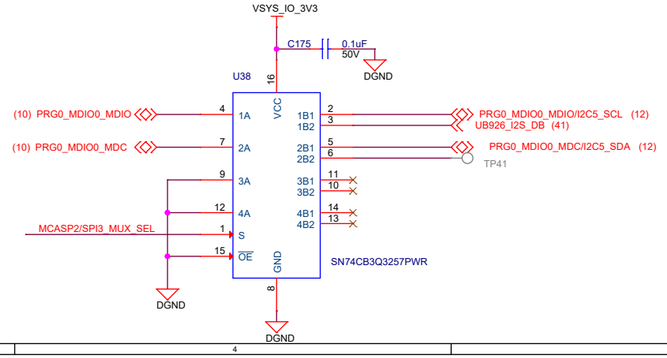
Project : J7 EVM		Title	USB 3.1 TYPE C INTERFACE
		Size C	PROC079 001 J721EXCP01EVM — Rev E3B
		Date: Thursday, November 21, 2019	Sheet 37 of 68

2:1 MUX's









Project : J7 EVM	TEXAS INSTRUMENTS	Title: 2:1 MUX's
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 38 of 68

MCU GB ETHERNET

VIO_MCURGMII IO SELECTION

VSYS_MCUIO_1V8 — R445 DNI — VIO_MCURGMII — TP119

VSYS_MCUIO_3V3 — R446 0E

Boards	Resistor Selection	
J7 SOM & Interposer	Mount-R446 & DNI-R445	(default)
Pre-silicon Test Interposer SOM	Mount-R445 & DNI-R446	

VIO_MCURGMII: C691 0.1uF 50V, C667 0.1uF 50V, C687 0.1uF 50V, C688 1uF 16V, C328 10uF 16V — DGND

VDD_1V0: C333 10uF 16V, C380 1uF 16V, C681 1uF 16V, C313 0.1uF 50V, C697 0.1uF 50V, C379 0.1uF 50V, C684 0.1uF 50V — DGND

VDD_2V5: C382 1uF 16V, C377 1uF 16V, C381 0.1uF 50V, C378 0.1uF 50V — DGND

VIO_MCURGMII, VDD_1V0, TP72 DNI, VDD_2V5

U160 DP83867ERGZT

(10) MCU_RGMII1_TD0	28	TX_D0/SGMII_SIN
(10) MCU_RGMII1_TD1	27	TX_D1/SGMII_SIP
(10) MCU_RGMII1_TD2	26	TX_D2
(10) MCU_RGMII1_TD3	25	TX_D3
(10) MCU_RGMII1_TX_CTL	37	TX_CTRL
(10) MCU_RGMII1_TXC	29	GTX_CLK
(10) MCU_RGMII1_RD0 — R816 22E 1% — MCU_RGMII1_RD0_R	33	RX_D0/SGMII_COP
(10) MCU_RGMII1_RD1 — R815 22E 1% — MCU_RGMII1_RD1_R	34	RX_D1/SGMII_CON
(10) MCU_RGMII1_RD2 — R814 22E 1% — MCU_RGMII1_RD2_R	35	RX_D2/SGMII_SOP
(10) MCU_RGMII1_RD3 — R813 22E 1% — MCU_RGMII1_RD3_R	36	RX_D3/SGMII_SON
(10) MCU_RGMII1_RX_CTL — R819 22E 1% — MCU_RGMII1_RX_CTL_R	38	RX_CTRL
(10) MCU_RGMII1_RXC — R817 22E 1% — MCU_RGMII1_RXC_R	32	RX_CLK
TP68 — MCU_RGMII1_CLK_OUT	18	CLK_OUT
C699 27pF — Y9 25.000MHz 445I23D25M00000 — C711 27pF — DGND	15 / 14	X_I / X_O
	16 / 17	MDC / MDIO
MCU_ENET_RSTz	43	RESET_N
	44	INT/PWDN
(10) MCU_MDIO0_MDC	20	JTAG_CLK
(10) MCU_MDIO0_MDIO	23	JTAG_TDI
	21	JTAG_TDO
	22	JTAG_TMS
	49	EP — DGND

MCU_RGMII1_RBIAS 11K_1% — R856 — DGND	12	RBIAS
MCU_RGMII1_GPIO0_100	39	GPIO_0
MCU_RGMII1_GPIO1	40	GPIO_1
MCU_RGMII1_D0_P	1	TD_P_A
MCU_RGMII1_D0_N	2	TD_M_A
MCU_RGMII1_D1_P	4	TD_P_B
MCU_RGMII1_D1_N	5	TD_M_B
MCU_RGMII1_D2_P	7	TD_P_C
MCU_RGMII1_D2_N	8	TD_M_C
MCU_RGMII1_D3_P	10	TD_P_D
MCU_RGMII1_D3_N	11	TD_M_D
MCU_RGMII1_LED0	47	LED0
MCU_RGMII1_LED1_1000	46	LED1
MCU_RGMII1_LED2_ACT	45	LED2

PU Provided on SoM

RJ45

J35

MCU_RGMII1_D0_N	10
MCU_RGMII1_D1_P	7
MCU_RGMII1_D1_N	8
MCU_RGMII1_D2_P	5
MCU_RGMII1_D2_N	6
MCU_RGMII1_D3_P	3
MCU_RGMII1_D3_N	4
MCU_RGMII1_LED2_ANODE — R568 220E_1%	11
MCU_RGMII1_ACT_LED	12
MCU_RGMII1_1000Mbps	13
MCU_RGMII1_100Mbps — R910 220E_1% — R909 220E_1% — VSYS_MCUIO_3V3	14
	1
	9
	2
SH1 / SH2	15 / 16

YELLOW / GREEN — RIGHT LED

YELLOW / GREEN — LEFT LED

LPJG16314A4NL
CON RJ-45 FEMALE 14POS RT TH

C745 1000pF 2KV — R565 1M_1% — DGND — MCU_ETH_EARTH

Silk Screen "MCU_RGMII1"

RESET LOGIC

VSYS_MCUIO_3V3 — R544 10K

VIO_MCURGMII — C410 0.1uF 50V — DGND

U95 SN74LVC1G08DBVRE4

(10,20) MCU_PORZ_OUT

(10) GPIO_MCU_RGMII1_RST#

From GPIO (default Pull-up pin) of MCU domain

R537 DNI — DGND

DGND

VSYS_MCUIO_3V3 — R841 2.2K — (10) MCU_RGMII1_INT#

To GPIO of MCU domain

RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	1000Mbps Speed
LEFT - YELLOW	100Mbps Speed

SPEED AND ACTIVITY LED DRIVERS

MCU_RGMII1_100Mbps — Q11 BSS138-7-F — MCU_RGMII1_GPIO0_100 — DGND

MCU_RGMII1_1000Mbps — Q15 BSS138-7-F — MCU_RGMII1_LED1_1000 — DGND

MCU_RGMII1_ACT_LED — Q12 BSS138-7-F — MCU_RGMII1_LED2_ACT — DGND

VIO_MCURGMII

R452 DNI	R453 DNI	R821 5.76K_1%
R458 DNI	R459 DNI	R820 2.49K_1%

R854 10K_1%	R498 DNI	R468 DNI
R849 2.49K_1%	R488 DNI	R479 DNI

R825 DNI	R511 DNI
R822 DNI	R504 DNI

MCU_RGMII1_RD0_R
MCU_RGMII1_RD2_R
MCU_RGMII1_RX_CTL_R
MCU_RGMII1_LED1_1000
MCU_RGMII1_LED2_ACT
MCU_RGMII1_GPIO0_100
MCU_RGMII1_GPIO1
MCU_RGMII1_LED0

DGND

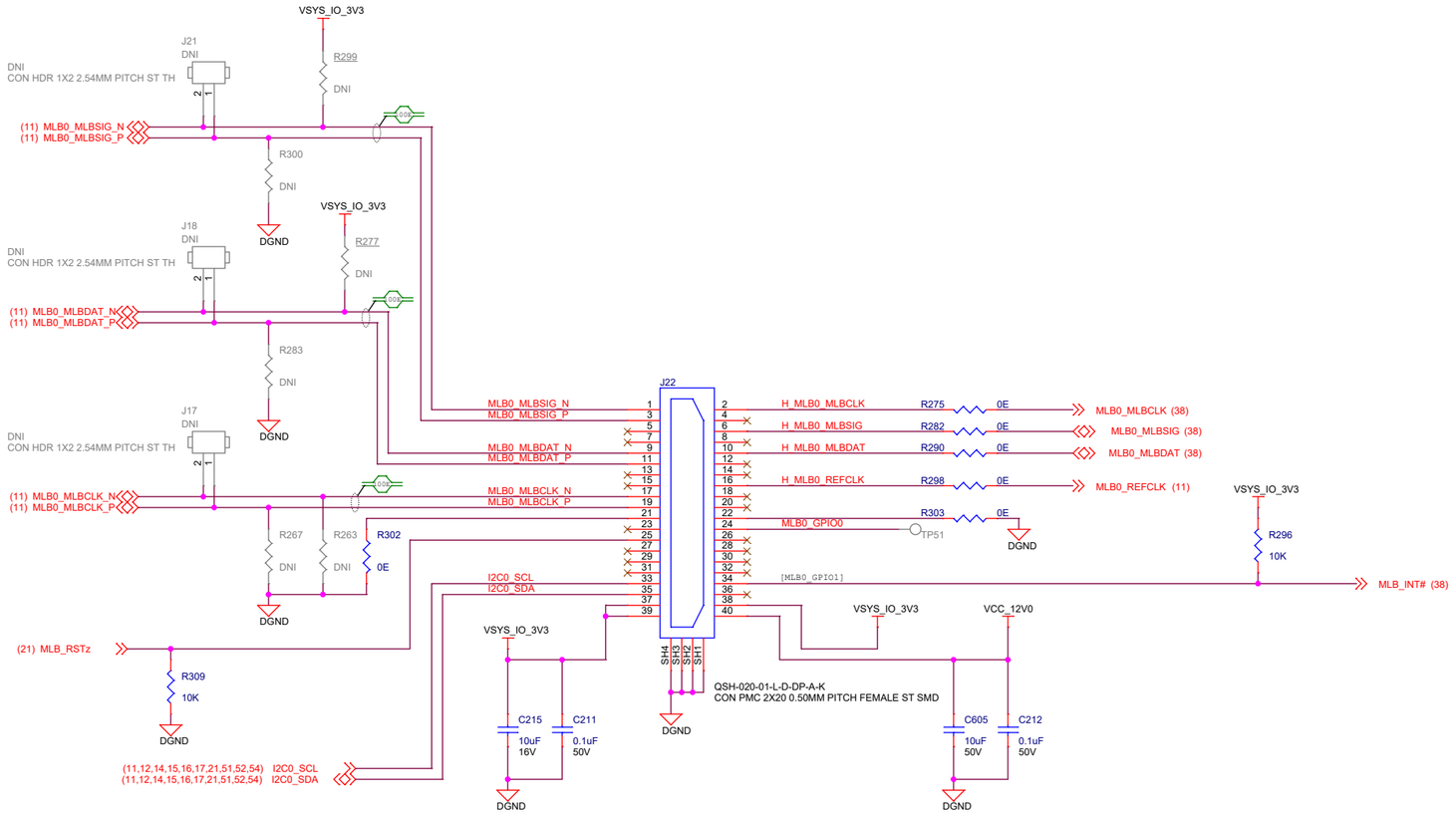
Set Mode 3 [Autoneg Disable - 0]

PHY ADD = 00000
Auto_neg = Enabled
ANEGsel 10/100/1000
RGMII Clock Skew TX = 0ns
RGMII Clock Skew RX = 2ns

LED_2-MODE1 & LED_1-MODE2-TX SKEW=0nS
GPIO0-MODE1 & GPIO1-MODE1-RX SKEW=2nS

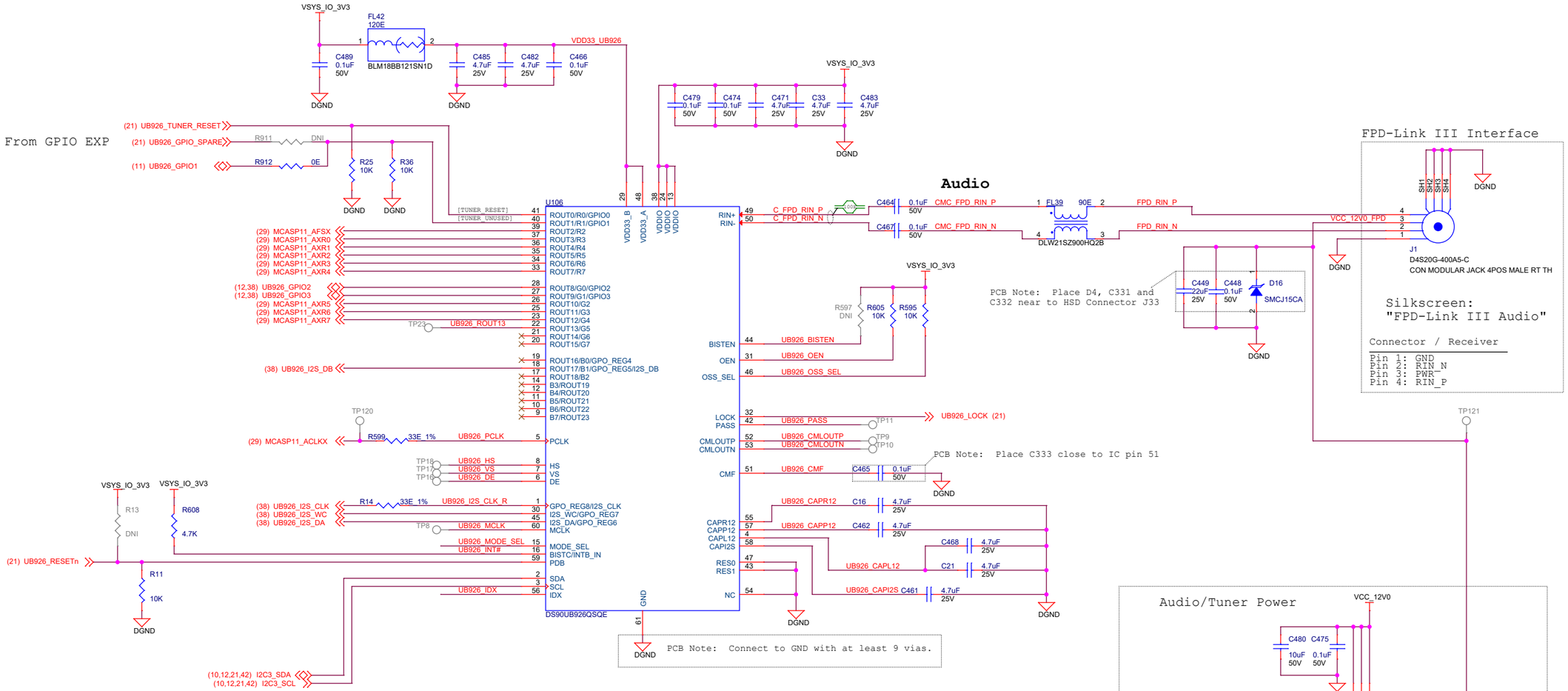
Project : J7 EVM	TEXAS INSTRUMENTS	Title: MCU GB ETHERNET	
		Size: C	PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 39 of 68

MLB INTERFACE



Project : J7 EVM	TEXAS INSTRUMENTS	Title: MDIO MDC MUX
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 40 of 68

FPD LINK-III DESERIALIZER



7b' I2C Address	R1	R2
0x2C	Open	40.2K
(other - see DM)		

Selected Mode: 0 (Default)	Software Config Only
LFMODE (15 - <85 MHz) REPEATER (OFF) BACK-COMPATIBLE (OFF) I2S-B OFF. 24B RGB	LFMODE (15 - <85 MHz) REPEATER (OFF) BACK-COMPATIBLE (OFF) I2S-B ON. 18B RGB
R3 = <open> R4 = 40.2K, 1% (or any)	R3 = <open> R4 = 40.2K, 1% (or any)

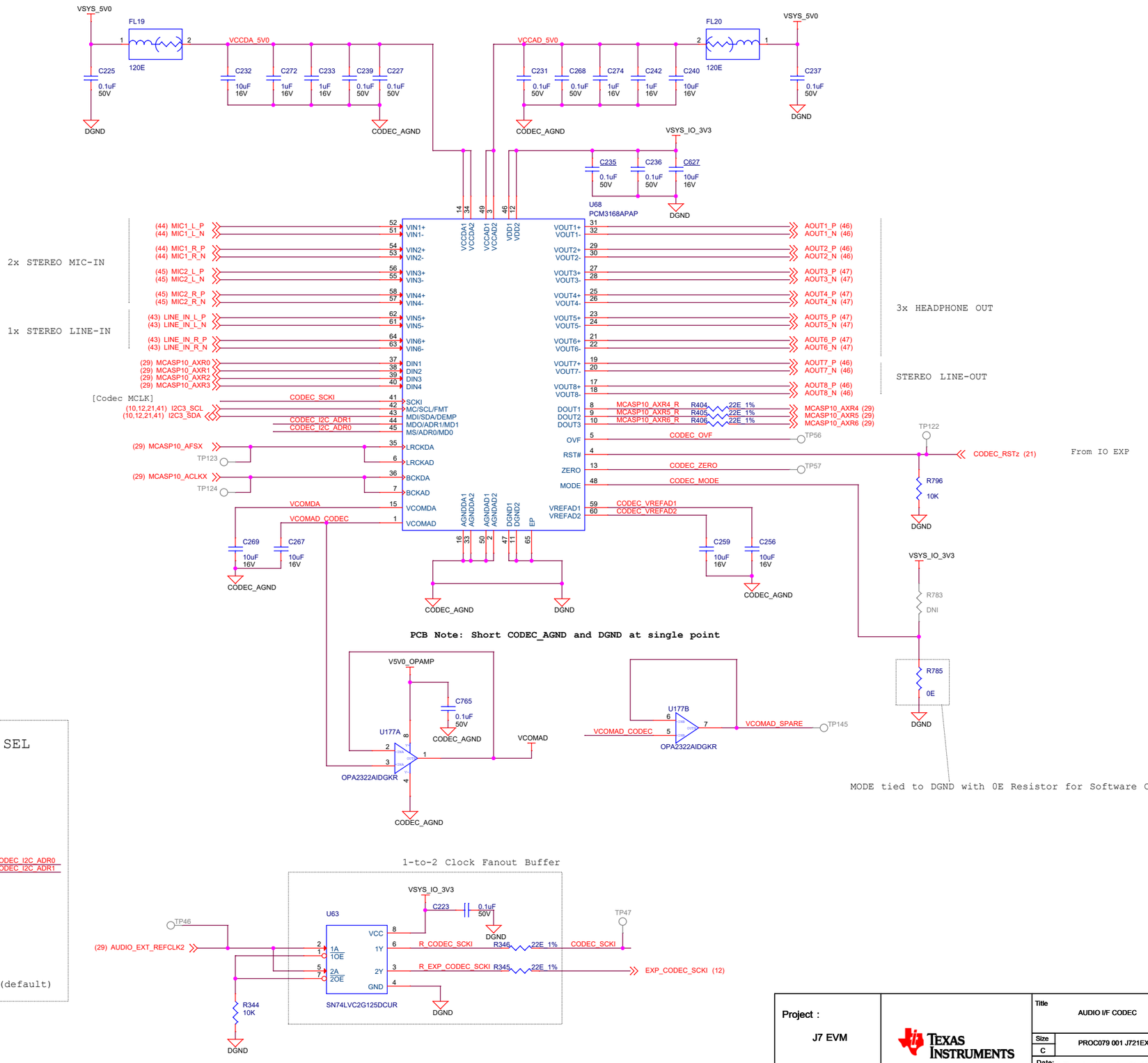
Project : J7 EVM

TEXAS INSTRUMENTS

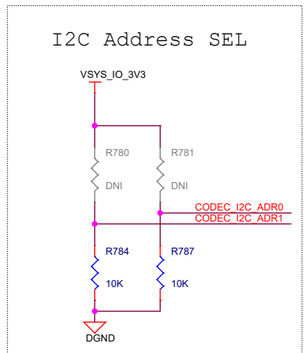
Title: FPD LINK-III DESERIALIZER

Size	PROC079 001 J721EXCP01EVM	Rev
C		E3B
Date: Thursday, November 21, 2019	Sheet 41 of 68	

AUDIO I/F CODEC



PCB Note: Short CODEC_AGND and DGND at single point



1-to-2 Clock Fanout Buffer

Project : J7 EVM	TEXAS INSTRUMENTS	Title: AUDIO I/F CODEC	
		Size: C	PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 42 of 68

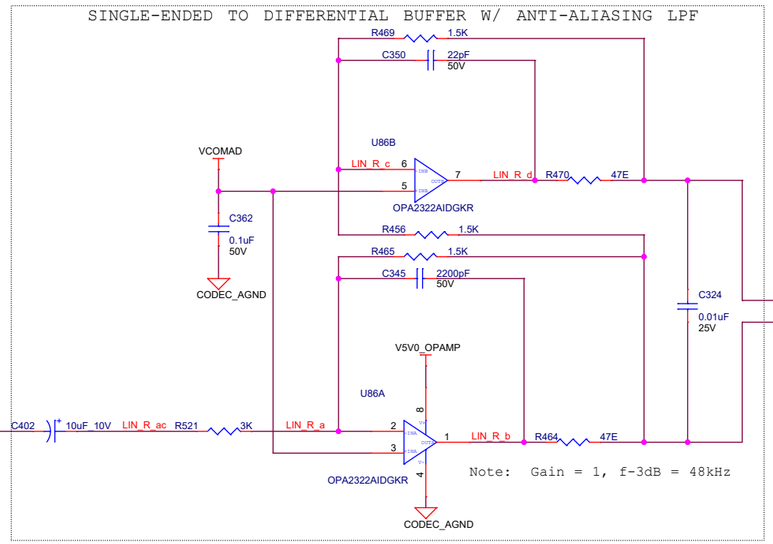
AUDIO I/F - STEREO LINE IN

Line-IN L VIN5
Line-IN R VIN6

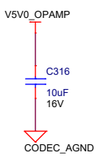
SJ-3524-SMT-TR
CON AUDIO JACK 4POS FEMALE RT SMD

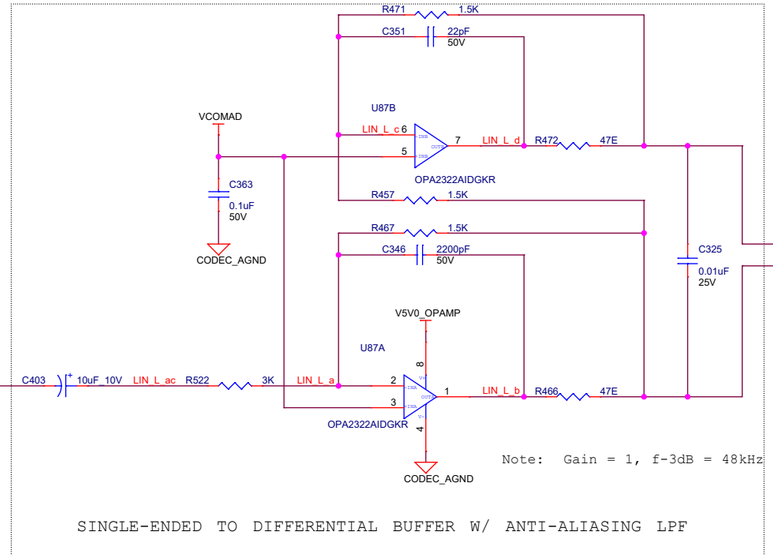
Silkscreen for J34:
"LINE-IN"

Note:Full scale is 2Vrms



Note: 1Vrms (or 2Vrms differentially)

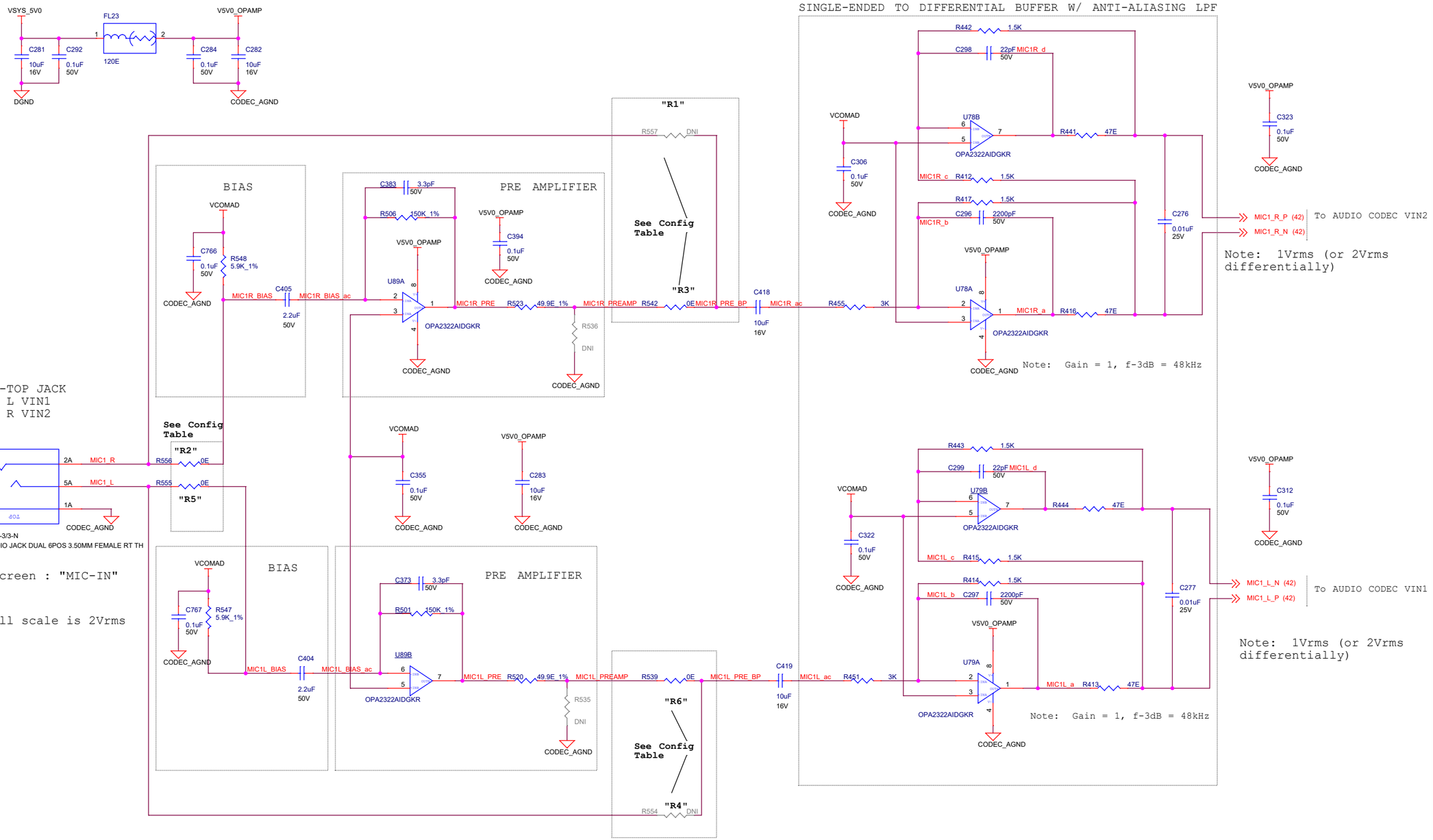




Note: 1Vrms (or 2Vrms differentially)

Project : J7 EVM	Title: AUDIO I/F - STEREO LINE IN	
	Size: C — PROC079 001 J721EXCP01EVM	Rev: E3B
	Date: Thursday, November 21, 2019	Sheet 43 of 68

AUDIO I/F - STEREO MIC #1

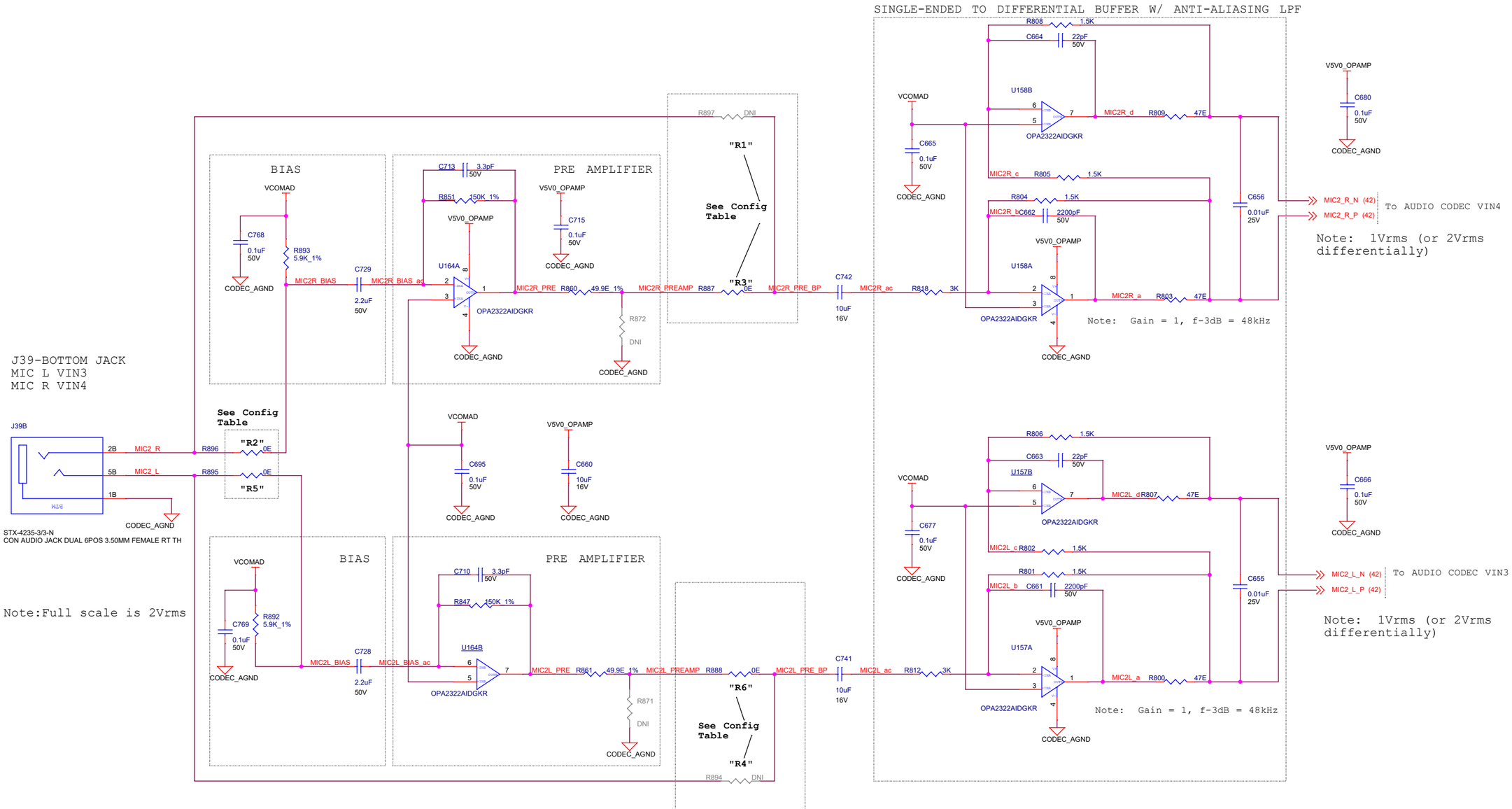


Config Table

		Install	Remove
PASSIVE-MIC (default)	BIAS + PREAMP	R2,R3,R5,R6	R1,R4
ACTIVE-MIC	BIAS ONLY	R1,R2,R4,R5	R3,R6
LINE-INPUT	NO BIAS/PREAMP	R1,R4	R2,R3,R5,R6

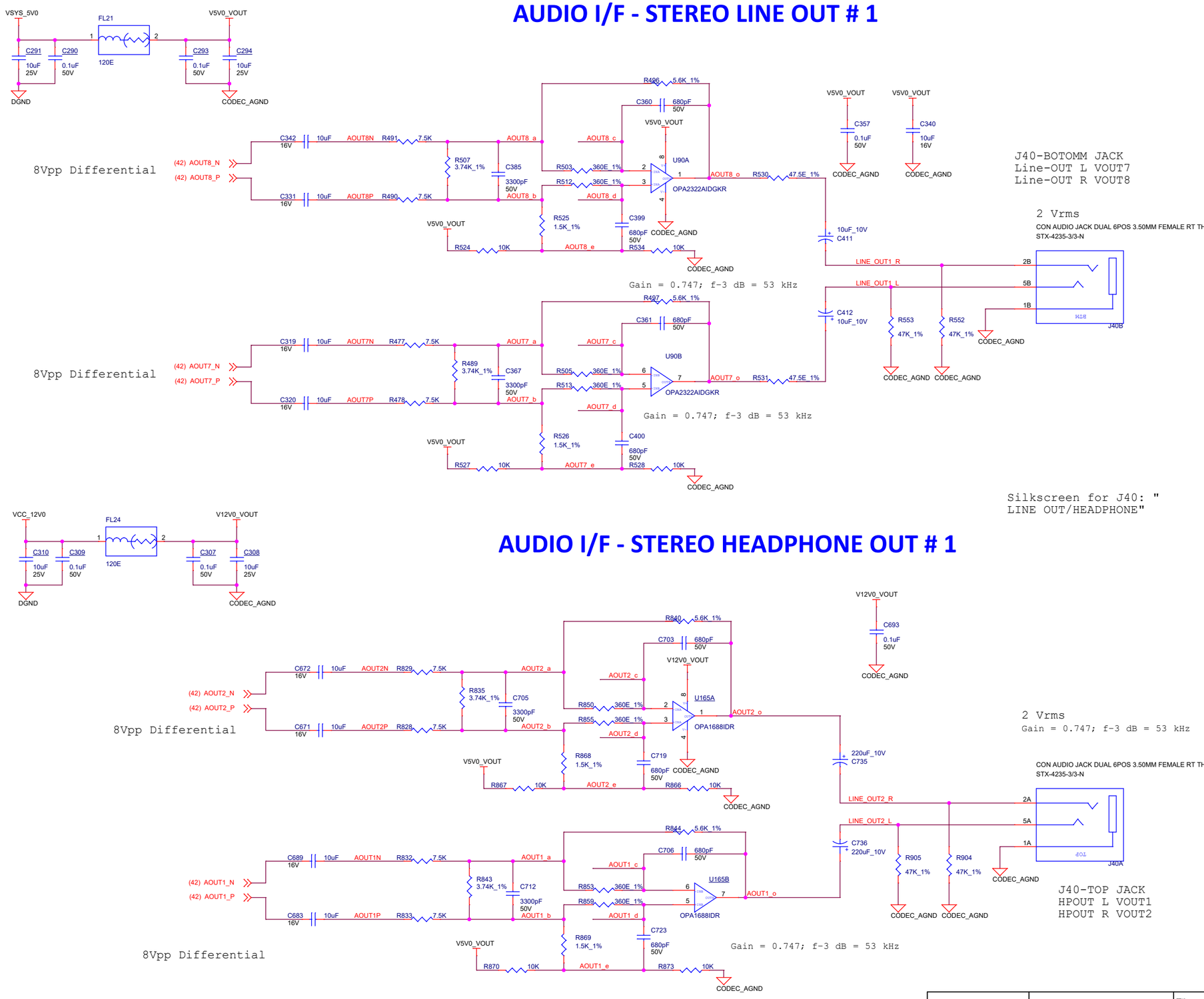
Project : J7 EVM	TEXAS INSTRUMENTS	Title: AUDIO I/F - STEREO MIC #1
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 44 of 68

AUDIO I/F - STEREO MIC #2



Project : J7 EVM	TEXAS INSTRUMENTS	Title: AUDIO I/F - STEREO MIC #2	
		Size: C	PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 45 of 68

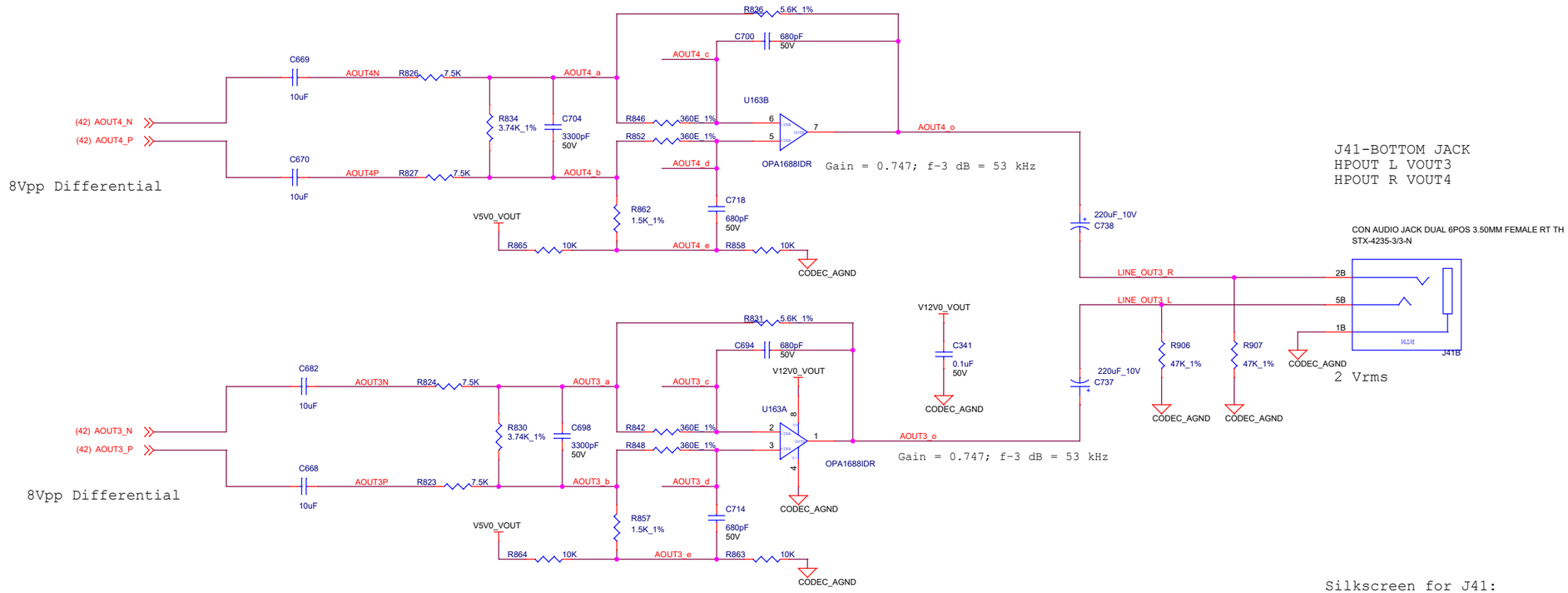
AUDIO I/F - STEREO LINE OUT # 1



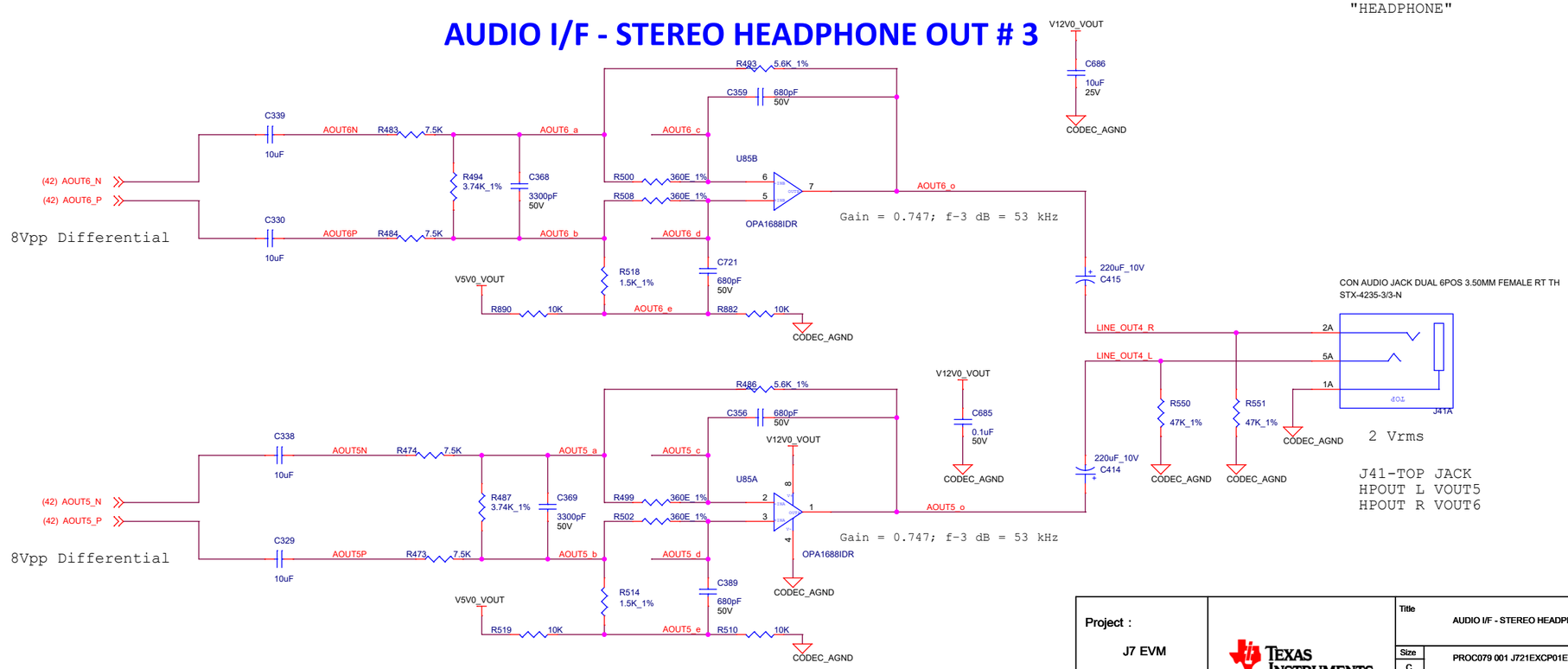
AUDIO I/F - STEREO HEADPHONE OUT # 1

Project : J7 EVM	TEXAS INSTRUMENTS	Title: AUDIO I/F - STEREO LINE OUT & HP OUT# 1	
		Size: C	PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 46 of 68

AUDIO I/F - STEREO HEADPHONE OUT # 2

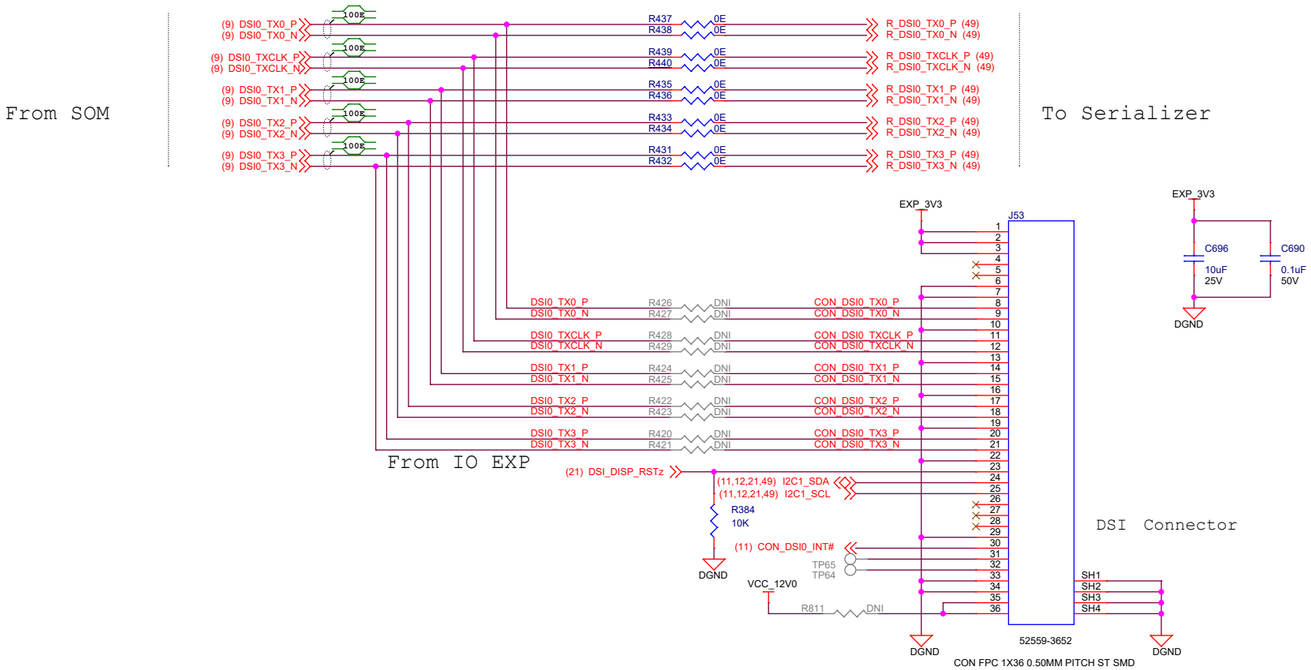


AUDIO I/F - STEREO HEADPHONE OUT # 3



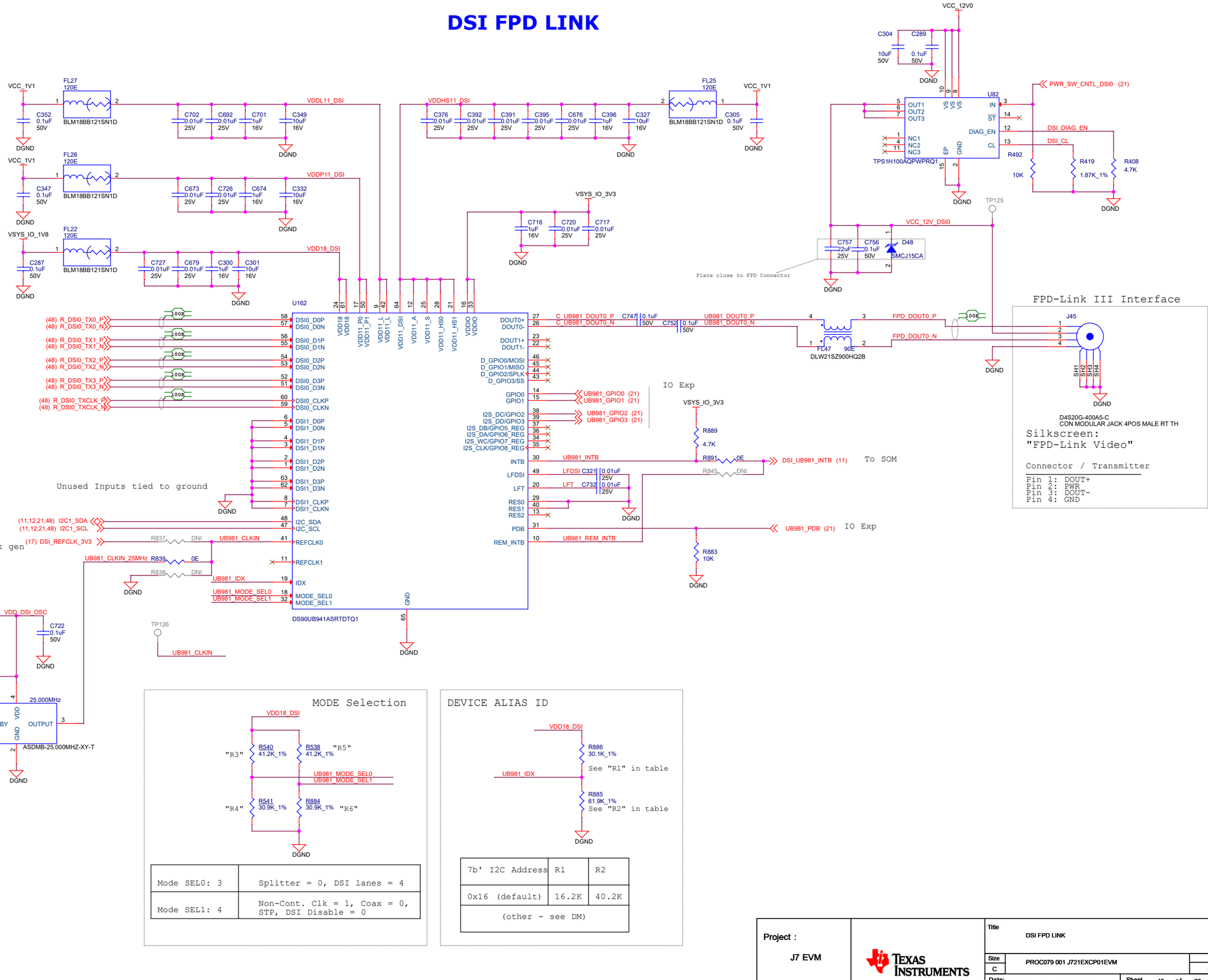
Project : J7 EVM	TEXAS INSTRUMENTS	Title: AUDIO I/F - STEREO HEADPHONE OUT # 2 & 3	
		Size: C	PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 47 of 68

DSI FPC



Project : J7 EVM	TEXAS INSTRUMENTS	Title: DSI FPC
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 48 of 68

DSI FPD LINK



Mode SEL0: 3	Splitter = 0, DSI lanes = 4
Mode SEL1: 4	Non-Cont. Clk = 1, Coax = 0, STP, DSI Disable = 0

7b' I2C Address	R1	R2
0x16 (default)	16.2K	40.2K
(other - see DM)		

Project : J7 EVM

TEXAS INSTRUMENTS

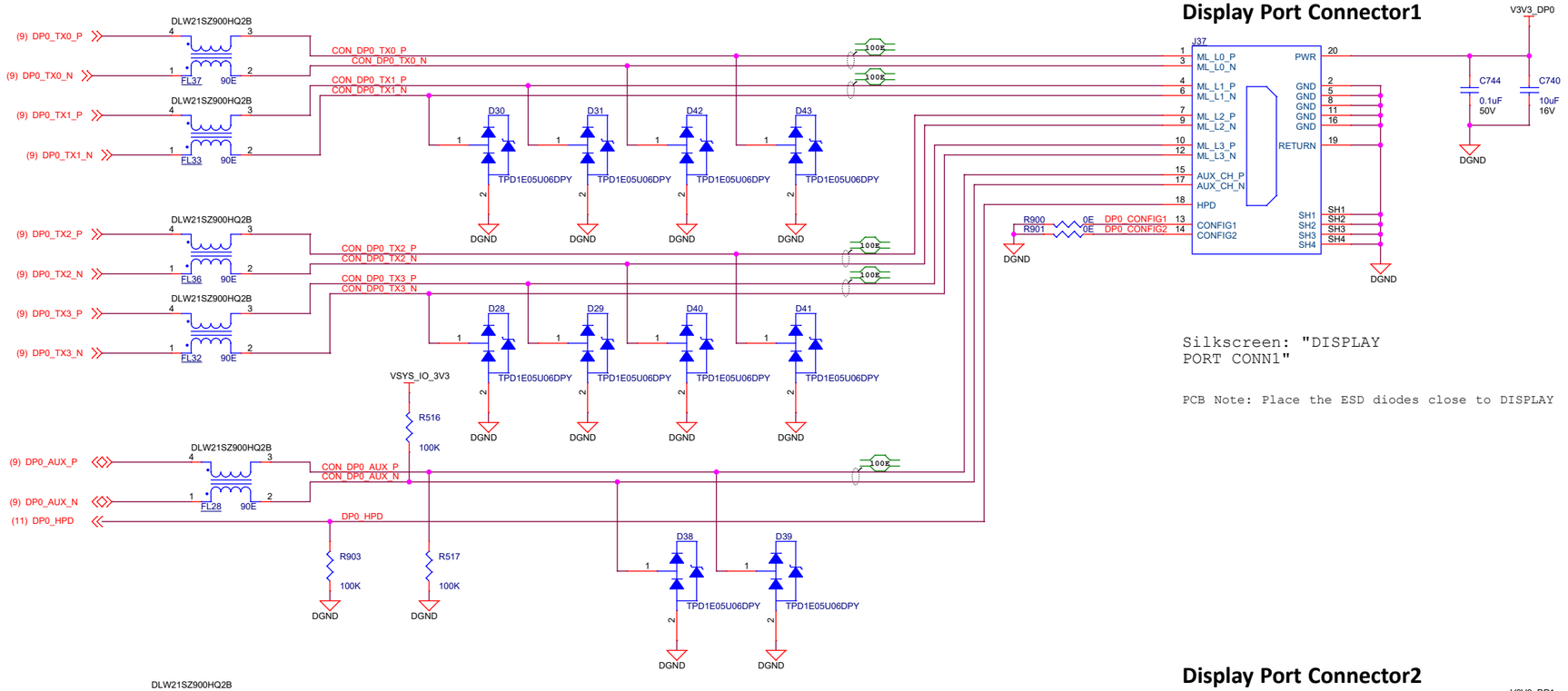
Title: DSI FPD LINK

Size: C | PROC079 001 J721EXCP01EVM | Rev: E3B

Date: Thursday, November 21, 2019 | Sheet 49 of 68

DISPLAY PORT INTERFACE

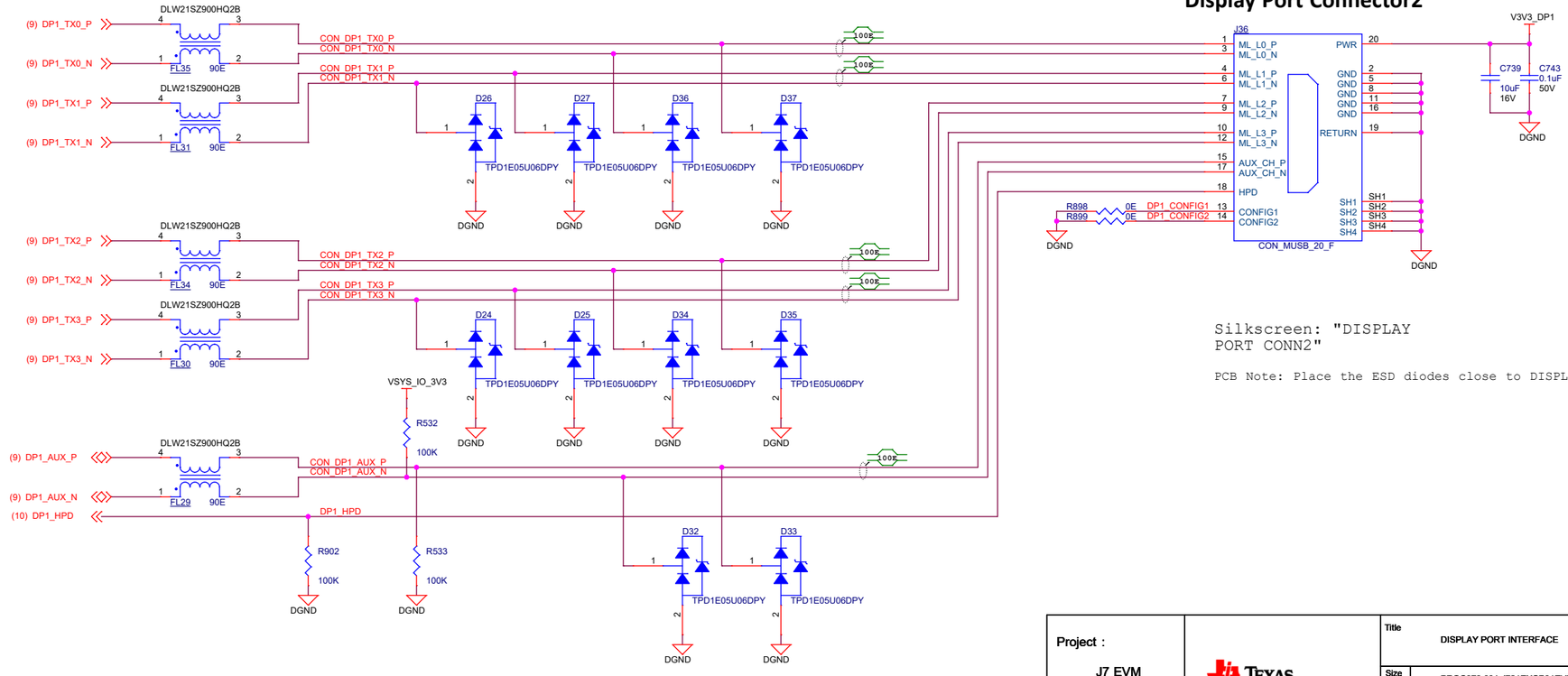
Display Port Connector1



Silkscreen: "DISPLAY PORT CONN1"

PCB Note: Place the ESD diodes close to DISPLAY PORT CONN1

Display Port Connector2

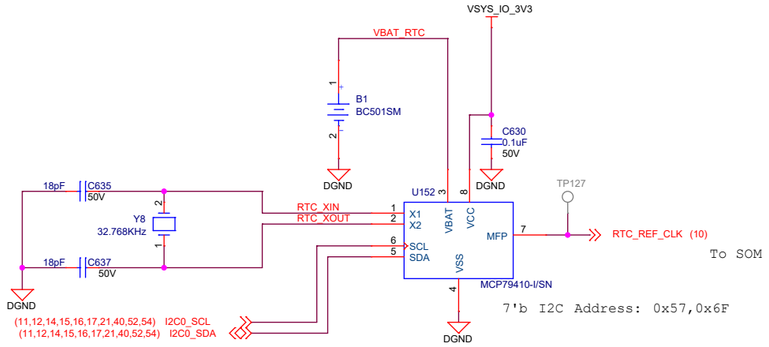


Silkscreen: "DISPLAY PORT CONN2"

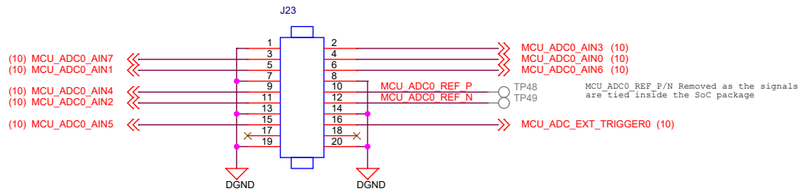
PCB Note: Place the ESD diodes close to DISPLAY PORT CONN2

Project : J7 EVM	TEXAS INSTRUMENTS	Title: DISPLAY PORT INTERFACE	
		Size: C	PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 50 of 68

RTC

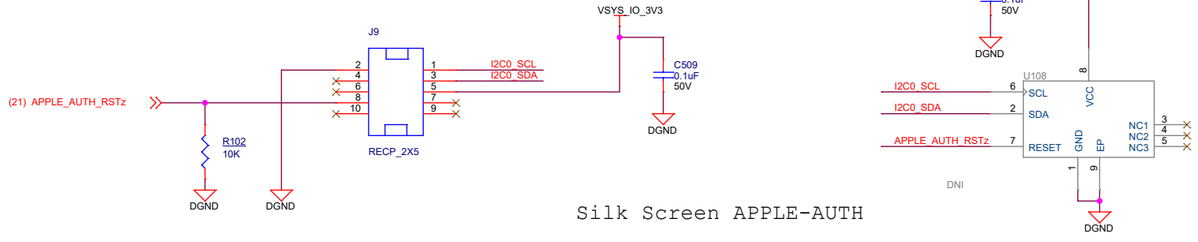


ADC INTERFACE



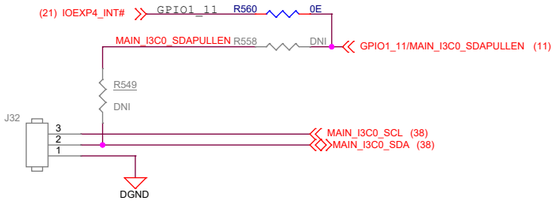
ADC Connector

Apple Authentication



Silk Screen APPLE-AUTH

I3C Headers



Silk Screen MAIN-I3C

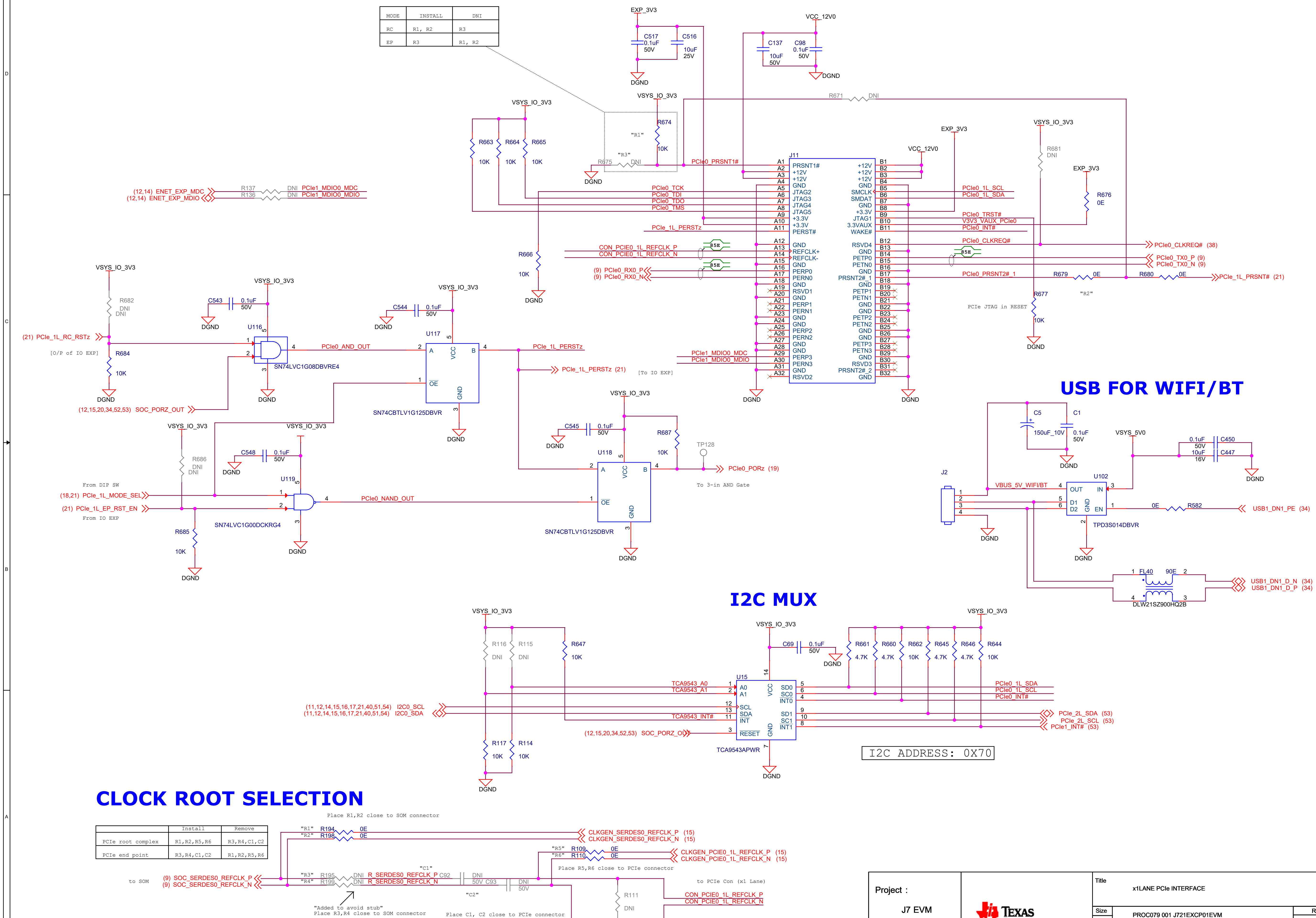
Silk Screen MCU-I3C

Project : J7 EVM	TEXAS INSTRUMENTS	Title: ADC,RTC,I3C,APPLE AUTH_INTERFACE
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 51 of 68

x1LANE PCIe Interface

x4 Lane PCIe Connector

MODE	INSTALL	DNI
RC	R1, R2	R3
EP	R3	R1, R2



EXP_3V3
C517 0.1uF 50V
C516 10uF 25V
VCC_12V0
C137 10uF 50V
C98 0.1uF 50V
DGND
VSYS_IO_3V3
R663 10K
R664 10K
R665 10K
R674 10K
"R1"
"R3"
R675 DNI
R671 DNI
PCIe0_PRSNT1#
J11
PRSNT1# +12V +12V GND JTAG2 JTAG3 JTAG4 JTAG5 +3.3V +3.3V PERST#
GND REFCLK+ REFCLK- GND PERP0 PERN0 GND RSVD1 GND PERP1 PERN1 GND GND PERP2 PERN2 GND GND PERP3 PERN3 GND RSVD2
+12V +12V +12V GND SMCLK SMDAT GND +3.3V JTAG1 3.3VAUX WAKE#
RSVD4 GND PETP0 PETN0 GND PRSNT2#_1 GND PETP1 PETN1 GND GND PETP2 PETN2 GND GND PETP3 PETN3 GND RSVD3 PRSNT2#_2 GND
PCIe0_TCK
PCIe0_TDI
PCIe0_TDO
PCIe0_TMS
PCIe_1L_PERSTz
(12,14) ENET_EXP_MDC
(12,14) ENET_EXP_MDIO
R137 DNI PCIe1_MDIO0_MDC
R136 DNI PCIe1_MDIO0_MDIO
R666 10K
CON_PCIE0_1L_REFCLK_P
CON_PCIE0_1L_REFCLK_N
85E
(9) PCIe0_RX0_P
(9) PCIe0_RX0_N
PCIe1_MDIO0_MDC
PCIe1_MDIO0_MDIO
PCIe0_1L_SCL
PCIe0_1L_SDA
PCIe0_TRST#
V3V3_VAUX_PCIe0
PCIe0_INT#
PCIe0_CLKREQ#
PCIe0_CLKREQ# (38)
PCIe0_TX0_P (9)
PCIe0_TX0_N (9)
PCIe0_PRSNT2#_1
R679 0E
R680 0E
PCIe_1L_PRSNT# (21)
"R2"
R681 DNI
R676 0E
R677 10K
PCIe JTAG in RESET
(21) PCIe_1L_RC_RSTz
R682 DNI
[O/P of IO EXP]
R684 10K
C543 0.1uF 50V
U116
SN74LVC1G08DBVRE4
PCIe0_AND_OUT
(12,15,20,34,52,53) SOC_PORZ_OUT
C544 0.1uF 50V
U117
SN74CBTLV1G125DBVR
PCIe_1L_PERSTz (21)
[To IO EXP]
R686 DNI
From DIP SW
(18,21) PCIe_1L_MODE_SEL
(21) PCIe_1L_EP_RST_EN
From IO EXP
R685 10K
C548 0.1uF 50V
U119
SN74LVC1G00DCKRG4
PCIe0_NAND_OUT
C545 0.1uF 50V
U118
R687 10K
TP128
PCIe0_PORz (19)
To 3-in AND Gate
USB FOR WIFI/BT
C5 150uF_10V
C1 0.1uF 50V
VSYS_5V0
C450 0.1uF 50V
C447 10uF 16V
J2
VBUS_5V_WIFI/BT
U102
OUT IN D1 D2 GND EN
TPD3S014DBVR
R582 0E
USB1_DN1_PE (34)
FL40 90E
DLW21SZ900HQ2B
USB1_DN1_D_N (34)
USB1_DN1_D_P (34)
I2C MUX
R116 DNI
R115 DNI
R647 10K
R117 10K
R114 10K
C69 0.1uF 50V
R661 4.7K
R660 4.7K
R662 10K
R645 4.7K
R646 4.7K
R644 10K
U15
TCA9543_A0
TCA9543_A1
(11,12,14,15,16,17,21,40,51,54) I2C0_SCL
(11,12,14,15,16,17,21,40,51,54) I2C0_SDA
TCA9543_INT#
(12,15,20,34,52,53) SOC_PORZ_OUT
A0 A1 SCL SDA INT RESET VCC GND SD0 SC0 INT0 SD1 SC1 INT1
TCA9543APWR
PCIe0_1L_SDA
PCIe0_1L_SCL
PCIe0_INT#
PCIe_2L_SDA (53)
PCIe_2L_SCL (53)
PCIe1_INT# (53)
I2C ADDRESS: 0X70
CLOCK ROOT SELECTION
Place R1,R2 close to SOM connector
"R1" R194 0E
"R2" R198 0E
CLKGEN_SERDES0_REFCLK_P (15)
CLKGEN_SERDES0_REFCLK_N (15)
"R5" R109 0E
"R6" R110 0E
CLKGEN_PCIE0_1L_REFCLK_P (15)
CLKGEN_PCIE0_1L_REFCLK_N (15)
Place R5,R6 close to PCIe connector
to SOM
(9) SOC_SERDES0_REFCLK_P
(9) SOC_SERDES0_REFCLK_N
"R3" R195 DNI
"R4" R199 DNI
R_SERDES0_REFCLK_P
R_SERDES0_REFCLK_N
"C1" C92 DNI 50V
C93 DNI 50V "C2"
R111 DNI
to PCIe Con (x1 Lane)
CON_PCIE0_1L_REFCLK_P
CON_PCIE0_1L_REFCLK_N
"Added to avoid stub"
Place R3,R4 close to SOM connector
Place C1, C2 close to PCIe connector

	Install	Remove
PCIe root complex	R1,R2,R5,R6	R3,R4,C1,C2
PCIe end point	R3,R4,C1,C2	R1,R2,R5,R6

Project : J7 EVM

Texas Instruments

Title: x1LANE PCIe INTERFACE

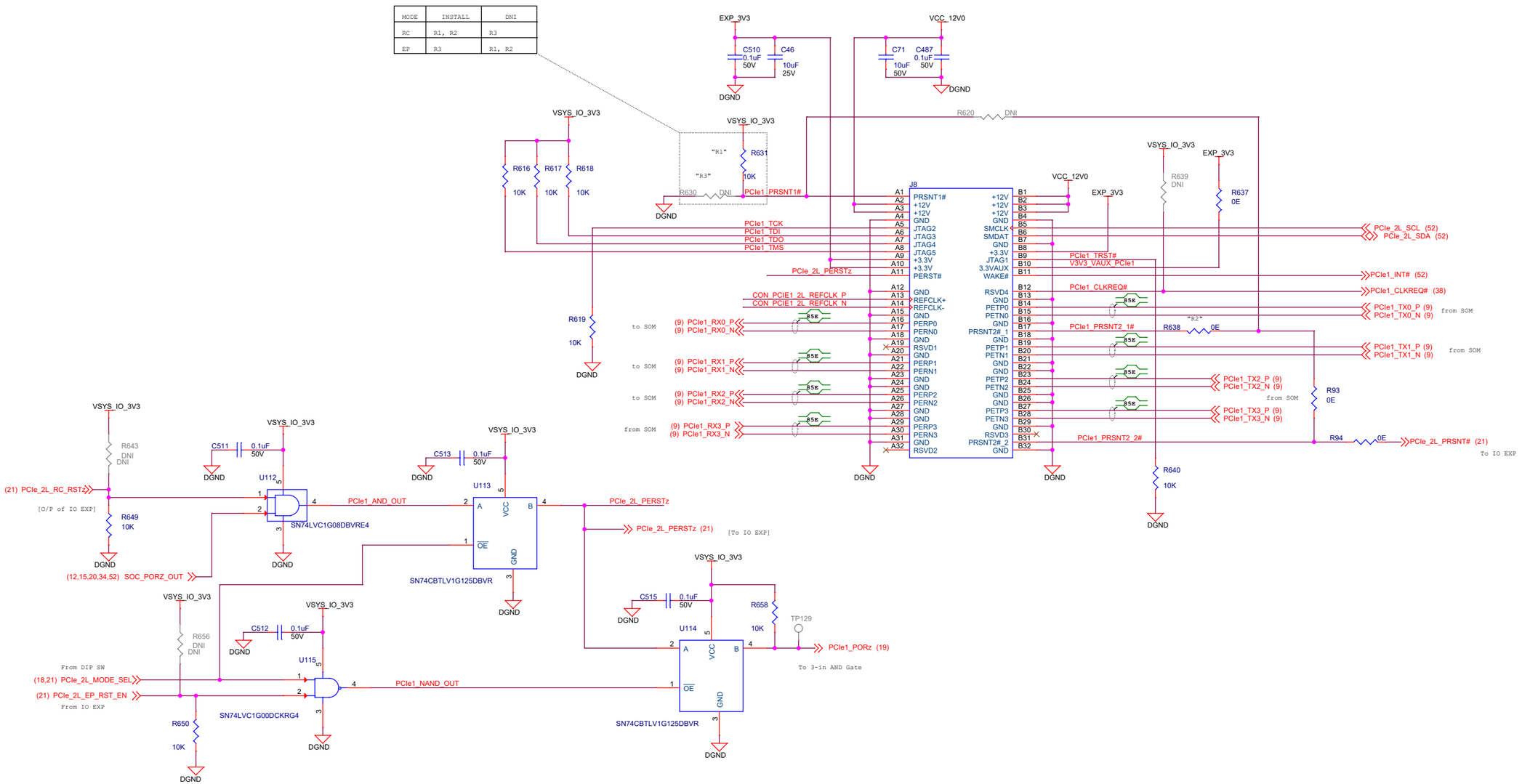
Size: C | PROC079 001 J721EXCP01EVM | Rev: E3B

Date: Thursday, November 21, 2019 | Sheet 52 of 68

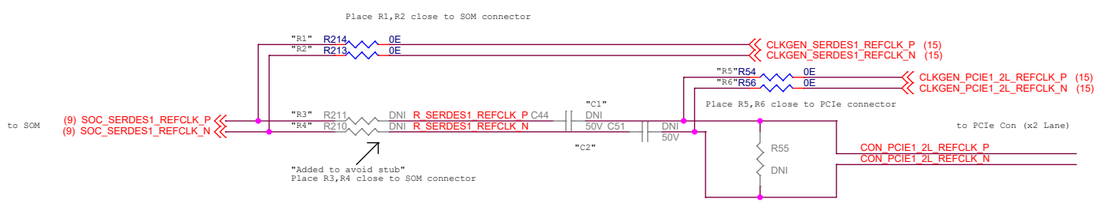
x4LANE PCIe Interface

x4 Lane PCIe Connector

MODE	INSTALL	DNI
RC	R1, R2	R3
EP	R3	R1, R2



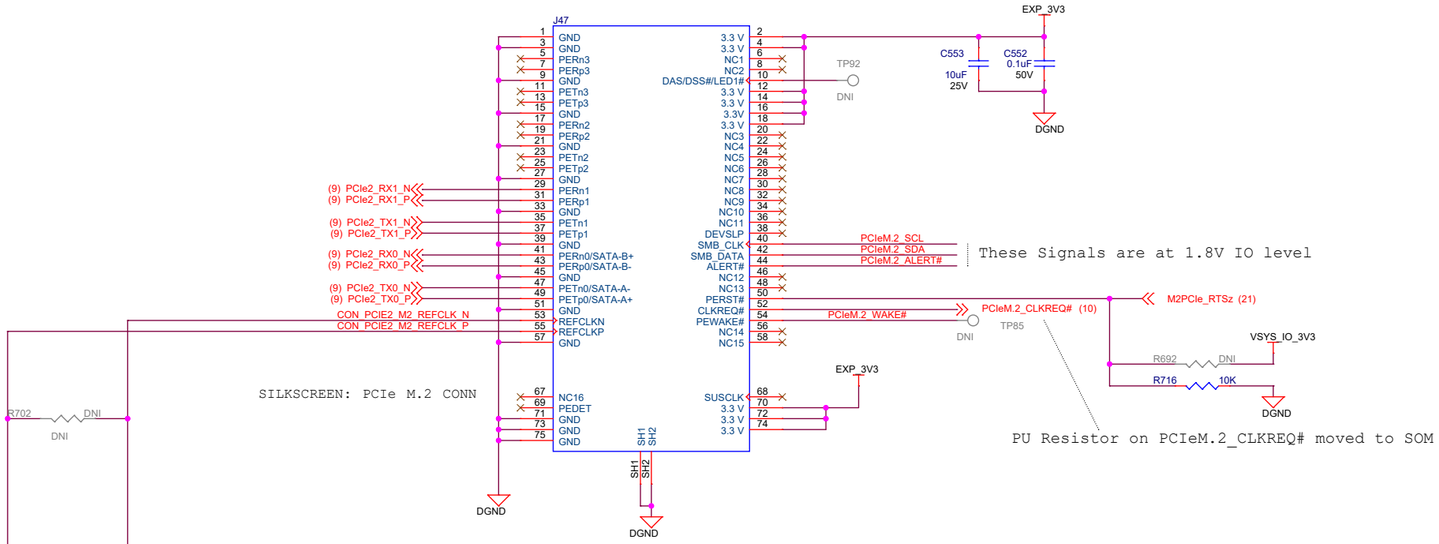
CLOCK ROOT SELECTION



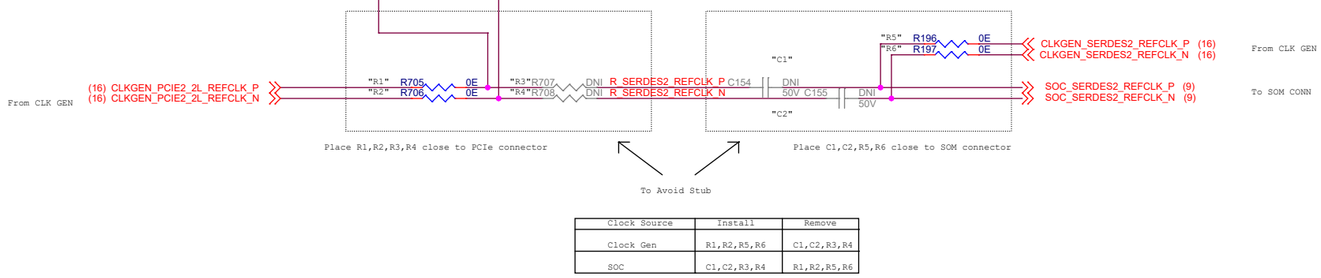
	Install	Remove
PCIe root complex	R1,R2,R5,R6	R3,R4,C1,C2
PCIe end point	R3,R4,C1,C2	R1,R2,R5,R6

Project : J7 EVM		Title	x2LANE PCIe Interface
		Size C	PROC079 001 J721EXCP01EVM — Rev E3B
		Date: Thursday, November 21, 2019	Sheet 53 of 68

PCIe_M.2_INTERFACE

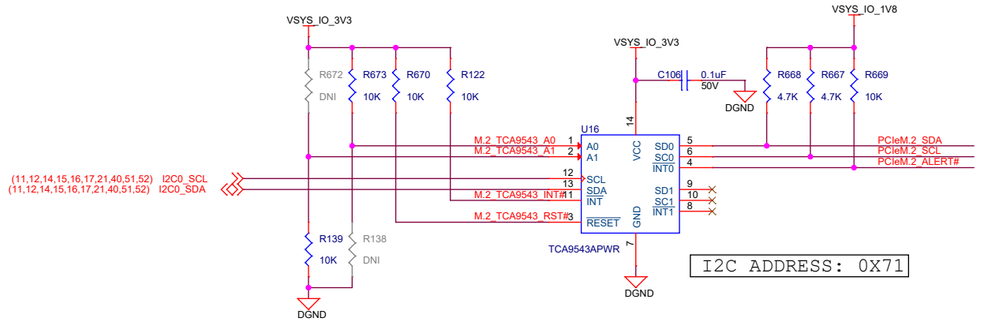


CLOCK ROOT SELECTION



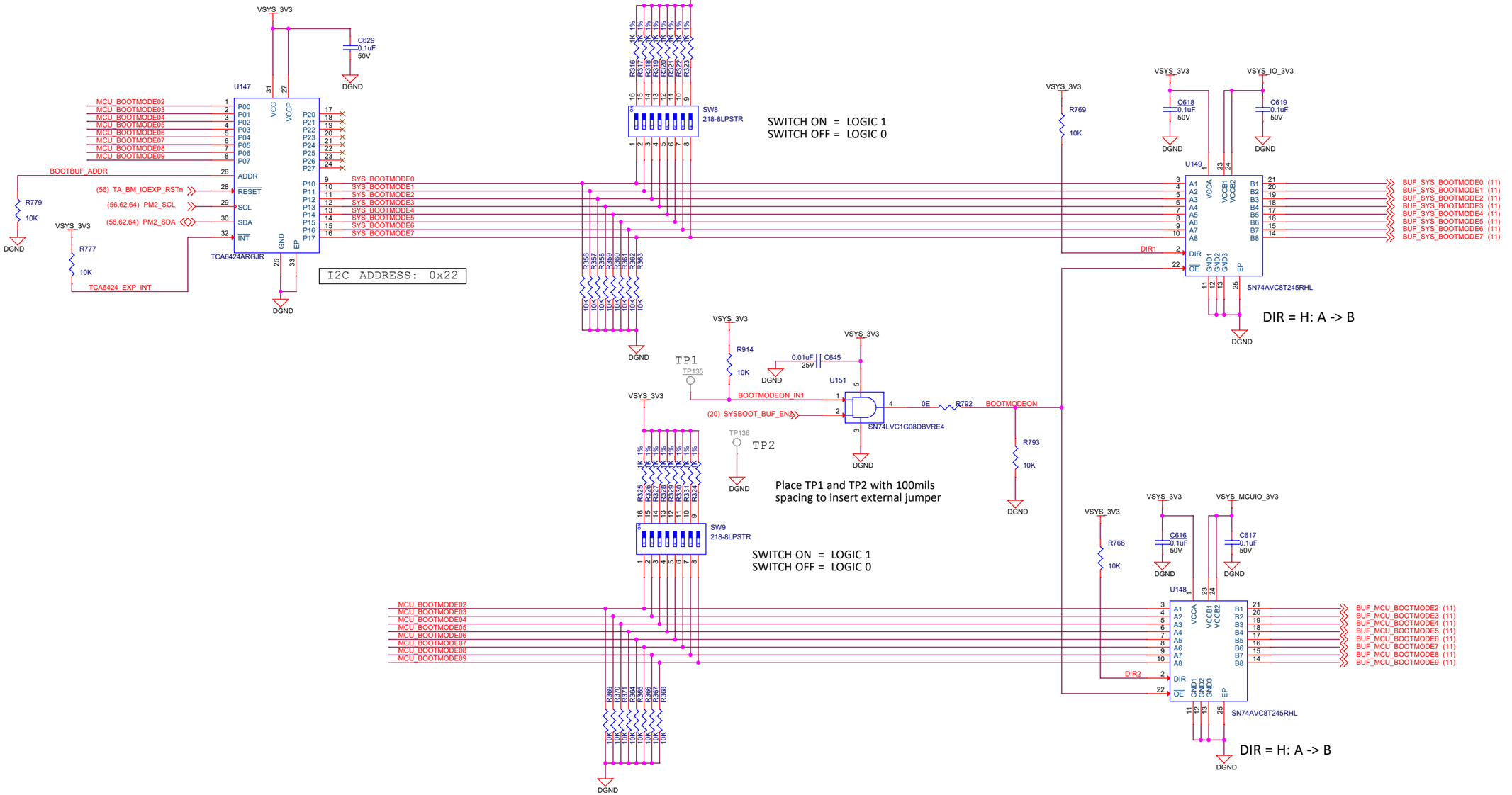
Clock Source	Install	Remove
Clock Gen	R1,R2,R5,R6	C1,C2,R3,R4
SOC	C1,C2,R3,R4	R1,R2,R5,R6

3.3V To 1V8 Level translator



Project : J7 EVM	TEXAS INSTRUMENTS	Title: PCIe_M.2_INTERFACE
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 54 of 68

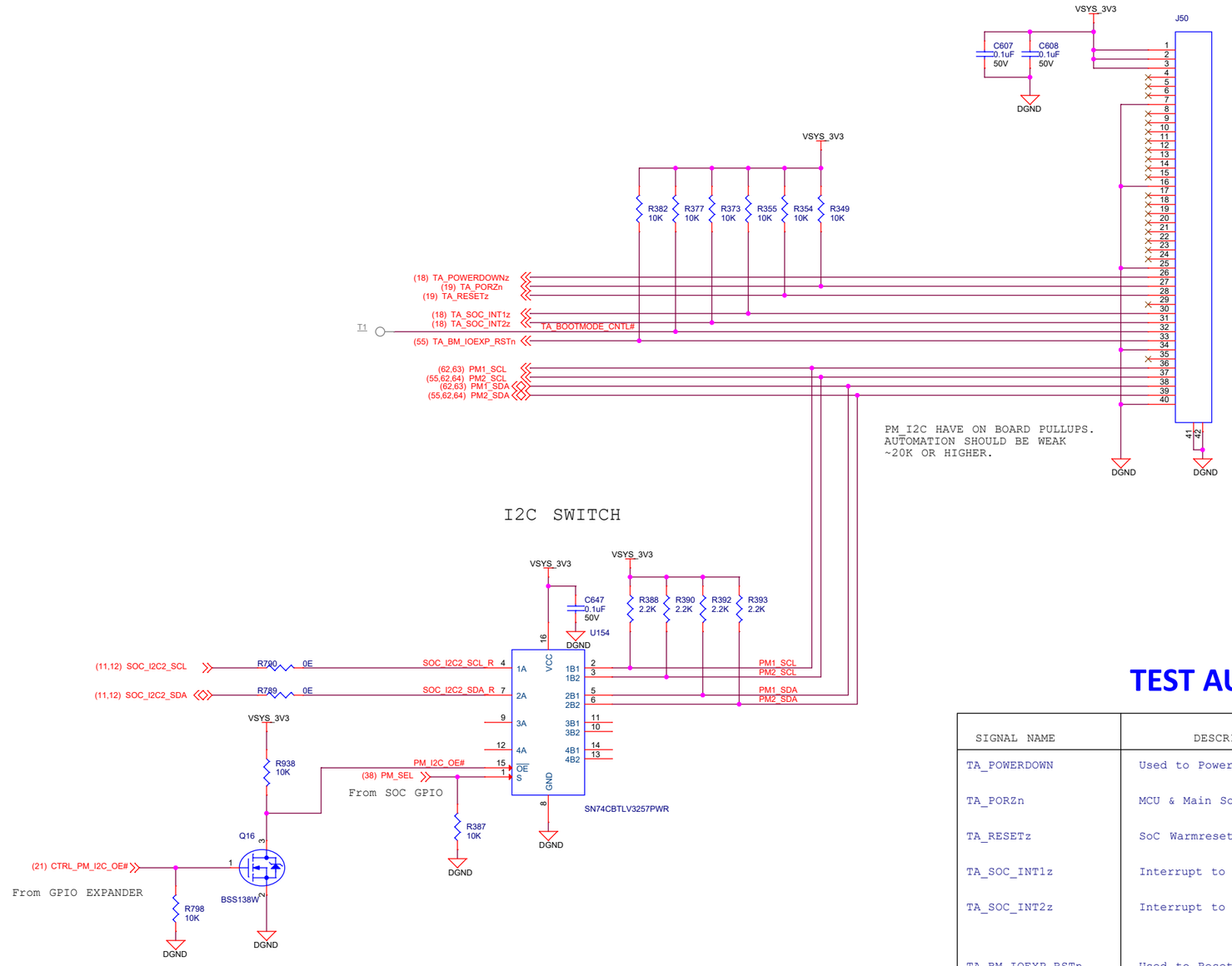
BOOT MODE BUFFER & SWITCHES



TA_BM_IOEXP_RSTn	SOC_PORZ_OUT	BOOTMODE Control from Test Automation HDR
HIGH	LOW	Enabled
HIGH	HIGH	Disabled

Project : J7 EVM	TEXAS INSTRUMENTS	Title: BOOT MODE BUFFER & SWITCHES
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 55 of 68

TEST AUTOMATION HEADER



AUTOMATION INTERFACE

ALL SIGNALS SHOULD BE
REFERENCED TO EVM_3V3

Cable : Parlex-050R40-76B, .5mm 3"

TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	MCU & Main SoC domain Power ON Reset	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_SOC_INT1z	Interrupt to SOC	OUTPUT	External Pullup
TA_SOC_INT2z	Interrupt to SOC	OUTPUT	External Pullup
TA_BM_IOEXP_RSTn	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

Project : J7 EVM	TEXAS INSTRUMENTS	Title: TEST AUTOMATION HEADER Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B Date: Thursday, November 21, 2019 — Sheet 56 of 68

OVER VOLTAGE PROTECTION CIRCUIT

Reverse Polarity protection CKT

VCAPL C472 2.2uF 50V VCAPH
U107
VCAPL VCAPH
ANODE CATHODE
GATE_PULL_DOWN
GATE_DRIVE NC1 NC2
LM74610QDDGKRQ1
GATE
U4
CSD18501Q5A

SPARE FUSE

F2
10A
0154010.DR

Power Input

PJ-082BH
J7
VMAIN_CONN
F1
10A
0154010.DR
VMAIN_FUSE
D11
SMCJ64CA
SH4 SH3 SH2 SH1
DGND DGND

SILK: POWER IN

Normal operation Range for VINPUT 6.5V to 28V.

C36 100uF_50V
C39 0.22uF 50V
C38 0.1uF 50V
C37 0.1uF 50V
R2 1K_1%

VMAIN

R576 715K_1%
R573 100K_1%
R580 5.62K_1%
R575 47K_1%
R574 47K_1%
C446 0.1uF 50V
C460 0.1uF 50V

U100
LM5060_SENSE
LM5060_OVP
LM5060_ULVO
LM5060_TIMER
LM5060_nPGD
SENSE OVP UVLO TIMER NPGD
VIN GATE OUT GND EN
LM5060MM
LM5060_GATE
LM5060_OUT
LM5060_EN

Q3 SUM60N10-17-E3
C459 DNI 50V
R593 0E
C7 4.7uF 50V
C8 0.1uF 50V
C6 100uF_50V
VINPUT
R1 1K_1%
LD2
5988170107F
R583 10K
SW2
1101M2S3CQE2
R50 1K_1%
LM5060_EN_LOW
LM5060_EN_HIGH

SILK: "POWER ON"
ON/OFF Control Switch

J54
LM5060_EN_HIGH 1
LM5060_EN 2
LM5060_EN_LOW 3

VINPUT VMAIN
TP19 DNI
TP20 DNI

Fault Indication

SILK: "POWER FAULT" **RED**

LD3
5988110107F
Q14
BSS138-7-F
R592 10K
R584 100K
LM5060_EN
LM5060_nPGD
D44
BZT52C13S

Condition	LED Status
VMAIN between 6.5 to 28V	OFF
VMAIN beyond 28V or below 6.5V	ON

Cooling FAN Header

J15
VCC_12V0
C574 0.1uF 50V

Mating Parts: 440129-3 & 1735801-1

Ground test points

TP73 5002
TP2 5002

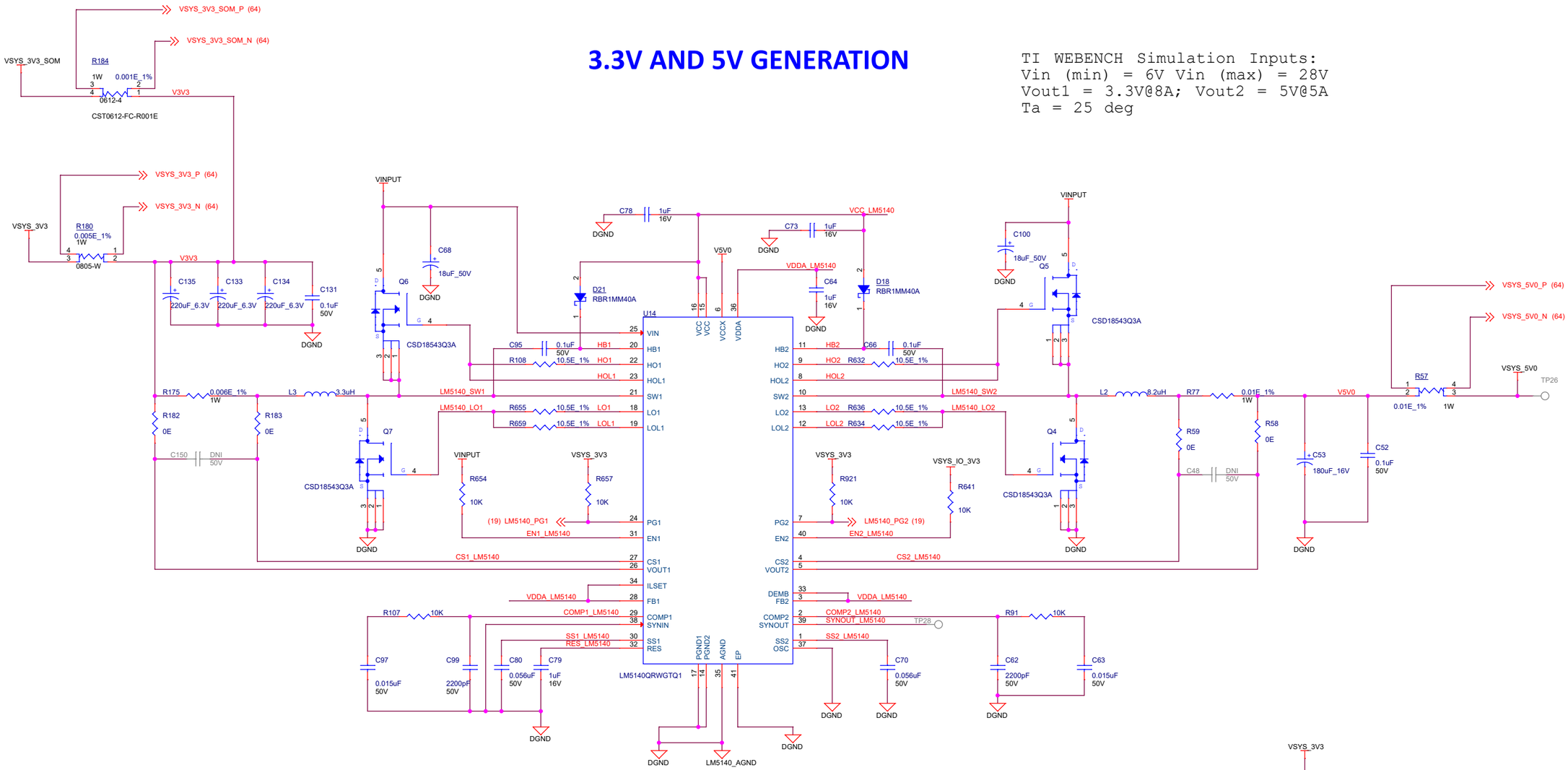
Note: When fault is indicated; set to proper voltage and power cycle the board.

Project : J7 EVM	TEXAS INSTRUMENTS	Title: OVER VOLTAGE PROTECTION CKT	
		Size: C — PROC079 001 J721EXCP01EVM	Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 57 of 68

POWER SUPPLY #1

3.3V AND 5V GENERATION

TI WEBENCH Simulation Inputs:
Vin (min) = 6V Vin (max) = 28V
Vout1 = 3.3V@8A; Vout2 = 5V@5A
Ta = 25 deg



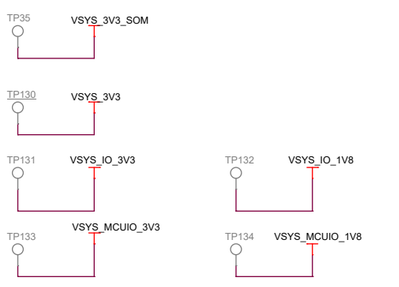
PCB Note: Short LM5140_AGND and DGND at single point

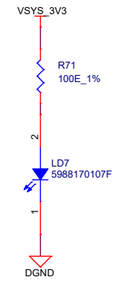
FB1 connected to VDDA to set VOUT1=3.3V
FB2 connected to VDDA to set VOUT2=5V

OSC pin to VCC sets fs=2.2MHz
OSC pin to GND sets fs=440kHz

DEMB-VDDA- FPWM mode operation
DEMB-GND- enables diode emulation

ILSET pin to VDDA sets current limit threshold to 73 mV
ILSET pin to GND sets current limit threshold to 48 mV

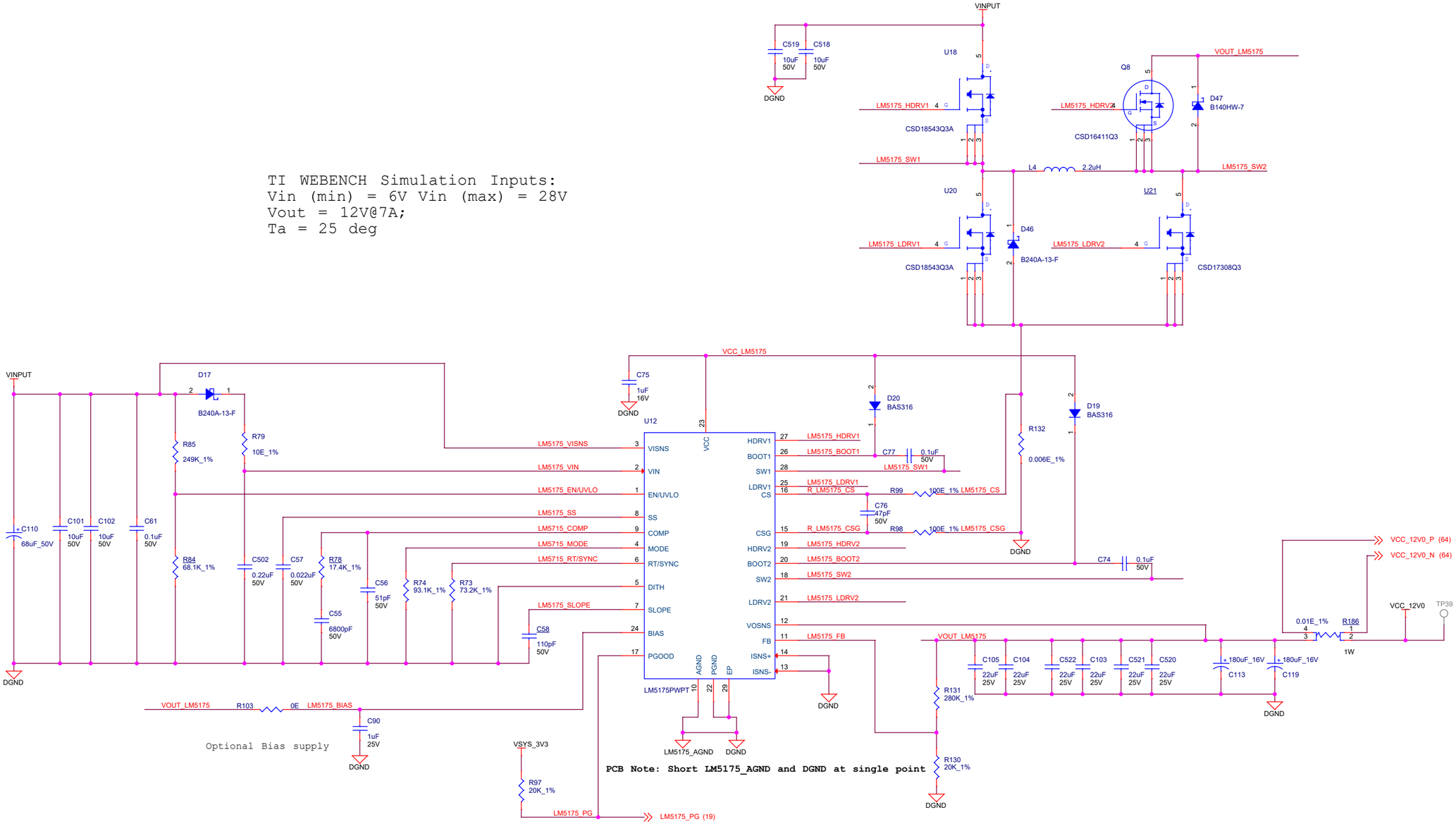




Project : J7 EVM	Title: POWER SUPPLY #1	
	Size: C — PROC079 001 J721EXCP01EVM	Rev: E3B
	Date: Thursday, November 21, 2019	Sheet 58 of 68

POWER SUPPLY #2

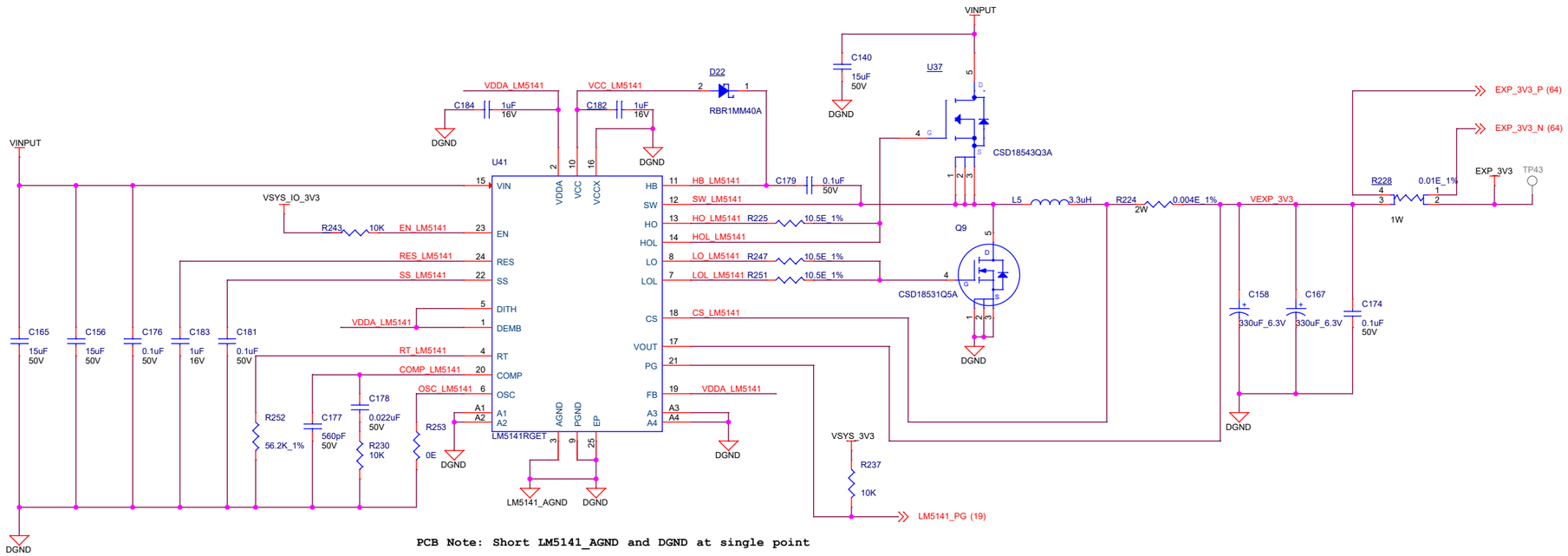
TI WEBENCH Simulation Inputs:
Vin (min) = 6V Vin (max) = 28V
Vout = 12V@7A;
Ta = 25 deg



Project : J7 EVM	TEXAS INSTRUMENTS	Title: POWER SUPPLY #2
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 59 of 68

POWER SUPPLY #3

TI WEBENCH Simulation Inputs:
Vin (min) = 8V Vin (max) = 28V
Vout = 3.3V@10A;
Ta = 25 deg



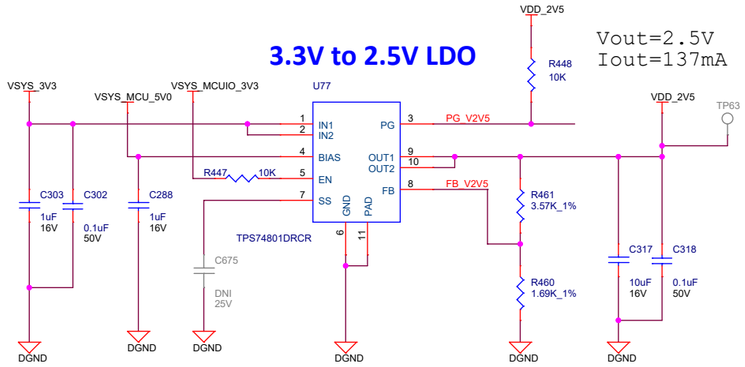
PCB Note: Short LM5141_AGND and DGND at single point

Project : J7 EVM	TEXAS INSTRUMENTS	Title: POWER SUPPLY #3	
		Size: C	PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019	Sheet 60 of 68

POWER SUPPLY #4

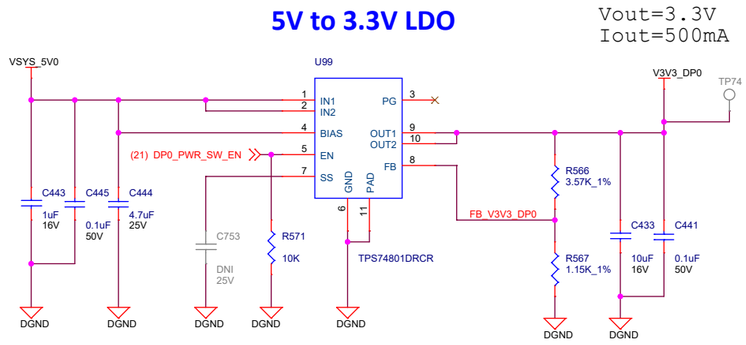
ETHERNET POWER

3.3V to 2.5V LDO



Display Port0

5V to 3.3V LDO



PCB NOTE:Keep 4.7uF capacitor close to BIAS pin.
Keep this circuit close to DP PORT0 Connector

3.3V to 1.0V LDO

PCB NOTE:Keep 4.7uF capacitor close BIAS pin

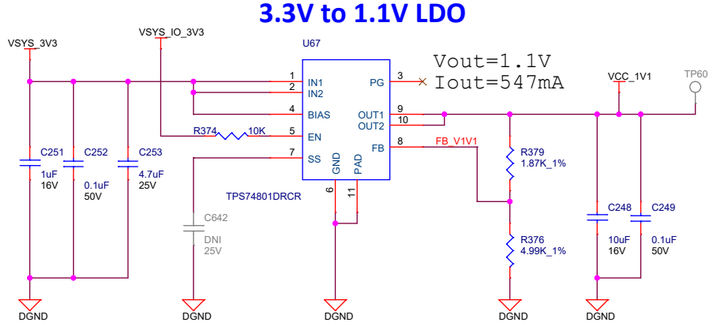
Display Port1

5V to 3.3V LDO

PCB NOTE:Keep 4.7uF capacitor close to BIAS pin.
Keep this circuit close to DP PORT1 Connector.

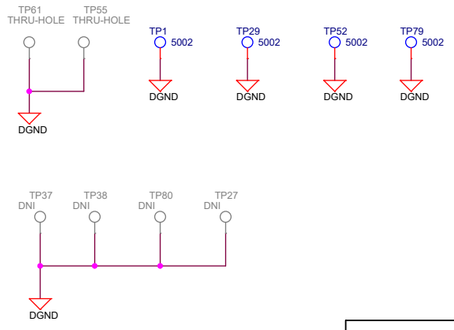
FPD-LINK4 and USB HUB POWER

3.3V to 1.1V LDO



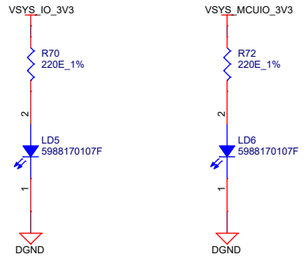
PCB NOTE:Keep 4.7uF capacitor close BIAS pin

GROUND TEST POINTS



PCB NOTE: Spread the SMD test points Top and Bottom Side of PCB

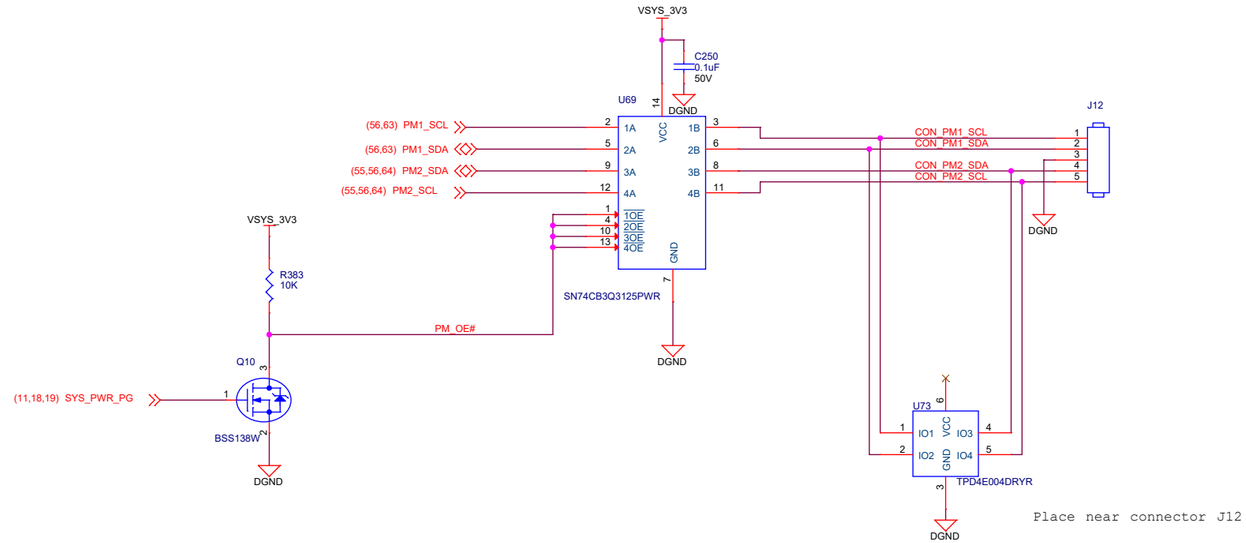
POWER INDICATION LED's



SOC PWR LED MCU PWR LED

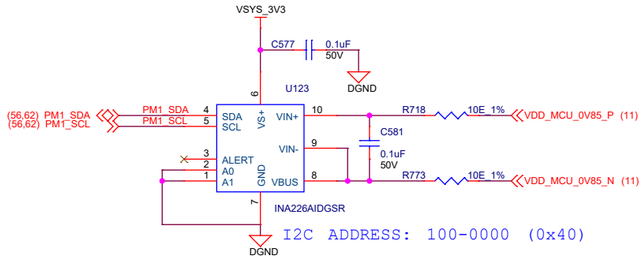
Project : J7 EVM	Title: POWER SUPPLY #4	
	Size: C — PROC079 001 J721EXCP01EVM	Rev: E3B
	Date: Thursday, November 21, 2019	Sheet 61 of 68

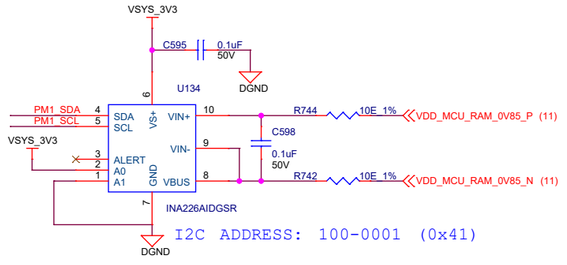
EXTERNAL POWER MEASUREMENT WITH ISOLATION

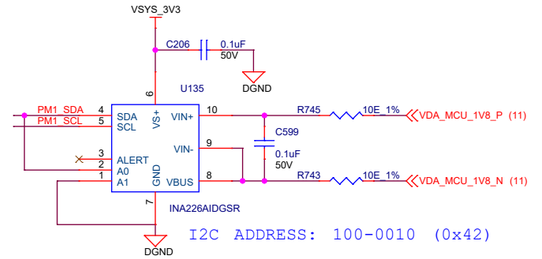


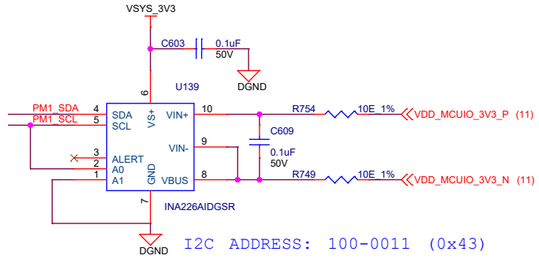
Project : J7 EVM	TEXAS INSTRUMENTS	Title: EXTERNAL POWER MEASUREMENT WITH ISOLATION
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 62 of 68

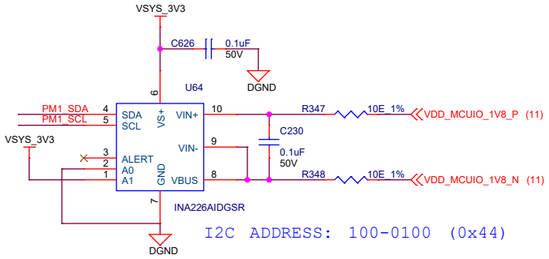
CURRENT MONITORS #1

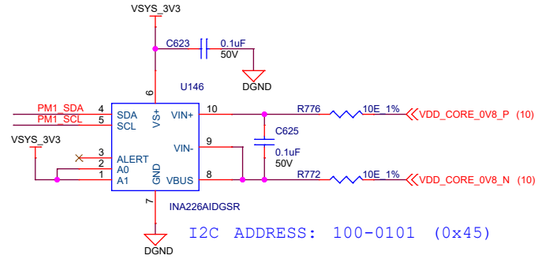


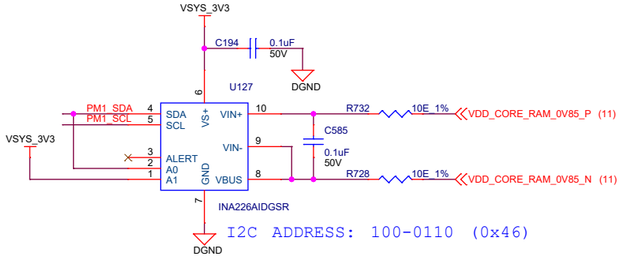


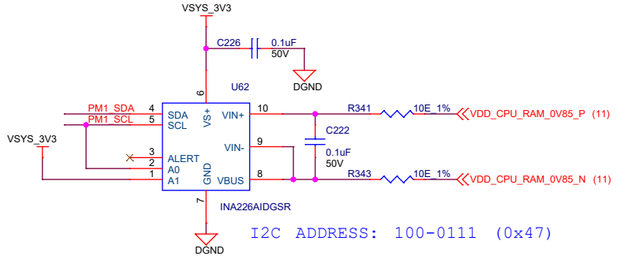


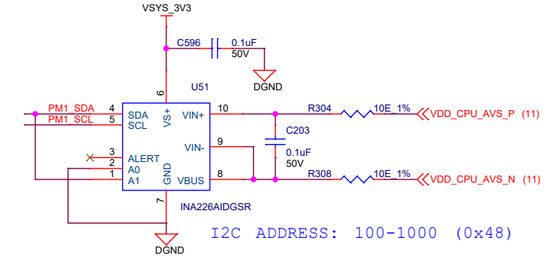


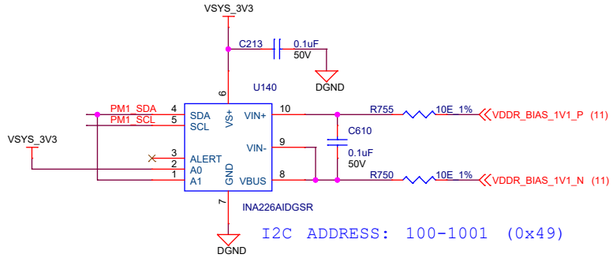


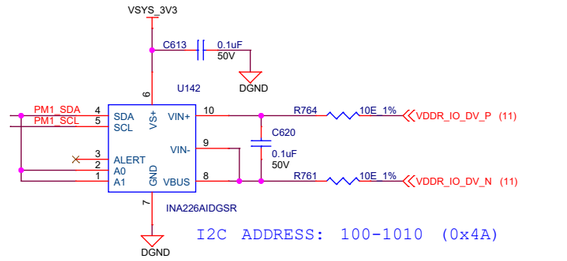


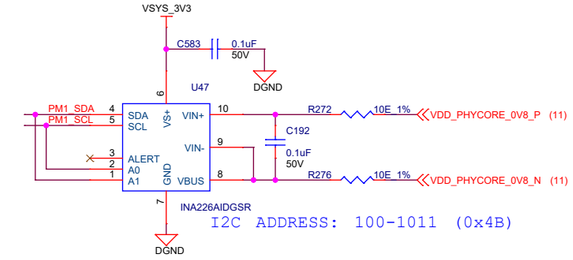


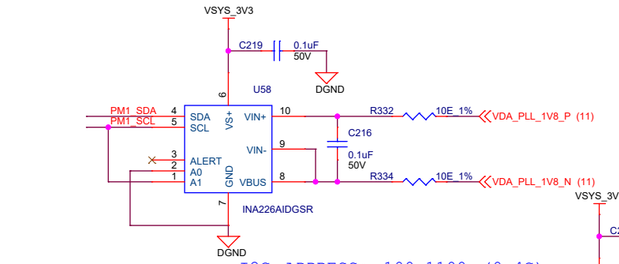


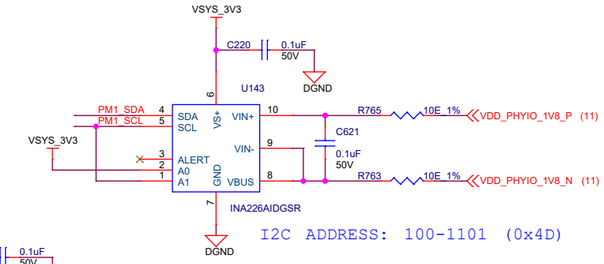


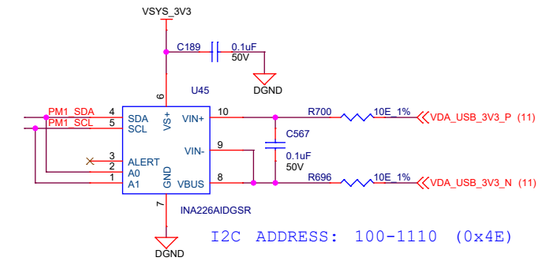


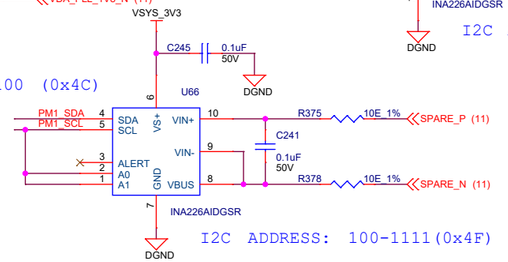






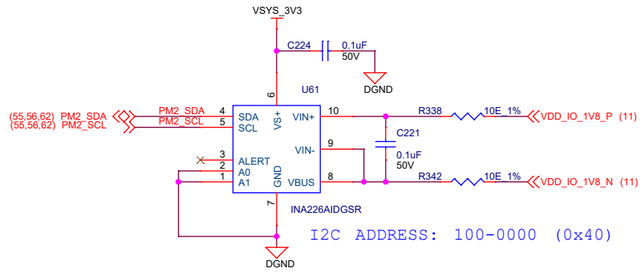


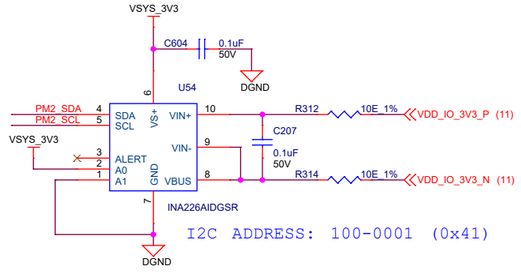


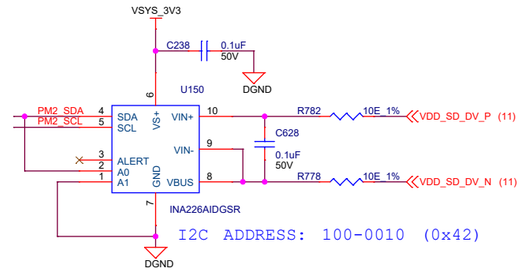


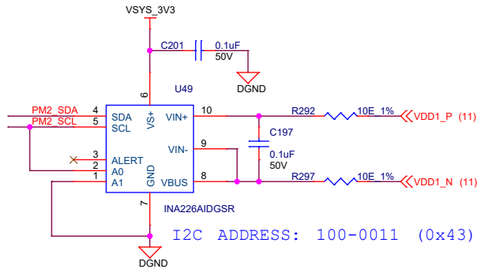
Project : J7 EVM	TEXAS INSTRUMENTS	Title: CURRENT MONITORS #1
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 63 of 68

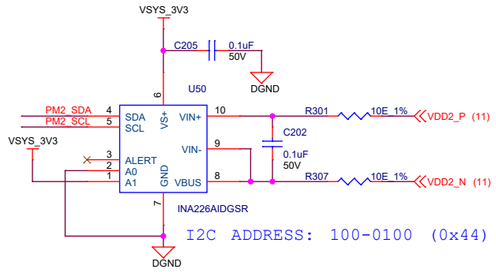
CURRENT MONITORS #2

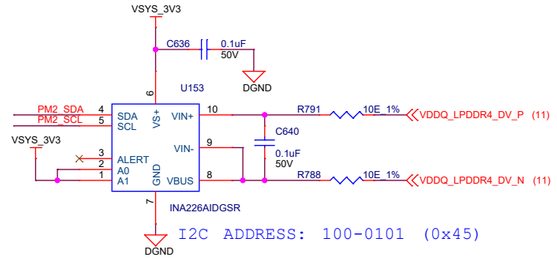


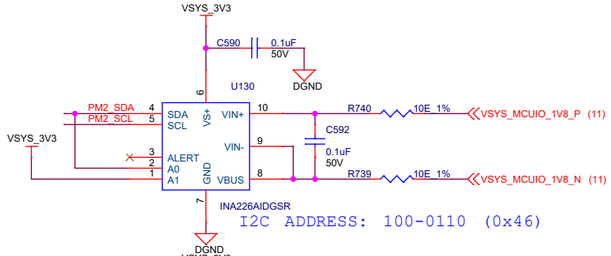


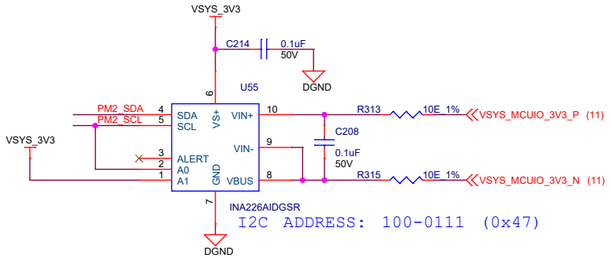


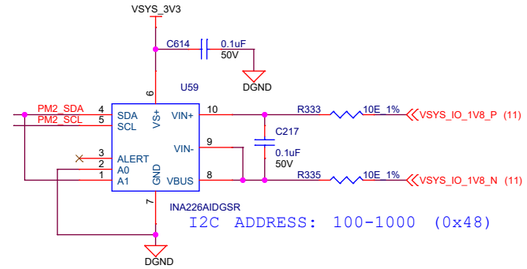


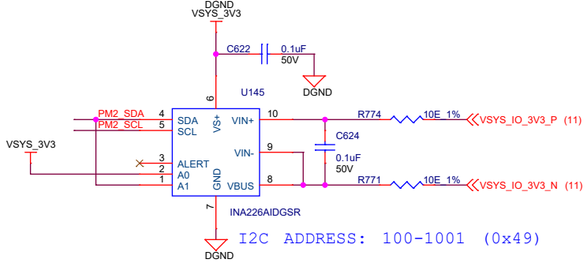


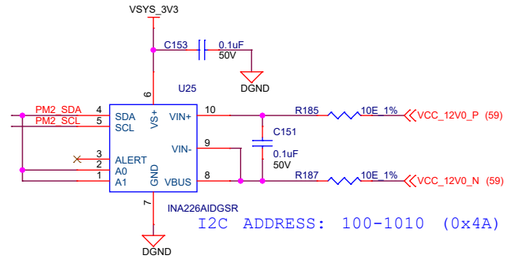


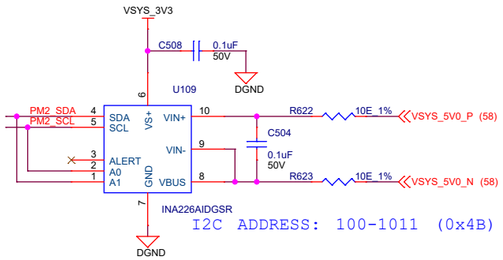


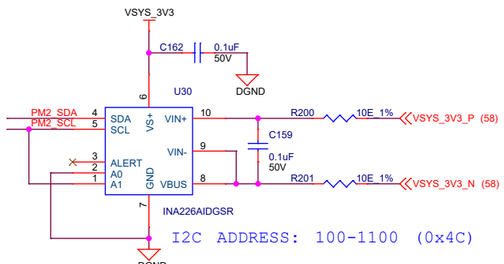


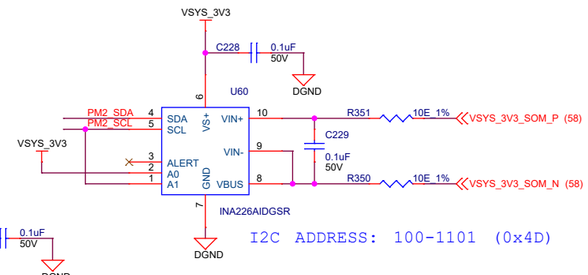


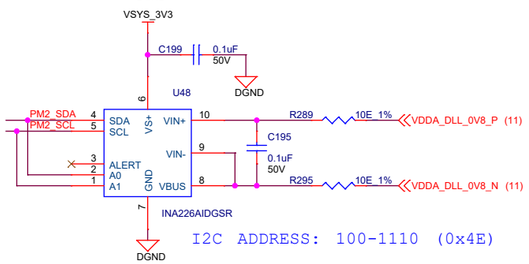


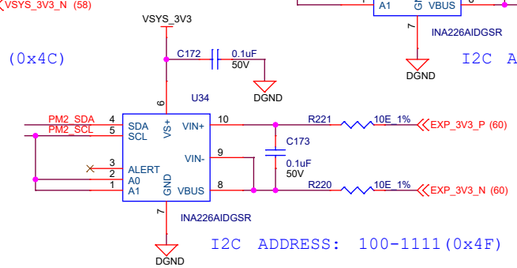












Project : J7 EVM	TEXAS INSTRUMENTS	Title: CURRENT MONITORS #2
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 64 of 68

THIS PAGE IS RESERVED

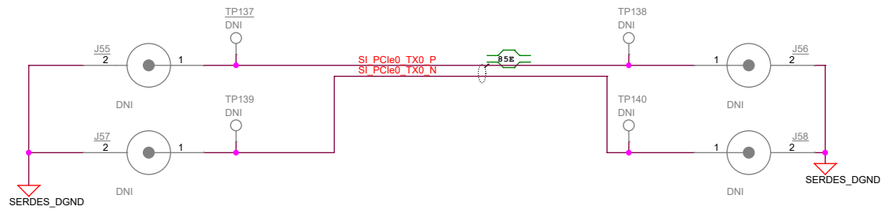
Project : J7 EVM	TEXAS INSTRUMENTS	Title: RESERVED #1
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 65 of 68

THIS PAGE IS RESERVED

Project : J7 EVM	TEXAS INSTRUMENTS	Title: RESERVED #2
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 66 of 68

SI_SIMULATION_COUPON_BD

Test coupon not part of EVM design, to be used for TI test only



Project : J7 EVM	TEXAS INSTRUMENTS	Title: SI_SIMULATION_ COUPON_BD
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 67 of 68

HARDWARE SCHEMATICS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions shall be observed.

5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

FIDUCIALS

FID1 DNI
FID2 DNI
FID3 DNI
FID4 DNI
FID5 DNI
FID6 DNI

LABELS

Board Serial No.

LBL1
PCB LABEL
THT-103-423-10

Assembly Revision.

LBL2
PCB LABEL
THT-103-423-10

STANDOFFs

MH2 MH3 MH4 MH5 MH6 MH7 MH8 MH9
970300321 970300321 970300321 970300321 970300321 970300321 970300321 970300321

MH18 MH19 MH20 MH21 MH22 MH23 MH24
R30-4000502 R30-4000502 R30-4000502 R30-4000502 R30-4000502 R30-4000502 R30-4000502

MH25 MH26 MH27 MH28 MH29 MH30 MH31 MH32
971150321 971150321 971150321 971150321 971150321 971150321 971150321 971050321

JACK SCREWS

ACC1 ACC2 ACC3 ACC4
JSO-0515-01 JSO-0515-01 JSO-0515-01 JSO-0515-01

SCREWS

MH10 MH11 MH12 MH13
RM3X8MM 2701 RM3X8MM 2701 RM3X8MM 2701 RM3X8MM 2701

MH14 MH15 MH16 MH17
RM3X8MM 2701 RM3X8MM 2701 RM3X8MM 2701 RM3X8MM 2701

RUBBER FEET

M1 M2 M3 M4
728 728 728 728

M5 M6 M7 M8
728 728 728 728

HEX NUT

MH33 MH34 MH35 MH36 MH37 MH38 MH39
4708 4708 4708 4708 4708 4708 4708

SCREW & WASHER FOR PCIe M.2

MH1
9774015243R

MH40
DNI

MH41
DNI

SCREW & WASHER for ENET EXP BRD

MH42 MH43
970050151 970050151

MH44
970050351

MH45 MH46 MH47 MH48
29300 29300 29300 29300

MH49
RM3X12MM 2701

CPB BARE PCB

PCB1
PROC079E3

QUAD PORT ETH EXP ASSEMBLED PCB

PCBA1
PROC080E2

LOGOs

PCB LOGO DNI
Texas Intruments

PCB LOGO DNI
For Evaluation only; not FCC approved for resale

PCB LOGO DNI
WEEE Mark

PCB LOGO DNI
CE Mark

Project : J7 EVM	TEXAS INSTRUMENTS	Title: HARDWARE SCHEMATICS
		Size: C — PROC079 001 J721EXCP01EVM — Rev: E3B
		Date: Thursday, November 21, 2019 — Sheet 68 of 68