检视重点

1、降额审查

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b 电阻降额 ---- 按照降额 50%

c 功率电感降额 ---- 按照饱和电流 80% 降额

d DCDC/LDO 降额 ---- 按照输出功率 80% 降额

e 二极管 三极管 MOS管 降额 ---- 75% 降额

注意 三极管 MOS管 的开启电压 VCE/VGS 在手册规定范围内

e 保险丝 ---- 75% 降额

f 光耦 ---- 工作电压 工作电流 电流传输比 70% 降额

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2、新封装封装和使用场景审查

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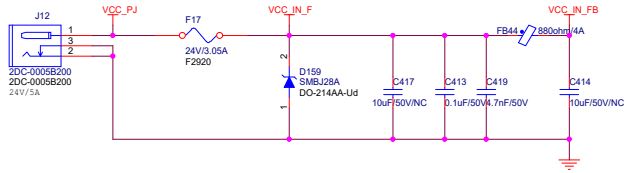
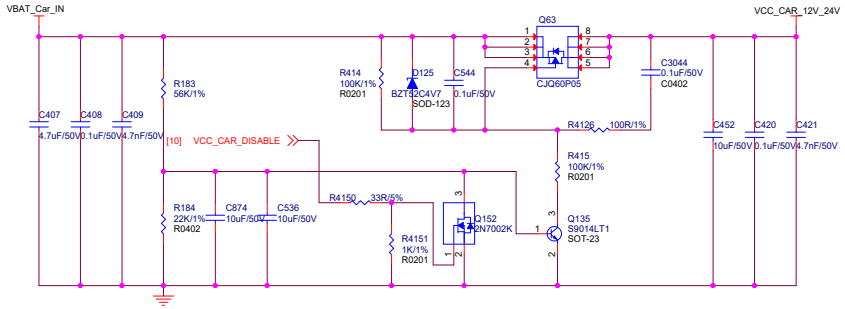
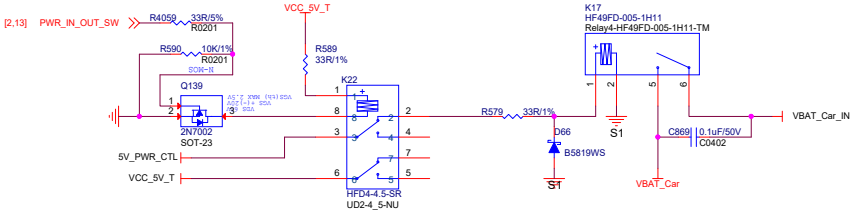
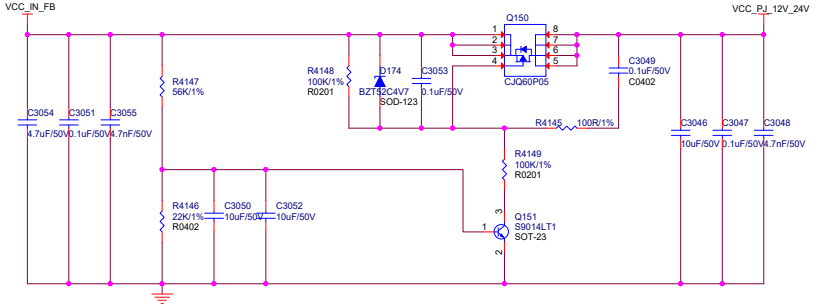
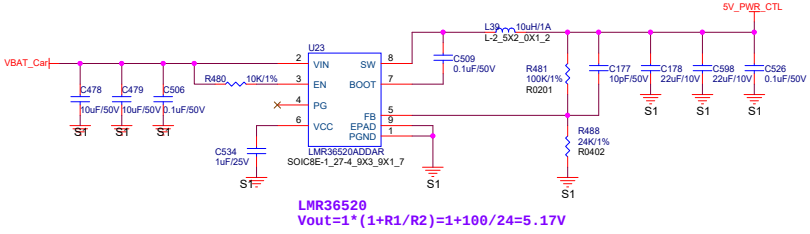
Design Name	DC1912		
Page Name	Block Diagram		
Designer	WANGTONG A22303	RevCode	V1
Reviewer	<Reviewer>	Page Size	C
Creat Time	Monday, August 01, 2022	Page Num	1 of 24

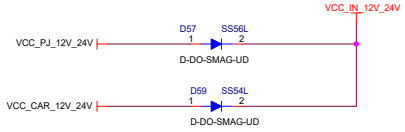












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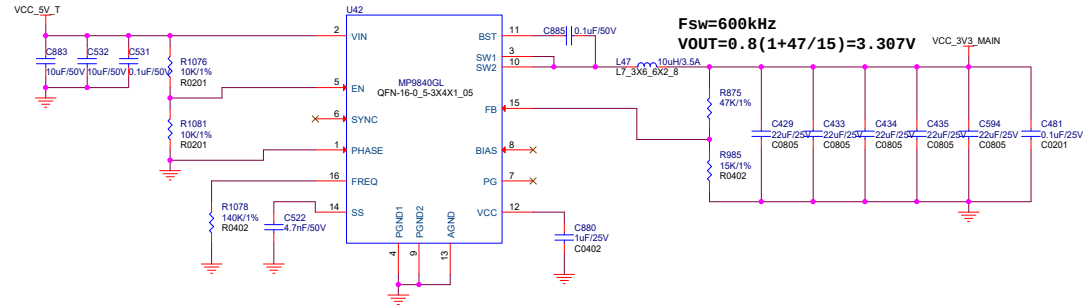
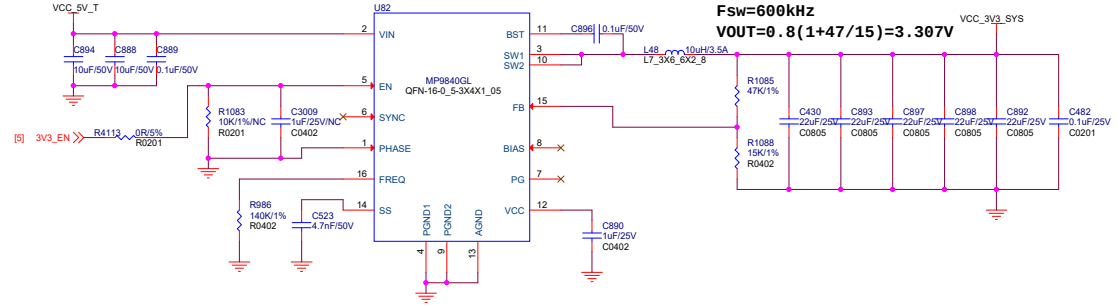
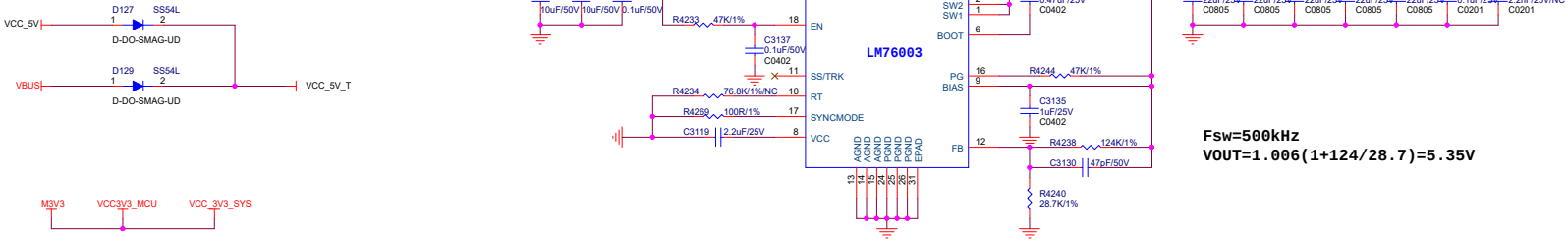
Page Name	Power Tree		
Designer	WANGTONG A22303	RevCode	V1
Reviewer	<Reviewer>	Page Size	C
Creat Time	Monday, August 01, 2022	Page Num	2 of 24







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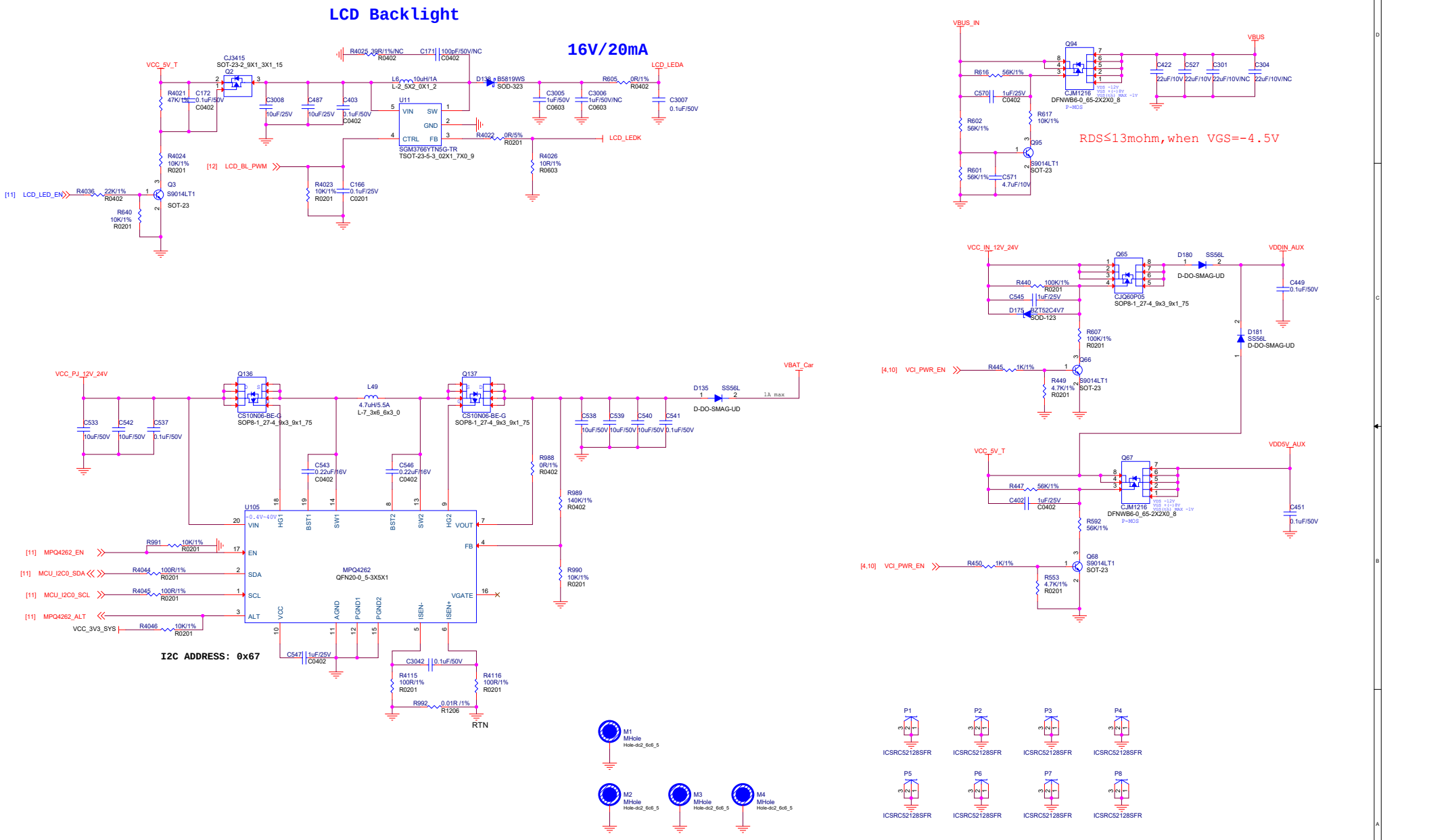
Designer	WANGTONG A22303	RevCode	V1
Reviewer	<Reviewer>	Page Size	C
Creat Time	Monday, August 01, 2022	Page Num	3 of 24



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Design Name	DC1912		
Page Name	Power		
Designer	WANGTONG A22303	RevCode	V1
Reviewer	<Reviewer>	Page Size	C
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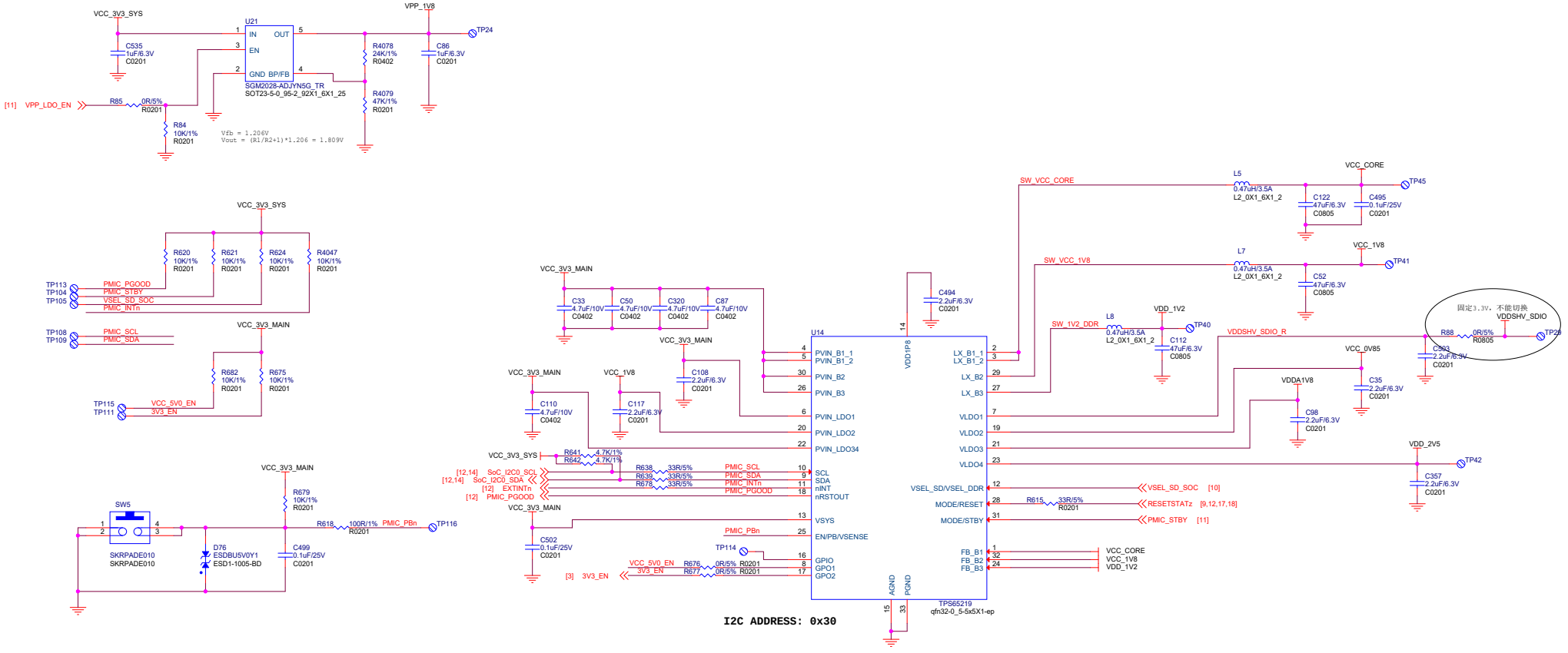
PMIC REGULATORS	VOLTAGE RAIL	CURRENT(mA)
BUCK 1	VCC_CORE(0.75V)	2700
BUCK 2	VCC_1V8	995
BUCK 3	VDD_1V2	936
LDO 1	VDDSHV_SDIO	50
LDO 2	VDDR_CORE	150
LDO 3	VDDA_1V8	200
LDO 4	VDD_2V5	300



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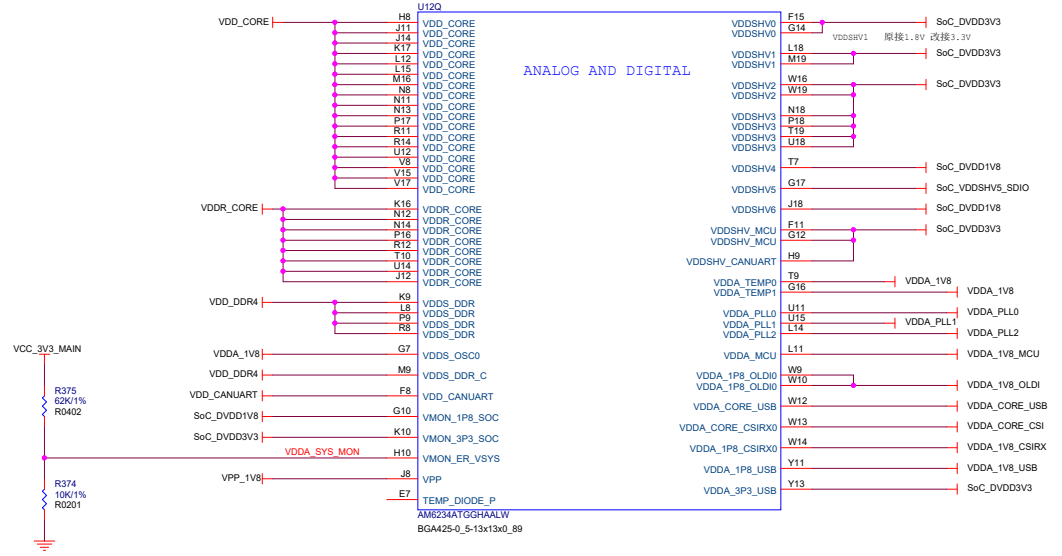
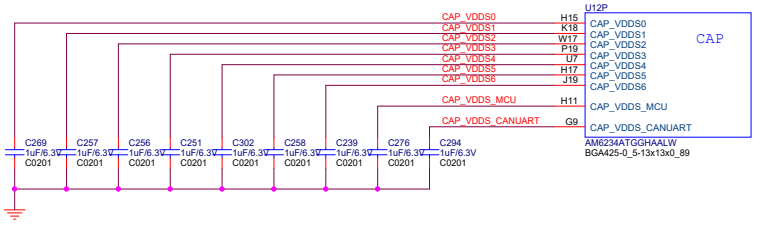
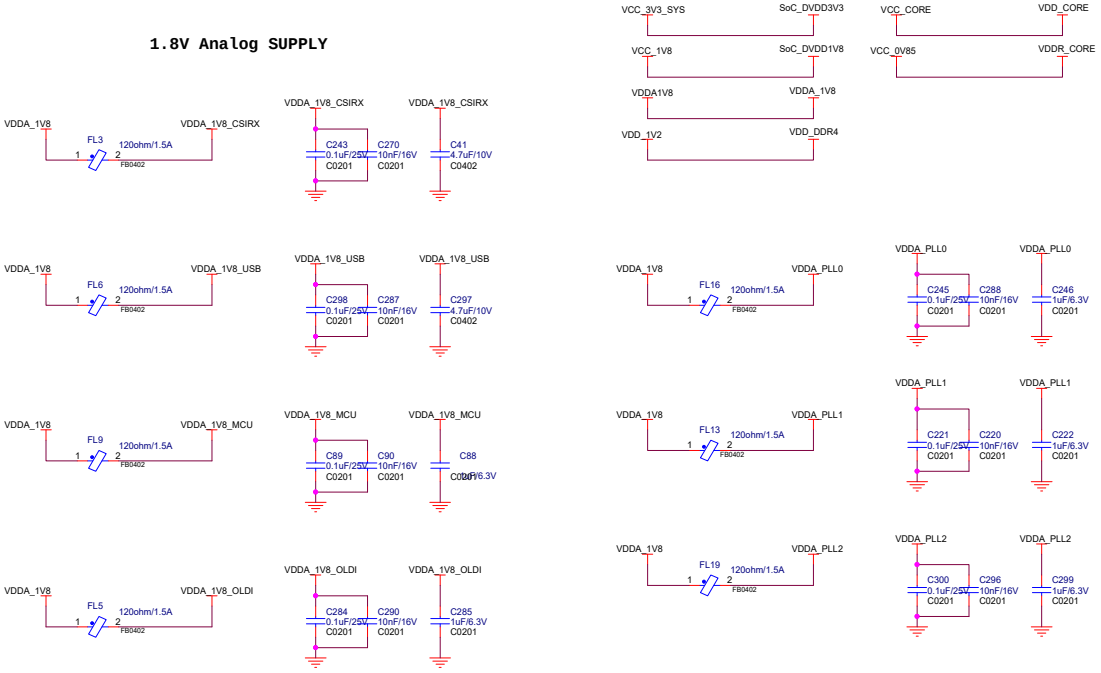
Design Name	DC1912		
Page Name	PMIC		
Designer	WANGTONG A22303	RevCode	V1
Reviewer	<Reviewer>	Page Size	C
Creat Time	Monday, August 01, 2022	Page Num	5 of 24

SOC POWER

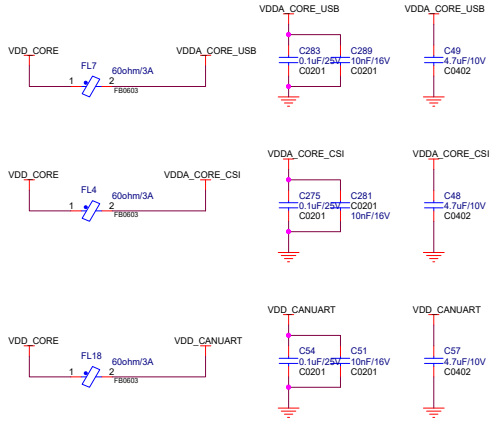




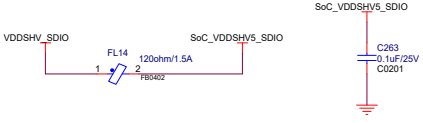
1.8V Analog SUPPLY



CORE SUPPLY



3.3V/1.8V MMC1 SUPPLY



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Page Name	SOC Power		
Designer	WANGTONG A22303	RevCode	V1
Reviewer	<Reviewer>	Page Size	C
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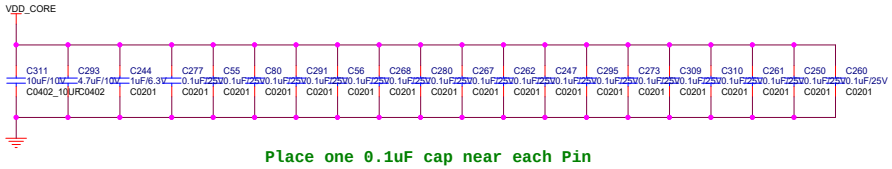
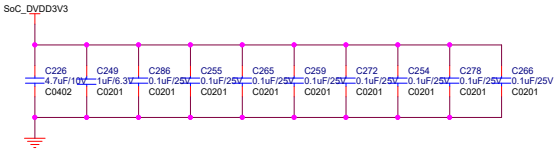
SOC POWER DECAPS



Place one 0.1uF cap near each Pin



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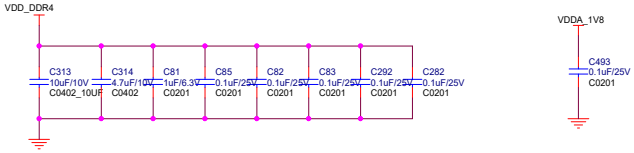

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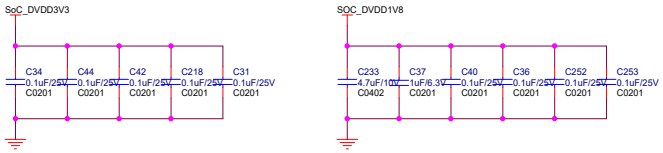

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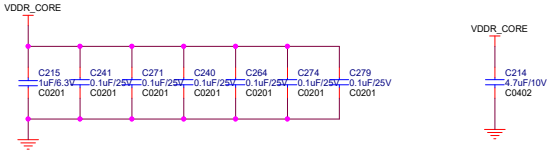

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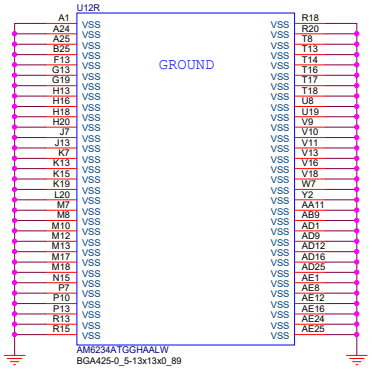
SOC VSS



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Page Name	SOC Power CAPs		
Designer	WANGTONG A22303	RevCode	V1
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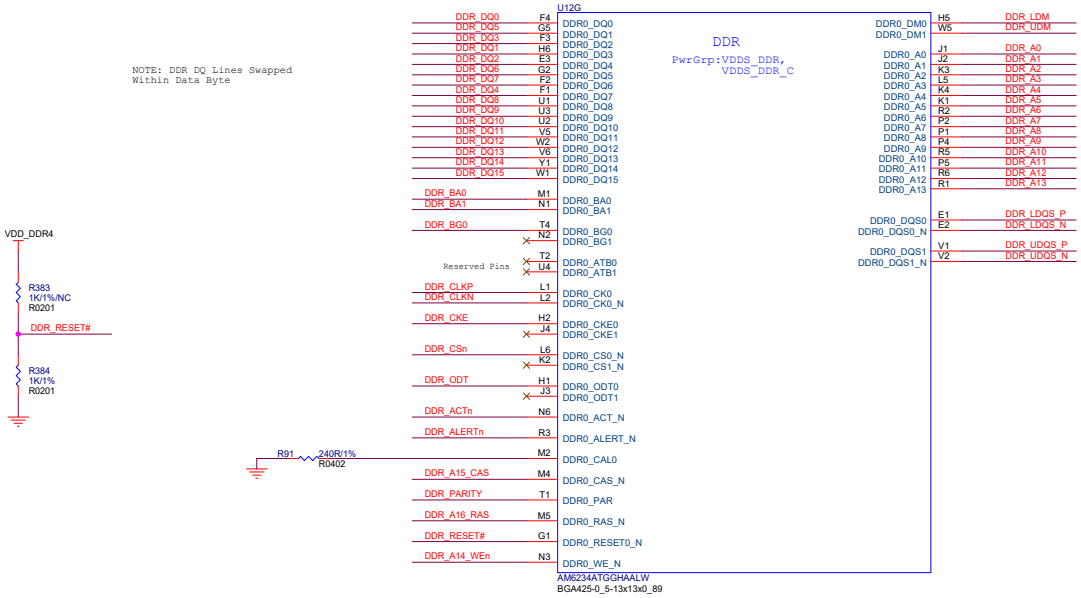
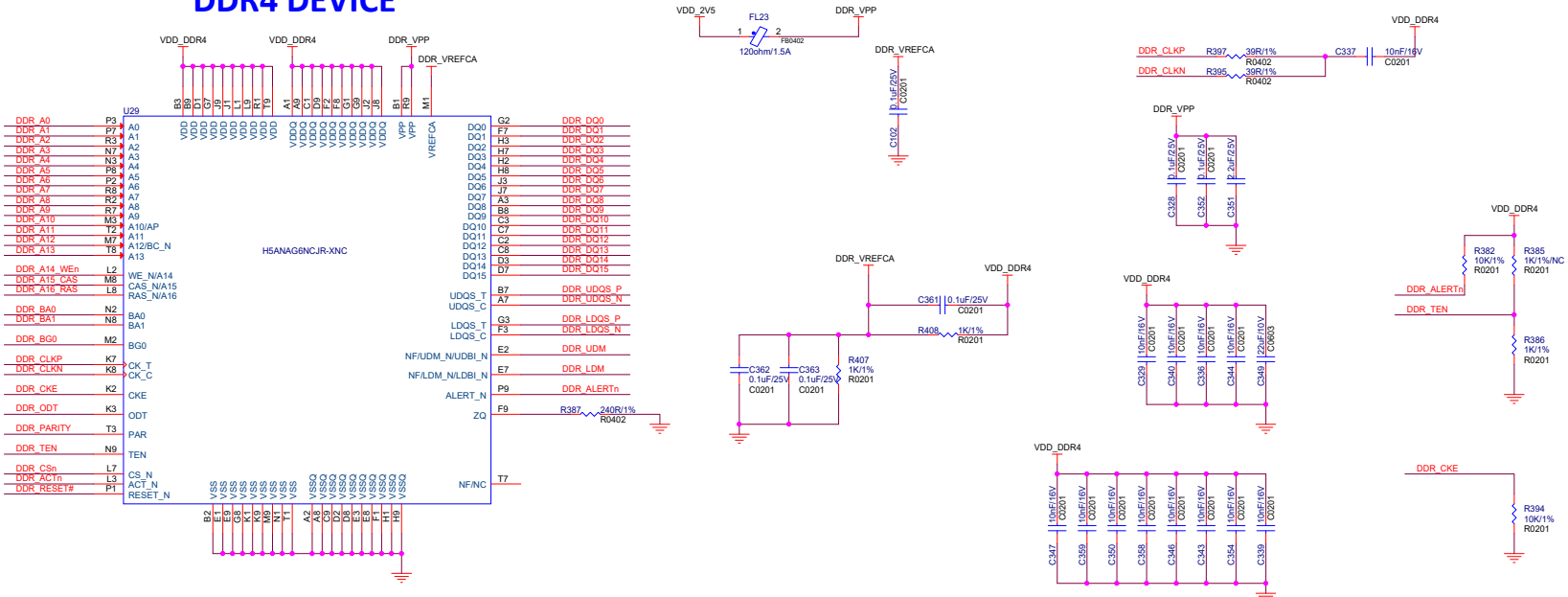
SOC DDR INTERFACE



DDR4 DEVICE



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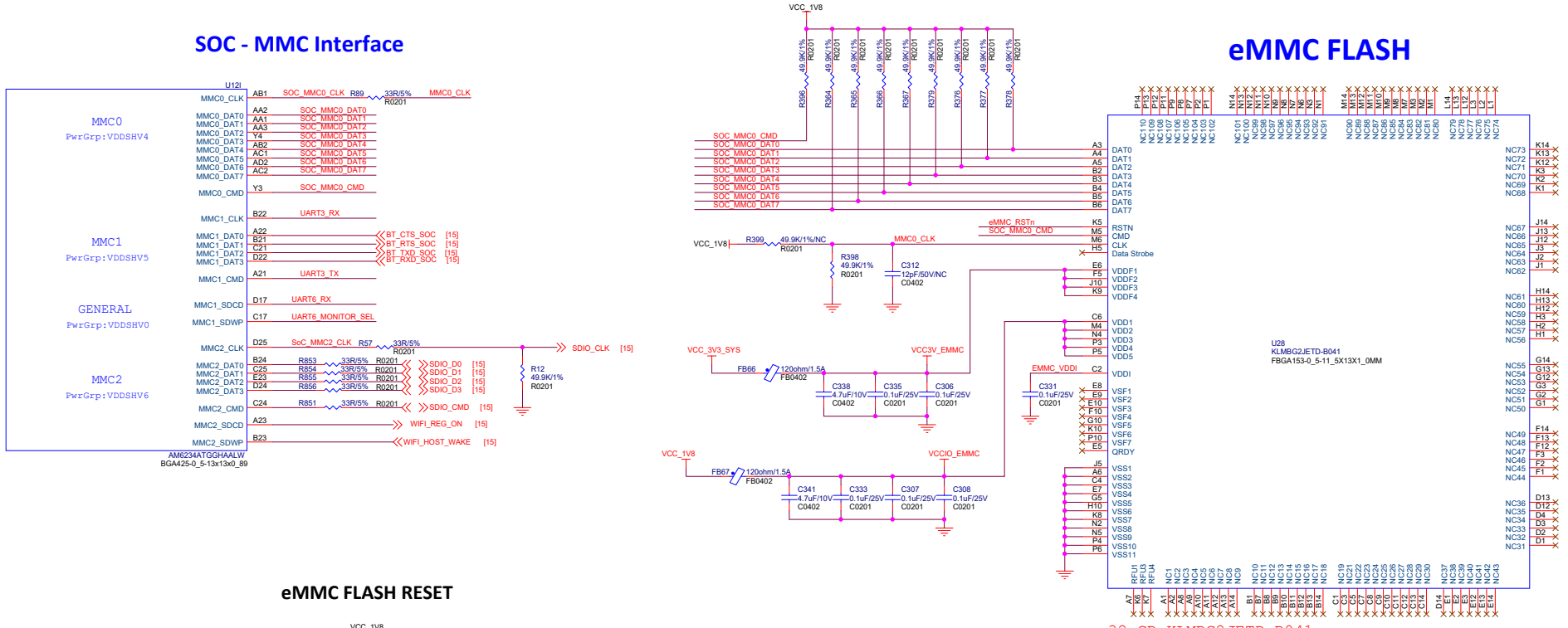
AUTEL	AUTEL TECH CO., LTD.		
Design Name	DC1912		
Page Name	SOC DDR4		
Designer	WANGTONG A22303	RevCode	V1
Reviewer	<Reviewer>	Page Size	C
Creat Time	Monday, August 01, 2022	Page Num	8 of 24



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Design Name	DC1912		
Page Name	SOC eMMC		
Designer	WANGTONG A22303	RevCode	V1
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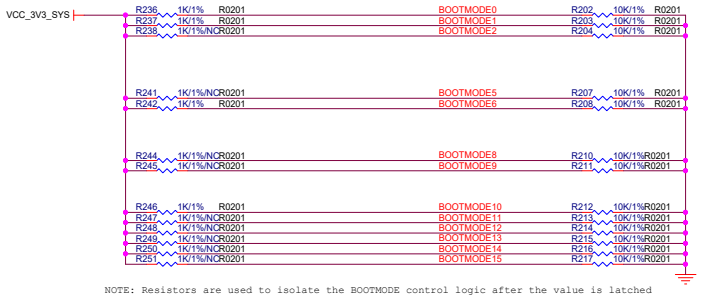
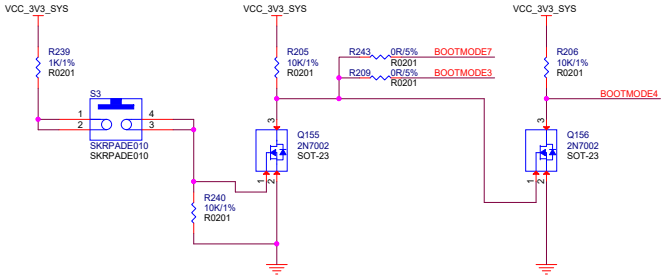
BOOTMODE PINS



NOTE: Resistors are used to isolate the BOOTMODE control logic after the value is latched



SOC GPMC

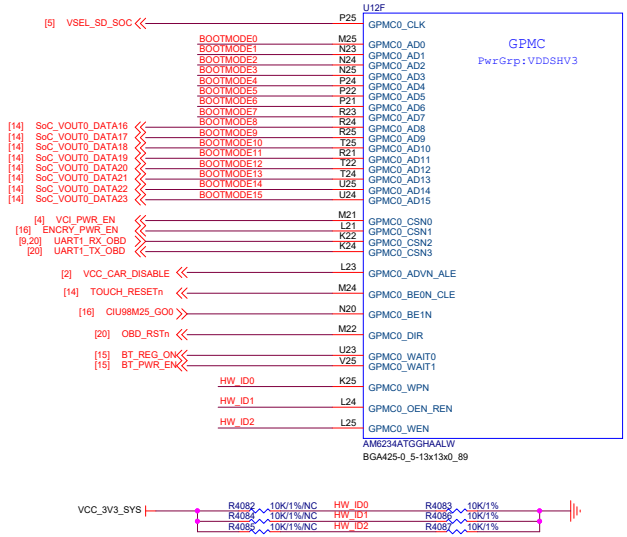


Table 4-2. BOOTMODE Pin Mapping

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Backup Boot Mode Config	Backup Boot Mode			Primary Boot Mode Config			Primary Boot Mode				PLL Config		

Table 4-3. PLL Reference Clock Selection

PLL Config Pins			Ref Clock (MHz)
B2	B1	B0	
0	0	0	19.2
0	0	1	20
0	1	0	24
0	1	1	25
1	0	0	26
1	0	1	27(1)
1	1	0	Reserved
1	1	1	Reserved

Table 4-4. Primary Boot Mode Selection

Primary Boot Mode Config							Primary Boot Mode
B9	B8	B7	B6	B5	B4	B3	
Reserved	Read Mode 2	Read Mode 1	0	0	0	0	Serial NAND
Reserved	Iclk	Csel	0	0	0	1	OSPI
Reserved	Iclk	Csel	0	0	1	0	QSPI
Reserved	Mode	Csel	0	0	1	1	SPI
Clkout	0	Link Info	0	1	0	0	Ethernet RGMII

Table 4-4. Primary Boot Mode Selection (continued)

Primary Boot Mode Config							Primary Boot Mode
B9	B8	B7	B6	B5	B4	B3	
Clkout	Clk src	0	0	1	0	1	Ethernet RMII
Bus reset	Reserved	Addr	0	1	1	0	I2C
Reserved	Reserved	Reserved	0	1	1	1	UART
1	Reserved	Fs/raw	1	0	0	0	MMCSD Boot (SD Card Boot or eMMC Boot using UDA)
Reserved	Reserved	Reserved	1	0	0	1	eMMC Boot
Core Volt	Mode	Lane Swap	1	0	1	0	USB
Reserved	Reserved	Reserved	1	0	1	1	GPMC NAND
Reserved	Reserved	Reserved	1	1	0	0	GPMC NOR
Reserved	Reserved	Reserved	1	1	0	1	Reserved
SFPD	Read Cmd	Mode	1	1	1	0	xSPI
Reserved	ARM/Thumb	No/Dev	1	1	1	1	No-boot/Dev boot

Table 4-5. Backup Mode Selection

Backup Boot Config	Backup Boot Mode Selection			Backup Boot Mode Selected
B13	B12	B11	B10	
Reserved	0	0	0	None
Mode	0	0	1	USB
Reserved	0	1	0	Reserved
Reserved	0	1	1	UART
IF	1	0	0	Ethernet
Port	1	0	1	MMCSD
Reserved	1	1	0	SPI
Reserved	1	1	1	I2C

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d DCDC/LDO 降额 ---- 按照输出功率 80% 降额

e 二极管 三极管 MOS管 降额 ---- 75% 降额

注意 三极管 MOS管 的开启电压 VCE/VGS 在手册规定范围内

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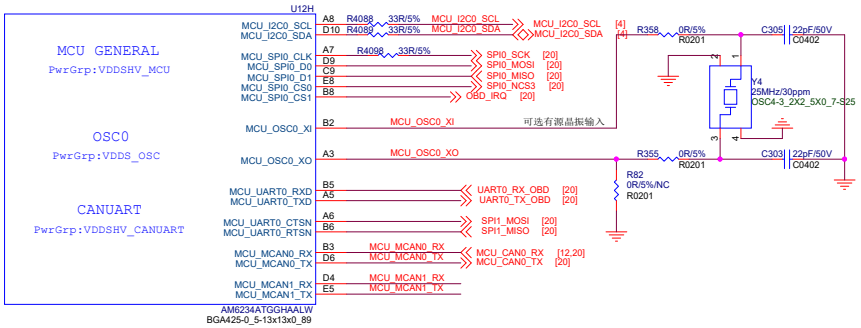
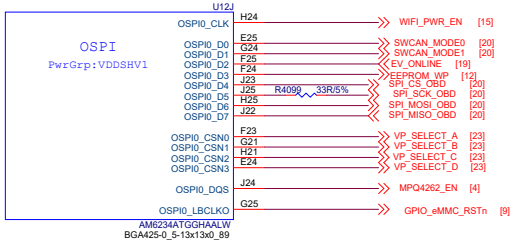
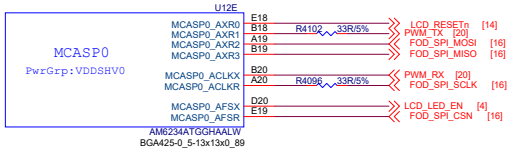
Design Name	DC1912		
Page Name	SOC		
Designer	WANGTONG A22303	RevCode	V1
Reviewer	<Reviewer>	Page Size	C
Creat Time	Monday, August 01, 2022	Page Num	10 of 24

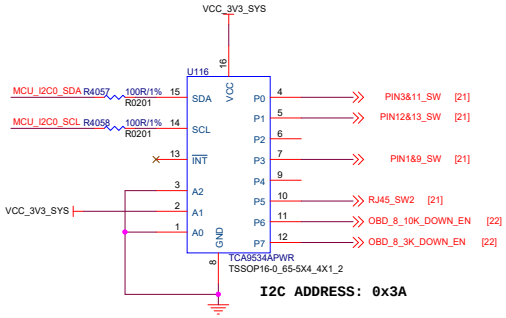
SOC - MCU DOMAIN

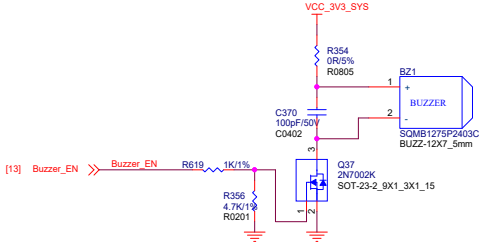


SOC OSPI INTERFACE

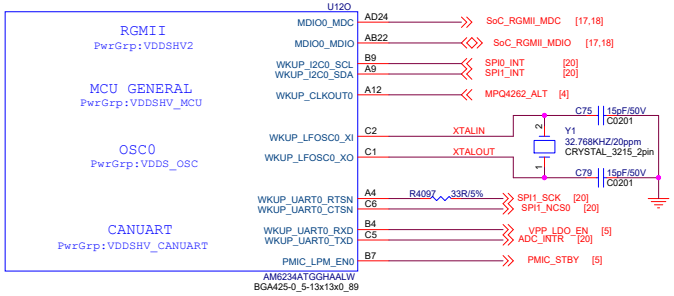


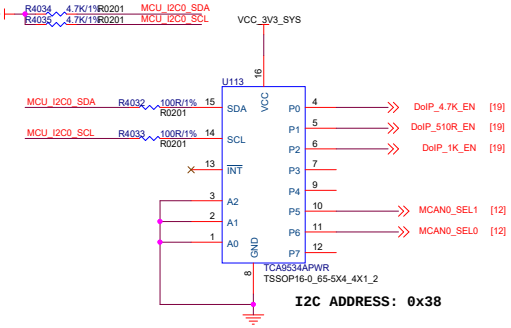


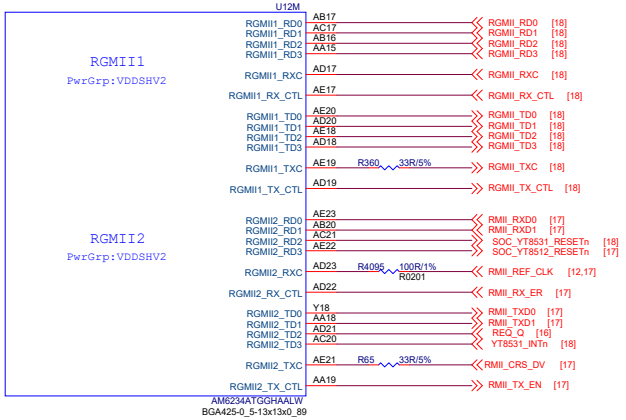




SOC WKUP DOMAIN







- MAIN domain: there are multiple CBASS components providing the connectivity among initiators and target interfaces for the processors and peripherals in the main domain. The main application processor such as A53SS is located.
- WKUP domain: this is where the device manger R5FSS is located. This is the domain active during deepsleep mode.
- MCU domain: this is where the MCU R5FSS is located. MCU domain can be isolated from the rest of SoC during safety use case.

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e 二极管 三极管 MOS管 降额 ---- 75% 降额

注意 三极管 MOS管 的开启电压 VCE/VGS 在手册规定范围内

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Designer	WANGTONG A22303	RevCode	V1
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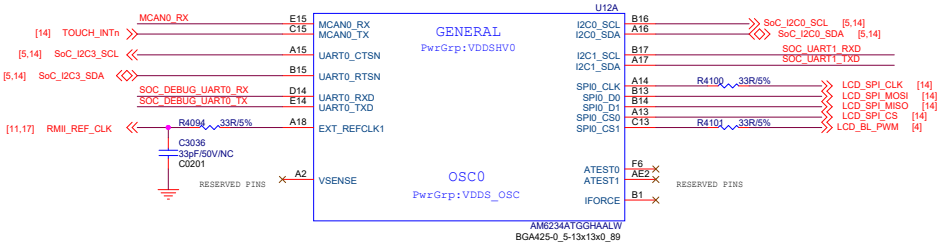
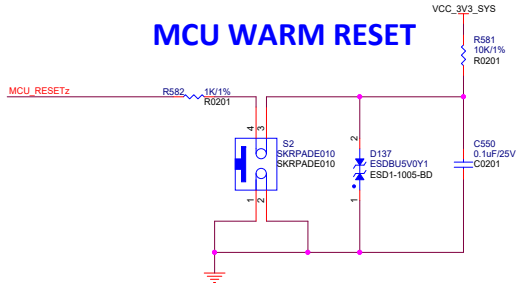
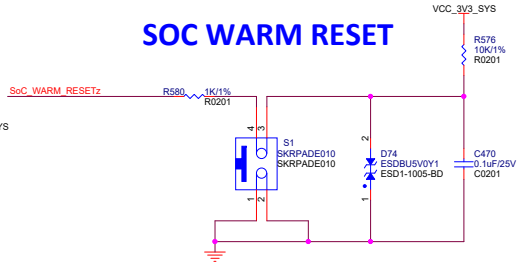
SOC - GENERAL

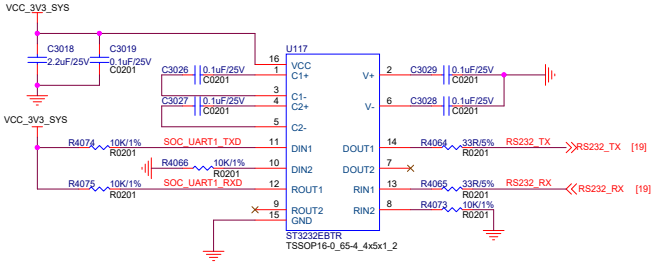


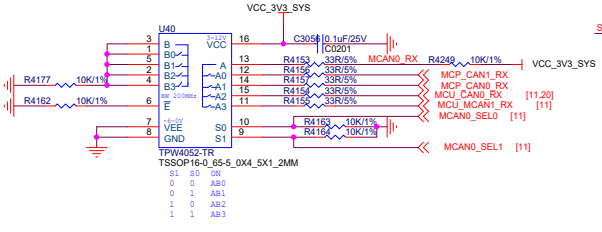
MCU WARM RESET

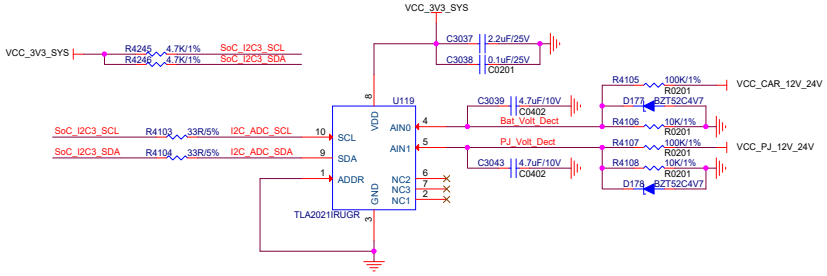


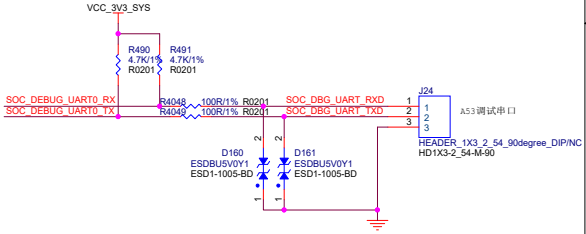
SOC WARM RESET

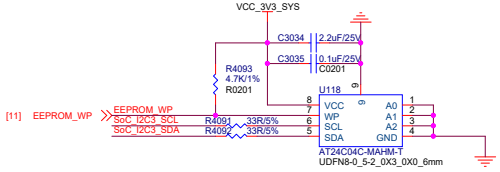






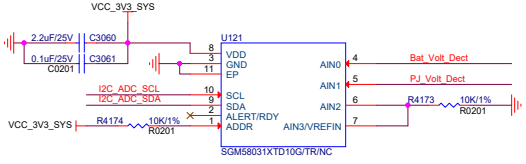






I2C ADDRESS: 0x50

I2C ADDRESS: 0x48



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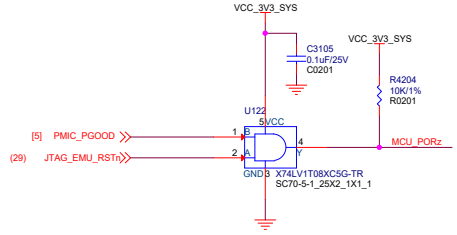
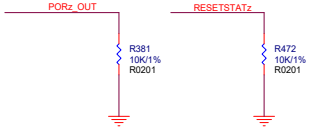
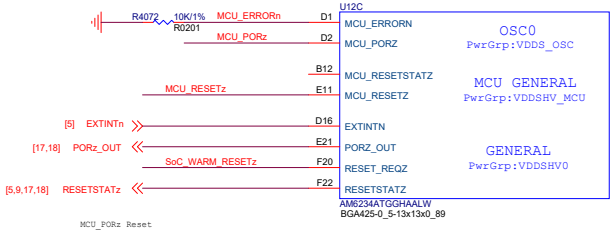




Pull-down resistor on PORz_OUT is provided to keep the signal low until the processor is released from reset during the power-up seqence

SOC - RESET



MCU_PORz Reset
This is the POR reset signal (active LOW) for the entire device, controlled by the MCU_PORz HW Pin.
When LOW, it performs a POR reset on the entire device (MCU and MAIN domains) and puts all IOs in a safe state (Reset/HHV state).
MCU Domain Effect
All modules in MCU domain are reset.
MCU IOs are in High-Heating-Value (HHV) state (Reset State).
When MCU_PORz is de-asserted, MCU IOs will enter the default state defined in the device Datasheet. MCU domain will be reconfigured by the R5FSS (secondary boot loader.
All modules in the MAIN domain are reset.
MAIN domain IOs are in HHV state (reset state).
When MCU_PORz is de-asserted, the MAIN domain IOs will enter default state as defined in the device Datasheet.
The R5FSS (secondary boot loader) will setup M4FSS as Safety or General-Purpose Processor.

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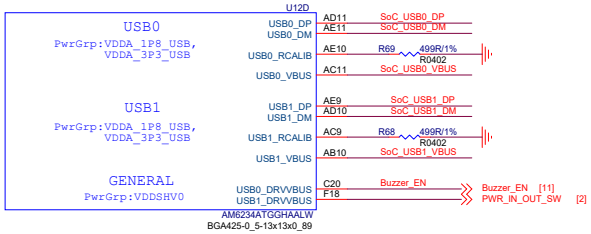
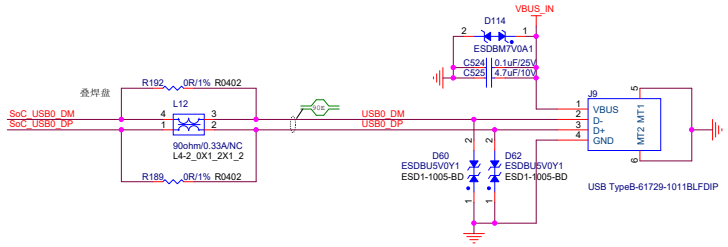
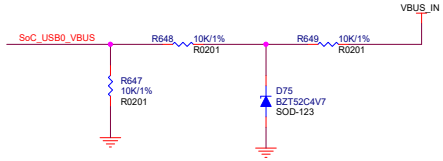
USB

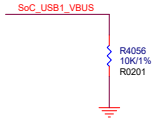




Note: Recommended VBUS circuit for SoC_USB0_VBUS



Note: Recommended VBUS circuit for SoC_USB1_VBUS



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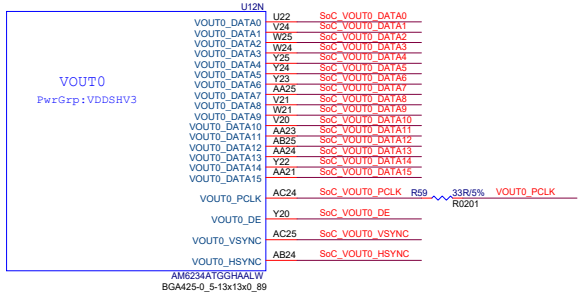
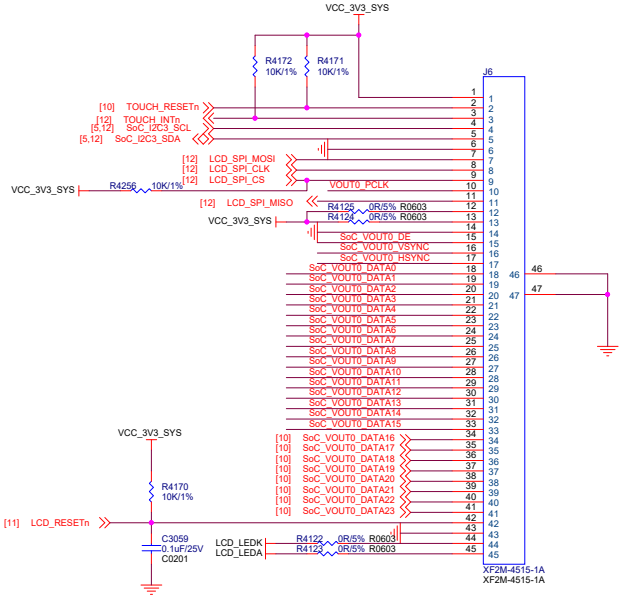
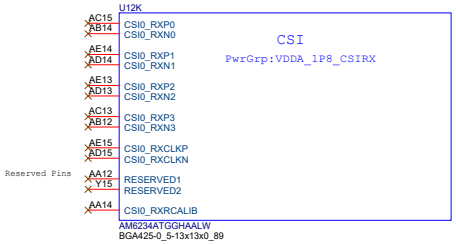
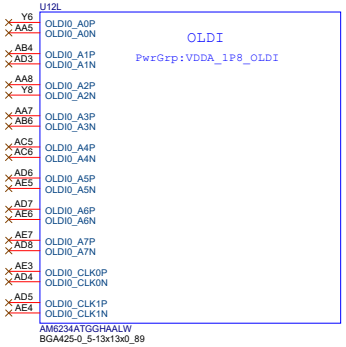
LCD









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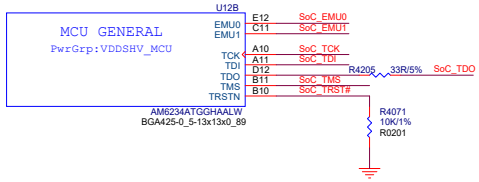
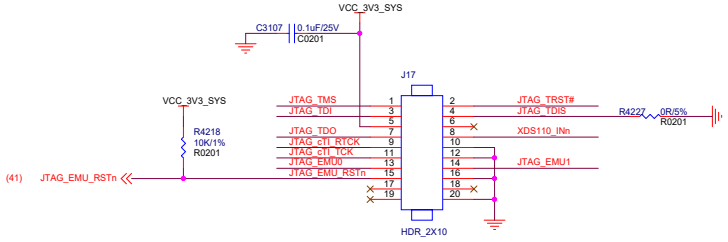
JTAG SOC SECTION

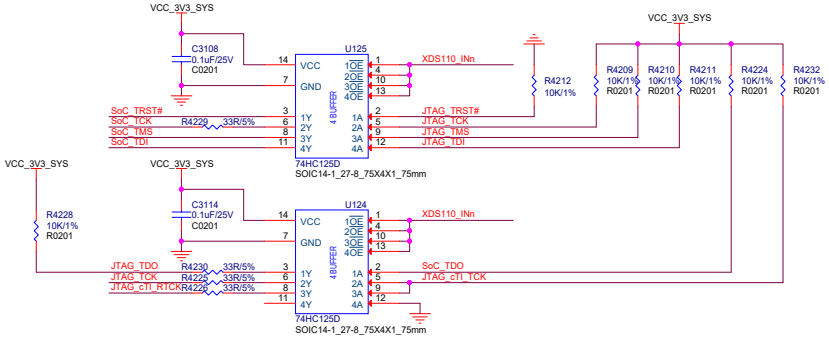


JTAG 20 PIN cTI CONNECTOR

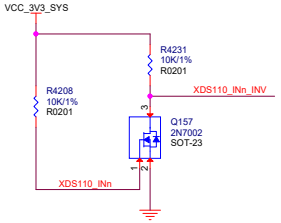


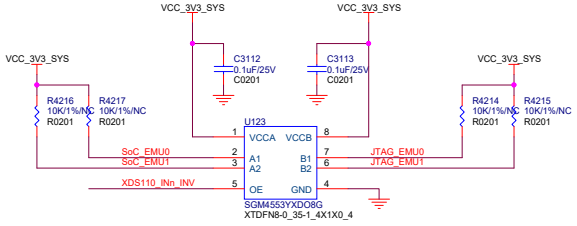
Silk: cTI

cTI20 JTAG BUFFERS



NOTE: Buffers U124 and U125 need to be placed closer to the cTI-20pin connector J17 to reduce Stub length of the JTAG signals.





检视重点	**1、降额审查**	**d DCDC/LDO 降额 ---- 按照输出功率 80% 降额**	**e 保险丝 ---- 75% 降额**
a 电容降额 ---- 禁用钽电容 ，陶瓷电容降额 70%		**e 二极管 三极管 MOS管 降额 ---- 75% 降额**	**f 光耦 ---- 工作电压 工作电流 电流传输比 70% 降额**
b 电阻降额 ---- 按照降额 50%		**注意 三极管 MOS管 的开启电压 VCE/VGS 在手册规定范围内**	**注 电源命名需标明实际电压或者做好电压注释**
c 功率电感降额 ---- 按照饱和电流 80% 降额			

2、新封装封装和使用场景审查

a 新建器件原理图 和PCB封装必须按照芯片手册仔细检查核对

b 新器件原理使用需要参考手册设计或者做好兼容

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