Agilent Technologies

DDR3 Test Report

Overall Result: FAIL

Test Configuration Details	
Device Description	
Burst Triggering Method	DQS-DQ Phase Difference
LPDDR3	No
DDR3L	No
Test Mode	Compliance
Speed Grade	DDR3-800
Test Session Details	
Infiniium SW Version	05.71.0000
Infiniium Model Number	DSO80604B
Infiniium Serial Number	No Serial
Application SW Version	2.20.9012
Debug Mode Used	No
Compliance Limits (official)	DDR3-800 Test Limit
Last Test Date	2003-01-04 02:24:36 UTC -07:00

Summary of Results

Test Statistics	
Failed	8
Passed	13
Total	21

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Last Actual	Last Margin	Pass Limits
✓	0	1	VIH.DQ(AC)	1.050480000000 V	16.7 %	VALUE >= VrefDQ_Volt+AcLevels_DQ_Volt V
✓	0	1	VIH.DQ(DC)	1.048505000000 V	30.5 %	VrefDQ_Volt+DcLevels_Volt V <= VALUE <= VDD_Volt V
✓	0	1	VIL.DQ(AC)	504.499000000 mV	15.9 %	VALUE <= VrefDQ_Volt-AcLevels_DQ_Volt V
✓	0	1	VIL.DQ(DC)	523.683600000 mV	19.4 %	0.000000000000 V <= VALUE <= VrefDQ_Volt-DcLevels_Volt V
✓	0	2	VOH(AC)	1.176060000000 V	30.7 %	VALUE >= VTT_Volt+0.1*VDDQ_Volt V
✗	2	2	VOH(DC)	1.176060000000 V	**-2.0 %**	VALUE >= 0.8*VDDQ_Volt V
✓	0	2	VOL(AC)	346.120000000 mV	42.3 %	VALUE <= VTT_Volt-0.1*VDDQ_Volt V
✗	2	2	VOL(DC)	346.120000000 mV	**-15.4 %**	VALUE <= 0.2*VDDQ_Volt V
✗	2	2	SRQseR	1.350642000000 V/ns	**-46.0 %**	2.500000000000 V/ns <= VALUE <= 5.000000000000 V/ns
✗	2	2	SRQseF	1.041345000000 V/ns	**-58.3 %**	2.500000000000 V/ns <= VALUE <= 5.000000000000 V/ns
✓	0	1	Overshoot amplitude (Clock, Data, Strobe, Mask)	-53.630000000 mV	113.4 %	VALUE <= 400.000000000 mV
✓	0	1	Overshoot area (Clock, Data, Strobe, Mask)	0.000000000000 V-ns	100.0 %	VALUE <= 250.000000000 mV-ns
✓	0	1	Undershoot amplitude (Clock, Data, Strobe, Mask)	-161.160000000 mV	140.3 %	VALUE <= 400.000000000 mV
✓	0	1	Undershoot area (Clock, Data, Strobe, Mask)	0.000000000000 V-ns	100.0 %	VALUE <= 250.000000000 mV-ns
✓	0	2	SRQdiffR	8.326396000000 V/ns	33.5 %	5.000000000000 V/ns <= VALUE <= 10.000000000000 V/ns
✓	0	2	SRQdiffF	8.505722000000 V/ns	29.9 %	5.000000000000 V/ns <= VALUE <= 10.000000000000 V/ns
✗	2	2	tWPRE	32.001030000 mtCK	**-96.4 %**	VALUE >= 900.000000000 mtCK
✗	1	2	tLZDQ	221.1 ps	14.9 %	-800.0 ps <= VALUE <= 400.0 ps
✗	2	2	tRPRE	529.530600000 mtCK	**-63.9 %**	900.000000000 mtCK <= VALUE <= 1.480000000000 tCK
✗	2	2	tLZDQS	1.0740 ns	**-56.2 %**	-800.0 ps <= VALUE <= 400.0 ps
✓	0	1	tCK(avg) Rising Edge Measurements	2.501 ns	**0.1 %**	2.500 ns <= VALUE <= 3.300 ns

Report Detail

Next

✓VIH.DQ(AC)

Reference: JEDEC Standard No. 79-3F, Table 24 (Vref=0.75)

Test Summary: Pass | Test Description: AC Input Logic High

Pass Limits: >= VrefDQ_Volt+AcLevels_DQ_Volt V | **VIH.DQ(AC)** 1.050480000000 V

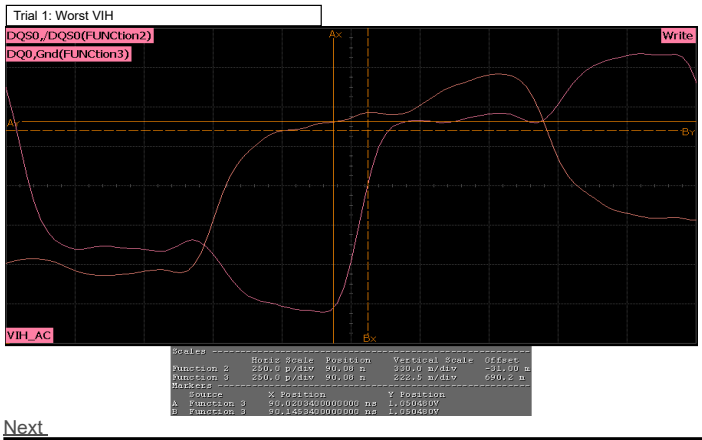
Result Details

Worst VIH (See image) | **Number of burst(s) measured** 1 | **NumOfMeas** 3.000 | **PUT** DQ0 | **PUT Src** Channel 3 | **Supporting Pin** DQS0,/DQS0 | **Supporting Pin Src** Channel 2 | **Chip Select Pin Source** N/A

PassLimit Min (VrefDQ_Volt+AcLevels_DQ_Volt) 900.000000000 mV

Trial 1

Trial 1: Worst VIH



Next

✓VIH.DQ(DC)

Reference: JEDEC Standard No. 79-3F, Table 24 (Vref=0.75; VDD=1.50)

Test Summary: Pass | Test Description: DC Input Logic High

Pass Limits: [VrefDQ_Volt+DcLevels_Volt V to VDD_Volt V] | **VIH.DQ(DC)** 1.048505000000 V

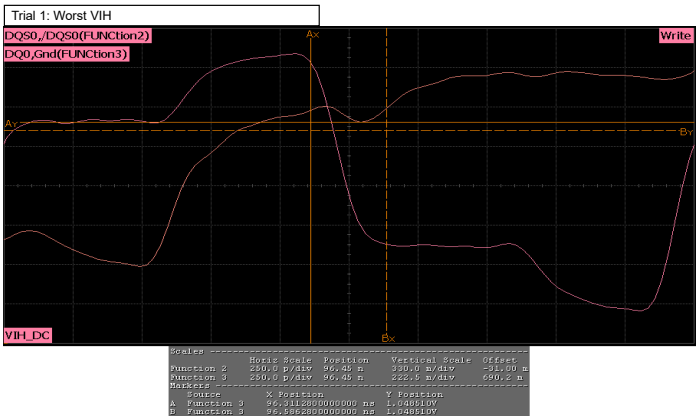
Result Details

Worst VIH (See image) | **Number of burst(s) measured** 1 | **NumOfMeas** 3.000 | **PUT** DQ0 | **PUT Src** Channel 3 | **Supporting Pin** DQS0,/DQS0 | **Supporting Pin Src** Channel 2 | **Chip Select Pin Source** N/A

PassLimit Min (VrefDQ_Volt+DcLevels_Volt) 850.000000000 mV | **PassLimit Max (VDD_Volt)** 1.500000000000 V

Trial 1

Trial 1: Worst VIH



Next

✓VIL.DQ(AC)

Reference: JEDEC Standard No. 79-3F, Table 24 (Vref=0.75)

Test Summary: Pass | Test Description: AC Input Logic Low

Pass Limits: <= VrefDQ_Volt-AcLevels_DQ_Volt V | **VIL.DQ(AC)** 504.499000000 mV

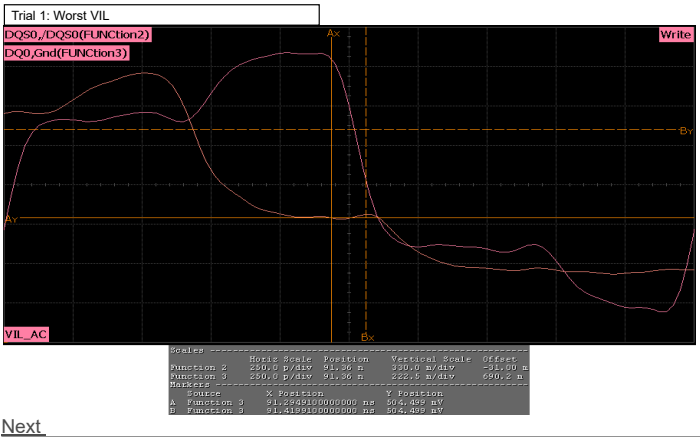
Result Details

Worst VIL (See image) | **Number of burst(s) measured** 1 | **NumOfMeas** 2.000 | **PUT** DQ0 | **PUT Src** Channel 3 | **Supporting Pin** DQS0,/DQS0 | **Supporting Pin Src** Channel 2 | **Chip Select Pin Source** N/A

PassLimit Max (VrefDQ_Volt-AcLevels_DQ_Volt) 600.000000000 mV

Trial 1

Trial 1: Worst VIL



Next

✓VIL.DQ(DC)

Reference: JEDEC Standard No. 79-3F, Table 24 (Vref=0.75; VSS=0.00)

Test Summary: Pass | Test Description: DC Input Logic Low

Pass Limits: [0.000000000000 V to VrefDQ_Volt-DcLevels_Volt V] | **VIL.DQ(DC)** 523.683600000 mV

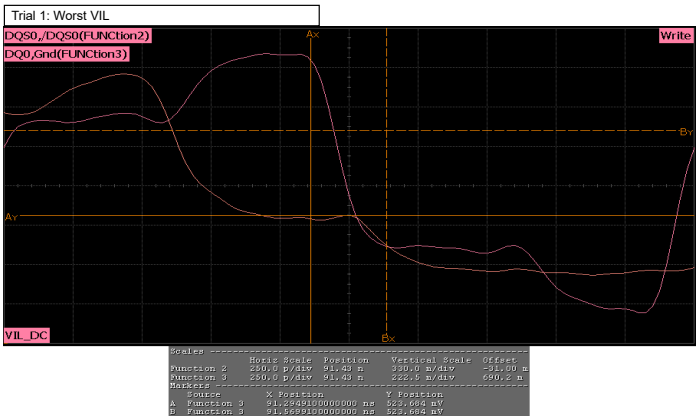
Result Details

Worst VIL (See image) | **Number of burst(s) measured** 1 | **NumOfMeas** 2.000 | **PUT** DQ0 | **PUT Src** Channel 3 | **Supporting Pin** DQS0,/DQS0 | **Supporting Pin Src** Channel 2 | **Chip Select Pin Source** N/A

PassLimit Max (VrefDQ_Volt-DcLevels_Volt) 650.000000000 mV

Trial 1

Trial 1: Worst VIL



Next

✓VOH(AC)

Reference: JEDEC Standard No. 79-3F, Table 30 (VTT=0.75; VDDQ=1.50)

Test Summary: Pass | Test Description: AC Output Logic High

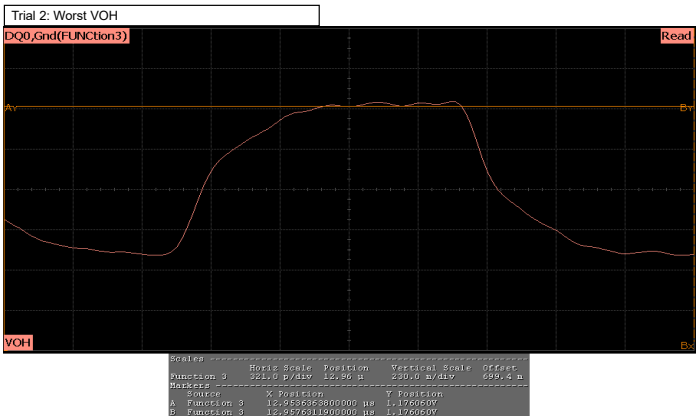
Pass Limits: >= VTT_Volt+0.1*VDDQ_Volt V | **VOH(AC) (Last of 2 Trials)** 1.176060000000 V | **# Trials Run:** 2 | **Last Trial:** Trial 2

Overall Summary + details of 1 last trials

Pass	Trial	Actual Value	Margin	NumOfMeas	PassLimit Min (VTT_Volt+0.1*VDDQ_Volt) (V)	Worst VOH	PUT	PUT Src	Supporting Pin	Supporting Pin Src	Chip Select Pin Source
	Avg	*1.178 V*	*30.91 %*	*4.500*	*900.0 mV*						
	StdDev	*3.005 mV*	*333.9 m%*	*2.121*	*0.000 V*						
	Range	*4.250 mV*	*472.2 m%*	*3.000*	*0.000 V*						
	Min	*1.176 V*	*30.67 %*	*3.000*	*900.0 mV*						
	Max	*1.180 V*	*31.15 %*	*6.000*	*900.0 mV*						
	Sum	*2.356 V*	*61.82 %*	*9.000*	*1.800 V*						
✓	Trial 2 (Last)	1.176060000000 V	30.7%	6.000	900.000000000 mV	(See image)	DQ0	Channel 3	DQS0,/DQS0	Channel 2	N/A

Trial 2

Trial 2: Worst VOH



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Function 3	321.0 p/div	12.96 µ	230.0 m/div	699.4 m

Markers

	Source	X Position	Y Position
A	Function 3	12.953636380000 µs	1.176060V
B	Function 3	12.957631190000 µs	1.176060V

Next

✗ VOH(DC)

Reference: JEDEC Standard No. 79-3F, Table 30 (VDDQ=1.50)

Test Summary: FAIL | Test Description: DC Output Logic High

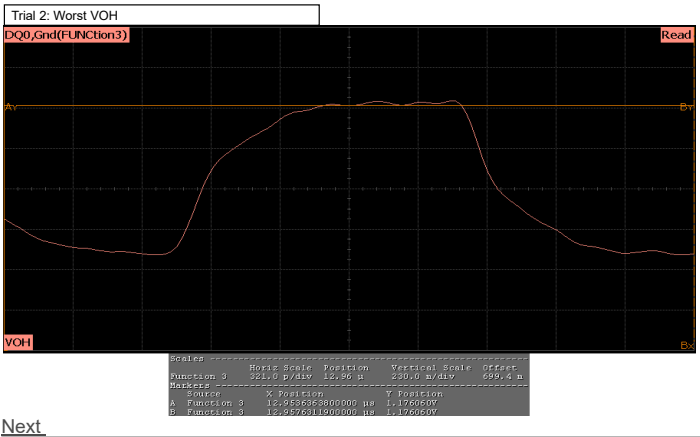
Pass Limits: >= 0.8*VDDQ_Volt V | **VOH(DC) (Last of 2 Trials)** 1.176060000000 V | **# Trials Run:** 2 | **Last Trial:** Trial 2

Overall Summary + details of 1 last trials

Pass	Trial	Actual Value	Margin	NumOfMeas	PassLimit Min (0.8*VDDQ_Volt) (V)	Worst VOH	PUT	PUT Src	Supporting Pin	Supporting Pin Src	Chip Select Pin Source
	Avg	*1.178 V*	*-1.818 %*	*4.500*	*1.200 V*						
	StdDev	*3.005 mV*	*250.4 m%*	*2.121*	*0.000 V*						
	Range	*4.250 mV*	*354.2 m%*	*3.000*	*0.000 V*						
	Min	*1.176 V*	*-1.995 %*	*3.000*	*1.200 V*						
	Max	*1.180 V*	*-1.641 %*	*6.000*	*1.200 V*						
	Sum	*2.356 V*	*-3.636 %*	*9.000*	*2.400 V*						
✗	Trial 2 (Last)	1.176060000000 V	**-2.0%**	6.000	1.200000000000 V	(See image)	DQ0	Channel 3	DQS0,/DQS0	Channel 2	N/A

Trial 2

Trial 2: Worst VOH



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Function 3	321.0 p/div	12.96 µ	230.0 m/div	699.4 m

Markers

	Source	X Position	Y Position
A	Function 3	12.953636380000 µs	1.176060V
B	Function 3	12.957631190000 µs	1.176060V

Next

✓ VOL(AC)

Reference: JEDEC Standard No. 79-3F, Table 30 (VTT=0.75; VDDQ=1.50)

Test Summary: Pass | Test Description: AC Output Logic Low

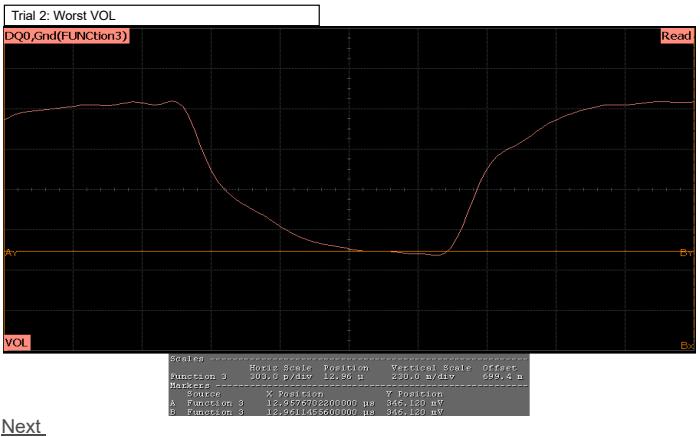
Pass Limits: <= VTT_Volt-0.1*VDDQ_Volt V | **VOL(AC) (Last of 2 Trials)** 346.120000000 mV | **# Trials Run:** 2 | **Last Trial:** Trial 2

Overall Summary + details of 1 last trials

Pass	Trial	Actual Value	Margin	NumOfMeas	PassLimit Max (VTT_Volt-0.1*VDDQ_Volt) (V)	Worst VOL	PUT	PUT Src	Supporting Pin	Supporting Pin Src	Chip Select Pin Source
	Avg	*359.6 mV*	*40.07 %*	*5.000*	*600.0 mV*						
	StdDev	*19.01 mV*	*3.169 %*	*2.828*	*0.000 V*						
	Range	*26.89 mV*	*4.482 %*	*4.000*	*0.000 V*						
	Min	*346.1 mV*	*37.83 %*	*3.000*	*600.0 mV*						
	Max	*373.0 mV*	*42.31 %*	*7.000*	*600.0 mV*						
	Sum	*719.1 mV*	*80.15 %*	*10.00*	*1.200 V*						
✓	Trial 2 (Last)	346.120000000 mV	42.3%	7.000	600.000000000 mV	(See image)	DQ0	Channel 3	DQS0,/DQS0	Channel 2	N/A

Trial 2

Trial 2: Worst VOL



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Function 3	309.0 p/div	12.96 µ	230.0 m/div	699.4 m

Markers

	Source	X Position	Y Position
A	Function 3	12.957670200000 µs	346.120 mV
B	Function 3	12.961145560000 µs	346.120 mV

Next

✗ VOL(DC)

Reference: JEDEC Standard No. 79-3F, Table 30 (VDDQ=1.50)

Test Summary: FAIL | Test Description: DC Output Logic Low

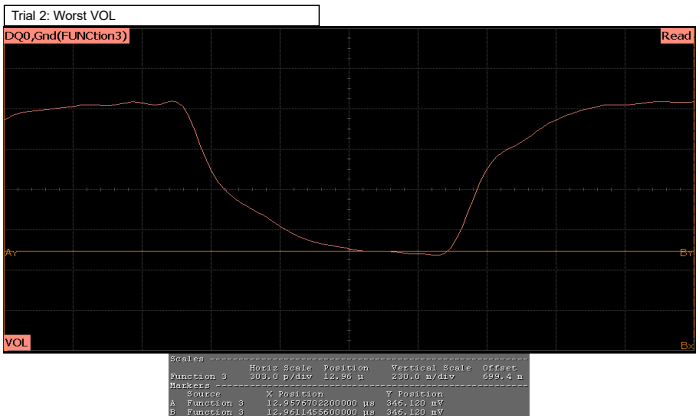
Pass Limits: <= 0.2*VDDQ_Volt V | **VOL(DC) (Last of 2 Trials)** 346.120000000 mV | **# Trials Run:** 2 | **Last Trial:** Trial 2

Overall Summary + details of 1 last trials

Pass	Trial	Actual Value	Margin	NumOfMeas	PassLimit Max (0.2*VDDQ_Volt) (V)	Worst VOL	PUT	PUT Src	Supporting Pin	Supporting Pin Src	Chip Select Pin Source
	Avg	*359.6 mV*	*-19.86 %*	*5.000*	*300.0 mV*						
	StdDev	*19.01 mV*	*6.338 %*	*2.828*	*0.000 V*						
	Range	*26.89 mV*	*8.963 %*	*4.000*	*0.000 V*						
	Min	*346.1 mV*	*-24.34 %*	*3.000*	*300.0 mV*						
	Max	*373.0 mV*	*-15.37 %*	*7.000*	*300.0 mV*						
	Sum	*719.1 mV*	*-39.71 %*	*10.00*	*600.0 mV*						
✗	Trial 2 (Last)	346.120000000 mV	**-15.4%**	7.000	300.000000000 mV	(See image)	DQ0	Channel 3	DQS0,/DQS0	Channel 2	N/A

Trial 2

Trial 2: Worst VOL



Next

✗ SRQseR

Reference: JEDEC Standard No. 79-3F, Table 33

Test Summary: **FAIL** | Test Description: Output signal minimum rising slew rate

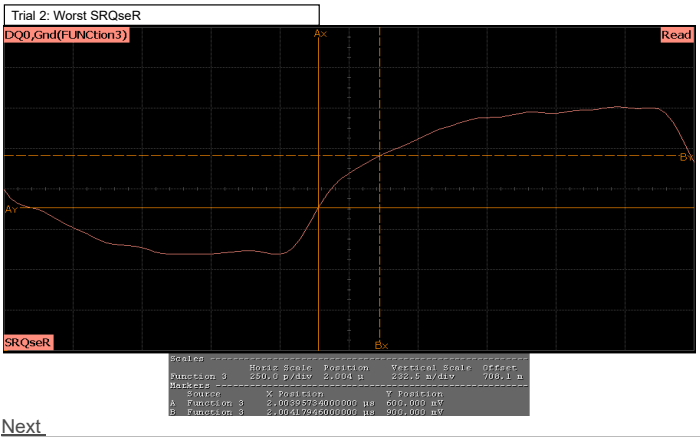
Pass Limits: [2.500000000000 V/ns to 5.000000000000 V/ns] | **SRQseR (Last of 2 Trials)** 1.350642000000 V/ns | **# Trials Run:** 2 | **Last Trial:** Trial 2

Overall Summary + details of 1 last trials

Pass	Trial	Actual Value	Margin	Number of burst(s) measured	NumOfMeas	SRQSeR_time (s)	Worst SRQseR	Vref	Voh_ac	Vol_ac	PUT	PUT Src	Supporting Pin	Supporting Pin Src	Chip Select Pin Source
	Avg	*1.397 V/ns*	*-44.11 %*	*1.000*	*2.500*	*215.0 ps*									
	StdDev	*65.77 mV/ns*	*2.631 %*	*0.000*	*707.1 m*	*10.12 ps*									
	Range	*93.02 mV/ns*	*3.721 %*	*0.000*	*1.000*	*14.31 ps*									
	Min	*1.351 V/ns*	*-45.97 %*	*1.000*	*2.000*	*207.8 ps*									
	Max	*1.444 V/ns*	*-42.25 %*	*1.000*	*3.000*	*222.1 ps*									
	Sum	*2.794 V/ns*	*-88.23 %*	*2.000*	*5.000*	*429.9 ps*									
✗	Trial 2 (Last)	1.350642000000 V/ns	**-46.0%**	1	3.000	222 ps	(See image)	750 mV	900 mV	600 mV	DQ0	Channel 3	DQS0,/DQS0	Channel 2	N/A

Trial 2

Trial 2: Worst SRQseR



Next

✗ SRQseF

Reference: JEDEC Standard No. 79-3F, Table 33

Test Summary: **FAIL** | Test Description: Output signal minimum falling slew rate

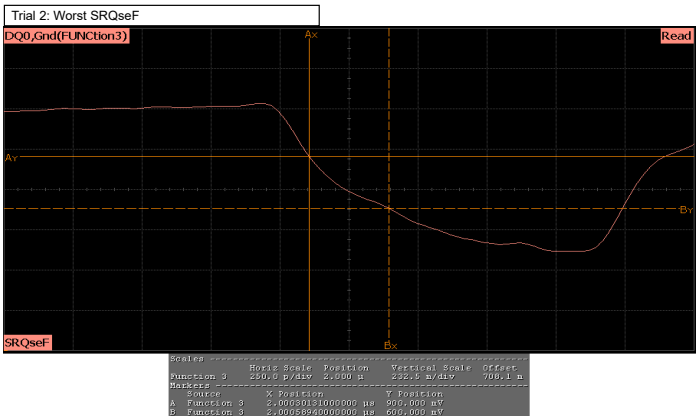
Pass Limits: [2.500000000000 V/ns to 5.000000000000 V/ns] | **SRQseF (Last of 2 Trials)** 1.041345000000 V/ns | **# Trials Run:** 2 | **Last Trial:** Trial 2

Overall Summary + details of 1 last trials

Pass	Trial	Actual Value	Margin	Number of burst(s) measured	NumOfMeas	SRQSeF_time (s)	Worst SRQseF	Vref	Voh_ac	Vol_ac	PUT	PUT Src	Supporting Pin	Supporting Pin Src	Chip Select Pin Source
	Avg	*1.038 V/ns*	*-58.50 %*	*1.000*	*3.000*	*289.1 ps*									
	StdDev	*5.281 mV/ns*	*211.2 m%*	*0.000*	*0.000*	*1.471 ps*									
	Range	*7.468 mV/ns*	*298.7 m%*	*0.000*	*0.000*	*2.081 ps*									
	Min	*1.034 V/ns*	*-58.64 %*	*1.000*	*3.000*	*288.1 ps*									
	Max	*1.041 V/ns*	*-58.35 %*	*1.000*	*3.000*	*290.2 ps*									
	Sum	*2.075 V/ns*	*-117.0 %*	*2.000*	*6.000*	*578.3 ps*									
✗	Trial 2 (Last)	1.041345000000 V/ns	**-58.3%**	1	3.000	288 ps	(See image)	750 mV	900 mV	600 mV	DQ0	Channel 3	DQS0,/DQS0	Channel 2	N/A

Trial 2

Trial 2: Worst SRQseF



Next

✓Overshoot amplitude (Clock, Data, Strobe, Mask)

Reference: JEDEC Standard No. 79-3F, Table 37

Test Summary: Pass | Test Description: Peak amplitude of AC overshoot

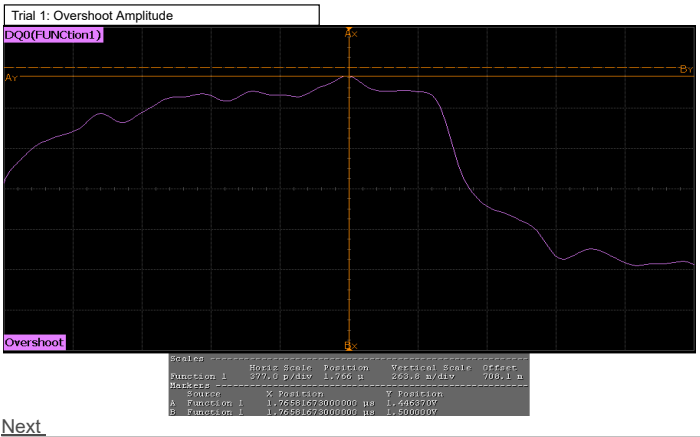
Pass Limits: <= 400.000000000 mV | **Overshoot amplitude (Clock, Data, Strobe, Mask)** -53.630000000 mV

Result Details

Overshoot Width 0.0000000000000 s | **Overshoot Reference** 1.500 V | **PUT** DQ0 | **PUT Src** Channel 3 | **Overshoot Amplitude** (See image)

Trial 1

Trial 1: Overshoot Amplitude



Next

✓Overshoot area (Clock, Data, Strobe, Mask)

Reference: JEDEC Standard No. 79-3F, Table 37

Test Summary: Pass | Test Description: OverShoot area above VDDQ

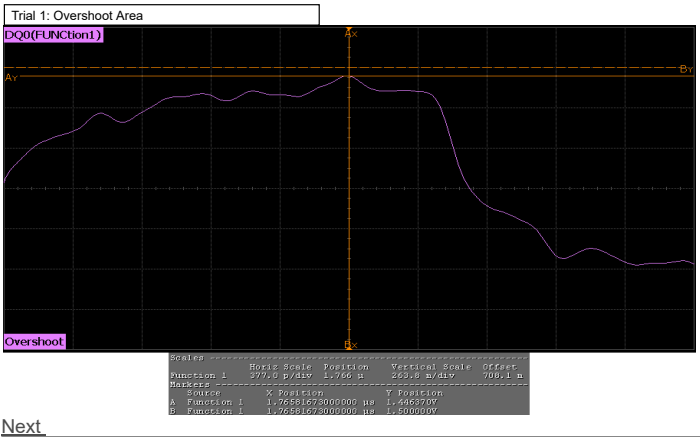
Pass Limits: <= 250.000000000 mV-ns | **Overshoot Area (Address, Control)** 0.0000000000000 V-ns

Result Details

Overshoot amplitude -54 mV | **Overshoot Width** 0.0000000000000 s | **Overshoot Reference** 1.500 V | **PUT** DQ0 | **PUT Src** Channel 3 | **Overshoot Area** (See image)

Trial 1

Trial 1: Overshoot Area



Next

✓Undershoot amplitude (Clock, Data, Strobe, Mask)

Reference: JEDEC Standard No. 79-3F, Table 37

Test Summary: Pass | Test Description: Peak amplitude of AC undershoot

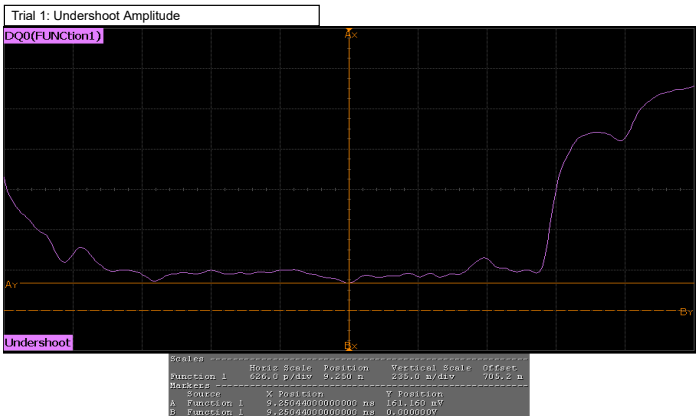
Pass Limits: <= 400.000000000 mV | **Undershoot amplitude (Clock, Data, Strobe, Mask)** -161.160000000 mV

Result Details

Undershoot Width 0.0000000000000 s | **Undershoot Reference** 0.000 V | **PUT** DQ0 | **PUT Src** Channel 3 | **Undershoot Amplitude** (See image)

Trial 1

Trial 1: Undershoot Amplitude



Next

✓Undershoot area (Clock, Data, Strobe, Mask)

Reference: JEDEC Standard No. 79-3F, Table 37

Test Summary: Pass | Test Description: UnderShoot area below VSSQ

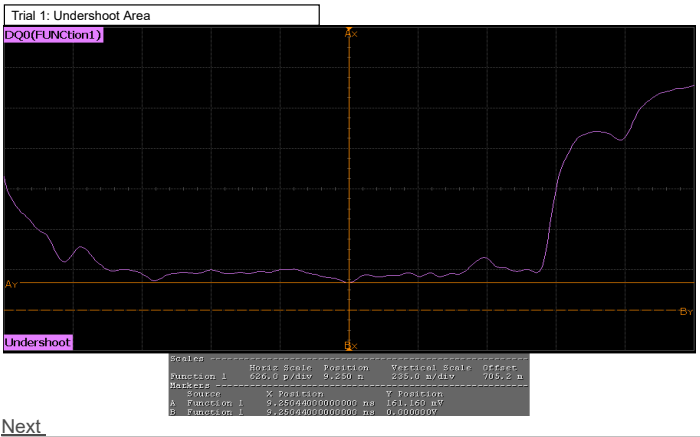
Pass Limits: <= 250.000000000 mV-ns | **Undershoot Area (Clock, Data, Strobe, Mask)** 0.000000000000 V-ns

Result Details

Undershoot Amplitude	-161 mV	Undershoot Width	0.0000000000000 s	Undershoot Reference	0.000 V	PUT	DQ0	PUT Src	Channel 3	Undershoot Area	(See image)

Trial 1

Trial 1: Undershoot Area



Next

✓SRQdiffR

Reference: JEDEC Standard No. 79-3F, Table 35

Test Summary: Pass | Test Description: Differential Output Rising Slew Rate

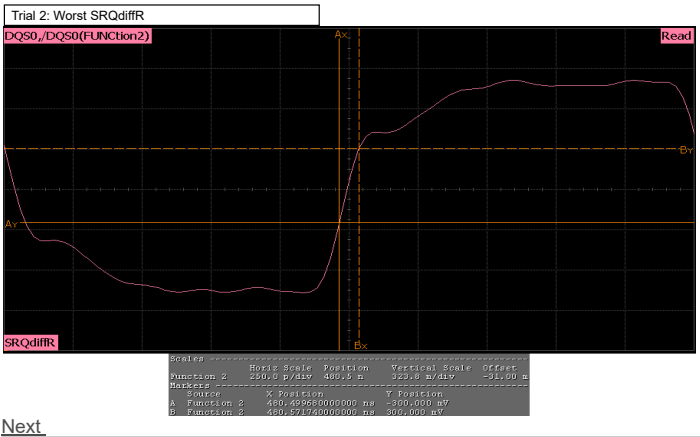
Pass Limits: [5.000000000000 V/ns to 10.000000000000 V/ns] | **SRQdiffR (Last of 2 Trials)** 8.326396000000 V/ns | **# Trials Run:** 2 | **Last Trial:** Trial 2

Overall Summary + details of 1 last trials

Pass	Trial	Actual Value	Margin	Number of burst(s) measured	NumOfMeas	SRQdiffR_time (s)	Min (V/ns)	Max (V/ns)	Worst SRQdiffR	VOHdiff_ac	VOLdiff_ac	PUT	PUT Src	Supporting Pin	Supporting Pin Src	Chip Select Pin Source
	Avg	*8.412 V/ns*	*31.76 %*	*1.000*	*8.000*	*71.33 ps*	*7.459 V/ns*	*8.412 V/ns*								
	StdDev	*121.4 mV/ns*	*2.428 %*	*0.000*	*0.000*	*1.029 ps*	*304.5 mV/ns*	*121.4 mV/ns*								
	Range	*171.7 mV/ns*	*3.433 %*	*0.000*	*0.000*	*1.456 ps*	*430.6 mV/ns*	*171.7 mV/ns*								
	Min	*8.326 V/ns*	*30.04 %*	*1.000*	*8.000*	*70.60 ps*	*7.243 V/ns*	*8.326 V/ns*								
	Max	*8.498 V/ns*	*33.47 %*	*1.000*	*8.000*	*72.06 ps*	*7.674 V/ns*	*8.498 V/ns*								
	Sum	*16.82 V/ns*	*63.51 %*	*2.000*	*16.00*	*142.7 ps*	*14.92 V/ns*	*16.82 V/ns*								
✓	Trial 2 (Last)	8.326396000000 V/ns	33.5%	1	8.000	72 ps	7.673813000000 V/ns	8.326396000000 V/ns	(See image)	300 mV	-300 mV	DQS0,/DQS0	Channel 2	DQ0	Channel 3	N/A

Trial 2

Trial 2: Worst SRQdiffR



Next

✓SRQdiffF

Reference: JEDEC Standard No. 79-3F, Table 35

Test Summary: Pass | Test Description: Differential Output Falling Slew Rate

Pass Limits: [5.000000000000 V/ns to 10.000000000000 V/ns] | **SRQdiffF (Last of 2 Trials)** 8.505722000000 V/ns | **# Trials Run:** 2 | **Last Trial:** Trial 2

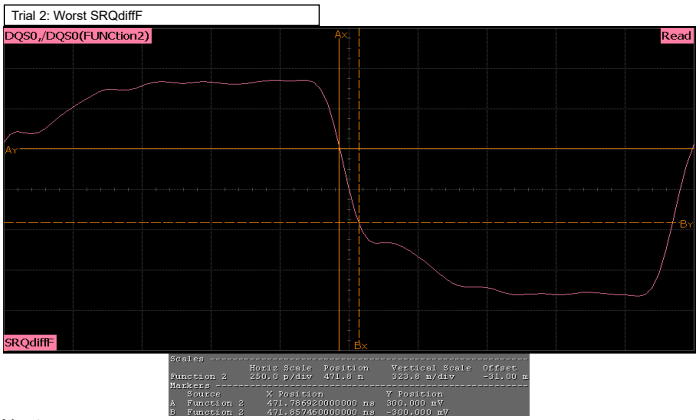
Overall Summary + details of 1 last trials

Pass	Trial	Actual Value	Margin	Number of burst(s) measured	NumOfMeas	SRQdiffF_time (s)	Min (V/ns)	Max (V/ns)	Worst SRQdiffF	VOHdiff_ac	VOLdiff_ac	PUT	PUT Src	Supporting Pin	Supporting Pin Src	Chip Select Pin Source

	Avg	*8.259 V/ns*	*34.82 %*	*1.000*		*8.000*	*72.71 ps*	*7.639 V/ns*	*8.259 V/ns*										
	StdDev	*349.1 mV/ns*	*6.982 %*	*0.000*		*0.000*	*3.074 ps*	*265.2 mV/ns*	*349.1 mV/ns*										
	Range	*493.7 mV/ns*	*9.874 %*	*0.000*		*0.000*	*4.347 ps*	*375.0 mV/ns*	*493.7 mV/ns*										
	Min	*8.012 V/ns*	*29.89 %*	*1.000*		*8.000*	*70.54 ps*	*7.451 V/ns*	*8.012 V/ns*										
	Max	*8.506 V/ns*	*39.76 %*	*1.000*		*8.000*	*74.89 ps*	*7.826 V/ns*	*8.506 V/ns*										
	Sum	*16.52 V/ns*	*69.65 %*	*2.000*		*16.00*	*145.4 ps*	*15.28 V/ns*	*16.52 V/ns*										
✓	Trial 2 (Last)	8.505722000000 V/ns	29.9%	1		8.000	71 ps	7.826406000000 V/ns	8.505722000000 V/ns	(See image)	300 mV	-300 mV	DQS0,/DQS0	Channel 2	DQ0		Channel 3	N/A	

Trial 2

Trial 2: Worst SRQdiffF



Next

✗tWPRE

Reference: JEDEC Standard No. 79-3F, Table 68

Test Summary: **FAIL** | Test Description: Write preamble

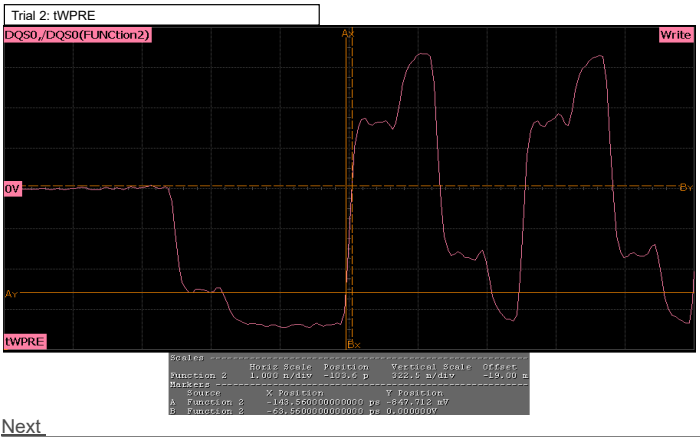
Pass Limits: >= 900.000000000 mtCK | **tWPRE (Last of 2 Trials)** 32.001030000 mtCK | **# Trials Run:** 2 | **Last Trial:** Trial 2

Overall Summary + details of 1 last trials

Pass	Trial	Actual Value	Margin	tWPRE(s) (s)	NumOfMeas	tWPRE	Number of burst(s) measured	CH1_PUT	CH1_Src	CH2_PUT	CH2_Src	CH3_PUT	CH3_Src	CH4_PUT	CH4_Src	Sampling Points (Pts)	Min	Max	Mean	Stdev
	Avg	*32.14 mtCK*	*-96.43 %*	*80.34 ps*	*1.000*															
	StdDev	*193.1 ÂµtCK*	*21.45 m%*	*482.7 fs*	*0.000*															
	Range	*273.0 ÂµtCK*	*30.34 m%*	*682.6 fs*	*0.000*															
	Min	*32.00 mtCK*	*-96.44 %*	*80.00 ps*	*1.000*															
	Max	*32.27 mtCK*	*-96.41 %*	*80.69 ps*	*1.000*															
	Sum	*64.28 mtCK*	*-192.9 %*	*160.7 ps*	*2.000*															
✗	Trial 2 (Last)	32.001030000 mtCK	**-96.4%**	80 ps	1.000	(See image)	1.000000e+000	Clock	CK0,/CK0	Strobe	DQS0,/DQS0	Data	DQ0,Gnd	Please select a signal	Not In Use	2000000	32.001030000 mtCK	32.001030000 mtCK	32.001030000 mtCK	0.0000 tCK

Trial 2

Trial 2: tWPRE



Next

✗tLZDQ

Reference: JEDEC Standard No. 79-3F, Table 68

Test Summary: **FAIL** | Test Description: DQ low-impedance time from CK,/CK

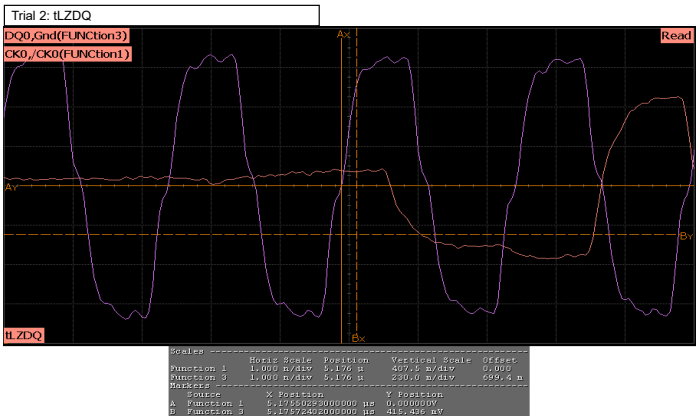
Pass Limits: [-800.0 ps to 400.0 ps] | **tLZDQ (Last of 2 Trials)** 221.1 ps | **# Trials Run:** 2 | **Last Trial:** Trial 2

Overall Summary + details of 1 last trials

Pass	Trial	Actual Value	Margin	NumOfMeas	tLZDQ	Number of burst(s) measured	CH1_PUT	CH1_Src	CH2_PUT	CH2_Src	CH3_PUT	CH3_Src	CH4_PUT	CH4_Src	tDQSCK Delay (cycle)	Sampling Points (Pts)	Min	Max	Mean	Stdev
	Avg	*686.4 ps*	*-23.87 %*	*1.000*																
	StdDev	*658.1 ps*	*54.84 %*	*0.000*																
	Range	*930.7 ps*	*77.56 %*	*0.000*																
	Min	*221.1 ps*	*-62.65 %*	*1.000*																
	Max	*1.152 ns*	*14.91 %*	*1.000*																
	Sum	*1.373 ns*	*-47.74 %*	*2.000*																
✓	Trial 2 (Last)	221.1 ps	14.9%	1.000	(See image)	1.000000e+000	Clock	CK0,/CK0	Strobe	DQS0,/DQS0	Data	DQ0,Gnd	Please select a signal	Not In Use	3	2000000	221.1 ps	221.1 ps	221.1 ps	0.0000000000000 s

Trial 2

Trial 2: tLZDQ



Next

✗ tRPRE

Reference: JEDEC Standard No. 79-3F, Table 68

Test Summary: **FAIL** | Test Description: Read preamble

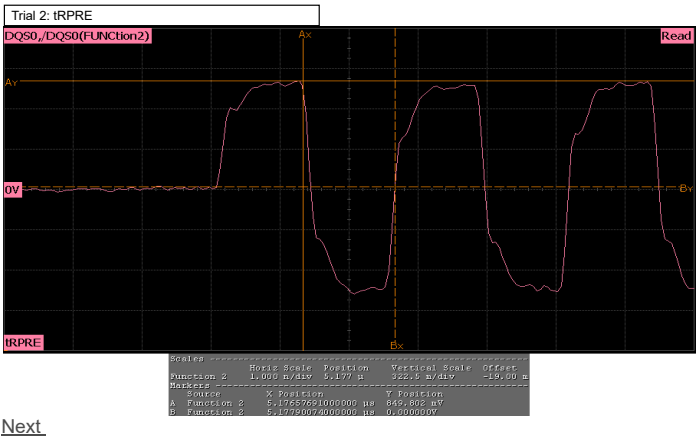
Pass Limits: [900.000000000 mtCK to 1.480000000000 tCK] | **tRPRE (Last of 2 Trials)** 529.530600000 mtCK | **# Trials Run:** 2 | **Last Trial:** Trial 2

Overall Summary + details of 1 last trials

Pass	Trial	Actual Value	Margin	tRPRE(s)	NumOfMeas	tRPRE	Number of burst(s) measured	CH1_PUT	CH1_Src	CH2_PUT	CH2_Src	CH3_PUT	CH3_Src	CH4_PUT	CH4_Src	Sampling Points (Pts)	Min	Max	Mean	St
	Avg	*527.7 mtCK*	*-64.20 %*	*1.319 ns*	*1.000*															
	StdDev	*2.656 mtCK*	*458.0 m%*	*6.640 ps*	*0.000*															
	Range	*3.756 mtCK*	*647.7 m%*	*9.391 ps*	*0.000*															
	Min	*525.8 mtCK*	*-64.52 %*	*1.314 ns*	*1.000*															
	Max	*529.5 mtCK*	*-63.87 %*	*1.324 ns*	*1.000*															
	Sum	*1.055 tCK*	*-128.4 %*	*2.638 ns*	*2.000*															
✗	Trial 2 (Last)	529.530600000 mtCK	**-63.9%**	1.324 ns	1.000	(See image)	1.000000e+000	Clock	CK0,/CK0	Strobe	DQS0,/DQS0	Data	DQ0,Gnd	Please select a signal	Not In Use	2000000	529.530600000 mtCK	529.530600000 mtCK	529.530600000 mtCK	0.(tC

Trial 2

Trial 2: tRPRE



Next

✗ tLZDQS

Reference: JEDEC Standard No. 79-3F, Table 68

Test Summary: **FAIL** | Test Description: DQS low-impedance time from CK,/CK

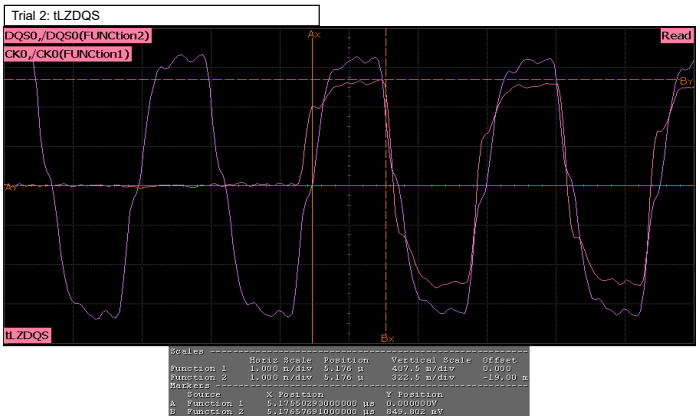
Pass Limits: [-800.0 ps to 400.0 ps] | **tLZDQS (Last of 2 Trials)** 1.0740 ns | **# Trials Run:** 2 | **Last Trial:** Trial 2

Overall Summary + details of 1 last trials

Pass	Trial	Actual Value	Margin	NumOfMeas	tLZDQS	Number of burst(s) measured	CH1_PUT	CH1_Src	CH2_PUT	CH2_Src	CH3_PUT	CH3_Src	CH4_PUT	CH4_Src	tDQSCK Delay (cycle)	Sampling Points (Pts)	Min	Max	Mean	Stdev
	Avg	*1.085 ns*	*-57.09 %*	*1.000*																
	StdDev	*15.63 ps*	*1.302 %*	*0.000*																
	Range	*22.10 ps*	*1.842 %*	*0.000*																
	Min	*1.074 ns*	*-58.01 %*	*1.000*																
	Max	*1.096 ns*	*-56.17 %*	*1.000*																
	Sum	*2.170 ns*	*-114.2 %*	*2.000*																
✗	Trial 2 (Last)	1.0740 ns	**-56.2%**	1.000	(See image)	1.000000e+000	Clock	CK0,/CK0	Strobe	DQS0,/DQS0	Data	DQ0,Gnd	Please select a signal	Not In Use	3	2000000	1.0740 ns	1.0740 ns	1.0740 ns	0.0000000000000 s

Trial 2

Trial 2: tLZDQS



Next

✓tCK(avg) Rising Edge Measurements

Reference: JEDEC Standard No. 79-3F, Table 62 (CL=6, CWL=5)

Test Summary: Pass | Test Description: tCK(avg) Rising Edge Measurements

Pass Limits: [2.500 ns to 3.300 ns] | **tCKavg Rising** 2.501 ns

Result Details

Min	2.501 ns	**Max**	2.510 ns	**Abs. Diff**	8.168 ps	**Average**	2.506 ns	**Periods**	19.949000 k	**Measurements**	19.750000 k	**Waveform Src**	Channel 1	**tWorstCase**	N/A