

Data Write

Data Write Worstcases

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- Click on the main header (e.g., "Setup" or "Hold") to view more details about how the margin was derived
- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column

Data Write Worstcases

#	Signal/Controller/DRAM			Status	Corner	Reference voltage used [mV]	Setup	Hold	Pulse Width	Min Slew Rate	Max Slew Rate	Min Slew Rate 2	Max Slew Rate 2	Voltage Margin between Signal and Eye-Mask	Peak Voltage	Overshoot	Undershoot	Overshoot Area	Undershoot Area	Overshoot Area 2	Undershoot Area 2
	Signal	Driving Controller.Pin	Receiving DRAM.Pin				Margin [ps]	Margin [ps]	Margin [ps]	Margin [V/ns]	Margin [V/ns]	Margin [V/ns]	Margin [V/ns]	Margin [V/ns]	Margin [V/ns]	Margin [V/ns]	Margin [mV]	Above/Below Reference Voltage Margin [mV]	Margin [mV]	Margin [mV]	Margin [V*ns]
1	DDR_DQ0	U15.F4	U16.G2	Pass	Typ	921.2	91.300	90.6	112.2	1.830	5.265	1.822	5.581	176.345	193.3	388.1	400.0	0.069	0.070	0.010	0.010
2	DDR_DQ1	U15.H6	U16.F7	Pass	Typ	921.2	92.1	92.5	114.6	1.794	5.255	1.725	5.580	175.715	199.6	386.9	400.0	0.068	0.070	0.010	0.010
3	DDR_DQ10	U15.U2	U16.C3	Pass	Typ	921.2	85.9	85.2	113.5	1.411	5.673	1.521	6.141	142.027	192.8	380.8	400.0	0.067	0.070	0.010	0.010
4	DDR_DQ11	U15.V5	U16.C7	Pass	Typ	921.2	88.9	88.800	112.4	1.809	5.452	1.929	5.659	175.691	192.5	384.4	400.0	0.069	0.070	0.010	0.010
5	DDR_DQ12	U15.W2	U16.C2	Pass	Typ	921.2	84.5	83.8	116.4	1.412	5.730	1.565	6.208	145.536	196.8	377.6	400.0	0.067	0.070	0.010	0.010
6	DDR_DQ13	U15.V6	U16.C8	Pass	Typ	921.2	90.200	90.0	110.4	1.889	5.407	1.953	5.655	175.538	190.8	385.1	400.0	0.069	0.070	0.010	0.010
7	DDR_DQ14	U15.Y1	U16.D3	Pass	Typ	921.2	85.5	86.5	115.8	1.344	5.887	1.616	6.216	154.929	196.9	378.7	400.0	0.067	0.070	0.010	0.010
8	DDR_DQ15	U15.W1	U16.D7	Pass	Typ	921.2	86.0	84.3	116.0	1.450	5.790	1.667	6.239	158.897	198.7	382.5	400.0	0.067	0.070	0.010	0.010
9	DDR_DQ2	U15.E3	U16.H3	Pass	Typ	921.2	88.6	87.4	112.6	1.543	5.611	1.755	6.002	175.034	199.9	383.0	400.0	0.067	0.070	0.010	0.010
10	DDR_DQ3	U15.F3	U16.H7	Pass	Typ	921.2	91.800	92.800	114.3	1.757	5.477	1.838	5.708	178.571	199.9	384.2	400.0	0.069	0.070	0.010	0.010
11	DDR_DQ4	U15.F1	U16.H2	Pass	Typ	921.2	85.3	83.8	116.9	1.285	5.700	1.464	6.102	162.160	199.4	382.2	400.0	0.067	0.070	0.010	0.010
12	DDR_DQ5	U15.G5	U16.H8	Pass	Typ	921.2	90.9	90.1	111.6	1.929	5.157	1.878	5.455	175.521	193.1	391.6	400.0	0.069	0.070	0.010	0.010
13	DDR_DQ6	U15.G2	U16.J3	Pass	Typ	921.2	84.0	81.3	108.7	1.254	5.538	1.407	5.917	161.604	196.9	378.1	400.0	0.067	0.070	0.010	0.010
14	DDR_DQ7	U15.F2	U16.J7	Pass	Typ	921.2	79.4	80.8	108.5	1.233	5.676	1.349	6.067	151.935	196.7	379.4	400.0	0.067	0.070	0.010	0.010
15	DDR_DQ8	U15.U1	U16.A3	Pass	Typ	921.2	86.300	84.1	114.6	1.393	5.832	1.577	6.245	146.693	192.6	378.4	400.0	0.068	0.070	0.010	0.010
16	DDR_DQ9	U15.U3	U16.B8	Pass	Typ	921.2	89.1	88.300	112.9	1.743	5.554	1.885	5.824	171.560	194.3	383.2	400.0	0.068	0.070	0.010	0.010
17	DDR_LDMN	U15.H5	U16.E7	Pass	Typ	921.2	89.800	90.4	111.7	1.711	5.065	1.616	5.481	169.053	196.3	385.7	400.0	0.068	0.070	0.010	0.010
18	DDR_UDMN	U15.W5	U16.E2	Pass	Typ	921.2	89.1	89.200	114.9	1.790	5.370	1.837	5.766	165.563	190.9	386.0	400.0	0.069	0.070	0.010	0.010
19	DDR_DQ0	U15.F4	U16.G2	Pass	Slow	868.3	89.300	88.700	109.9	1.756	5.305	1.705	5.491	163.943	178.0	386.1	400.0	0.069	0.070	0.010	0.010
20	DDR_DQ1	U15.H6	U16.F7	Pass	Slow	868.3	89.800	90.4	110.8	1.676	5.333	1.599	5.578	162.793	182.9	385.1	400.0	0.068	0.070	0.010	0.010
21	DDR_DQ10	U15.U2	U16.C3	Pass	Slow	868.3	84.6	84.1	113.6	1.266	5.629	1.330	6.032	130.897	181.7	379.7	400.0	0.067	0.070	0.010	0.010
22	DDR_DQ11	U15.V5	U16.C7	Pass	Slow	868.3	87.0	86.0	108.6	1.679	5.423	1.736	5.610	158.166	179.1	381.5	400.0	0.069	0.070	0.010	0.010
23	DDR_DQ12	U15.W2	U16.C2	Pass	Slow	868.3	82.7	81.7	113.9	1.251	5.685	1.382	6.098	134.572	179.6	376.4	400.0	0.067	0.070	0.010	0.010
24	DDR_DQ13	U15.V6	U16.C8	Pass	Slow	868.3	88.6	87.700	110.3	1.750	5.404	1.786	5.585	158.603	177.1	383.5	400.0	0.069	0.070	0.010	0.010
25	DDR_DQ14	U15.Y1	U16.D3	Pass	Slow	868.3	85.1	85.3	112.2	1.221	5.816	1.431	6.172	141.102	186.2	377.3	400.0	0.067	0.070	0.010	0.010
26	DDR_DQ15	U15.W1	U16.D7	Pass	Slow	868.3	83.8	83.2	114.1	1.318	5.761	1.522	6.133	143.029	184.4	381.6	400.0	0.067	0.070	0.010	0.010
27	DDR_DQ2	U15.E3	U16.H3	Pass	Slow	868.3	86.4	86.4	108.7	1.508	5.610	1.643	5.857	161.713	184.4	380.8	400.0	0.067	0.070	0.010	0.010
28	DDR_DQ3	U15.F3	U16.H7	Pass	Slow	868.3	89.800	89.700	109.9	1.616	5.454	1.744	5.690	164.477	183.3	382.2	400.0	0.068	0.070	0.010	0.010
29	DDR_DQ4	U15.F1	U16.H2	Pass	Slow	868.3	84.4	82.0	114.5	1.230	5.726	1.344	6.038	150.068	183.0	383.9	400.0	0.067	0.070	0.010	0.010
30	DDR_DQ5	U15.G5	U16.H8	Pass	Slow	868.3	87.0	87.4	108.7	1.819	5.214	1.773	5.435	162.392	177.4	388.9	400.0	0.069	0.070	0.010	0.010

	Signal/Controller/DRAM			Status	Corner		Setup	Hold	Pulse Width	Min Slew Rate	Max Slew Rate	Min Slew Rate 2	Max Slew Rate 2	Voltage Margin between Signal and Eye-Mask	Peak Voltage	Overshoot	Undershoot	Overshoot Area	Undershoot Area	Overshoot Area 2	Undershoot Area 2
#	Signal	Driving Controller.Pin	Receiving DRAM.Pin	Pass/Fail	Case	Reference voltage used [mV]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [V/ns]	Margin [V/ns]	Margin [V/ns]	Margin [V/ns]	Margin [mV]	Above/Below Reference Voltage Margin [mV]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Margin [V*ns]	Margin [V*ns]
31	DDR_DQ6	U15.G2	U16.J3	Pass	Slow	868.3	82.0	81.7	107.0	1.218	5.550	1.296	5.885	147.835	183.6	380.2	400.0	0.067	0.070	0.010	0.010
32	DDR_DQ7	U15.F2	U16.J7	Pass	Slow	868.3	77.8	78.4	107.2	1.182	5.707	1.252	6.014	136.452	182.8	381.4	400.0	0.067	0.070	0.010	0.010
33	DDR_DQ8	U15.U1	U16.A3	Pass	Slow	868.3	82.7	82.5	111.4	1.259	5.746	1.380	6.149	131.964	181.2	376.9	400.0	0.068	0.070	0.010	0.010
34	DDR_DQ9	U15.U3	U16.B8	Pass	Slow	868.3	86.700	86.700	110.8	1.609	5.562	1.711	5.780	155.812	179.0	381.6	400.0	0.068	0.070	0.010	0.010
35	DDR_LDMN	U15.H5	U16.E7	Pass	Slow	868.3	89.5	89.300	109.6	1.651	5.208	1.511	5.485	156.451	180.5	388.2	400.0	0.068	0.070	0.010	0.010
36	DDR_UDMN	U15.W5	U16.E2	Pass	Slow	868.3	87.200	85.7	112.4	1.638	5.329	1.659	5.662	150.536	179.1	385.9	400.0	0.068	0.070	0.010	0.010
37	DDR_DQ0	U15.F4	U16.G2	Pass	Fast	971.3	90.6	90.800	112.7	1.760	5.108	1.905	5.453	182.517	205.6	388.2	400.0	0.069	0.070	0.010	0.010
38	DDR_DQ1	U15.H6	U16.F7	Pass	Fast	971.3	92.0	90.6	114.5	1.708	5.112	1.761	5.501	187.281	212.0	386.7	400.0	0.068	0.070	0.010	0.010
39	DDR_DQ10	U15.U2	U16.C3	Pass	Fast	971.3	86.200	85.0	112.9	1.473	5.616	1.666	6.083	152.347	200.8	383.0	400.0	0.067	0.070	0.010	0.010
40	DDR_DQ11	U15.V5	U16.C7	Pass	Fast	971.3	88.300	89.300	112.4	1.830	5.328	2.074	5.521	184.073	205.0	385.6	400.0	0.069	0.070	0.010	0.010
41	DDR_DQ12	U15.W2	U16.C2	Pass	Fast	971.3	82.2	84.3	116.1	1.459	5.653	1.725	6.081	153.510	208.3	379.5	400.0	0.067	0.070	0.010	0.010
42	DDR_DQ13	U15.V6	U16.C8	Pass	Fast	971.3	89.200	90.1	111.3	1.878	5.301	2.068	5.532	183.908	203.1	387.3	400.0	0.069	0.070	0.010	0.010
43	DDR_DQ14	U15.Y1	U16.D3	Pass	Fast	971.3	86.0	86.200	115.3	1.444	5.797	1.755	6.141	162.243	207.6	381.5	400.0	0.067	0.070	0.010	0.010
44	DDR_DQ15	U15.W1	U16.D7	Pass	Fast	971.3	84.2	86.0	117.4	1.489	5.681	1.799	6.115	166.578	209.2	382.4	400.0	0.067	0.070	0.010	0.010
45	DDR_DQ2	U15.E3	U16.H3	Pass	Fast	971.3	86.9	88.4	113.2	1.579	5.562	1.907	5.813	186.537	211.6	383.3	400.0	0.067	0.070	0.010	0.010
46	DDR_DQ3	U15.F3	U16.H7	Pass	Fast	971.3	92.200	92.5	114.1	1.764	5.348	1.900	5.551	186.851	212.6	383.8	400.0	0.069	0.070	0.010	0.010
47	DDR_DQ4	U15.F1	U16.H2	Pass	Fast	971.3	81.7	83.1	115.2	1.282	5.569	1.574	5.955	169.885	211.2	381.2	400.0	0.067	0.070	0.010	0.010
48	DDR_DQ5	U15.G5	U16.H8	Pass	Fast	971.3	90.200	91.4	111.7	1.835	5.013	1.952	5.364	182.421	206.4	391.9	400.0	0.070	0.070	0.010	0.010
49	DDR_DQ6	U15.G2	U16.J3	Pass	Fast	971.3	85.7	82.2	109.6	1.206	5.374	1.534	5.800	170.062	205.4	376.8	400.0	0.067	0.070	0.010	0.010
50	DDR_DQ7	U15.F2	U16.J7	Pass	Fast	971.3	79.2	80.1	106.2	1.198	5.545	1.515	5.936	162.693	209.0	378.4	400.0	0.066	0.070	0.010	0.010
51	DDR_DQ8	U15.U1	U16.A3	Pass	Fast	971.3	82.9	84.1	112.3	1.466	5.763	1.715	6.141	154.522	200.6	380.9	400.0	0.068	0.070	0.010	0.010
52	DDR_DQ9	U15.U3	U16.B8	Pass	Fast	971.3	88.5	88.200	112.0	1.754	5.394	2.018	5.725	180.619	206.9	384.6	400.0	0.068	0.070	0.010	0.010
53	DDR_LDMN	U15.H5	U16.E7	Pass	Fast	971.3	88.5	90.4	111.7	1.603	4.880	1.693	5.373	177.265	210.5	385.2	400.0	0.068	0.070	0.010	0.010
54	DDR_UDMN	U15.W5	U16.E2	Pass	Fast	971.3	88.0	89.300	113.2	1.754	5.284	1.937	5.662	176.347	201.9	386.7	400.0	0.069	0.070	0.010	0.010

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#	Signal/DRAM/Controller			Status	Corner	Reference Voltage Used [mV]	Setup	Hold	Pulse Width
	Signal	Driving DRAM.Pin	Receiving Controller.Pin	Pass/Fail	Case		Margin [ps]	Margin [ps]	Margin [ps]
1	DDR_DQ0	U16.G2	U15.F4	Pass	Typ	891.1	99.6	99.5	N/A
2	DDR_DQ1	U16.F7	U15.H6	Pass	Typ	891.1	99.9	100.200	N/A
3	DDR_DQ10	U16.C3	U15.U2	Pass	Typ	887.7	95.4	94.700	N/A
4	DDR_DQ11	U16.C7	U15.V5	Pass	Typ	887.7	99.200	101.5	N/A
5	DDR_DQ12	U16.C2	U15.W2	Pass	Typ	887.7	95.800	98.4	N/A
6	DDR_DQ13	U16.C8	U15.V6	Pass	Typ	887.7	99.6	97.4	N/A
7	DDR_DQ14	U16.D3	U15.Y1	Pass	Typ	887.7	96.6	96.200	N/A
8	DDR_DQ15	U16.D7	U15.W1	Pass	Typ	887.7	96.9	96.700	N/A
9	DDR_DQ2	U16.H3	U15.E3	Pass	Typ	891.1	98.4	96.800	N/A
10	DDR_DQ3	U16.H7	U15.F3	Pass	Typ	891.1	99.700	98.4	N/A
11	DDR_DQ4	U16.H2	U15.F1	Pass	Typ	891.1	95.0	94.0	N/A
12	DDR_DQ5	U16.H8	U15.G5	Pass	Typ	891.1	98.700	100.300	N/A
13	DDR_DQ6	U16.J3	U15.G2	Pass	Typ	891.1	93.800	93.100	N/A
14	DDR_DQ7	U16.J7	U15.F2	Pass	Typ	891.1	94.6	96.4	N/A
15	DDR_DQ8	U16.A3	U15.U1	Pass	Typ	887.7	95.300	94.700	N/A
16	DDR_DQ9	U16.B8	U15.U3	Pass	Typ	887.7	99.300	101.700	N/A
17	DDR_DQ0	U16.G2	U15.F4	Pass	Slow	859.1	94.1	94.1	N/A
18	DDR_DQ1	U16.F7	U15.H6	Pass	Slow	859.1	93.4	94.800	N/A
19	DDR_DQ10	U16.C3	U15.U2	Pass	Slow	855.1	90.0	89.9	N/A
20	DDR_DQ11	U16.C7	U15.V5	Pass	Slow	855.1	95.200	97.700	N/A
21	DDR_DQ12	U16.C2	U15.W2	Pass	Slow	855.1	91.5	93.4	N/A
22	DDR_DQ13	U16.C8	U15.V6	Pass	Slow	855.1	96.700	90.4	N/A
23	DDR_DQ14	U16.D3	U15.Y1	Pass	Slow	855.1	92.5	92.100	N/A
24	DDR_DQ15	U16.D7	U15.W1	Pass	Slow	855.1	92.2	90.2	N/A
25	DDR_DQ2	U16.H3	U15.E3	Pass	Slow	859.1	92.600	91.100	N/A
26	DDR_DQ3	U16.H7	U15.F3	Pass	Slow	859.1	94.0	93.100	N/A
27	DDR_DQ4	U16.H2	U15.F1	Pass	Slow	859.1	88.9	88.800	N/A
28	DDR_DQ5	U16.H8	U15.G5	Pass	Slow	859.1	93.800	95.0	N/A
29	DDR_DQ6	U16.J3	U15.G2	Pass	Slow	859.1	88.4	88.800	N/A
30	DDR_DQ7	U16.J7	U15.F2	Pass	Slow	859.1	87.600	91.5	N/A
31	DDR_DQ8	U16.A3	U15.U1	Pass	Slow	855.1	90.4	90.0	N/A
32	DDR_DQ9	U16.B8	U15.U3	Pass	Slow	855.1	95.800	97.9	N/A
33	DDR_DQ0	U16.G2	U15.F4	Pass	Fast	907.3	103.4	101.0	N/A
34	DDR_DQ1	U16.F7	U15.H6	Pass	Fast	907.3	104.4	101.300	N/A
35	DDR_DQ10	U16.C3	U15.U2	Pass	Fast	905.6	96.700	97.4	N/A
36	DDR_DQ11	U16.C7	U15.V5	Pass	Fast	905.6	102.6	103.6	N/A
37	DDR_DQ12	U16.C2	U15.W2	Pass	Fast	905.6	98.5	101.0	N/A

	Signal/DRAM/Controller			Status	Corner		Setup	Hold	Pulse Width
#	Signal	Driving DRAM.Pin	Receiving Controller.Pin	Pass/Fail	Case	Reference Voltage Used [mV]	Margin [ps]	Margin [ps]	Margin [ps]
38	DDR_DQ13	U16.C8	U15.V6	Pass	Fast	905.6	103.0	101.9	N/A
39	DDR_DQ14	U16.D3	U15.Y1	Pass	Fast	905.6	98.4	98.9	N/A
40	DDR_DQ15	U16.D7	U15.W1	Pass	Fast	905.6	99.200	100.200	N/A
41	DDR_DQ2	U16.H3	U15.E3	Pass	Fast	907.3	101.300	100.300	N/A
42	DDR_DQ3	U16.H7	U15.F3	Pass	Fast	907.3	103.0	99.0	N/A
43	DDR_DQ4	U16.H2	U15.F1	Pass	Fast	907.3	97.5	96.200	N/A
44	DDR_DQ5	U16.H8	U15.G5	Pass	Fast	907.3	101.5	104.6	N/A
45	DDR_DQ6	U16.J3	U15.G2	Pass	Fast	907.3	96.4	95.4	N/A
46	DDR_DQ7	U16.J7	U15.F2	Pass	Fast	907.3	97.200	100.200	N/A
47	DDR_DQ8	U16.A3	U15.U1	Pass	Fast	905.6	97.300	96.4	N/A
48	DDR_DQ9	U16.B8	U15.U3	Pass	Fast	905.6	101.800	103.5	N/A

Address

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#	Signal/Dram		Status	Corner	Setup	Hold	Overshoot	Undershoot	Overshoot Area	Undershoot Area	Overshoot Area 2	Undershoot Area 2
	Signal	Accessed DRAM	Pass/Fail	Case	Margin [ps]	Margin [ps]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Margin [V*ns]	Margin [V*ns]
1	DDR_A0	U16.P3	Pass	Typ	95.500	227.1	167.3	172.6	0.158	0.165	0.005	N/A
2	DDR_A1	U16.P7	Pass	Typ	96.600	222.8	203.7	197.2	0.161	0.166	0.005	N/A
3	DDR_A10	U16.M3	Pass	Typ	128.100	175.2	139.8	173.0	0.160	0.168	0.005	N/A
4	DDR_A11	U16.T2	Pass	Typ	118.700	188.0	81.4	115.3	0.154	0.162	0.005	N/A
5	DDR_A12	U16.M7	Pass	Typ	133.2	179.600	208.8	199.9	0.165	0.170	0.005	N/A
6	DDR_A13	U16.T8	Pass	Typ	80.800	229.500	156.4	157.2	0.155	0.161	0.005	N/A
7	DDR_A14_WEN	U16.L2	Pass	Typ	112.100	205.200	151.5	156.4	0.158	0.165	0.005	N/A
8	DDR_A15_CASN	U16.M8	Pass	Typ	125.000	187.3	145.4	152.4	0.159	0.166	0.005	N/A
9	DDR_A16_RASN	U16.L8	Pass	Typ	116.6	189.800	110.9	91.6	0.154	0.157	0.005	N/A
10	DDR_A2	U16.R3	Pass	Typ	100.2	219.6	207.1	168.8	0.162	0.165	0.005	N/A
11	DDR_A3	U16.N7	Pass	Typ	124.300	187.100	148.7	162.6	0.160	0.167	0.005	N/A
12	DDR_A4	U16.N3	Pass	Typ	119.3	189.500	146.6	160.7	0.160	0.166	0.005	N/A
13	DDR_A5	U16.P8	Pass	Typ	96.100	233.600	165.5	178.6	0.158	0.164	0.005	N/A
14	DDR_A6	U16.P2	Pass	Typ	97.000	216.600	168.4	166.9	0.158	0.164	0.005	N/A
15	DDR_A7	U16.R8	Pass	Typ	96.900	229.3	184.4	145.0	0.160	0.161	0.005	N/A
16	DDR_A8	U16.R2	Pass	Typ	92.8	228.000	178.3	172.0	0.158	0.163	0.005	N/A
17	DDR_A9	U16.R7	Pass	Typ	116.1	195.1	142.8	151.8	0.158	0.165	0.005	N/A
18	DDR_ACTN	U16.L3	Pass	Typ	157.9	142.200	209.5	183.1	0.164	0.168	0.005	N/A
19	DDR_BA0	U16.N2	Pass	Typ	91.0	228.5	138.1	132.7	0.154	0.158	0.005	N/A
20	DDR_BA1	U16.N8	Pass	Typ	93.600	225.5	191.0	141.1	0.157	0.160	0.005	N/A
21	DDR_BG0	U16.M2	Pass	Typ	111.9	198.300	134.4	148.6	0.157	0.164	0.005	N/A
22	DDR_CKE	U16.K2	Pass	Typ	113.200	194.600	250.3	128.7	0.167	0.161	0.005	N/A
23	DDR_CSN	U16.L7	Pass	Typ	161.7	144.6	224.0	189.9	0.164	0.169	0.005	N/A
24	DDR_ODT	U16.K3	Pass	Typ	97.300	198.9	137.9	128.9	0.155	0.158	0.005	N/A
25	DDR_PARITY	U16.T3	Pass	Typ	95.7	213.400	115.3	73.2	0.151	0.151	0.005	N/A
26	DDR_A0	U16.P3	Pass	Slow	97.7	226.5	169.8	188.5	0.157	0.167	0.005	N/A
27	DDR_A1	U16.P7	Pass	Slow	101.800	219.100	218.1	203.4	0.162	0.167	0.005	N/A
28	DDR_A10	U16.M3	Pass	Slow	130.9	177.2	141.6	210.9	0.159	0.170	0.005	N/A
29	DDR_A11	U16.T2	Pass	Slow	117.800	188.8	90.0	175.3	0.154	0.166	0.005	N/A
30	DDR_A12	U16.M7	Pass	Slow	134.4	175.400	220.8	240.8	0.166	0.172	0.005	N/A
31	DDR_A13	U16.T8	Pass	Slow	84.700	229.7	168.4	173.5	0.156	0.163	0.005	N/A
32	DDR_A14_WEN	U16.L2	Pass	Slow	111.4	198.900	146.4	197.5	0.157	0.168	0.005	N/A
33	DDR_A15_CASN	U16.M8	Pass	Slow	124.200	187.100	146.6	201.5	0.159	0.169	0.005	N/A
34	DDR_A16_RASN	U16.L8	Pass	Slow	116.5	188.400	138.0	139.2	0.156	0.162	0.005	N/A
35	DDR_A2	U16.R3	Pass	Slow	100.9	216.000	199.1	198.3	0.162	0.168	0.005	N/A
36	DDR_A3	U16.N7	Pass	Slow	123.2	187.400	156.0	209.6	0.160	0.170	0.005	N/A
37	DDR_A4	U16.N3	Pass	Slow	120.900	189.5	153.8	206.7	0.160	0.169	0.005	N/A

	Signal/Dram		Status	Corner	Setup	Hold	Overshoot	Undershoot	Overshoot Area	Undershoot Area	Overshoot Area 2	Undershoot Area 2
#	Signal	Accessed DRAM	Pass/Fail	Case	Margin [ps]	Margin [ps]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Margin [V*ns]	Margin [V*ns]
38	DDR_A5	U16.P8	Pass	Slow	99.9	225.2	165.5	198.7	0.156	0.167	0.005	N/A
39	DDR_A6	U16.P2	Pass	Slow	99.1	214.900	175.5	180.7	0.159	0.166	0.005	N/A
40	DDR_A7	U16.R8	Pass	Slow	96.6	224.6	183.7	176.7	0.160	0.165	0.005	N/A
41	DDR_A8	U16.R2	Pass	Slow	93.300	227.8	179.1	186.7	0.157	0.165	0.005	N/A
42	DDR_A9	U16.R7	Pass	Slow	115.500	195.000	131.5	194.2	0.157	0.168	0.005	N/A
43	DDR_ACTN	U16.L3	Pass	Slow	160.2	145.400	220.7	210.3	0.164	0.169	0.005	N/A
44	DDR_BA0	U16.N2	Pass	Slow	93.800	226.4	148.4	149.4	0.155	0.160	0.005	N/A
45	DDR_BA1	U16.N8	Pass	Slow	95.700	224.9	183.5	170.2	0.158	0.164	0.005	N/A
46	DDR_BG0	U16.M2	Pass	Slow	112.700	197.8	130.9	201.8	0.156	0.169	0.005	N/A
47	DDR_CKE	U16.K2	Pass	Slow	115.400	198.2	248.7	148.4	0.167	0.163	0.005	N/A
48	DDR_CSN	U16.L7	Pass	Slow	163.0	145.7	231.3	216.0	0.165	0.170	0.005	N/A
49	DDR_ODT	U16.K3	Pass	Slow	115.100	203.0	149.6	151.8	0.155	0.161	0.005	N/A
50	DDR_PARITY	U16.T3	Pass	Slow	106.2	219.900	110.6	118.8	0.151	0.157	0.005	N/A
51	DDR_A0	U16.P3	Pass	Fast	65.6	205.5	163.9	141.4	0.158	0.160	0.005	N/A
52	DDR_A1	U16.P7	Pass	Fast	30.900	200.0	215.9	170.0	0.161	0.161	0.005	N/A
53	DDR_A10	U16.M3	Pass	Fast	59.1	157.600	153.6	130.9	0.162	0.165	0.005	N/A
54	DDR_A11	U16.T2	Pass	Fast	105.200	169.0	105.9	79.6	0.157	0.159	0.005	N/A
55	DDR_A12	U16.M7	Pass	Fast	23.600	162.900	218.3	165.6	0.167	0.169	0.005	N/A
56	DDR_A13	U16.T8	Pass	Fast	62.100	203.900	149.1	147.8	0.155	0.159	0.005	N/A
57	DDR_A14_WEN	U16.L2	Pass	Fast	98.1	189.900	164.4	125.7	0.160	0.161	0.005	N/A
58	DDR_A15_CASN	U16.M8	Fail	Fast	Bad Signal	Bad Signal	155.8	123.2	0.161	0.162	0.005	N/A
59	DDR_A16_RASN	U16.L8	Fail	Fast	103.3	-104.1	112.9	56.3	0.156	0.152	0.005	N/A
60	DDR_A2	U16.R3	Pass	Fast	62.8	195.4	224.5	137.7	0.161	0.161	0.005	N/A
61	DDR_A3	U16.N7	Pass	Fast	107.1	168.2	162.4	128.7	0.162	0.163	0.005	N/A
62	DDR_A4	U16.N3	Pass	Fast	104.8	171.0	169.7	133.1	0.162	0.163	0.005	N/A
63	DDR_A5	U16.P8	Pass	Fast	50.900	218.7	170.1	151.4	0.159	0.160	0.005	N/A
64	DDR_A6	U16.P2	Pass	Fast	69.9	195.600	163.2	137.5	0.159	0.161	0.005	N/A
65	DDR_A7	U16.R8	Pass	Fast	71.700	211.300	199.4	129.2	0.160	0.159	0.005	N/A
66	DDR_A8	U16.R2	Pass	Fast	54.300	203.4	170.3	136.7	0.158	0.158	0.005	N/A
67	DDR_A9	U16.R7	Pass	Fast	96.7	175.200	141.0	122.3	0.158	0.161	0.005	N/A
68	DDR_ACTN	U16.L3	Pass	Fast	118.400	127.9	238.3	180.8	0.164	0.167	0.005	N/A
69	DDR_BA0	U16.N2	Pass	Fast	70.4	205.1	136.9	123.1	0.154	0.157	0.005	N/A
70	DDR_BA1	U16.N8	Pass	Fast	64.3	203.9	208.1	116.7	0.158	0.156	0.005	N/A
71	DDR_BG0	U16.M2	Fail	Fast	94.3	-84.4	146.2	113.6	0.158	0.160	0.005	N/A
72	DDR_CKE	U16.K2	Pass	Fast	39.200	175.8	256.6	113.7	0.168	0.158	0.005	N/A
73	DDR_CSN	U16.L7	Pass	Fast	130.1	133.4	252.6	181.4	0.166	0.168	0.005	N/A
74	DDR_ODT	U16.K3	Pass	Fast	57.500	191.900	168.7	128.5	0.156	0.155	0.005	N/A
75	DDR_PARITY	U16.T3	Pass	Fast	68.900	203.100	128.7	34.9	0.154	0.145	0.005	N/A

Differential Nets

Differential Nets Worstcases

- To investigate any result further, click on the link in the cell to open the waveforms. Viewing waveforms requires a valid EZwave license.
- Click on the main header (e.g., "Setup" or "Hold") to view more details about how the margin was derived
- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column

Differential Nets Worstcases

#	Signal/Driver/Receiver				Status	Corner	Overshoot	Undershoot	Overshoot Area	Undershoot Area	Overshoot Area 2	Undershoot Area 2	tDVAC	Vix	
	Signal	Driver.Pins	Receiver.Pins	Operation											
1	DDR_CKP	U15.L1&L2	U16.K7&K8	Write rank(1,1)	Pass	Typ	300.0	300.0	0.075	0.076	0.003	N/A	142	52.0	Pass
2	DDR_LDQS_P	U16.G3&F3	U15.E1&E2	Read rank(1,1)	Pass	Typ	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
3	DDR_LDQS_P	U15.E1&E2	U16.G3&F3	Write rank(1,1)	Pass	Typ	400.0	400.0	0.070	0.070	0.010	0.010	N/A	116.8	N/A
4	DDR_UDQS_P	U16.B7&A7	U15.V1&V2	Read rank(1,1)	Pass	Typ	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
5	DDR_UDQS_P	U15.V1&V2	U16.B7&A7	Write rank(1,1)	Pass	Typ	390.8	400.0	0.070	0.070	0.010	0.010	N/A	116.9	N/A
6	DDR_CKP	U15.L1&L2	U16.K7&K8	Write rank(1,1)	Pass	Slow	300.0	300.0	0.075	0.076	0.003	N/A	132	55.8	Pass
7	DDR_LDQS_P	U16.G3&F3	U15.E1&E2	Read rank(1,1)	Pass	Slow	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
8	DDR_LDQS_P	U15.E1&E2	U16.G3&F3	Write rank(1,1)	Pass	Slow	400.0	400.0	0.070	0.070	0.010	0.010	N/A	111.0	N/A
9	DDR_UDQS_P	U16.B7&A7	U15.V1&V2	Read rank(1,1)	Pass	Slow	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
10	DDR_UDQS_P	U15.V1&V2	U16.B7&A7	Write rank(1,1)	Pass	Slow	390.2	400.0	0.070	0.070	0.010	0.010	N/A	111.4	N/A
11	DDR_CKP	U15.L1&L2	U16.K7&K8	Write rank(1,1)	Pass	Fast	300.0	300.0	0.075	0.076	0.003	N/A	146	26.2	Pass
12	DDR_LDQS_P	U16.G3&F3	U15.E1&E2	Read rank(1,1)	Pass	Fast	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
13	DDR_LDQS_P	U15.E1&E2	U16.G3&F3	Write rank(1,1)	Pass	Fast	400.0	400.0	0.070	0.070	0.010	0.010	N/A	116.0	N/A
14	DDR_UDQS_P	U16.B7&A7	U15.V1&V2	Read rank(1,1)	Pass	Fast	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
15	DDR_UDQS_P	U15.V1&V2	U16.B7&A7	Write rank(1,1)	Pass	Fast	388.9	400.0	0.070	0.070	0.010	0.010	N/A	115.9	N/A

CLK-DQS Skew

CLK-DQS Skew Worstcases

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- Click on the main header (e.g., "Setup" or "Hold") to view more details about how the margin was derived
- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column

CLK-DQS Skew Worstcases

#	Signal/Dram				Status	Corner	DQSS - Earliest DQS	DQSS - Latest DQS	tDSS	tDSH
	Signal	Accessed DRAM	DRAM CLK Pins	DRAM DQS Pins	Pass/Fail	Case	Margin [ps]	Margin [ps]	Margin [ps]	Margin [ps]
1	DDR_LDQS_P	U16	K7&K8	G3&F3	Pass	Typ	158.9	151.7	185.4	190.2
2	DDR_UDQS_P	U16	K7&K8	B7&A7	Pass	Typ	160.3	150.9	184.8	191.9
3	DDR_LDQS_P	U16	K7&K8	G3&F3	Pass	Slow	158.1	148.1	184.2	190.7
4	DDR_UDQS_P	U16	K7&K8	B7&A7	Pass	Slow	159.8	147.5	183.4	192.6
5	DDR_LDQS_P	U16	K7&K8	G3&F3	Pass	Fast	159.3	153.1	187.5	190.9
6	DDR_UDQS_P	U16	K7&K8	B7&A7	Pass	Fast	160.7	152.3	186.5	192.7

Eye Density Links

Eye Density Links

Eye Density Links

#	Eye Density Links	Data/Address	Case
1	Load Eye Density Plots	Data	Typ
2	Load Eye Density Plots	Data	Slow
3	Load Eye Density Plots	Data	Fast

Setup Info

Design: PCB_501-1-04356_A0-67.hyp

VX2.12 build 21158655

Date: May-20-2024 16h-10m

Setup Information

Interface Setup

Parameter	Value
DDR Interface	DDR4
Crosstalk	Disabled
Power-Aware	Disabled
IC Corners	Fast, Typ, Slow
Probing location	Controller - at Die, DRAM - at Die
Total Run Time	0 Days, 00 Hours, 03 Minutes 40 Seconds

Rank Setup

Rank	Ref. Des.	IBIS File	Component	Timing Model	Speed Grade
Controller	U15	spm766d.ibs	AM62	C:\MentorGraphics\HLVX2.12\SDD_HOME\hyperlynx64\Libs\ddr4_ctl.v	DDR4_3200
Rank[1,1]	U16	z42b_ait.ibs	MT40A1G16TD	C:\MentorGraphics\HLVX2.12\SDD_HOME\hyperlynx64\Libs\ddr4_dram.v	DDR4_3200

IBIS Model Selectors

Rank	CLK	Addr	CTL
Controller	ddr4_ocd_60p_60n_diff	ddr4_ocd_60p_60n	ddr4_ocd_60p_60n
No Data	No Data	No Data	No Data

ODT - Write to Slot 1

Rank	DQS	DQ	DM
Controller	ddr4_ocd_60p_60n_diff,	ddr4_ocd_60p_60n,	ddr4_ocd_60p_60n,
Rank[1,1]	DQS_IN_ODT48_3200	DQ_IN_ODT48_3200	DM_ODT48_3200

ODT - Read from Slot 1

Rank	DQS	DQ	DM
Controller	ddr4_odt_48_diff,	ddr4_odt_48,	ddr4_odt_48,
Rank[1,1]	DQS_48_3200	DQ_48_3200	DQ_48_3200