

Data Write

Data Write Worstcases

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- Click on the main header (e.g., "Setup" or "Hold") to view more details about how the margin was derived
- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column

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#	Signal/Controller/DRAM			Status	Corner	Reference voltage used [mV]	Setup	Hold	Pulse Width	Min Slew Rate	Max Slew Rate	Min Slew Rate 2	Max Slew Rate 2	Voltage Margin between Signal and Eye-Mask	Peak Voltage	Overshoot	Undershoot	Overshoot Area	Undershoot Area	Overshoot Area 2	Undershoot Area 2
	Signal	Driving Controller.Pin	Receiving DRAM.Pin				Margin [ps]	Margin [ps]	Margin [ps]	Margin [V/ns]	Margin [V/ns]	Margin [V/ns]	Margin [V/ns]	Margin [V/ns]	Margin [V/ns]	Margin [V/ns]	Margin [mV]	Above/Below Reference Voltage Margin [mV]	Margin [mV]	Margin [mV]	Margin [V*ns]
1	DDR_DQ0	U15.F4	U16.G2	Pass	Typ	916.5	81.9	80.2	108.1	0.889	6.134	1.074	6.395	146.465	184.2	387.5	400.0	0.069	0.070	0.010	0.010
2	DDR_DQ1	U15.H6	U16.F7	Pass	Typ	916.5	82.5	82.6	109.0	0.875	5.907	0.798	6.703	145.349	186.0	383.3	400.0	0.068	0.070	0.010	0.010
3	DDR_DQ10	U15.U2	U16.C3	Pass	Typ	916.5	77.2	76.6	109.5	0.627	6.537	1.124	6.831	123.305	182.8	383.8	400.0	0.068	0.070	0.010	0.010
4	DDR_DQ11	U15.V5	U16.C7	Pass	Typ	916.5	80.4	79.5	109.3	0.963	6.467	1.372	6.332	140.648	182.7	390.8	400.0	0.070	0.070	0.010	0.010
5	DDR_DQ12	U15.W2	U16.C2	Pass	Typ	916.5	73.9	73.0	111.1	0.665	6.775	1.407	6.544	127.770	179.5	383.3	400.0	0.068	0.070	0.010	0.010
6	DDR_DQ13	U15.V6	U16.C8	Pass	Typ	916.5	82.4	81.9	105.1	0.974	6.333	1.314	6.376	145.901	183.5	393.0	400.0	0.070	0.070	0.010	0.010
7	DDR_DQ14	U15.Y1	U16.D3	Pass	Typ	916.5	80.0	78.4	112.8	0.725	6.697	1.277	6.659	137.323	189.0	382.1	400.0	0.069	0.070	0.010	0.010
8	DDR_DQ15	U15.W1	U16.D7	Pass	Typ	916.5	78.8	78.4	110.9	0.738	6.758	1.520	6.439	137.751	188.4	388.5	400.0	0.068	0.070	0.010	0.010
9	DDR_DQ2	U15.E3	U16.H3	Pass	Typ	916.5	79.8	79.0	107.6	0.792	6.404	1.489	6.245	148.213	188.5	389.4	400.0	0.069	0.070	0.010	0.010
10	DDR_DQ3	U15.F3	U16.H7	Pass	Typ	916.5	85.6	86.6	108.2	1.094	5.590	0.655	6.665	143.972	184.9	384.1	400.0	0.069	0.070	0.010	0.010
11	DDR_DQ4	U15.F1	U16.H2	Pass	Typ	916.5	75.0	72.3	112.2	0.543	6.278	1.120	6.972	148.105	187.5	381.9	400.0	0.068	0.070	0.010	0.010
12	DDR_DQ5	U15.G5	U16.H8	Pass	Typ	916.5	79.0	79.2	106.7	0.895	6.042	0.916	6.519	143.481	185.8	390.1	400.0	0.069	0.070	0.010	0.010
13	DDR_DQ6	U15.G2	U16.J3	Pass	Typ	916.5	72.0	71.1	105.4	0.438	6.096	1.112	6.924	142.029	181.9	375.5	400.0	0.067	0.070	0.010	0.010
14	DDR_DQ7	U15.F2	U16.J7	Pass	Typ	916.5	69.8	70.3	102.6	0.529	6.404	1.498	6.737	140.788	186.8	379.1	400.0	0.068	0.070	0.010	0.010
15	DDR_DQ8	U15.U1	U16.A3	Pass	Typ	916.5	77.6	77.5	107.2	0.694	6.681	1.242	6.841	128.041	184.4	382.6	400.0	0.069	0.070	0.010	0.010
16	DDR_DQ9	U15.U3	U16.B8	Pass	Typ	916.5	80.1	80.5	107.5	0.930	6.370	1.289	6.498	138.903	182.8	391.7	400.0	0.069	0.070	0.010	0.010
17	DDR_LDMN	U15.H5	U16.E7	Pass	Typ	916.5	81.1	80.5	109.6	0.771	6.022	0.863	6.625	141.827	188.6	381.9	400.0	0.068	0.070	0.010	0.010
18	DDR_UDMN	U15.W5	U16.E2	Pass	Typ	916.5	81.6	81.3	109.7	0.999	6.211	1.120	6.712	135.377	184.6	389.6	400.0	0.069	0.070	0.010	0.010
19	DDR_DQ0	U15.F4	U16.G2	Pass	Slow	867.1	69.8	72.7	105.7	0.465	6.852	1.625	6.565	125.298	165.9	382.6	400.0	0.067	0.070	0.010	0.010
20	DDR_DQ1	U15.H6	U16.F7	Pass	Slow	867.1	72.1	73.3	114.0	0.455	6.856	1.352	6.726	114.365	161.9	378.8	400.0	0.067	0.070	0.010	0.010
21	DDR_DQ10	U15.U2	U16.C3	Pass	Slow	867.1	66.8	70.2	111.2	0.289	6.828	1.273	7.011	97.169	151.6	380.3	400.0	0.068	0.070	0.010	0.010
22	DDR_DQ11	U15.V5	U16.C7	Pass	Slow	867.1	70.8	71.5	110.0	0.415	6.766	1.580	6.628	126.827	167.1	373.3	400.0	0.068	0.070	0.010	0.010
23	DDR_DQ12	U15.W2	U16.C2	Pass	Slow	867.1	66.7	67.2	110.6	0.353	6.797	1.371	6.898	101.621	159.5	379.6	400.0	0.067	0.070	0.010	0.010
24	DDR_DQ13	U15.V6	U16.C8	Pass	Slow	867.1	70.6	70.5	108.9	0.440	6.794	1.573	6.625	127.062	165.4	373.7	400.0	0.068	0.070	0.010	0.010
25	DDR_DQ14	U15.Y1	U16.D3	Pass	Slow	867.1	66.3	67.9	110.2	0.312	6.767	1.345	6.944	108.514	157.8	380.0	400.0	0.068	0.070	0.010	0.010
26	DDR_DQ15	U15.W1	U16.D7	Pass	Slow	867.1	68.4	70.2	113.0	0.357	6.791	1.427	6.850	113.581	163.8	388.2	400.0	0.068	0.070	0.010	0.010
27	DDR_DQ2	U15.E3	U16.H3	Pass	Slow	867.1	69.3	71.5	105.8	0.462	6.804	1.556	6.555	128.915	166.4	382.4	400.0	0.067	0.070	0.010	0.010
28	DDR_DQ3	U15.F3	U16.H7	Pass	Slow	867.1	70.6	73.0	106.9	0.429	6.802	1.398	6.762	121.987	162.4	383.7	400.0	0.067	0.070	0.010	0.010
29	DDR_DQ4	U15.F1	U16.H2	Pass	Slow	867.1	66.5	66.7	110.0	0.288	6.931	1.300	6.858	111.493	156.6	377.9	400.0	0.067	0.070	0.010	0.010
30	DDR_DQ5	U15.G5	U16.H8	Pass	Slow	867.1	66.9	69.4	106.9	0.457	6.893	1.583	6.613	119.754	166.4	386.5	400.0	0.068	0.070	0.010	0.010

	Signal/Controller/DRAM			Status	Corner		Setup	Hold	Pulse Width	Min Slew Rate	Max Slew Rate	Min Slew Rate 2	Max Slew Rate 2	Voltage Margin between Signal and Eye-Mask	Peak Voltage	Overshoot	Undershoot	Overshoot Area	Undershoot Area	Overshoot Area 2	Undershoot Area 2
#	Signal	Driving Controller.Pin	Receiving DRAM.Pin	Pass/Fail	Case	Reference voltage used [mV]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [V/ns]	Margin [V/ns]	Margin [V/ns]	Margin [V/ns]	Margin [mV]	Above/Below Reference Voltage Margin [mV]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Margin [V*ns]	Margin [V*ns]
31	DDR_DQ6	U15.G2	U16.J3	Pass	Slow	867.1	65.8	66.6	104.4	0.235	6.840	1.055	6.784	98.768	155.6	376.6	400.0	0.067	0.070	0.010	0.010
32	DDR_DQ7	U15.F2	U16.J7	Pass	Slow	867.1	63.3	65.9	101.8	0.298	6.875	1.230	6.767	104.479	157.6	377.9	400.0	0.067	0.070	0.010	0.010
33	DDR_DQ8	U15.U1	U16.A3	Pass	Slow	867.1	67.4	67.5	107.1	0.322	6.835	1.371	6.918	104.147	151.2	382.1	400.0	0.068	0.070	0.010	0.010
34	DDR_DQ9	U15.U3	U16.B8	Pass	Slow	867.1	67.8	70.2	107.0	0.384	6.810	1.449	6.669	124.227	160.3	372.7	400.0	0.067	0.070	0.010	0.010
35	DDR_LDMN	U15.H5	U16.E7	Pass	Slow	867.1	70.5	71.4	111.3	0.407	6.826	1.313	6.593	109.214	161.7	379.7	400.0	0.067	0.070	0.010	0.010
36	DDR_UDMN	U15.W5	U16.E2	Pass	Slow	867.1	71.5	72.3	111.9	0.446	6.724	1.438	6.789	114.085	161.3	380.9	400.0	0.068	0.070	0.010	0.010
37	DDR_DQ0	U15.F4	U16.G2	Pass	Fast	964.7	82.5	82.5	105.7	0.904	4.612	1.045	5.905	138.948	176.1	388.6	400.0	0.069	0.070	0.010	0.010
38	DDR_DQ1	U15.H6	U16.F7	Pass	Fast	964.7	79.5	81.2	107.9	0.798	4.343	0.826	5.741	145.329	187.0	383.5	400.0	0.069	0.070	0.010	0.010
39	DDR_DQ10	U15.U2	U16.C3	Pass	Fast	964.7	77.4	78.1	107.7	0.818	6.060	1.117	6.707	146.949	197.5	386.7	400.0	0.069	0.070	0.010	0.010
40	DDR_DQ11	U15.V5	U16.C7	Pass	Fast	964.7	82.1	81.3	107.7	1.123	5.094	1.148	6.241	123.969	177.0	389.0	400.0	0.070	0.070	0.010	0.010
41	DDR_DQ12	U15.W2	U16.C2	Pass	Fast	964.7	76.9	78.1	109.1	0.830	6.192	1.496	6.381	150.910	198.9	390.3	400.0	0.069	0.070	0.010	0.010
42	DDR_DQ13	U15.V6	U16.C8	Pass	Fast	964.7	84.2	83.5	104.1	1.157	5.114	1.189	6.206	127.859	177.2	391.6	400.0	0.070	0.070	0.010	0.010
43	DDR_DQ14	U15.Y1	U16.D3	Pass	Fast	964.7	83.3	81.9	108.5	0.876	5.695	1.445	6.524	150.383	198.9	389.5	400.0	0.069	0.070	0.010	0.010
44	DDR_DQ15	U15.W1	U16.D7	Pass	Fast	964.7	81.3	81.8	108.9	0.981	6.123	1.612	6.210	149.597	193.1	391.1	400.0	0.070	0.070	0.010	0.010
45	DDR_DQ2	U15.E3	U16.H3	Pass	Fast	964.7	84.5	83.4	105.7	1.002	4.976	1.326	6.065	146.733	182.7	389.8	400.0	0.070	0.070	0.010	0.010
46	DDR_DQ3	U15.F3	U16.H7	Pass	Fast	964.7	85.8	86.4	105.5	1.138	4.023	0.878	4.994	137.193	179.4	383.1	400.0	0.069	0.070	0.010	0.010
47	DDR_DQ4	U15.F1	U16.H2	Pass	Fast	964.7	80.5	81.5	108.1	0.903	5.269	1.148	6.375	153.684	192.7	385.0	400.0	0.069	0.070	0.010	0.010
48	DDR_DQ5	U15.G5	U16.H8	Pass	Fast	964.7	82.6	83.7	107.6	0.954	4.440	0.975	5.643	137.396	176.7	389.3	400.0	0.069	0.070	0.010	0.010
49	DDR_DQ6	U15.G2	U16.J3	Pass	Fast	964.7	79.3	79.8	107.3	0.844	5.292	1.033	6.357	156.212	203.1	378.7	400.0	0.068	0.070	0.010	0.010
50	DDR_DQ7	U15.F2	U16.J7	Pass	Fast	964.7	79.9	80.3	105.5	0.917	5.977	1.195	6.077	155.470	201.7	382.8	400.0	0.069	0.070	0.010	0.010
51	DDR_DQ8	U15.U1	U16.A3	Pass	Fast	964.7	77.0	80.8	110.1	0.755	6.079	1.174	6.604	151.122	203.0	390.7	400.0	0.069	0.070	0.010	0.010
52	DDR_DQ9	U15.U3	U16.B8	Pass	Fast	964.7	80.8	82.7	106.0	1.104	5.039	1.169	6.066	124.842	175.8	388.6	400.0	0.069	0.070	0.010	0.010
53	DDR_LDMN	U15.H5	U16.E7	Pass	Fast	964.7	79.6	79.2	109.2	0.824	4.557	0.879	6.054	151.471	188.7	382.4	400.0	0.069	0.070	0.010	0.010
54	DDR_UDMN	U15.W5	U16.E2	Pass	Fast	964.7	82.6	80.4	107.6	1.008	5.069	0.875	6.446	134.555	186.8	387.2	400.0	0.069	0.070	0.010	0.010

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#	Signal/DRAM/Controller			Status	Corner	Reference Voltage Used [mV]	Setup	Hold	Pulse Width
	Signal	Driving DRAM.Pin	Receiving Controller.Pin	Pass/Fail	Case		Margin [ps]	Margin [ps]	Margin [ps]
1	DDR_DQ0	U16.G2	U15.F4	Pass	Typ	890.3	99.1	99.1	N/A
2	DDR_DQ1	U16.F7	U15.H6	Pass	Typ	890.3	98.800	100.300	N/A
3	DDR_DQ10	U16.C3	U15.U2	Pass	Typ	889.7	96.300	96.5	N/A
4	DDR_DQ11	U16.C7	U15.V5	Pass	Typ	889.7	100.800	100.800	N/A
5	DDR_DQ12	U16.C2	U15.W2	Pass	Typ	889.7	97.700	96.800	N/A
6	DDR_DQ13	U16.C8	U15.V6	Pass	Typ	889.7	101.700	99.300	N/A
7	DDR_DQ14	U16.D3	U15.Y1	Pass	Typ	889.7	98.300	98.0	N/A
8	DDR_DQ15	U16.D7	U15.W1	Pass	Typ	889.7	98.1	98.300	N/A
9	DDR_DQ2	U16.H3	U15.E3	Pass	Typ	890.3	98.9	98.800	N/A
10	DDR_DQ3	U16.H7	U15.F3	Pass	Typ	890.3	99.4	98.200	N/A
11	DDR_DQ4	U16.H2	U15.F1	Pass	Typ	890.3	96.9	95.300	N/A
12	DDR_DQ5	U16.H8	U15.G5	Pass	Typ	890.3	97.800	100.1	N/A
13	DDR_DQ6	U16.J3	U15.G2	Pass	Typ	890.3	94.200	93.600	N/A
14	DDR_DQ7	U16.J7	U15.F2	Pass	Typ	890.3	94.1	98.1	N/A
15	DDR_DQ8	U16.A3	U15.U1	Pass	Typ	889.7	97.700	97.0	N/A
16	DDR_DQ9	U16.B8	U15.U3	Pass	Typ	889.7	100.5	101.800	N/A
17	DDR_DQ0	U16.G2	U15.F4	Pass	Slow	858.3	89.600	90.4	N/A
18	DDR_DQ1	U16.F7	U15.H6	Pass	Slow	858.3	89.4	89.9	N/A
19	DDR_DQ10	U16.C3	U15.U2	Pass	Slow	857.0	84.100	82.5	N/A
20	DDR_DQ11	U16.C7	U15.V5	Pass	Slow	857.0	85.800	84.5	N/A
21	DDR_DQ12	U16.C2	U15.W2	Pass	Slow	857.0	83.100	82.800	N/A
22	DDR_DQ13	U16.C8	U15.V6	Pass	Slow	857.0	87.5	86.5	N/A
23	DDR_DQ14	U16.D3	U15.Y1	Pass	Slow	857.0	84.7	84.300	N/A
24	DDR_DQ15	U16.D7	U15.W1	Pass	Slow	857.0	84.7	83.800	N/A
25	DDR_DQ2	U16.H3	U15.E3	Pass	Slow	858.3	90.9	87.9	N/A
26	DDR_DQ3	U16.H7	U15.F3	Pass	Slow	858.3	89.100	90.9	N/A
27	DDR_DQ4	U16.H2	U15.F1	Pass	Slow	858.3	87.2	86.7	N/A
28	DDR_DQ5	U16.H8	U15.G5	Pass	Slow	858.3	90.0	91.7	N/A
29	DDR_DQ6	U16.J3	U15.G2	Pass	Slow	858.3	89.100	88.300	N/A
30	DDR_DQ7	U16.J7	U15.F2	Pass	Slow	858.3	87.2	86.300	N/A
31	DDR_DQ8	U16.A3	U15.U1	Pass	Slow	857.0	83.4	82.600	N/A
32	DDR_DQ9	U16.B8	U15.U3	Pass	Slow	857.0	87.4	83.600	N/A
33	DDR_DQ0	U16.G2	U15.F4	Pass	Fast	905.3	104.6	105.300	N/A
34	DDR_DQ1	U16.F7	U15.H6	Pass	Fast	905.3	103.200	102.9	N/A
35	DDR_DQ10	U16.C3	U15.U2	Pass	Fast	905.3	99.5	99.6	N/A
36	DDR_DQ11	U16.C7	U15.V5	Pass	Fast	905.3	101.800	105.700	N/A
37	DDR_DQ12	U16.C2	U15.W2	Pass	Fast	905.3	98.5	106.0	N/A

	Signal/DRAM/Controller			Status	Corner		Setup	Hold	Pulse Width
#	Signal	Driving DRAM.Pin	Receiving Controller.Pin	Pass/Fail	Case	Reference Voltage Used [mV]	Margin [ps]	Margin [ps]	Margin [ps]
38	DDR_DQ13	U16.C8	U15.V6	Pass	Fast	905.3	103.9	98.300	N/A
39	DDR_DQ14	U16.D3	U15.Y1	Pass	Fast	905.3	101.200	103.4	N/A
40	DDR_DQ15	U16.D7	U15.W1	Pass	Fast	905.3	101.6	100.200	N/A
41	DDR_DQ2	U16.H3	U15.E3	Pass	Fast	905.3	104.9	105.800	N/A
42	DDR_DQ3	U16.H7	U15.F3	Pass	Fast	905.3	104.300	105.200	N/A
43	DDR_DQ4	U16.H2	U15.F1	Pass	Fast	905.3	101.700	100.4	N/A
44	DDR_DQ5	U16.H8	U15.G5	Pass	Fast	905.3	105.800	105.300	N/A
45	DDR_DQ6	U16.J3	U15.G2	Pass	Fast	905.3	99.0	97.4	N/A
46	DDR_DQ7	U16.J7	U15.F2	Pass	Fast	905.3	99.700	100.200	N/A
47	DDR_DQ8	U16.A3	U15.U1	Pass	Fast	905.3	100.700	98.5	N/A
48	DDR_DQ9	U16.B8	U15.U3	Pass	Fast	905.3	102.4	104.5	N/A

Address

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#	Signal/Dram		Status	Corner	Setup	Hold	Overshoot	Undershoot	Overshoot Area	Undershoot Area	Overshoot Area 2	Undershoot Area 2
	Signal	Accessed DRAM	Pass/Fail	Case	Margin [ps]	Margin [ps]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Margin [V*ns]	Margin [V*ns]
1	DDR_A0	U16.P3	Pass	Typ	94.000	199.200	263.3	255.4	0.167	0.172	0.005	N/A
2	DDR_A1	U16.P7	Pass	Typ	82.800	203.400	258.9	239.7	0.165	0.170	0.005	N/A
3	DDR_A10	U16.M3	Pass	Typ	94.500	186.900	251.0	248.2	0.165	0.172	0.005	N/A
4	DDR_A11	U16.T2	Pass	Typ	76.3	191.0	253.5	252.5	0.166	0.171	0.005	N/A
5	DDR_A12	U16.M7	Pass	Typ	94.2	193.5	261.3	258.8	0.166	0.172	0.005	N/A
6	DDR_A13	U16.T8	Pass	Typ	81.1	200.5	254.8	246.5	0.166	0.172	0.005	N/A
7	DDR_A14_WEN	U16.L2	Pass	Typ	96.000	191.800	249.1	252.7	0.165	0.173	0.005	N/A
8	DDR_A15_CASN	U16.M8	Pass	Typ	96.500	183.100	259.6	249.5	0.166	0.171	0.005	N/A
9	DDR_A16_RASN	U16.L8	Pass	Typ	87.9	205.3	204.6	202.0	0.162	0.167	0.005	N/A
10	DDR_A2	U16.R3	Pass	Typ	87.0	206.4	254.4	253.4	0.166	0.171	0.005	N/A
11	DDR_A3	U16.N7	Pass	Typ	96.1	183.8	258.4	255.1	0.166	0.172	0.005	N/A
12	DDR_A4	U16.N3	Pass	Typ	92.3	186.600	256.7	256.0	0.166	0.172	0.005	N/A
13	DDR_A5	U16.P8	Pass	Typ	86.900	208.0	248.3	246.9	0.165	0.172	0.005	N/A
14	DDR_A6	U16.P2	Pass	Typ	86.6	201.100	248.3	242.5	0.165	0.171	0.005	N/A
15	DDR_A7	U16.R8	Pass	Typ	83.200	210.400	259.5	238.0	0.165	0.172	0.005	N/A
16	DDR_A8	U16.R2	Pass	Typ	82.500	202.100	249.0	239.9	0.166	0.170	0.005	N/A
17	DDR_A9	U16.R7	Pass	Typ	88.7	189.800	257.8	258.3	0.166	0.172	0.005	N/A
18	DDR_ACTN	U16.L3	Pass	Typ	121.400	165.700	243.6	201.8	0.164	0.166	0.005	N/A
19	DDR_BA0	U16.N2	Pass	Typ	94.300	208.000	213.1	215.9	0.163	0.168	0.005	N/A
20	DDR_BA1	U16.N8	Pass	Typ	87.800	208.500	234.3	222.2	0.162	0.169	0.005	N/A
21	DDR_BG0	U16.M2	Pass	Typ	94.800	185.800	248.1	254.9	0.166	0.172	0.005	N/A
22	DDR_CKE	U16.K2	Pass	Typ	112.700	172.500	300.0	231.9	0.170	0.170	0.005	N/A
23	DDR_CSN	U16.L7	Pass	Typ	130.3	168.6	236.3	246.8	0.164	0.172	0.005	N/A
24	DDR_ODT	U16.K3	Pass	Typ	130.600	167.200	231.9	236.2	0.163	0.172	0.005	N/A
25	DDR_PARITY	U16.T3	Pass	Typ	115.8	170.000	224.3	207.0	0.161	0.167	0.005	N/A
26	DDR_A0	U16.P3	Pass	Slow	84.800	219.8	253.1	251.7	0.165	0.172	0.005	N/A
27	DDR_A1	U16.P7	Pass	Slow	82.9	224.000	250.3	258.5	0.163	0.173	0.005	N/A
28	DDR_A10	U16.M3	Pass	Slow	88.100	201.6	257.3	249.1	0.164	0.172	0.005	N/A
29	DDR_A11	U16.T2	Pass	Slow	77.1	217.100	276.6	276.1	0.168	0.174	0.005	N/A
30	DDR_A12	U16.M7	Pass	Slow	93.2	226.4	255.6	248.6	0.165	0.172	0.005	N/A
31	DDR_A13	U16.T8	Pass	Slow	71.300	218.000	270.7	264.0	0.168	0.174	0.005	N/A
32	DDR_A14_WEN	U16.L2	Pass	Slow	88.4	202.700	249.7	253.5	0.164	0.172	0.005	N/A
33	DDR_A15_CASN	U16.M8	Pass	Slow	90.900	207.500	252.2	249.1	0.165	0.172	0.005	N/A
34	DDR_A16_RASN	U16.L8	Pass	Slow	88.8	211.400	244.6	247.0	0.165	0.171	0.005	N/A
35	DDR_A2	U16.R3	Pass	Slow	84.400	219.100	245.2	247.7	0.164	0.172	0.005	N/A
36	DDR_A3	U16.N7	Pass	Slow	87.900	208.600	259.7	266.2	0.167	0.174	0.005	N/A
37	DDR_A4	U16.N3	Pass	Slow	87.2	204.500	267.1	258.4	0.167	0.173	0.005	N/A

	Signal/Dram		Status	Corner	Setup	Hold	Overshoot	Undershoot	Overshoot Area	Undershoot Area	Overshoot Area 2	Undershoot Area 2
#	Signal	Accessed DRAM	Pass/Fail	Case	Margin [ps]	Margin [ps]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Margin [V*ns]	Margin [V*ns]
38	DDR_A5	U16.P8	Pass	Slow	81.5	212.300	255.6	240.4	0.164	0.172	0.005	N/A
39	DDR_A6	U16.P2	Pass	Slow	80.500	207.9	246.9	262.3	0.165	0.174	0.005	N/A
40	DDR_A7	U16.R8	Pass	Slow	75.700	216.4	261.1	259.2	0.165	0.173	0.005	N/A
41	DDR_A8	U16.R2	Pass	Slow	76.700	231.900	261.1	247.1	0.165	0.172	0.005	N/A
42	DDR_A9	U16.R7	Pass	Slow	83.9	213.700	262.1	270.5	0.167	0.174	0.005	N/A
43	DDR_ACTN	U16.L3	Pass	Slow	121.2	190.400	202.0	197.6	0.158	0.164	0.005	N/A
44	DDR_BA0	U16.N2	Pass	Slow	84.200	223.7	243.0	256.2	0.163	0.172	0.005	N/A
45	DDR_BA1	U16.N8	Pass	Slow	89.1	224.7	259.4	244.0	0.165	0.169	0.005	N/A
46	DDR_BG0	U16.M2	Pass	Slow	89.800	203.3	247.4	271.7	0.164	0.173	0.005	N/A
47	DDR_CKE	U16.K2	Pass	Slow	110.200	196.2	280.3	223.0	0.169	0.167	0.005	N/A
48	DDR_CSN	U16.L7	Pass	Slow	127.7	190.300	223.7	188.0	0.163	0.165	0.005	N/A
49	DDR_ODT	U16.K3	Pass	Slow	121.900	185.400	220.4	202.0	0.159	0.165	0.005	N/A
50	DDR_PARITY	U16.T3	Pass	Slow	111.700	196.7	218.4	211.8	0.162	0.167	0.005	N/A
51	DDR_A0	U16.P3	Pass	Fast	71.0	140.0	281.3	284.0	0.168	0.175	0.005	N/A
52	DDR_A1	U16.P7	Pass	Fast	74.900	146.5	278.8	268.4	0.163	0.174	0.005	N/A
53	DDR_A10	U16.M3	Pass	Fast	31.100	124.4	266.5	271.9	0.166	0.173	0.005	N/A
54	DDR_A11	U16.T2	Pass	Fast	49.400	134.8	267.6	273.9	0.168	0.174	0.005	N/A
55	DDR_A12	U16.M7	Pass	Fast	63.0	137.8	275.5	259.8	0.167	0.173	0.005	N/A
56	DDR_A13	U16.T8	Pass	Fast	53.700	141.3	281.3	269.6	0.169	0.174	0.005	N/A
57	DDR_A14_WEN	U16.L2	Pass	Fast	69.300	130.1	271.7	274.7	0.167	0.174	0.005	N/A
58	DDR_A15_CASN	U16.M8	Pass	Fast	44.600	124.600	267.2	275.2	0.166	0.174	0.005	N/A
59	DDR_A16_RASN	U16.L8	Pass	Fast	78.0	141.5	254.4	228.4	0.167	0.170	0.005	N/A
60	DDR_A2	U16.R3	Pass	Fast	74.900	145.0	284.0	280.3	0.168	0.175	0.005	N/A
61	DDR_A3	U16.N7	Pass	Fast	30.600	126.400	274.3	273.5	0.168	0.173	0.005	N/A
62	DDR_A4	U16.N3	Pass	Fast	60.400	126.800	300.0	275.3	0.170	0.174	0.005	N/A
63	DDR_A5	U16.P8	Pass	Fast	76.600	145.0	270.0	276.0	0.168	0.174	0.005	N/A
64	DDR_A6	U16.P2	Pass	Fast	66.800	142.200	280.7	282.3	0.169	0.175	0.005	N/A
65	DDR_A7	U16.R8	Pass	Fast	68.300	151.7	271.1	268.3	0.168	0.174	0.005	N/A
66	DDR_A8	U16.R2	Pass	Fast	69.6	145.9	273.2	269.8	0.168	0.174	0.005	N/A
67	DDR_A9	U16.R7	Pass	Fast	55.700	131.7	291.9	276.3	0.169	0.174	0.005	N/A
68	DDR_ACTN	U16.L3	Pass	Fast	116.600	112.800	275.9	264.5	0.168	0.172	0.005	N/A
69	DDR_BA0	U16.N2	Pass	Fast	75.000	150.900	245.0	236.1	0.162	0.171	0.005	N/A
70	DDR_BA1	U16.N8	Pass	Fast	83.3	151.400	254.7	233.2	0.166	0.170	0.005	N/A
71	DDR_BG0	U16.M2	Pass	Fast	34.0	126.500	290.3	274.3	0.169	0.174	0.005	N/A
72	DDR_CKE	U16.K2	Pass	Fast	96.4	128.1	300.0	243.9	0.170	0.172	0.005	N/A
73	DDR_CSN	U16.L7	Pass	Fast	113.9	110.9	282.8	275.9	0.168	0.174	0.005	N/A
74	DDR_ODT	U16.K3	Pass	Fast	116.800	116.0	276.9	268.0	0.168	0.173	0.005	N/A
75	DDR_PARITY	U16.T3	Pass	Fast	101.4	120.500	249.0	255.9	0.166	0.173	0.005	N/A

Differential Nets

Differential Nets Worstcases

- To investigate any result further, click on the link in the cell to open the waveforms. Viewing waveforms requires a valid EZwave license.
- Click on the main header (e.g., "Setup" or "Hold") to view more details about how the margin was derived
- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column

Differential Nets Worstcases

#	Signal/Driver/Receiver				Status	Corner	Overshoot	Undershoot	Overshoot Area	Undershoot Area	Overshoot Area 2	Undershoot Area 2	tDVAC	Vix	
	Signal	Driver.Pins	Receiver.Pins	Operation											
1	DDR_CKP	U15.L1&L2	U16.K7&K8	Write rank(1,1)	Pass	Typ	300.0	300.0	0.075	0.076	0.003	N/A	122	71.3	Pass
2	DDR_LDQS_P	U16.G3&F3	U15.E1&E2	Read rank(1,1)	Pass	Typ	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
3	DDR_LDQS_P	U15.E1&E2	U16.G3&F3	Write rank(1,1)	Pass	Typ	400.0	400.0	0.070	0.070	0.010	0.010	N/A	123.6	N/A
4	DDR_UDQS_P	U16.B7&A7	U15.V1&V2	Read rank(1,1)	Pass	Typ	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
5	DDR_UDQS_P	U15.V1&V2	U16.B7&A7	Write rank(1,1)	Pass	Typ	386.1	400.0	0.069	0.070	0.010	0.010	N/A	122.5	N/A
6	DDR_CKP	U15.L1&L2	U16.K7&K8	Write rank(1,1)	Pass	Slow	300.0	300.0	0.075	0.076	0.003	N/A	114	84.1	Pass
7	DDR_LDQS_P	U16.G3&F3	U15.E1&E2	Read rank(1,1)	Pass	Slow	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
8	DDR_LDQS_P	U15.E1&E2	U16.G3&F3	Write rank(1,1)	Pass	Slow	388.5	400.0	0.070	0.070	0.010	0.010	N/A	115.7	N/A
9	DDR_UDQS_P	U16.B7&A7	U15.V1&V2	Read rank(1,1)	Pass	Slow	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
10	DDR_UDQS_P	U15.V1&V2	U16.B7&A7	Write rank(1,1)	Pass	Slow	388.4	400.0	0.070	0.070	0.010	0.010	N/A	117.2	N/A
11	DDR_CKP	U15.L1&L2	U16.K7&K8	Write rank(1,1)	Pass	Fast	300.0	300.0	0.075	0.076	0.003	N/A	123	45.6	Pass
12	DDR_LDQS_P	U16.G3&F3	U15.E1&E2	Read rank(1,1)	Pass	Fast	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
13	DDR_LDQS_P	U15.E1&E2	U16.G3&F3	Write rank(1,1)	Pass	Fast	400.0	400.0	0.070	0.070	0.010	0.010	N/A	100.3	N/A
14	DDR_UDQS_P	U16.B7&A7	U15.V1&V2	Read rank(1,1)	Pass	Fast	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
15	DDR_UDQS_P	U15.V1&V2	U16.B7&A7	Write rank(1,1)	Pass	Fast	400.0	400.0	0.070	0.070	0.010	0.010	N/A	116.6	N/A

CLK-DQS Skew

CLK-DQS Skew Worstcases

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- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column

CLK-DQS Skew Worstcases

#	Signal/Dram				Status	Corner	DQSS - Earliest DQS	DQSS - Latest DQS	tDSS	tDSH
	Signal	Accessed DRAM	DRAM CLK Pins	DRAM DQS Pins	Pass/Fail	Case	Margin [ps]	Margin [ps]	Margin [ps]	Margin [ps]
1	DDR_LDQS_P	U16	K7&K8	G3&F3	Pass	Typ	160.2	149.0	185.1	192.3
2	DDR_UDQS_P	U16	K7&K8	B7&A7	Pass	Typ	161.7	151.8	188.7	193.6
3	DDR_LDQS_P	U16	K7&K8	G3&F3	Pass	Slow	161.7	160.5	190.9	187.5
4	DDR_UDQS_P	U16	K7&K8	B7&A7	Pass	Slow	153.2	161.5	192.0	182.6
5	DDR_LDQS_P	U16	K7&K8	G3&F3	Pass	Fast	160.7	160.7	191.2	188.3
6	DDR_UDQS_P	U16	K7&K8	B7&A7	Pass	Fast	160.8	157.3	190.7	188.8

Eye Density Links

Eye Density Links

Eye Density Links

#	Eye Density Links	Data/Address	Case
1	Load Eye Density Plots	Data	Typ
2	Load Eye Density Plots	Data	Slow
3	Load Eye Density Plots	Data	Fast

Setup Info

Design: PCB_501-1-04356_A0-67.hyp

VX2.12 build 21158655

Date: May-20-2024 17h-36m

Setup Information

Interface Setup

Parameter	Value
DDR Interface	DDR4
Crosstalk	Disabled
Power-Aware	Disabled
IC Corners	Fast, Typ, Slow
Probing location	Controller - at Die, DRAM - at Pin
Total Run Time	0 Days, 00 Hours, 03 Minutes 43 Seconds

Rank Setup

Rank	Ref. Des.	IBIS File	Component	Timing Model	Speed Grade
Controller	U15	spm766d.ibs	AM62	C:\MentorGraphics\HLVX2.12\SDD_HOME\hyperlynx64\Libs\ddr4_ctl.v	DDR4_3200
Rank[1,1]	U16	z42b_ait.ibs	MT40A1G16TD	C:\MentorGraphics\HLVX2.12\SDD_HOME\hyperlynx64\Libs\ddr4_dram.v	DDR4_3200

IBIS Model Selectors

Rank	CLK	Addr	CTL
Controller	ddr4_ocd_60p_60n_diff	ddr4_ocd_60p_60n	ddr4_ocd_60p_60n
No Data	No Data	No Data	No Data

ODT - Write to Slot 1

Rank	DQS	DQ	DM
Controller	ddr4_ocd_60p_60n_diff,	ddr4_ocd_60p_60n,	ddr4_ocd_60p_60n,
Rank[1,1]	DQS_IN_ODT48_3200	DQ_IN_ODT48_3200	DM_ODT48_3200

ODT - Read from Slot 1

Rank	DQS	DQ	DM
Controller	ddr4_odt_48_diff,	ddr4_odt_48,	ddr4_odt_48,
Rank[1,1]	DQS_48_3200	DQ_48_3200	DQ_48_3200