FAE Alert: If Unsuitable PLL Settings are Chosen, Synthesized Clocks May Exceed VCO and SOC Fmax Limits

Devices affected:

TMS320DM816x and AM389x

Revisions affected:

All

Speed Grades Affected:

All

Problem Summary:

This device uses FAPLLs to generate the clocks needed by the various processing elements and interfaces. FAPLLs contain an analog PLL and a Flying Adder digital clock synthesizer. This allows generation of arbitrary frequencies through programming. The resulting synthesized clocks contain some period jitter. Fmax of the processing elements must account for the minimum period of the synthesized clock and not the average period of the synthesized clock.

Customers must choose FAPLL settings according to the minimum cycle period. This Alert provides new information designed to reinforce guidelines in the Datasheet and Technical Reference Manual so customers avoid inadvertently clocking various processing elements beyond their rated frequencies. Additionally, RDK and EZSDK reference software contains revised settings consistent with these guidelines.

Detailed Description:

Background Information:

This device is a complex video processing SOC containing many independent processing elements, accelerators and interfaces. A network of clock generators is needed to provide many different clock frequencies all from a single 27MHz crystal oscillator input. Flying Adder PLLs (FAPLLs) are frequency synthesizers that can be programmed to generate a wide range of frequencies.

FAPLL synthesizers use a multi-phase PLL to generate clocks that are edge aligned. This is achieved by dithering the clock period to force this alignment. Clock period dithering results in clock jitter. Since FAPLLs have flexible programming, some choices result in more clock jitter than others.

FAPLL Issue #1:

In synchronous SOC timing closure, maximum operating rate, Fmax, is limited by the maximum setup time, Tsu, between synchronous logic elements plus all asynchronous logic and routing delays. Use of the term Fmax assumes that the clock has a constant period. This implies Fmax=1/Tclk(nom). However, in systems that use a synthesized clock containing period jitter, the Fmax rating is the maximum instantaneous clock rate which is due to the minimum clock period. This can be restated as Fmax=1/Tclk(min).

FAPLL configuration examples in previous versions of the Datasheet (DS) and Technical Reference Manual (TRM) and sample software in the RDK and EZSDK use the average frequency from the FAPLL synthesizers in most cases. It must be noted, however, that the minimum clock period is the limiting factor

The following table is a revised Table 8-13, PLL Clock Minimum Cycle. It lists all of the clocks generated by the FAPLLs within the device.

Table 8-13. PLL Clock Minimum Cycle Period

CLOCK	DEVICE SPEED RANGE(1)	MIN CYCLE (ps)
Main PLL		
Clock 1	Blank	1250
	2	1000
	4	889
Clock 2	Blank	1000
	2	833
	4	741
Clock 3	Blank	1876
	2	1667
	4	1481
Clock 4	Blank	2000
	2	1786
	4	1667
DDR PLL		
Clock 2	Blank, 2, 4	18519
Clock 3	Blank	2632
	2	2632
	4	2222
Video PLL		
Clock 1	Blank, 2, 4	1515
Clock 2	Blank, 2, 4	1515
Clock 3	Blank, 2, 4	1515
Audio PLL		
Clock 2	Blank, 2, 4	6329
Clock 3	Blank, 2, 4	5076
Clock 4	Blank, 2, 4	5076
Clock 5	Blank, 2, 4	5076

(1) For more information on the available device speed ranges for each part number, see Table 10-1 in the Datasheet

Note: Some early versions of silicon were shipped with speed ratings different than shown in the latest Datasheet tables. Please refer to the documentation provided at the time of purchase for the maximum rated speeds of the clocks within those devices.

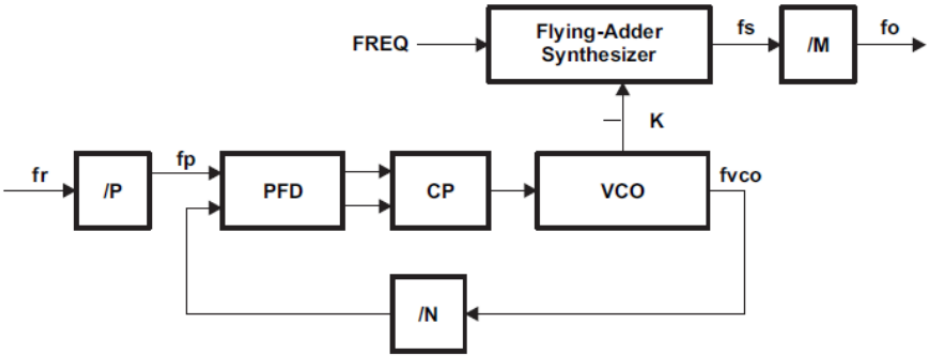
FAPLL Issue #2:

The analog VCO contained in the FAPLLs implemented in this device are rated for a maximum speed of 1600MHz. EZSDK code and older versions of the RDK code contain configurations operating the VCO at 1728MHz. This is the result of using a reference clock input of 27MHz and a PLL multiplier (PLL_N) of 64. More recent versions of the RDK code now use a PLL multiplier of 56 which operates the VCO within its rated range.

Configuration examples in the TRM recommend VCO operation at 1593MHz which is also within the rated range of the VCO. However, 1593MHz cannot be used if USB is a system requirement. The required 24 MHz USB frequency cannot be derived from a VCO rate of 1593MHz.

FAPLL Operation:

The flying-adder PLL has two main components: a multi-phase PLL and the flying-adder synthesizer. The multi-phase PLL takes an input reference clock (fr), multiplies it with factor, N, and provides a K-phase output to the flying-adder synthesizer. The flying-adder synthesizer takes this multi-phase clock input and produces a variable frequency clock (fs). There can be a post divider on this clock which takes in clock fs and drives out clock fo.



The frequency of the clock driven out, fo, is given by:

$$\mathbf{fo} = \left[\frac{(\mathbf{N} * \mathbf{K})}{(\mathbf{M} * \mathbf{FREQ} * \mathbf{P})}\right] * \mathbf{fr} = \mathbf{F_{avg}}$$

The output fo is the nominal or average frequency generated by the PLL and Flying Adder Synthesizer combination. This can also be called Favg.

There can be multiple flying-adder synthesizers attached to one multi-phase PLL to generate separate clocks at different frequencies. In this case, FREQ (4 bits of integer and 24 bits of fractional value) and M (1 to 255) values can be adjusted for each clock separately, based on the frequency needed. The multi-phase PLL used in this device has a value of K = 8.

The PLL and Flying Adder synthesizers support generation of a wide range of clocks that are all generated from the same input clock source. Therefore, these clocks are all synchronous. The flying-adder synthesizers take the multi-phase clock from the PLL and produce variable frequency clocks (fs) as stated above. Each variable frequency clock is then divided by a post divider before use.

The clock outputs from the PLL, synthesizer and post divider contain period variations that must be considered. They result in clock period jitter. The minimum period of the generated clock defines the maximum instantaneous clock rate.

$$\mathbf{F_{Max}} = \frac{\mathbf{1}}{\mathbf{Minimum\ Clock\ Period}}$$

Different configurations of the PLL dividers, synthesizer and output dividers will have larger or smaller amounts of phase variation. The equation below will calculate the minimum cycle period for a provided configuration. The result of the minimum cycle equation must be greater than the 1/Fmax for the processing element that it drives.

$$\textbf{Minimum Clock Period} = \left(\frac{\textbf{Floor}(\textbf{M} * \textbf{FREQ}) * \textbf{P} * \textbf{10}^{\textbf{6}}}{\textbf{PLL\_CLKIN} * \textbf{8} * \textbf{N}}\right) - \sqrt{\frac{\textbf{A} * \textbf{M} * \textbf{FREQ}}{\textbf{8}}} - \textbf{H}$$

The first term of equation is a characteristic of the Flying Adder PLL. The selection of M*FREQ is important. Choosing a non-integer product of M*FREQ will result in larger period variation and a higher peak instantaneous frequency. Use of a non-integer M*FREQ product can be done to create a specific average frequency at the cost of higher phase variation. Using integer values of the product M*FREQ+ or at least a value that has a small fractional part will result in minimum phase variation. The second and third terms are PLL phase jitter terms associated with the frequency synthesis. The second term is about 20ps and the third is normally 10ps. They are the only phase jitter terms when M*FREQ is selected as an integer.

Example:

Recent versions of the RDK software contain a revised value for SYSCLK5. Speed grade 2 devices are rated to operate SYSCLK5 at a maximum speed of 280MHz. Recent versions of the RDK software configure SYSCLK5 for Speed Grade 2 devices for a nominal frequency of 274.9MHz. This configuration does not exceed the device rating for the minimum clock cycle and it is the optimum setting. The minimum clock cycle is 1787ps which results in a maximum instantaneous clock rate of 279.7MHz (after a divide by 2). The table below shows the calculations and the intermediate terms.

The table below also shows in the last column the configuration contained in the prior software release that provided an average clock of 280MHz. However, the minimum cycle period due to jitter is 1705ps which equates to a maximum instantaneous clock rate of 293.3MHz. This maximum instantaneous clock rate exceeds the operating limits for circuitry driven by SYSCLK5.

Parameter	Latest Settings	Prior Configuration
M	2	2
FREQ	11	10.8
Floor(M*FREQ)	22	21
P	1	1
PLL_CLKIN (MHz)	27	27
N	56	56
fo (MHz)	549.8	560
fo/2 (MHz)	274.9	280
A (constant value of 169 for the Main PLL)	169	169
First term in minimum cycle equation (ps)	1818.7	1736.1
Second term in minimum cycle equation (ps)	21.5	21.3
Third term in minimum cycle equation (ps)	10.0	10.0
Minimum clock period (ps)	1787.2	1704.7
Maximum SYSCLK4 frequency (MHz)	559.5	586.6
Maximum SYSCLK5 frequency (MHz)	279.7	293.3

Impact of Minimum Cycle Violation:

Operation of the FAPLL VCO above the maximum rated frequency is not characterized and may lead to unpredictable results. Similarly, operation of processing elements with clocks that exceed the minimum clock period due to clock period jitter may lead to unpredictable results.

Solution:

In order to comply with device specifications, new production units need to contain revised software that operates the device within its rated limits. The PLL configuration is contained in UBOOT in the RDK and EZSDK sample software. Fielded units that can be upgraded with new software should be loaded with new configurations.

Patch files for the RDK code base are available on the external Arago tree under the dvrrdk_uboot_int_branch at: http://arago-project.org/git/projects/?p=u-boot-dvr-rdk-dm81xx.git;a=commit;h=84808db76d9f5f830d07a653a9a2b55261af38d4.

The TRM contains tables that contain FAPLL configuration settings that generate the maximum allowable clock speeds that are within the rated minimum cycle limits. These tables are copied below. The configurations shown have been tested for all three speed grades.

Table 1-77. Example for Main PLL Frequencies for Speed Grade Blank

Input Ref Freq	Pre-Divider	Mult	VCO Output Freq	4 Bits Integer	24 Bits Fract	FAPLL Output	Post Divider	Post Divider Output		PRCM Divider		System Clock Domain	SYSCLK Freq (MHz)
								Mean[1]	Max[2]				
f_r (MHz)	P[3]	N[3]	f_{vco} (MHz)	FREQ[3]		f_s (MHz)	M[3]	f_o (MHz)					
27	1	56	1512	8	0	1512	2	756	767	1		SYSCLK1	756
				13	0	930	1	930	954	1		SYSCLK2	930
										3		SYSCLK23	310
				12	0	1008	2	504	510	1		SYSCLK3	504
				13	0	930	2	465	473	1		SYSCLK4	465
										1	2	SYSCLK5	233
										1	4	SYSCLK6	116
										1	5	SYSCLK7	93
				12	0.096	1000	8	125	127	1		SYSCLK24	125

(1) Mean frequency is an average FAPLL output frequency over time when P, N, M, and FREQ are tuned.
(2) Maximum frequency is an instantaneous frequency when FAPLL generates clock at minimum clock cycle.
(3) The values of Pre-Divider (P), Multiplier (N), FREQ, and Post Divider (M) can be tuned in order to obtain different frequencies; however, the software must respect the limitations (and requirements) described in the device-specific data manual for PLL Programming Limits.

Table 1-78. Example for Main PLL Frequencies for Speed Grade 2

Input Ref Freq	Pre-Divider	Mult	VCO Output Freq	4 Bits Integer	24 Bits Fract	FAPLL Output	Post Divider	Post Divider Output		PRCM Divider		System Clock Domain	SYSCLK Freq (MHz)
								Mean[1]	Max[2]				
f_r (MHz)	P[3]	N[3]	f_{vco} (MHz)	FREQ[3]		f_s (MHz)	M[3]	f_o (MHz)					
27	1	56	1512	13	0	930	1	930	954	1		SYSCLK1	930
				11	0	1100	1	1100	1131	1		SYSCLK2	1100
										4		SYSCLK23	275
				11	0	1100	2	550	560	1		SYSCLK3	550
				11	0	1100	2	550	560	1		SYSCLK4	550
										1	2	SYSCLK5	275
										1	4	SYSCLK6	138
										1	5	SYSCLK7	110
				12	0.096	1000	8	125	127	1		SYSCLK24	125

(1) Mean frequency is an average FAPLL output frequency over time when P, N, M, and FREQ are tuned.
(2) Maximum frequency is an instantaneous frequency when FAPLL generates clock at minimum clock cycle.
(3) The values of Pre-Divider (P), Multiplier (N), FREQ, and Post Divider (M) can be tuned in order to obtain different frequencies; however, the software must respect the limitations (and requirements) described in the device-specific data manual for PLL Programming Limits.

Table 1-79. Example for Main PLL Frequencies for Speed Grade 4

Input Ref Freq	Pre-Divider	Mult	VCO Output Freq	4 Bits Integer	24 Bits Fract	FAPLL Output	Post Divider	Post Divider Output		PRCM Divider		System Clock Domain	SYSCLK Freq (MHz)
								Mean[1]	Max[2]				
f_r (MHz)	P[3]	N[3]	f_{vco} (MHz)	FREQ[3]		f_s (MHz)	M[3]	f_o (MHz)					
27	1	56	1512	12	0	1008	1	1008	1035	1		SYSCLK1	1008
				10	0	1210	1	1210	1247	1		SYSCLK2	1210
										4		SYSCLK23	303
				9	0.5	1273	2	637	649	1		SYSCLK3	637
				10	0.5	1152	2	576	586	1		SYSCLK4	576
										1	2	SYSCLK5	288
										1	4	SYSCLK6	144
										1	5	SYSCLK7	115
				12	0.096	1000	8	125	127	1		SYSCLK24	125

(1) Mean frequency is an average FAPLL output frequency over time when P, N, M, and FREQ are tuned.
(2) Maximum frequency is an instantaneous frequency when FAPLL generates clock at minimum clock cycle.
(3) The values of Pre-Divider (P), Multiplier (N), FREQ, and Post Divider (M) can be tuned in order to obtain different frequencies; however, the software must respect the limitations (and requirements) described in the device-specific data manual for PLL Programming Limits.

Table 1-83. Example for DDR PLL Frequencies for Speed Grade Blank and Grade 2

Input Ref Freq	Pre-Divider	Mult	VCO Output Freq	4 Bits Integer	24 Bits Fract	FAPLL Output	Post Divider	Post Divider Output		PRCM Divider	System Clock Domain	SYSCLK Freq (MHz)
								Mean[1]	Max[2]			
f_r (MHz)	P[3]	N[3]	f_{vco} (MHz)	FREQ[3]		f_s (MHz)	M[3]	f_o (MHz)				
27	1	59	1593	11	0.666667	1092	3	364	369	1	SYSCLK8	364
				8	0.85	1440	30	48	48	3	SYSCLK9	16
				8	0.85	1440	30	48	48	1	SYSCLK10	48
				NA	NA	NA	2	797	797	NA	DDR External Clock	797
				NA	NA	NA	4	398	398	NA	DDR Clock	398

(1) Mean frequency is an average FAPLL output frequency over time when P, N, M, and FREQ are tuned.
(2) Maximum frequency is an instantaneous frequency when FAPLL generates clock at minimum clock cycle.
(3) The values of Pre-Divider (P), Multiplier (N), FREQ, and Post Divider (M) can be tuned in order to obtain different frequencies; however, the software must respect the limitations (and requirements) described in the device-specific data manual for PLL Programming Limits.

Table 1-84. Example for DDR PLL Frequencies for Speed Grade 4

Input Ref Freq	Pre-Divider	Mult	VCO Output Freq	4 Bits Integer	24 Bits Fract	FAPLL Output	Post Divider	Post Divider Output		PRCM Divider	System Clock Domain	SYSCLK Freq (MHz)
								Mean[1]	Max[2]			
f_r (MHz)	P[3]	N[3]	f_{vco} (MHz)	FREQ[3]		f_s (MHz)	M[3]	f_o (MHz)				
27	1	59	1593	10	0	1274	3	425	431	1	SYSCLK8	425
				8	0.85	1440	30	48	48	3	SYSCLK9	16
				8	0.85	1440	30	48	48	1	SYSCLK10	48
				NA	NA	NA	2	797	797	NA	DDR External Clock	797
				NA	NA	NA	4	398	398	NA	DDR Clock	398

(1) Mean frequency is an average FAPLL output frequency over time when P, N, M, and FREQ are tuned.
(2) Maximum frequency is an instantaneous frequency when FAPLL generates clock at minimum clock cycle.
(3) The values of Pre-Divider (P), Multiplier (N), FREQ, and Post Divider (M) can be tuned in order to obtain different frequencies; however, the software must respect the limitations (and requirements) described in the device-specific data manual for PLL Programming Limits.

Solution Without USB:

The examples above provide valid clocks to all subsystems, including the USB interface. This limits the PLL multiplier N for the Main PLL to 56. In systems which do not use the USB interface; the PLL multiplier N for the Main PLL can be increased to 59. This multiplier runs the PLL at 1593MHz which can provide faster clocks to some subsystems due to the finer granularity but will result in lower clocks to other subsystems. The tables below show the optimum Main PLL programming when not using USB.

Example for Main PLL Frequencies Without USB (Speed Grade Blank)

Input Ref Freq	Pre-Divider	Mult	VCO Output Freq.	4 Bits Integer	24 Bits Fract	Output	Post Divider	Post Divider Output	PRCM Divider		System Clock Domain	SYSCLK Freq. (MHz)
fr (MHz)	P	N	fvco (MHz)	FREQ		fs (MHz)	M	fo (MHz)				
27	1	59	1593	8	0.5	1499	2	750	1		SYSCLK1	750
				14	0	910	1	910	1		SYSCLK2	910
									3		SYSCLK23	303
				12	0	1062	1	1062	1		SYSCLK3	1062
				13	0	980	2	490	1		SYSCLK4	490
									1	2	SYSCLK5	245
									1	4	SYSCLK6	123
									1	5	SYSCLK7	98
				12	0.75	1000	8	125	1		SYSCLK24	125

Example for Main PLL Frequencies Without USB (Speed Grade 2)

Input Ref Freq	Pre-Divider	Mult	VCO Output Freq.	4 Bits Integer	24 Bits Fract	Output	Post Divider	Post Divider Output	PRCM Divider		System Clock Domain	SYSCLK Freq. (MHz)
fr (MHz)	P	N	fvco (MHz)	FREQ		fs (MHz)	M	fo (MHz)				
27	1	59	1593	14	0	910	1	910	1		SYSCLK1	910
				11	0	1159	1	1159	1		SYSCLK2	1159
									4		SYSCLK23	290
				11	0	1159	2	579	1		SYSCLK3	579
				12	0	1062	2	531	1		SYSCLK4	531
									1	2	SYSCLK5	266
									1	4	SYSCLK6	133
									1	5	SYSCLK7	106
				12	0.75	1000	8	125	1		SYSCLK24	125

Example for Main PLL Frequencies Without USB (Speed Grade 4)

Input Ref Freq	Pre-Divider	Mult	VCO Output Freq.	4 Bits Integer	24 Bits Fract	Output	Post Divider	Post Divider Output	PRCM Divider		System Clock Domain	SYSCLK Freq. (MHz)
fr (MHz)	P	N	fvco (MHz)	FREQ		fs (MHz)	M	fo (MHz)				
27	1	59	1593	12	0	1062	1	1062	1		SYSCLK1	1062
				10	0	1274	1	1274	1		SYSCLK2	1274
									4		SYSCLK23	319
				10	0	1274	2	637	1		SYSCLK3	637
				11	0	1159	2	579	1		SYSCLK4	579
									1	2	SYSCLK5	290
									1	4	SYSCLK6	145
									1	5	SYSCLK7	116
				12	0.75	1000	8	125	1		SYSCLK24	125

Performance Impact:

Implementing these configurations will result in clock speed reductions. Due to the granularity available in these configuration options, some clocks will be reduced more than others. The table below highlights the performance reductions.

SYSCLK	Device Speed Range	Max Rated Freq (MHz)	Average Freq (Mhz)	Performance Less than Ideal(%)	Average Freq - No USB (Mhz)	Performance Less than Ideal - No USB (%)
SYSCLK1 (DSP)	Blank	800	756	5.5	750	6.3
	2	**1000**	**930**	**7.0**	910	9.0
	4	1125	1008	10.4	1062	5.6
SYSCLK2 (ARM)	Blank	1000	930	7.0	910	9.0
	2	**1200**	**1100**	**8.4**	1159	3.5
	4	1350	1210	10.4	1274	5.6
SYSCLK3 (HDVICP)	Blank	532	504	5.3	490	7.9
	2	**600**	**550**	**8.4**	579	3.5
	4	675	637	5.7	637	5.7
SYSCLK4 (L3, EDMA)	Blank	500	465	7.0	490	2.0
	2	**560**	**550**	**1.8**	531	5.2
	4	600	576	4.0	579	3.5
SYSCLK5 (M3)	Blank	250	233	7.0	245	2.0
	2	**280**	**275**	**1.8**	266	5.2
	4	300	288	4.0	290	3.5
SYSCLK6 (UART, I2C)	Blank	125	116	7.0	123	2.0
	2	**140**	**137**	**1.8**	133	5.2
	4	150	144	4.0	145	3.5
SYSCLK7	Blank	100	93	7.0	98	2.0
	2	**112**	**110**	**1.8**	106	5.2
	4	120	115	4.0	116	3.5
SYSCLK23 (SGX530)	Blank	333	310	6.9	303	8.9
	2	**300**	**275**	**8.4**	290	3.5
	4	337.5	302	10.4	319	5.6
SYSCLK24 (EMAC)	Blank,2,4	130	125	3.8	125	3.9