root@vdms:~# lspci

00:00.0 PCI bridge: Texas Instruments Device b00f

01:00.0 PCI bridge: Microchip Technology / SMSC Device a048 (rev b0)

02:01.0 PCI bridge: Microchip Technology / SMSC Device a049 (rev b0)

02:02.0 PCI bridge: Microchip Technology / SMSC Device a04a (rev b0)

02:03.0 PCI bridge: Microchip Technology / SMSC Device a04b (rev b0)

02:04.0 PCI bridge: Microchip Technology / SMSC Device a04c (rev b0)

04:00.0 USB controller: Microchip Technology / SMSC Device a040 (rev b0)

05:00.0 Ethernet controller: Microchip Technology / SMSC Device a041 (rev b0)

06:00.0 Serial controller: Microchip Technology / SMSC Device a042 (rev b0)

06:00.1 SMBus: Microchip Technology / SMSC Device a043 (rev b0)

06:00.2 Serial bus controller: Microchip Technology / SMSC Device a044 (rev b0)

06:00.3 Non-Essential Instrumentation [1300]: Microchip Technology / SMSC Device a045 (rev b0)

root@vdms:~# lspci -vv

00:00.0 PCI bridge: Texas Instruments Device b00f (prog-if 00 [Normal decode])

        Control: I/O- Mem+ BusMaster+ SpecCycle- MemWINV- VGASnoop- ParErr- Stepping- SERR- FastB2B- DisINTx+

        Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort+ >SERR- <PERR- INTx-

        Latency: 0

        Interrupt: pin A routed to IRQ 537

        Bus: primary=00, secondary=01, subordinate=06, sec-latency=0

        I/O behind bridge: [disabled]

        Memory behind bridge: 18100000-183fffff [size=3M]

        Prefetchable memory behind bridge: [disabled]

        Secondary status: 66MHz- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort- <SERR- <PERR-

        BridgeCtl: Parity- SERR+ NoISA- VGA- VGA16- MAbort- >Reset- FastB2B-

                PriDiscTmr- SecDiscTmr- DiscTmrStat- DiscTmrSERREn-

        Capabilities: [80] Power Management version 3

                Flags: PMEClk- DSI- D1+ D2- AuxCurrent=0mA PME(D0+,D1+,D2-,D3hot+,D3cold-)

                Status: D0 NoSoftRst+ PME-Enable- DSel=0 DScale=0 PME-

        Capabilities: [90] MSI: Enable+ Count=1/1 Maskable+ 64bit+

                Address: 0000000001000000  Data: 0000

                Masking: 00000000  Pending: 00000000

        Capabilities: [b0] MSI-X: Enable- Count=1 Masked-

                Vector table: BAR=0 offset=00000000

                PBA: BAR=0 offset=00000008

        Capabilities: [c0] Express (v2) Root Port (Slot+), MSI 00

                DevCap: MaxPayload 256 bytes, PhantFunc 0

                        ExtTag- RBE+

                DevCtl: CorrErr+ NonFatalErr+ FatalErr+ UnsupReq+

                        RlxdOrd+ ExtTag- PhantFunc- AuxPwr- NoSnoop+

                        MaxPayload 128 bytes, MaxReadReq 512 bytes

                DevSta: CorrErr- NonFatalErr- FatalErr- UnsupReq- AuxPwr- TransPend-

                LnkCap: Port #0, Speed 8GT/s, Width x1, ASPM L1, Exit Latency L1 <8us

                        ClockPM- Surprise- LLActRep- BwNot+ ASPMOptComp+

                LnkCtl: ASPM Disabled; RCB 64 bytes, Disabled- CommClk-

                        ExtSynch- ClockPM- AutWidDis- BWInt- AutBWInt-

                LnkSta: Speed 8GT/s (ok), Width x1 (ok)

                        TrErr- Train- SlotClk- DLActive- BWMgmt- ABWMgmt+

                SltCap: AttnBtn- PwrCtrl- MRL- AttnInd- PwrInd- HotPlug- Surprise-

                        Slot #0, PowerLimit 0.000W; Interlock- NoCompl-

                SltCtl: Enable: AttnBtn- PwrFlt- MRL- PresDet- CmdCplt- HPIrq- LinkChg-

                        Control: AttnInd Off, PwrInd Off, Power+ Interlock-

                SltSta: Status: AttnBtn- PowerFlt- MRL+ CmdCplt- PresDet- Interlock-

                        Changed: MRL- PresDet- LinkState-

                RootCap: CRSVisible-

                RootCtl: ErrCorrectable- ErrNon-Fatal- ErrFatal- PMEIntEna+ CRSVisible-

                RootSta: PME ReqID 0000, PMEStatus- PMEPending-

                DevCap2: Completion Timeout: Range B, TimeoutDis+ NROPrPrP- LTR+

                         10BitTagComp+ 10BitTagReq- OBFF Via message, ExtFmt+ EETLPPrefix+, MaxEETLPPrefixes 1

                         EmergencyPowerReduction Not Supported, EmergencyPowerReductionInit-

                         FRS- LN System CLS Not Supported, TPHComp- ExtTPHComp- ARIFwd+

                         AtomicOpsCap: Routing- 32bit- 64bit- 128bitCAS-

                DevCtl2: Completion Timeout: 50us to 50ms, TimeoutDis- LTR+ OBFF Disabled, ARIFwd+

                         AtomicOpsCtl: ReqEn- EgressBlck-

                LnkCap2: Supported Link Speeds: 2.5-8GT/s, Crosslink- Retimer- 2Retimers- DRS-

                LnkCtl2: Target Link Speed: 8GT/s, EnterCompliance- SpeedDis-

                         Transmit Margin: Normal Operating Range, EnterModifiedCompliance- ComplianceSOS-

                         Compliance De-emphasis: -6dB

                LnkSta2: Current De-emphasis Level: -6dB, EqualizationComplete+ EqualizationPhase1+

                         EqualizationPhase2+ EqualizationPhase3+ LinkEqualizationRequest-

                         Retimer- 2Retimers- CrosslinkRes: unsupported

        Capabilities: [100 v2] Advanced Error Reporting

                UESta:  DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC- UnsupReq- ACSViol-

                UEMsk:  DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC- UnsupReq- ACSViol-

                UESvrt: DLP+ SDES+ TLP- FCP+ CmpltTO- CmpltAbrt- UnxCmplt- RxOF+ MalfTLP+ ECRC- UnsupReq- ACSViol-

                CESta:  RxErr- BadTLP- BadDLLP- Rollover- Timeout- AdvNonFatalErr-

                CEMsk:  RxErr- BadTLP- BadDLLP- Rollover- Timeout- AdvNonFatalErr+

                AERCap: First Error Pointer: 00, ECRCGenCap+ ECRCGenEn- ECRCChkCap+ ECRCChkEn-

                        MultHdrRecCap- MultHdrRecEn- TLPPfxPres- HdrLogCap-

                HeaderLog: 00000000 00000000 00000000 00000000

                RootCmd: CERptEn+ NFERptEn+ FERptEn+

                RootSta: CERcvd- MultCERcvd- UERcvd- MultUERcvd-

                         FirstFatal- NonFatalMsg- FatalMsg- IntMsg 0

                ErrorSrc: ERR\_COR: 0000 ERR\_FATAL/NONFATAL: 0000

        Capabilities: [150 v1] Device Serial Number 00-00-00-00-00-00-00-00

        Capabilities: [300 v1] Secondary PCI Express

                LnkCtl3: LnkEquIntrruptEn- PerformEqu-

                LaneErrStat: 0

        Capabilities: [4c0 v1] Virtual Channel

                Caps:   LPEVC=0 RefClk=100ns PATEntryBits=1

                Arb:    Fixed- WRR32- WRR64- WRR128-

                Ctrl:   ArbSelect=Fixed

                Status: InProgress-

                VC0:    Caps:   PATOffset=00 MaxTimeSlots=1 RejSnoopTrans-

                        Arb:    Fixed- WRR32- WRR64- WRR128- TWRR128- WRR256-

                        Ctrl:   Enable+ ID=0 ArbSelect=Fixed TC/VC=ff

                        Status: NegoPending- InProgress-

                VC1:    Caps:   PATOffset=00 MaxTimeSlots=1 RejSnoopTrans-

                        Arb:    Fixed- WRR32- WRR64- WRR128- TWRR128- WRR256-

                        Ctrl:   Enable- ID=1 ArbSelect=Fixed TC/VC=00

                        Status: NegoPending- InProgress-

                VC2:    Caps:   PATOffset=00 MaxTimeSlots=1 RejSnoopTrans-

                        Arb:    Fixed- WRR32- WRR64- WRR128- TWRR128- WRR256-

                        Ctrl:   Enable- ID=2 ArbSelect=Fixed TC/VC=00

                        Status: NegoPending- InProgress-

                VC3:    Caps:   PATOffset=00 MaxTimeSlots=1 RejSnoopTrans-

                        Arb:    Fixed- WRR32- WRR64- WRR128- TWRR128- WRR256-

                        Ctrl:   Enable- ID=3 ArbSelect=Fixed TC/VC=00

                        Status: NegoPending- InProgress-

        Capabilities: [5c0 v1] Address Translation Service (ATS)

                ATSCap: Invalidate Queue Depth: 01

                ATSCtl: Enable-, Smallest Translation Unit: 00

        Capabilities: [640 v1] Page Request Interface (PRI)

                PRICtl: Enable- Reset-

                PRISta: RF- UPRGI- Stopped+

                Page Request Capacity: 00000001, Page Request Allocation: 00000000

        Capabilities: [900 v1] L1 PM Substates

                L1SubCap: PCI-PM\_L1.2+ PCI-PM\_L1.1+ ASPM\_L1.2+ ASPM\_L1.1+ L1\_PM\_Substates+

                          PortCommonModeRestoreTime=255us PortTPowerOnTime=26us

                L1SubCtl1: PCI-PM\_L1.2- PCI-PM\_L1.1- ASPM\_L1.2- ASPM\_L1.1-

                           T\_CommonMode=0us LTR1.2\_Threshold=0ns

                L1SubCtl2: T\_PwrOn=10us

        Kernel driver in use: pcieport

        Kernel modules: pci\_endpoint\_test

01:00.0 PCI bridge: Microchip Technology / SMSC Device a048 (rev b0) (prog-if 00 [Normal decode])

        Control: I/O- Mem+ BusMaster+ SpecCycle- MemWINV- VGASnoop- ParErr- Stepping- SERR- FastB2B- DisINTx+

        Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort- >SERR- <PERR- INTx-

        Latency: 0

        Interrupt: pin A routed to IRQ 538

        Bus: primary=01, secondary=02, subordinate=06, sec-latency=0

        I/O behind bridge: [disabled]

        Memory behind bridge: 18100000-183fffff [size=3M]

        Prefetchable memory behind bridge: [disabled]

        Secondary status: 66MHz- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort- <SERR- <PERR-

        BridgeCtl: Parity- SERR+ NoISA- VGA- VGA16- MAbort- >Reset- FastB2B-

                PriDiscTmr- SecDiscTmr- DiscTmrStat- DiscTmrSERREn-

        Capabilities: [80] Express (v2) Upstream Port, MSI 00

                DevCap: MaxPayload 512 bytes, PhantFunc 0

                        ExtTag+ AttnBtn- AttnInd- PwrInd- RBE+ SlotPowerLimit 0.000W

                DevCtl: CorrErr+ NonFatalErr+ FatalErr+ UnsupReq+

                        RlxdOrd+ ExtTag+ PhantFunc- AuxPwr- NoSnoop+

                        MaxPayload 128 bytes, MaxReadReq 512 bytes

                DevSta: CorrErr+ NonFatalErr- FatalErr- UnsupReq+ AuxPwr+ TransPend-

                LnkCap: Port #0, Speed 8GT/s, Width x4, ASPM not supported

                        ClockPM- Surprise- LLActRep- BwNot- ASPMOptComp+

                LnkCtl: ASPM Disabled; Disabled- CommClk-

                        ExtSynch- ClockPM- AutWidDis- BWInt- AutBWInt-

                LnkSta: Speed 8GT/s (ok), Width x1 (downgraded)

                        TrErr- Train- SlotClk- DLActive- BWMgmt- ABWMgmt-

                DevCap2: Completion Timeout: Not Supported, TimeoutDis- NROPrPrP- LTR+

                         10BitTagComp- 10BitTagReq- OBFF Via message/WAKE#, ExtFmt+ EETLPPrefix-

                         EmergencyPowerReduction Not Supported, EmergencyPowerReductionInit-

                         FRS-

                         AtomicOpsCap: Routing+

                DevCtl2: Completion Timeout: 50us to 50ms, TimeoutDis- LTR+ OBFF Disabled,

                         AtomicOpsCtl: EgressBlck-

                LnkCap2: Supported Link Speeds: 2.5-8GT/s, Crosslink- Retimer- 2Retimers- DRS-

                LnkCtl2: Target Link Speed: 8GT/s, EnterCompliance- SpeedDis-

                         Transmit Margin: Normal Operating Range, EnterModifiedCompliance- ComplianceSOS-

                         Compliance De-emphasis: -6dB

                LnkSta2: Current De-emphasis Level: -6dB, EqualizationComplete+ EqualizationPhase1+

                         EqualizationPhase2+ EqualizationPhase3+ LinkEqualizationRequest-

                         Retimer- 2Retimers- CrosslinkRes: unsupported

        Capabilities: [e0] MSI: Enable+ Count=1/1 Maskable- 64bit+