serdes\_wiz0: wiz@5060000 {

                compatible = "ti,j721e-wiz-10g";

                #address-cells = <1>;

                #size-cells = <1>;

                power-domains = <&k3\_pds 292 TI\_SCI\_PD\_EXCLUSIVE>;

                clocks = <&k3\_clks 292 11>, <&k3\_clks 292 85>, <&serdes\_refclk>;

                clock-names = "fck", "core\_ref\_clk", "ext\_ref\_clk";

                num-lanes = <4>;

                #reset-cells = <1>;

                ranges = <0x5060000 0x0 0x5060000 0x10000>;

                assigned-clocks = <&k3\_clks 292 85>;

                assigned-clock-parents = <&k3\_clks 292 89>;

                wiz0\_pll0\_refclk: pll0-refclk {

                        clocks = <&k3\_clks 292 85>, <&serdes\_refclk>;

                        clock-output-names = "wiz0\_pll0\_refclk";

                        #clock-cells = <0>;

                        assigned-clocks = <&wiz0\_pll0\_refclk>;

                        assigned-clock-parents = <&k3\_clks 292 85>;

                };

                wiz0\_pll1\_refclk: pll1-refclk {

                        clocks = <&k3\_clks 292 85>, <&serdes\_refclk>;

                        clock-output-names = "wiz0\_pll1\_refclk";

                        #clock-cells = <0>;

                        assigned-clocks = <&wiz0\_pll1\_refclk>;

                        assigned-clock-parents = <&k3\_clks 292 85>;

                };

                wiz0\_refclk\_dig: refclk-dig {

                        clocks = <&k3\_clks 292 85>, <&serdes\_refclk>;

                        clock-output-names = "wiz0\_refclk\_dig";

                        #clock-cells = <0>;

                        assigned-clocks = <&wiz0\_refclk\_dig>;

                        assigned-clock-parents = <&k3\_clks 292 85>;

                };

                wiz0\_cmn\_refclk\_dig\_div: cmn-refclk-dig-div {

                        clocks = <&wiz0\_refclk\_dig>;

                        #clock-cells = <0>;

                };

                serdes0: serdes@5060000 {

                        compatible = "ti,j721e-serdes-10g";

                        reg = <0x05060000 0x00010000>;

                        reg-names = "torrent\_phy";

                        resets = <&serdes\_wiz0 0>;

                        reset-names = "torrent\_reset";

                        clocks = <&wiz0\_pll0\_refclk>;

                        clock-names = "refclk";

                        #address-cells = <1>;

                        #size-cells = <0>;

                };

        };

pcie1\_rc: pcie@2910000 {

                compatible = "ti,j7200-pcie-host", "ti,j721e-pcie-host";

                reg = <0x00 0x02910000 0x00 0x1000>,

                        <0x00 0x02917000 0x00 0x400>,

                        <0x00 0x0d800000 0x00 0x00800000>,

                        <0x00 0x18000000 0x00 0x00001000>;

                reg-names = "intd\_cfg", "user\_cfg", "reg", "cfg";

                interrupt-names = "link\_state";

                interrupts = <GIC\_SPI 330 IRQ\_TYPE\_EDGE\_RISING>;

                device\_type = "pci";

                ti,syscon-pcie-ctrl = <&scm\_conf 0x4074>;

                max-link-speed = <3>;

                num-lanes = <4>;

                power-domains = <&k3\_pds 240 TI\_SCI\_PD\_EXCLUSIVE>;

                clocks = <&k3\_clks 240 6>;

                clock-names = "fck";

                #address-cells = <3>;

                #size-cells = <2>;

                bus-range = <0x0 0xff>;

                cdns,no-bar-match-nbits = <64>;

                vendor-id = <0x104c>;

                device-id = <0xb00f>;

                msi-map = <0x0 &gic\_its 0x0 0x10000>;

                dma-coherent;

                ranges = <0x01000000 0x0 0x18001000  0x00 0x18001000  0x0 0x0010000>,

                        <0x02000000 0x0 0x18011000  0x00 0x18011000  0x0 0x7fef000>;

                dma-ranges = <0x02000000 0x0 0x0 0x0 0x0 0x10000 0x0>;

                #interrupt-cells = <1>;

                interrupt-map-mask = <0 0 0 7>;

                interrupt-map = <0 0 0 1 &pcie1\_intc 0>, /\* INT A \*/

                                <0 0 0 2 &pcie1\_intc 0>, /\* INT B \*/

                                <0 0 0 3 &pcie1\_intc 0>, /\* INT C \*/

                                <0 0 0 4 &pcie1\_intc 0>; /\* INT D \*/

                pcie1\_intc: interrupt-controller {

                        interrupt-controller;

                        #interrupt-cells = <1>;

                        #address-cells = <0>;

                        interrupt-parent = <&gic500>;

                        interrupts = <GIC\_SPI 324 IRQ\_TYPE\_EDGE\_RISING>;

                };

        };

pcie1\_ep: pcie-ep@2910000 {

                compatible = "ti,j7200-pcie-ep", "ti,j721e-pcie-ep";

                reg = <0x00 0x02910000 0x00 0x1000>,

                        <0x00 0x02917000 0x00 0x400>,

                        <0x00 0x0d800000 0x00 0x00800000>,

                        <0x00 0x18000000 0x00 0x08000000>;

                reg-names = "intd\_cfg", "user\_cfg", "reg", "mem";

                interrupt-names = "link\_state";

                interrupts = <GIC\_SPI 330 IRQ\_TYPE\_EDGE\_RISING>;

                ti,syscon-pcie-ctrl = <&scm\_conf 0x4074>;

                max-link-speed = <3>;

                num-lanes = <4>;

                power-domains = <&k3\_pds 240 TI\_SCI\_PD\_EXCLUSIVE>;

                clocks = <&k3\_clks 240 6>;

                clock-names = "fck";

                max-functions = /bits/ 8 <6>;

                max-virtual-functions = /bits/ 8 <4 4 4 4 0 0>;

                dma-coherent;

        };

&serdes\_ln\_ctrl {

        idle-states = <J7200\_SERDES0\_LANE0\_PCIE1\_LANE0>, <J7200\_SERDES0\_LANE1\_PCIE1\_LANE1>,

                      <J7200\_SERDES0\_LANE2\_PCIE1\_LANE2>, <J7200\_SERDES0\_LANE3\_PCIE1\_LANE3>;

};

&serdes\_refclk {

        clock-frequency = <100000000>;

};

&serdes0 {

        #address-cells = <1>;

        #size-cells = <0>;

        serdes0\_pcie\_link: phy@0 {

                reg = <0>;

                cdns,num-lanes = <4>;

                #phy-cells = <0>;

                cdns,phy-type = <PHY\_TYPE\_PCIE>;

                resets = <&serdes\_wiz0 1>, <&serdes\_wiz0 2>, <&serdes\_wiz0 3>, <&serdes\_wiz0 4>;

        };

};

&pcie1\_rc {

        phys = <&serdes0\_pcie\_link>;

        phy-names = "pcie-phy";

        num-lanes = <4>;

};

&pcie1\_ep {

        phys = <&serdes0\_pcie\_link>;

        phy-names = "pcie-phy";

        num-lanes = <4>;

        status = "disable";

};