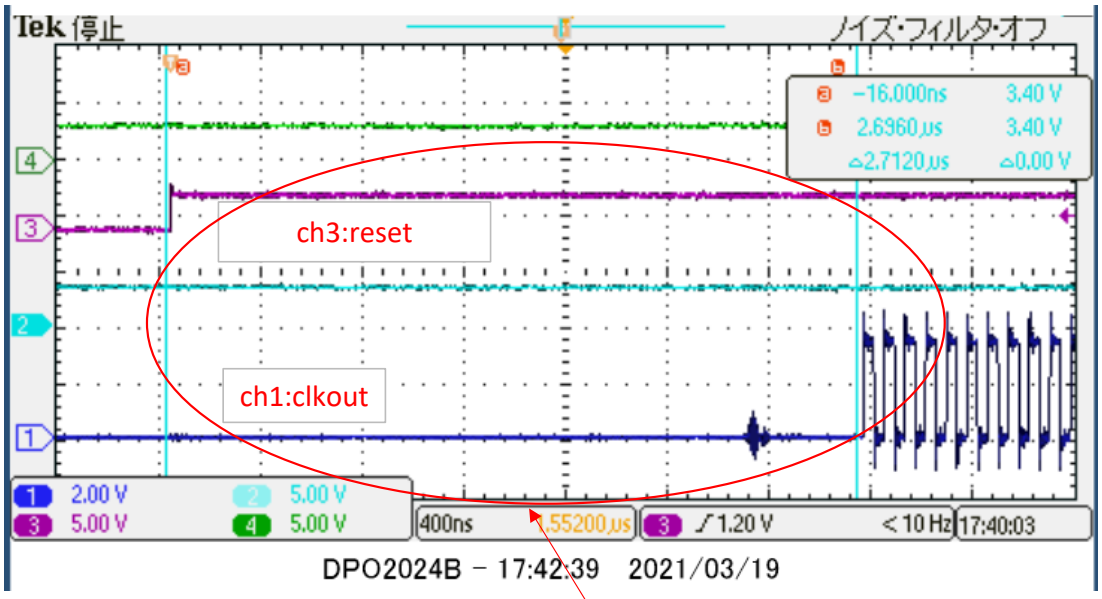
Silicon behavior

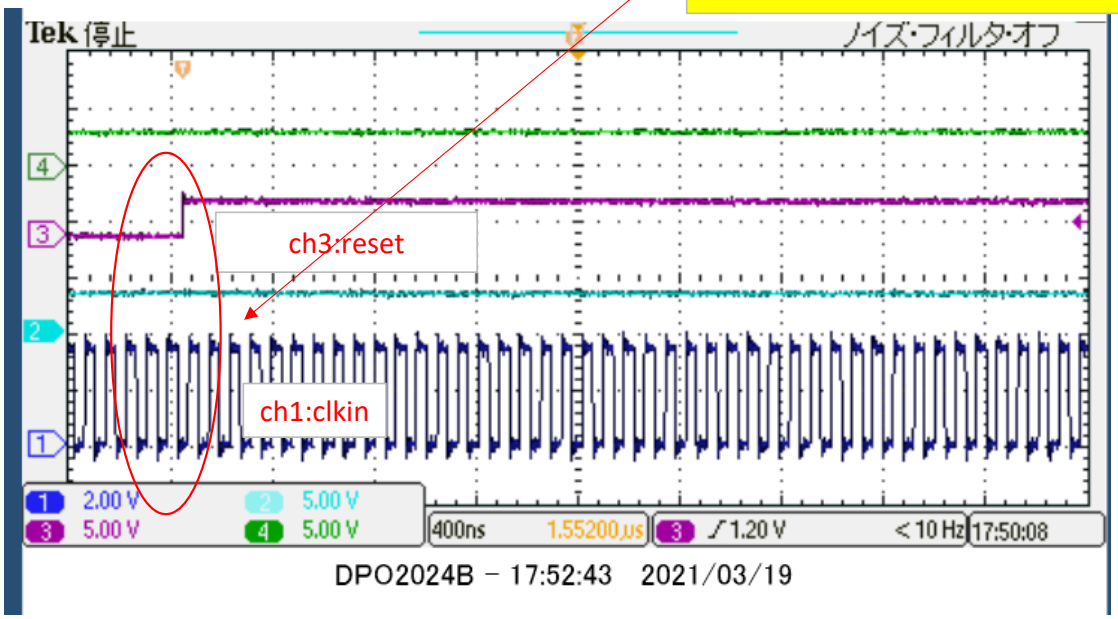
2021/3/19

reset clock



Clock is provided to X2/CLKIN pin all the time.
But CLKOUT is on 2.7usec after reset release.

clkin



Datasheet

5.8.2 Power-Up Reset (On-Chip Oscillator Inactive)

Table 5−12 and Table 5−13 assume testing over recommended operating conditions (see Figure 5−16).

Table 5−12. Power-Up Reset (On-Chip Oscillator Inactive) Timing Requirements

NO.			CV_{DD} = 1.2 V CV_{DD} = 1.35 V		CV_{DD} = 1.6 V		UNIT
			MIN	MAX	MIN	MAX	
R2	$t_{h(CLKOUTV-RSTL)}$	Hold time, CLKOUT valid to $\overline{RESET}$ low	3P‡		3P‡		ns

‡ P = 1/(input clock frequency) in ns. For example, when input clock is 12 MHz, P = 83.33 ns.

Table 5−13. Power-Up Reset (On-Chip Oscillator Inactive) Switching Characteristics

NO.	PARAMETER		CV_{DD} = 1.2 V CV_{DD} = 1.35 V		CV_{DD} = 1.6 V		UNIT
			MIN	MAX	MIN	MAX	
R3	$t_{d(CLKINV-CLKOUTV)}$	Delay time, CLKIN valid to CLKOUT valid		30		30	ns

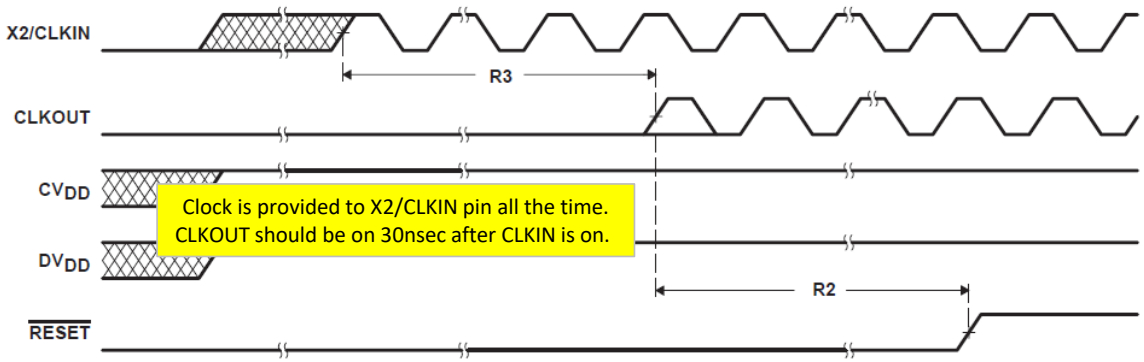


Figure 5−16. Power-Up Reset (On-Chip Oscillator Inactive) Timings