Centaurus FAE alert

Affected devices

All Centaurus class devices including…

- XAM3874BCYE
- TMX320DM8148BCYE
- TMX320C6A8148BCYE
- XDRA6XXBCYE

Issue :

It has been discovered that the video PLLs are particularly sensitive to power supply noise. This jitter is particularly an issue when the DVO is connected to an external analog DAC since the issue causes the h-sync period to jitter significantly. For analog DAC applications the receiving TV/monitor needs to re-construct the pixel sampling clock by measuring and locking to the h-sync period. If this signal has jitter then the measurements taken by the receiver will be delayed, hence incorrect sampling will be used resulting in bad displayed image quality.

For DVO1 (VOut1) which feeds the HDMI core the jitter can be reduced to acceptable levels (less than 1.5ns) by placing the PLL in a higher operating VCO range than the default range.

DVO2 (VOut0) jitter is not improved sufficiently even when the PLL operating frequency is increased, and a h-sync jitter of 15ns or more will be seen for pixel rates in the 148MHz range. This will cause the displayed image to be extremely distorted when driving an analog DAC.

Digital interfaces such as HDMI, DVI, Display Port, LVDS etc… are not susceptible to image quality degradation cause by jitter since these interfaces are fully clock/data synchronous, meaning that the clock and data are both sent completely and together from the source and across the cable link to the receiving device.

Solution :

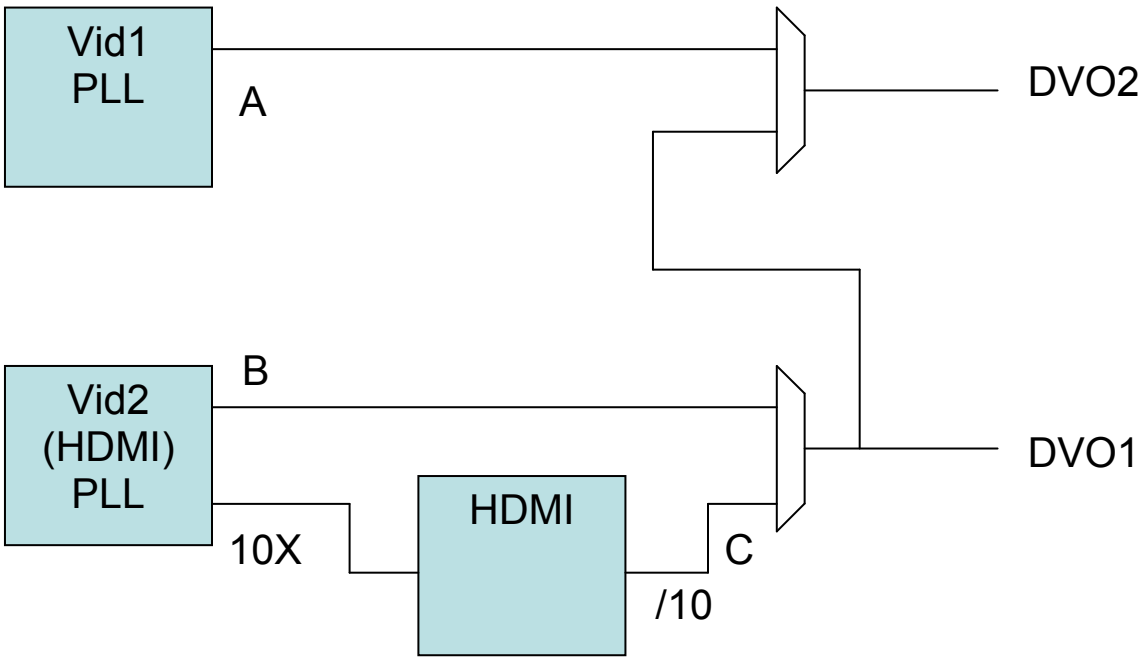
The jitter is extremely sensitive to PLL power supply noise. Noise can be reduced by disabling digital IO switching interfaces which are not needed and by ensuring that the HDMI core is powered down when not in use.

For DVO1 the jitter can be reduced to around 1.5ns by ensuring that the PLL power supply pins VSSA_HDMI and VDDA_HDMI are isolated as much as possible from the core and IO digital supply power and grounds. It is not recommended to connect the VDDA_HDMI_1P8 directly to any digital 1V8 supplies. This supply should be as isolated as possible from all other 1V8 supplies. Additionally the PLL should be configured to operate in a high frequency range. A software patch is available to ensure that the DVO1 PLL operates in the optimal, low jitter range.

For DVO2 the jitter cannot currently be reduced sufficiently for acceptable analog DAC connection without introducing image stability issues. Operating the DVO2 PLL in a high frequency range will reduce the jitter significantly though, and should be implemented even for digital transmitters.

DVO2 can receive its clock from the DVO1 PLL but in this use case DVO1 and DVO2 (VOut0 & VOut1/HDMI) will have the same pixel clock frequency.

The following clock diagram shows the potential clock sources for each output…



From this diagram it can be seen that DVO2 clock source can be selected from either Vid1 PLL or Vid2 PLL but DVO1 and the HDMI core can only be sourced from Vid2 PLL.

PSP 04.01.00.06 Patch2 release will have the software to configure Vid1 PLL and VId2 PLL into their higher operating frequencies for given output pixel frequencies to reduce the clock jitter accordingly.