```
// SPDX-License-Identifier: GPL-2.0
/*
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 */

/dts-v1/;

#include <dt-bindings/phy/phy.h>
#include <dt-bindings/mux/ti-serdes.h>
#include <dt-bindings/leds/common.h>
#include <dt-bindings/gpio/gpio.h>
#include <dt-bindings/net/ti-dp83867.h>
#include "k3-am642.dtsi"

/ {
	compatible =	"ti,am642-evm", "ti,am642";
	model = "Texas Instruments AM642 EVM";

	chosen {
		stdout-path = "serial2:115200n8";
		bootargs = "console=ttyS2,115200n8 earlycon=ns16550a,mmio32,0x02800000";
	};

	aliases {
		ethernet2 = &icssg0_emac0;
	};
	memory@80000000 {
		device_type = "memory";
		/* 2G RAM */
		reg = <0x00000000 0x80000000 0x00000000 0x80000000>;

	};

	reserved-memory {
		#address-cells = <2>;
		#size-cells = <2>;
		ranges;

		secure_ddr: optee@9e800000 {
			reg = <0x00 0x9e800000 0x00 0x01800000>; /* for OP-TEE */
			alignment = <0x1000>;
			no-map;
		};
```

```
            main_r5fss0_core0_dma_memory_region: r5f-dma-memory@a0000000 {
                compatible = "shared-dma-pool";
                reg = <0x00 0xa0000000 0x00 0x100000>;
                no-map;
            };

            main_r5fss0_core0_memory_region: r5f-memory@a0100000 {
                compatible = "shared-dma-pool";
                reg = <0x00 0xa0100000 0x00 0xf00000>;
                no-map;
            };

//          main_r5fss0_core1_dma_memory_region: r5f-dma-memory@a1000000 {
//              compatible = "shared-dma-pool";
//              reg = <0x00 0xa1000000 0x00 0x100000>;
//              no-map;
//          };
//
//          main_r5fss0_core1_memory_region: r5f-memory@a1100000 {
//              compatible = "shared-dma-pool";
//              reg = <0x00 0xa1100000 0x00 0xf00000>;
//              no-map;
//          };

            main_r5fss1_core0_dma_memory_region: r5f-dma-memory@a2000000 {
                compatible = "shared-dma-pool";
                reg = <0x00 0xa2000000 0x00 0x100000>;
                no-map;
            };

            main_r5fss1_core0_memory_region: r5f-memory@a2100000 {
                compatible = "shared-dma-pool";
                reg = <0x00 0xa2100000 0x00 0xf00000>;
                no-map;
            };

//          main_r5fss1_core1_dma_memory_region: r5f-dma-memory@a3000000 {
//              compatible = "shared-dma-pool";
//              reg = <0x00 0xa3000000 0x00 0x100000>;
//              no-map;
//          };
//
//          main_r5fss1_core1_memory_region: r5f-memory@a3100000 {
//              compatible = "shared-dma-pool";
```

```
//                reg = <0x00 0xa3100000 0x00 0xf00000>;
//                no-map;
//          };

          mcu_m4fss_dma_memory_region: m4f-dma-memory@a4000000 {
                compatible = "shared-dma-pool";
                reg = <0x00 0xa4000000 0x00 0x100000>;
                no-map;
          };

          mcu_m4fss_memory_region: m4f-memory@a4100000 {
                compatible = "shared-dma-pool";
                reg = <0x00 0xa4100000 0x00 0xf00000>;
                no-map;
          };

          rtos_ipc_memory_region: ipc-memories@a5000000 {
                reg = <0x00 0xa5000000 0x00 0x00800000>;
                alignment = <0x1000>;
                no-map;
          };
    };

    transceiver1: can-phy0 {
          compatible = "ti,tcan1042";
          #phy-cells = <0>;
          max-bitrate = <5000000>;
    };

    transceiver2: can-phy1 {
          compatible = "ti,tcan1042";
          #phy-cells = <0>;
          max-bitrate = <5000000>;
    };

    icssg0_eth: icssg0-eth {
          compatible = "ti,am642-icssg-prueth";
          pinctrl-names = "default";
          pinctrl-0 = <&pru_icssg0_mii_g_rt_pins_default>;

          sram = <&oc_sram>;
          ti,prus = <&pru0_0>, <&rtu0_0>, <&tx_pru0_0>, <&pru0_1>, <&rtu0_1>,
<&tx_pru0_1>;
          firmware-name = "ti-pruss/am65x-sr2-pru0-prueth-fw.elf",
```

```
                "ti-pruss/am65x-sr2-rtu0-prueth-fw.elf",
                "ti-pruss/am65x-sr2-txpru0-prueth-fw.elf",
                "ti-pruss/am65x-sr2-pru1-prueth-fw.elf",
                "ti-pruss/am65x-sr2-rtu1-prueth-fw.elf",
                "ti-pruss/am65x-sr2-txpru1-prueth-fw.elf";

        ti,pruss-gp-mux-sel = <2>,      /* MII mode */
                              <2>,
                              <2>,
                              <2>,     /* MII mode */
                              <2>,
                              <2>;

        mii-g-rt = <&icssg0_mii_g_rt>;
        mii-rt = <&icssg0_mii_rt>;
        iep = <&icssg0_iep0>,    <&icssg0_iep1>;

        interrupt-parent = <&icssg0_intc>;
        interrupts = <24 0 2>, <25 1 3>;
        interrupt-names = "tx_ts0", "tx_ts1";

        dmas = <&main_pktdma 0xc100 15>, /* egress slice 0 */
               <&main_pktdma 0xc101 15>, /* egress slice 0 */
               <&main_pktdma 0xc102 15>, /* egress slice 0 */
               <&main_pktdma 0xc103 15>, /* egress slice 0 */
               <&main_pktdma 0xc104 15>, /* egress slice 1 */
               <&main_pktdma 0xc105 15>, /* egress slice 1 */
               <&main_pktdma 0xc106 15>, /* egress slice 1 */
               <&main_pktdma 0xc107 15>, /* egress slice 1 */
               <&main_pktdma 0x4100 15>, /* ingress slice 0 */
               <&main_pktdma 0x4101 15>, /* ingress slice 1 */
               <&main_pktdma 0x4102 0>, /* mgmnt rsp slice 0 */
               <&main_pktdma 0x4103 0>; /* mgmnt rsp slice 1 */
        dma-names = "tx0-0", "tx0-1", "tx0-2", "tx0-3",
                "tx1-0", "tx1-1", "tx1-2", "tx1-3",
                "rx0", "rx1";//,
//              "rxmgm0", "rxmgm1";

            icssg0_emac0: ethernet-mii0 {
                phy-handle = <&icssg0_phy1>;
                phy-mode = "mii";
                /*ti,syscon-rgmii-delay = <&main_conf 0x4100>;*/
                /* Filled in by bootloader */
                local-mac-address = [00 00 00 00 00 00];
```

```
//                      fixed-link {
//              speed = <100>;
//              full-duplex;
//     };
            };
            icssg0_emac1: ethernet-mii1 {
                phy-mode = "mii";
                local-mac-address = [00 00 00 00 00 00];
                status = "disabled";
            };
        };

        leds {
            compatible = "gpio-leds";
            pinctrl-names = "default";
            pinctrl-0 = <&usr_led_pins_default>;

            led-0 {
                label = "am64-evm:green:heartbeat";
                gpios = <&main_gpio1 44 GPIO_ACTIVE_HIGH>;
                linux,default-trigger = "heartbeat";
                function = LED_FUNCTION_HEARTBEAT;
                default-state = "off";
            };
        };
};
&main_r5fss0_core0 {
        mboxes = <&mailbox0_cluster2 &mbox_main_r5fss0_core0>;
        memory-region = <&main_r5fss0_core0_dma_memory_region>,
                <&main_r5fss0_core0_memory_region>;
};

//&main_r5fss0_core1 {
//      mboxes = <&mailbox0_cluster2 &mbox_main_r5fss0_core1>;
//      memory-region = <&main_r5fss0_core1_dma_memory_region>,
//              <&main_r5fss0_core1_memory_region>;
//};

&main_r5fss1_core0 {
        mboxes = <&mailbox0_cluster4 &mbox_main_r5fss1_core0>;
        memory-region = <&main_r5fss1_core0_dma_memory_region>,
                <&main_r5fss1_core0_memory_region>;
};
```

```
//&main_r5fss1_core1 {
//    mboxes = <&mailbox0_cluster4 &mbox_main_r5fss1_core1>;
//    memory-region = <&main_r5fss1_core1_dma_memory_region>,
//                    <&main_r5fss1_core1_memory_region>;
//};

&mcu_m4fss {
    mboxes = <&mailbox0_cluster6 &mbox_m4_0>;
    memory-region = <&mcu_m4fss_dma_memory_region>,
                    <&mcu_m4fss_memory_region>;
};

&main_pmx0 {
    main_mmc1_pins_default: main-mmc1-pins-default {
        pinctrl-single,pins = <
            AM64X_IOPAD(0x0294, PIN_INPUT, 0) /* (J19) MMC1_CMD */
            AM64X_IOPAD(0x0290, PIN_INPUT, 0) /* (#N/A) MMC1_CLKLB */
            AM64X_IOPAD(0x028c, PIN_INPUT, 0) /* (L20) MMC1_CLK */
            AM64X_IOPAD(0x0288, PIN_INPUT, 0) /* (K21) MMC1_DAT0 */
            AM64X_IOPAD(0x0284, PIN_INPUT, 0) /* (L21) MMC1_DAT1 */
            AM64X_IOPAD(0x0280, PIN_INPUT, 0) /* (K19) MMC1_DAT2 */
            AM64X_IOPAD(0x027c, PIN_INPUT, 0) /* (K18) MMC1_DAT3 */
            AM64X_IOPAD(0x0298, PIN_INPUT, 0) /* (D19) MMC1_SDCD */
        >;
    };

    main_uart0_pins_default: main-uart0-pins-default {
        pinctrl-single,pins = <
            AM64X_IOPAD(0x0230, PIN_INPUT, 0) /* (D15) UART0_RXD */
            AM64X_IOPAD(0x0234, PIN_OUTPUT, 0) /* (C16) UART0_TXD */
        >;
    };

    main_uart1_pins_default: main-uart1-pins-default {
        pinctrl-single,pins = <
            AM64X_IOPAD(0x0248, PIN_INPUT, 0) /* (D16) UART1_CTSn */
            AM64X_IOPAD(0x024c, PIN_OUTPUT, 0) /* (E16) UART1_RTSn */
            AM64X_IOPAD(0x0240, PIN_INPUT, 0) /* (E15) UART1_RXD */
            AM64X_IOPAD(0x0244, PIN_OUTPUT, 0) /* (E14) UART1_TXD */
        >;
    };

    main_uart2_pins_default: main-uart2-pins-default {
        pinctrl-single,pins = <
```

```
                AM64X_IOPAD(0x0238, PIN_INPUT, 3) /* (B16) UART2_RXD    UART0_CTSn*/
                AM64X_IOPAD(0x023c, PIN_OUTPUT, 3) /* (A16) UART2_TXD    UART0_RTSn*/
            >;
        };


//      main_uart4_pins_default: main-uart4-pins-default {
//          pinctrl-single,pins = <
//              AM64X_IOPAD(0x01DC,       PIN_INPUT,       10)       /*       (W4)       UART4_RXD
PRG0_PRU1_GPO11*/
//              AM64X_IOPAD(0x01cc,       PIN_OUTPUT,       10)       /*       (W5)       UART4_TXD
PRG0_PRU1_GPO7*/
//          >;
//      };

//      main_uart5_pins_default: main-uart5-pins-default {
//          pinctrl-single,pins = <
//              AM64X_IOPAD(0x01E4,       PIN_INPUT,       10)       /*       (T6)       UART5_RXD
PRG0_PRU1_GPO13*/
//              AM64X_IOPAD(0x01B4,       PIN_OUTPUT,       10)       /*       (W2)       UART5_TXD
PRG0_PRU1_GPO1*/
//          >;
//      };

//      main_uart6_pins_default: main-uart6-pins-default {
//          pinctrl-single,pins = <
//              AM64X_IOPAD(0x01E8,       PIN_INPUT,       10)       /*       (U6)       UART6_RXD
PRG0_PRU1_GPO14*/
//              AM64X_IOPAD(0x01C0,       PIN_OUTPUT,       10)       /*       (W3)       UART6_TXD
PRG0_PRU1_GPO4*/
//          >;
//      };
        main_i2c0_pins_default: main-i2c0-pins-default {
            pinctrl-single,pins = <
                AM64X_IOPAD(0x0260, PIN_INPUT_PULLUP, 0) /* (A18) I2C1_SCL */
                AM64X_IOPAD(0x0264, PIN_INPUT_PULLUP, 0) /* (B18) I2C1_SDA */
            >;
        };

        mdio1_pins_default: mdio1-pins-default {
            pinctrl-single,pins = <
                AM64X_IOPAD(0x01fc, PIN_OUTPUT, 4) /* (R2) PRG0_PRU1_GPO19.MDIO0_MDC
*/
                AM64X_IOPAD(0x01f8, PIN_INPUT, 4) /* (P5) PRG0_PRU1_GPO18.MDIO0_MDIO
```

```
*/
            >;
        };

        di_do_pins_default: di_do_pins_default {
            pinctrl-single,pins = <
//                  AM64X_IOPAD(0x01E0, PIN_OUTPUT, 7) /* (Y4) PRG0_PRU1_GPO12 GPIO1_32 */
//                  AM64X_IOPAD(0x01D8, PIN_OUTPUT, 7) /* (V6) PRG0_PRU1_GPO10 GPIO1_30 */
//                  AM64X_IOPAD(0x01D4, PIN_OUTPUT, 7) /* (Y5) PRG0_PRU1_GPO9 GPIO1_29 */
//                  AM64X_IOPAD(0x01D0, PIN_OUTPUT, 7) /* (R1) PRG0_PRU1_GPO8 GPIO1_28 */

                    AM64X_IOPAD(0x01A4, PIN_INPUT, 7) /* (U1) PRG0_PRU0_GPO17 GPIO1_17 */
                    AM64X_IOPAD(0x01A8, PIN_INPUT, 7) /* (V1) PRG0_PRU0_GPO18 GPIO1_18 */
                    AM64X_IOPAD(0x017C, PIN_INPUT, 7) /* (T1) PRG0_PRU0_GPO7    GPIO1_7 */

//                  AM64X_IOPAD(0x01B8, PIN_INPUT, 7) /* (V3) PRG0_PRU1_GPO2    GPIO1_22 */


            >;
        };

        rgmii1_pins_default: rgmii1-pins-default {
            pinctrl-single,pins = <
                AM64X_IOPAD(0x011c, PIN_INPUT, 4) /* (AA13) PRG1_PRU1_GPO5.RGMII1_RD0
*/
                AM64X_IOPAD(0x0128, PIN_INPUT, 4) /* (U12) PRG1_PRU1_GPO8.RGMII1_RD1 */
                AM64X_IOPAD(0x0150, PIN_INPUT, 4) /* (Y13) PRG1_PRU1_GPO18.RGMII1_RD2
*/
                AM64X_IOPAD(0x0154, PIN_INPUT, 4) /* (V12) PRG1_PRU1_GPO19.RGMII1_RD3
*/
                AM64X_IOPAD(0x00d8, PIN_INPUT, 4) /* (W13) PRG1_PRU0_GPO8.RGMII1_RXC
*/
                AM64X_IOPAD(0x00cc, PIN_INPUT, 4) /* (V13) PRG1_PRU0_GPO5.RGMII1_RX_CTL
*/
                AM64X_IOPAD(0x0124, PIN_OUTPUT, 4) /* (V15) PRG1_PRU1_GPO7.RGMII1_TD0
*/
                AM64X_IOPAD(0x012c, PIN_OUTPUT, 4) /* (V14) PRG1_PRU1_GPO9.RGMII1_TD1
*/
                AM64X_IOPAD(0x0130, PIN_OUTPUT, 4) /* (W14)
PRG1_PRU1_GPO10.RGMII1_TD2 */
                AM64X_IOPAD(0x014c, PIN_OUTPUT, 4) /* (AA14)
PRG1_PRU1_GPO17.RGMII1_TD3 */
                AM64X_IOPAD(0x00e0, PIN_OUTPUT, 4) /* (U14)
PRG1_PRU0_GPO10.RGMII1_TXC */
```

```
                AM64X_IOPAD(0x00dc, PIN_OUTPUT, 4) /* (U15)
PRG1_PRU0_GPO9.RGMII1_TX_CTL */
            >;
        };

            rgmii2_pins_default: rgmii2-pins-default {
             pinctrl-single,pins = <
                AM64X_IOPAD(0x0108, PIN_INPUT, 4) /* (W11) PRG1_PRU1_GPO0.RGMII2_RD0
*/
                AM64X_IOPAD(0x010c, PIN_INPUT, 4) /* (V11) PRG1_PRU1_GPO1.RGMII2_RD1 */
                AM64X_IOPAD(0x0110, PIN_INPUT, 4) /* (AA12) PRG1_PRU1_GPO2.RGMII2_RD2
*/
                AM64X_IOPAD(0x0114, PIN_INPUT, 4) /* (Y12) PRG1_PRU1_GPO3.RGMII2_RD3 */
                AM64X_IOPAD(0x0120, PIN_INPUT, 4) /* (U11) PRG1_PRU1_GPO6.RGMII2_RXC */
                AM64X_IOPAD(0x0118, PIN_INPUT, 4) /* (W12)
PRG1_PRU1_GPO4.RGMII2_RX_CTL */
                AM64X_IOPAD(0x0134, PIN_OUTPUT, 4) /* (AA10)
PRG1_PRU1_GPO11.RGMII2_TD0 */
                AM64X_IOPAD(0x0138, PIN_OUTPUT, 4) /* (V10)
PRG1_PRU1_GPO12.RGMII2_TD1 */
                AM64X_IOPAD(0x013c, PIN_OUTPUT, 4) /* (U10)
PRG1_PRU1_GPO13.RGMII2_TD2 */
                AM64X_IOPAD(0x0140, PIN_OUTPUT, 4) /* (AA11)
PRG1_PRU1_GPO14.RGMII2_TD3 */
                AM64X_IOPAD(0x0148, PIN_OUTPUT, 4) /* (Y10) PRG1_PRU1_GPO16.RGMII2_TXC
*/
                AM64X_IOPAD(0x0144, PIN_OUTPUT, 4) /* (Y11)
PRG1_PRU1_GPO15.RGMII2_TX_CTL */
            >;
        };

        icssg0_mdio0_pins_default: icssg0_mdio_pins_default {
            pinctrl-single,pins = <
                AM64X_IOPAD(0x0204, PIN_OUTPUT, 0) /* (P3) PRG0_MDIO0_MDC */
                AM64X_IOPAD(0x0200, PIN_INPUT, 0) /* (P2) PRG0_MDIO0_MDIO */
            >;
        };

        pru_icssg0_mii_g_rt_pins_default: pru_icssg0_mii_g_rt_pins_default {
            pinctrl-single,pins = <
                AM64X_IOPAD(0x01a0, PIN_INPUT, 1) /* (U4)
PRG0_PRU0_GPO16.PR0_MII_MT0_CLK */
                AM64X_IOPAD(0x019c, PIN_OUTPUT, 0) /* (T5)
PRG0_PRU0_GPO15.PR0_MII0_TXEN */
```

```
		AM64X_IOPAD(0x0198, PIN_OUTPUT, 0) /* (V4) PRG0_PRU0_GPO14.PR0_MII0_TXD3 */
		AM64X_IOPAD(0x0194, PIN_OUTPUT, 0) /* (R6) PRG0_PRU0_GPO13.PR0_MII0_TXD2 */
		AM64X_IOPAD(0x0190, PIN_OUTPUT, 0) /* (AA3) PRG0_PRU0_GPO12.PR0_MII0_TXD1 */
		AM64X_IOPAD(0x018c, PIN_OUTPUT, 0) /* (Y3) PRG0_PRU0_GPO11.PR0_MII0_TXD0 */
		AM64X_IOPAD(0x0170, PIN_INPUT, 1) /* (AA2) PRG0_PRU0_GPO4.PR0_MII0_RXDV */
		AM64X_IOPAD(0x0178, PIN_INPUT, 1) /* (T3) PRG0_PRU0_GPO6.PR0_MII_MR0_CLK */
		AM64X_IOPAD(0x016c, PIN_INPUT, 1) /* (V2) PRG0_PRU0_GPO3.PR0_MII0_RXD3 */
		AM64X_IOPAD(0x0168, PIN_INPUT, 1) /* (U2) PRG0_PRU0_GPO2.PR0_MII0_RXD2 */
		AM64X_IOPAD(0x0188, PIN_INPUT, 1) /* (AA5) PRG0_PRU0_GPO10.PR0_MII0_CRS */
		AM64X_IOPAD(0x0174, PIN_INPUT, 1) /* (R3) PRG0_PRU0_GPO5.PR0_MII0_RXER */
		AM64X_IOPAD(0x0164, PIN_INPUT, 1) /* (R4) PRG0_PRU0_GPO1.PR0_MII0_RXD1 */
		AM64X_IOPAD(0x0160, PIN_INPUT, 1) /* (Y1) PRG0_PRU0_GPO0.PR0_MII0_RXD0 */
		AM64X_IOPAD(0x0184, PIN_INPUT, 1) /* (W6) PRG0_PRU0_GPO9.PR0_MII0_COL */
		AM64X_IOPAD(0x0180, PIN_INPUT, 1) /* (T2) PRG0_PRU0_GPO8.PR1_MII0_RXLINK */

		AM64X_IOPAD(0x01f0, PIN_INPUT, 1) /* (AA4) PRG0_PRU1_GPO16.PR0_MII_MT1_CLK */
		AM64X_IOPAD(0x01ec, PIN_OUTPUT, 0) /* (U5) PRG0_PRU1_GPO15.PR0_MII1_TXEN */
		AM64X_IOPAD(0x01e8, PIN_OUTPUT, 0) /* (U6) PRG0_PRU1_GPO14.PR0_MII1_TXD3 */
		AM64X_IOPAD(0x01e4, PIN_OUTPUT, 0) /* (T6) PRG0_PRU1_GPO13.PR0_MII1_TXD2 */
		AM64X_IOPAD(0x01e0, PIN_OUTPUT, 0) /* (Y4) PRG0_PRU1_GPO12.PR0_MII1_TXD1 */
		AM64X_IOPAD(0x01dc, PIN_OUTPUT, 0) /* (W4) PRG0_PRU1_GPO11.PR0_MII1_TXD0 */
		AM64X_IOPAD(0x01c0, PIN_INPUT, 1) /* (W3) PRG0_PRU1_GPO4.PR0_MII1_RXDV */
		AM64X_IOPAD(0x01c8, PIN_INPUT, 1) /* (R5)
```

```
PRG0_PRU1_GPO6.PR0_MII_MR1_CLK */
                AM64X_IOPAD(0x01bc, PIN_INPUT, 1) /* (T4) PRG0_PRU1_GPO3.PR0_MII1_RXD3
*/
                AM64X_IOPAD(0x01b8, PIN_INPUT, 1) /* (V3) PRG0_PRU1_GPO2.PR0_MII1_RXD2
*/
                AM64X_IOPAD(0x01d8, PIN_INPUT, 1) /* (V6) PRG0_PRU1_GPO10.PR0_MII1_CRS
*/
                AM64X_IOPAD(0x01c4, PIN_INPUT, 1) /* (P4) PRG0_PRU1_GPO5.PR0_MII1_RXER
*/
                AM64X_IOPAD(0x01b4, PIN_INPUT, 1) /* (W2)
PRG0_PRU1_GPO1.PR0_MII1_RXD1 */
                AM64X_IOPAD(0x01b0, PIN_INPUT, 1) /* (Y2) PRG0_PRU1_GPO0.PR0_MII1_RXD0
*/
                AM64X_IOPAD(0x01d4, PIN_INPUT, 1) /* (Y5) PRG0_PRU1_GPO9.PR0_MII1_COL
*/
                AM64X_IOPAD(0x01d0, PIN_INPUT, 1) /* (R1)
PRG0_PRU1_GPO8.PR0_MII1_RXLINK */
            >;
        };

        ospi0_pins_default: ospi0-pins-default {
            pinctrl-single,pins = <
                AM64X_IOPAD(0x0000, PIN_OUTPUT, 0) /* (N20) OSPI0_CLK */
                AM64X_IOPAD(0x002c, PIN_OUTPUT, 0) /* (L19) OSPI0_CSn0 */
                AM64X_IOPAD(0x000c, PIN_INPUT, 0) /* (M19) OSPI0_D0 */
                AM64X_IOPAD(0x0010, PIN_INPUT, 0) /* (M18) OSPI0_D1 */
                AM64X_IOPAD(0x0014, PIN_INPUT, 0) /* (M20) OSPI0_D2 */
                AM64X_IOPAD(0x0018, PIN_INPUT, 0) /* (M21) OSPI0_D3 */
                AM64X_IOPAD(0x001c, PIN_INPUT, 0) /* (P21) OSPI0_D4 */
                AM64X_IOPAD(0x0020, PIN_INPUT, 0) /* (P20) OSPI0_D5 */
                AM64X_IOPAD(0x0024, PIN_INPUT, 0) /* (N18) OSPI0_D6 */
                AM64X_IOPAD(0x0028, PIN_INPUT, 0) /* (M17) OSPI0_D7 */
                AM64X_IOPAD(0x0008, PIN_INPUT, 0) /* (N19) OSPI0_DQS */
            >;
        };

        main_mcan0_pins_default: main-mcan0-pins-default {
            pinctrl-single,pins = <
                AM64X_IOPAD(0x0254, PIN_INPUT, 0) /* (B17) MCAN0_RX */
                AM64X_IOPAD(0x0250, PIN_OUTPUT, 0) /* (A17) MCAN0_TX */
            >;
        };

        main_mcan1_pins_default: main-mcan1-pins-default {
```

```
            pinctrl-single,pins = <
                AM64X_IOPAD(0x025c, PIN_INPUT, 0) /* (D17) MCAN1_RX */
                AM64X_IOPAD(0x0258, PIN_OUTPUT, 0) /* (C17) MCAN1_TX */
            >;
        };

        usr_led_pins_default: usr-led-pins-default {
            pinctrl-single,pins = <
                AM64X_IOPAD(0x210, PIN_OUTPUT, 7) /* (D13) PRG1_PRU0_GPO15.GPIO1_44 */
            >;
        };
};

&main_gpio1 {
        pinctrl-names = "default";
        pinctrl-0 = <&di_do_pins_default>;
        status = "okay";
};

&main_uart0 {
        pinctrl-names = "default";
        pinctrl-0 = <&main_uart0_pins_default>;
};

/* main_uart1 is reserved for firmware usage */
&main_uart1 {
        pinctrl-names = "default";
        pinctrl-0 = <&main_uart1_pins_default>;
};

&main_uart2 {
        pinctrl-names = "default";
        pinctrl-0 = <&main_uart2_pins_default>;
};

&main_uart3 {
            status = "disabled";
};

&main_uart4 {
//      pinctrl-names = "default";
//      pinctrl-0 = <&main_uart4_pins_default>;
        status = "disabled";
};
```

```
&main_uart5 {
//     pinctrl-names = "default";
//     pinctrl-0 = <&main_uart5_pins_default>;
status = "disabled";
};

&main_uart6 {
//     pinctrl-names = "default";
//     pinctrl-0 = <&main_uart6_pins_default>;
            status = "disabled";
};

&mcu_uart0 {
        status = "disabled";
};

&mcu_uart1 {
        status = "disabled";
};

&main_i2c1 {
        status = "disabled";

};

/* mcu_gpio0 is reserved for mcu firmware usage */
&mcu_gpio0 {
        status = "reserved";
};

&mcu_i2c0 {
        status = "disabled";
};

&main_i2c0 {
        pinctrl-names = "default";
        pinctrl-0 = <&main_i2c0_pins_default>;
        clock-frequency = <400000>;
};
&mcu_i2c1 {
        status = "disabled";
};
```

```
&mcu_spi0 {
	status = "disabled";
};

&mcu_spi1 {
	status = "disabled";
};

&main_spi0 {
	status = "disabled";
};

&sdhci0 {
	/* emmc */
	bus-width = <8>;
	non-removable;
	ti,driver-strength-ohm = <50>;
	disable-wp;
};

&sdhci1 {
	/* SD/MMC */
	pinctrl-names = "default";
	bus-width = <4>;
	pinctrl-0 = <&main_mmc1_pins_default>;
	ti,driver-strength-ohm = <50>;
	disable-wp;
	no-1-8-v;
};

&serdes_wiz0
{
	status = "disabled";
};

&cpsw3g {
	pinctrl-names = "default";
	pinctrl-0 = <&mdio1_pins_default
			&rgmii1_pins_default
			&rgmii2_pins_default>;
		cpts@3d000 {
		ti,pps = <7 1>;
	};
};
```

```
&cpsw_port1 {
	phy-mode = "rgmii-rxid";
	phy-handle = <&cpsw3g_phy0>;
};

&cpsw_port2 {
	phy-mode = "rgmii-rxid";
	phy-handle = <&cpsw3g_phy1>;
};

&cpsw3g_mdio {
	cpsw3g_phy0: ethernet-phy@1 {
		reg = <1>;
		ti,rx-internal-delay = <DP83867_RGMIIDCTL_2_00_NS>;
		ti,fifo-depth = <DP83867_PHYCR_FIFO_DEPTH_4_B_NIB>;
	};

	cpsw3g_phy1: ethernet-phy@0 {
		reg = <0>;
		ti,rx-internal-delay = <DP83867_RGMIIDCTL_2_00_NS>;
		ti,fifo-depth = <DP83867_PHYCR_FIFO_DEPTH_4_B_NIB>;
	};
};

#define TS_OFFSET(pa, val)	(0x4+(pa)*4) (0x10000 | val)

&timesync_router {
	pinctrl-names = "default";
	pinctrl-0 = <&mcu_cpts_pps>;

	/* Example of the timesync routing */
	mcu_cpts_pps: mcu-cpts-pps {
		pinctrl-single,pins = <
			/* pps [cpts genf1] in22 -> out37 [cpts hw8_push] */
			TS_OFFSET(37, 22)
			/* pps [cpts genf1] in22 -> out25 [SYNC1_OUT pin] */
			TS_OFFSET(25, 22)
			>;
	};
};

/* set R5F subsystem 0 to single-CPU mode */
&main_r5fss0 {
```

```
        ti,cluster-mode = <2>;
};
&main_r5fss1 {
        ti,cluster-mode = <2>;
};

&mailbox0_cluster2 {
        mbox_main_r5fss0_core0: mbox-main-r5fss0-core0 {
                ti,mbox-rx = <0 0 2>;
                ti,mbox-tx = <1 0 2>;
        };

//      mbox_main_r5fss0_core1: mbox-main-r5fss0-core1 {
//              ti,mbox-rx = <2 0 2>;
//              ti,mbox-tx = <3 0 2>;
//      };
};

&mailbox0_cluster3 {
        status = "disabled";
};

&mailbox0_cluster4 {
        mbox_main_r5fss1_core0: mbox-main-r5fss1-core0 {
                ti,mbox-rx = <0 0 2>;
                ti,mbox-tx = <1 0 2>;
        };

//      mbox_main_r5fss1_core1: mbox-main-r5fss1-core1 {
//              ti,mbox-rx = <2 0 2>;
//              ti,mbox-tx = <3 0 2>;
//      };
};

&mailbox0_cluster5 {
        status = "disabled";
};

&mailbox0_cluster6 {
        mbox_m4_0: mbox-m4-0 {
                ti,mbox-rx = <0 0 2>;
                ti,mbox-tx = <1 0 2>;
        };
};
```

```
&mailbox0_cluster7 {
	status = "disabled";
};

&serdes_ln_ctrl {
	idle-states = <AM64_SERDES0_LANE0_PCIE0>;
};

&serdes0 {
	status = "disabled";
};

&pcie0_rc {
	status = "disabled";
};

&pcie0_ep {
	status = "disabled";
};

&tscadc0 {
	/* ADC is reserved for R5 usage */
	status = "reserved";
};

&ospi0 {
	pinctrl-names = "default";
	pinctrl-0 = <&ospi0_pins_default>;

	flash@0{
		compatible = "jedec,spi-nor";
		reg = <0x0>;
		spi-tx-bus-width = <8>;
		spi-rx-bus-width = <8>;
		spi-max-frequency = <25000000>;
		cdns,tshsl-ns = <60>;
		cdns,tsd2d-ns = <60>;
		cdns,tchsh-ns = <60>;
		cdns,tslch-ns = <60>;
		cdns,read-delay = <4>;
		cdns,phy-mode;
		#address-cells = <1>;
		#size-cells = <1>;
```

```
        };
};

&main_mcan0 {
        status = "okay";
        pinctrl-names = "default";
        pinctrl-0 = <&main_mcan0_pins_default>;
        phys = <&transceiver1>;
};

&main_mcan1 {
        status = "okay";
        pinctrl-names = "default";
        pinctrl-0 = <&main_mcan1_pins_default>;
        phys = <&transceiver2>;
};

&icssg0_mdio {
        status = "okay";
        pinctrl-names = "default";
        pinctrl-0 = <&icssg0_mdio0_pins_default>;

        icssg0_phy1: ethernet-phy@3 {
                reg = <0x3>;
                tx-internal-delay-ps = <250>;
                rx-internal-delay-ps = <2000>;
        };
//      icssg0_phy2: ethernet-phy@4 {
//              reg = <0x4>;
//              tx-internal-delay-ps = <250>;
//              rx-internal-delay-ps = <2000>;
//      };
};

&icssg1_mdio {
        status = "disabled";
};
```