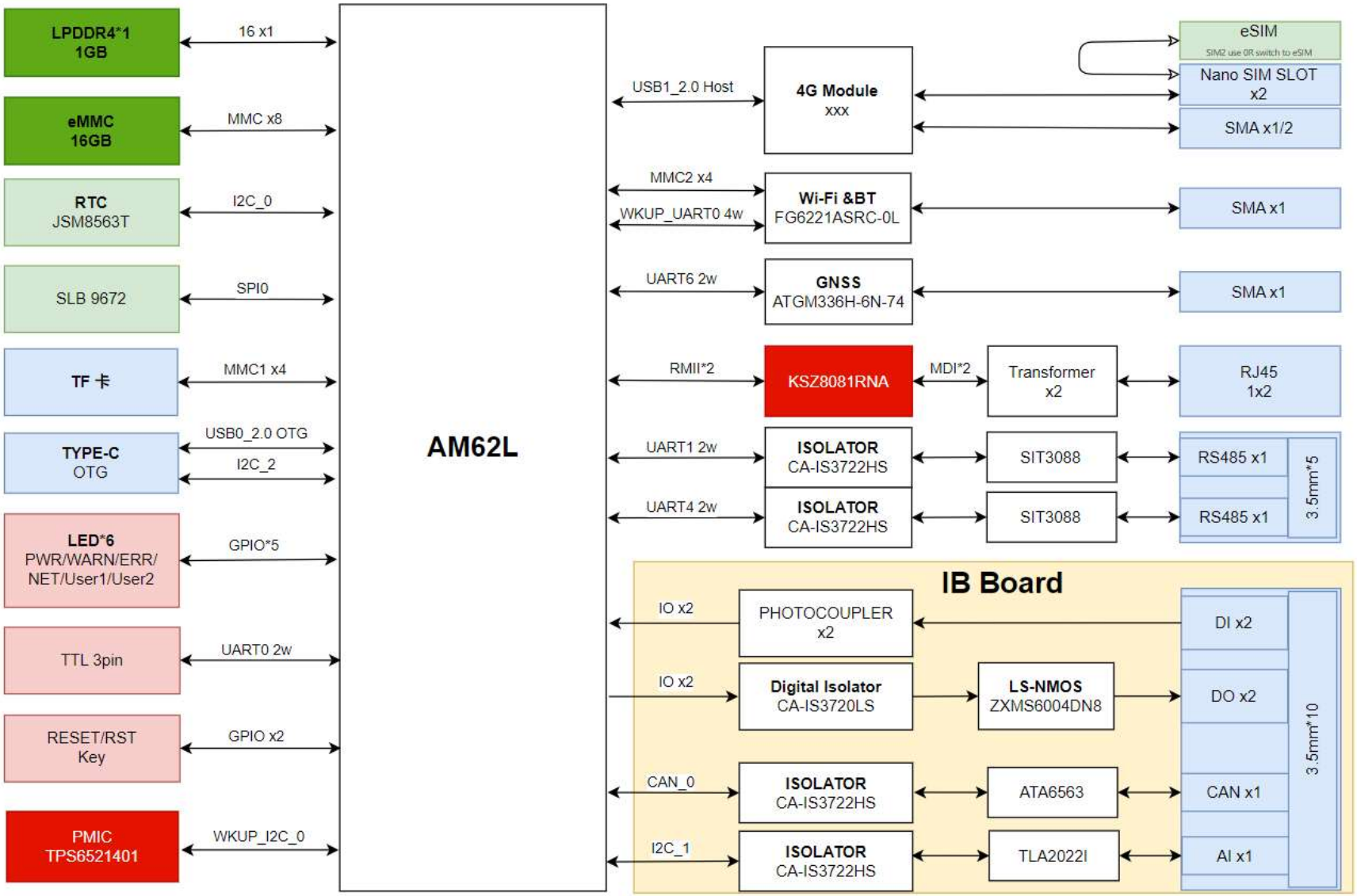
BLOCK DIAGRAM - AM62L EVM



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Project:			
File:	03. BLOCK DGM AM62L-EVM	Size:	
Date:	Saturday, September 06, 2025	Rev:	V1.0
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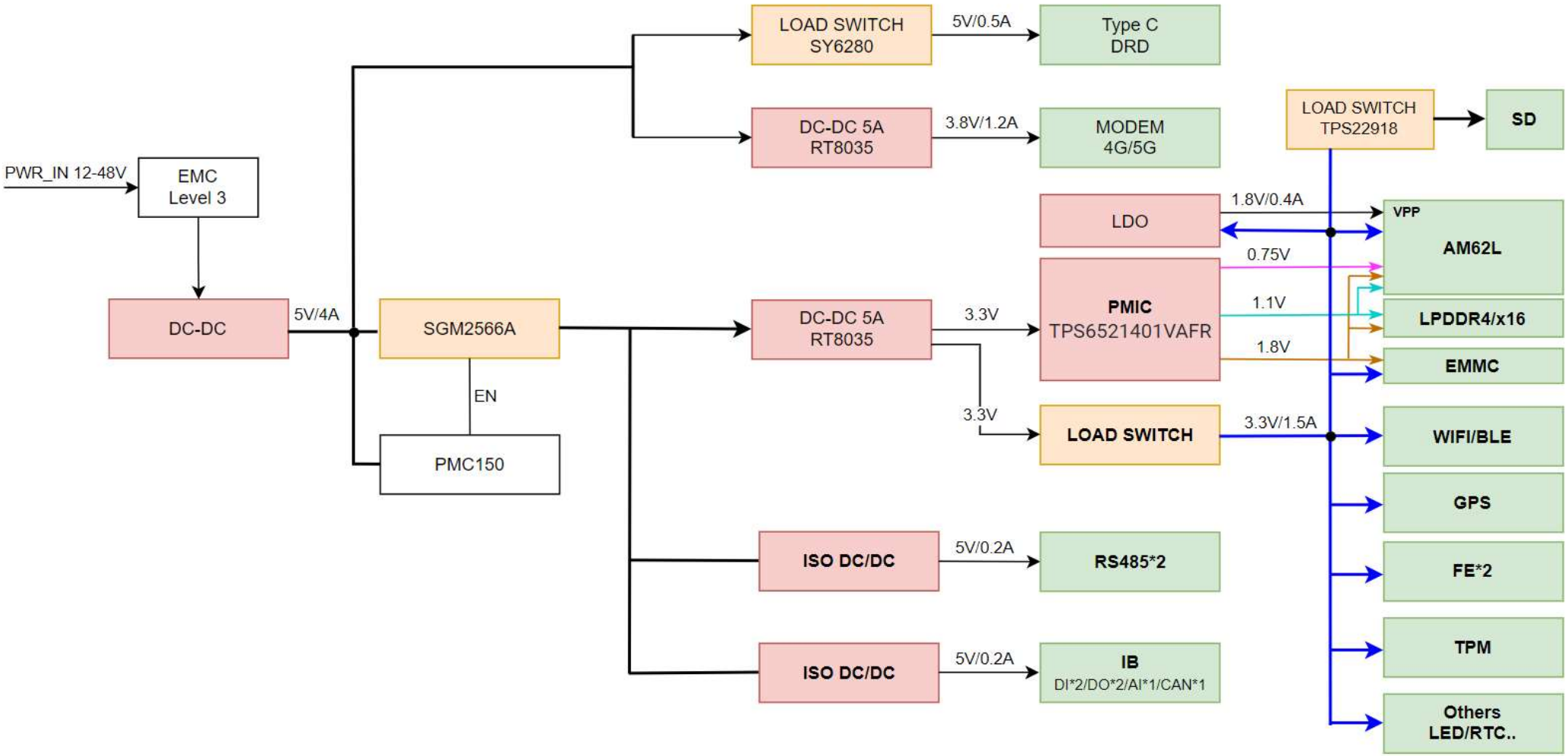
POWER ARCHITECTURE BLOCK DIAGRAM



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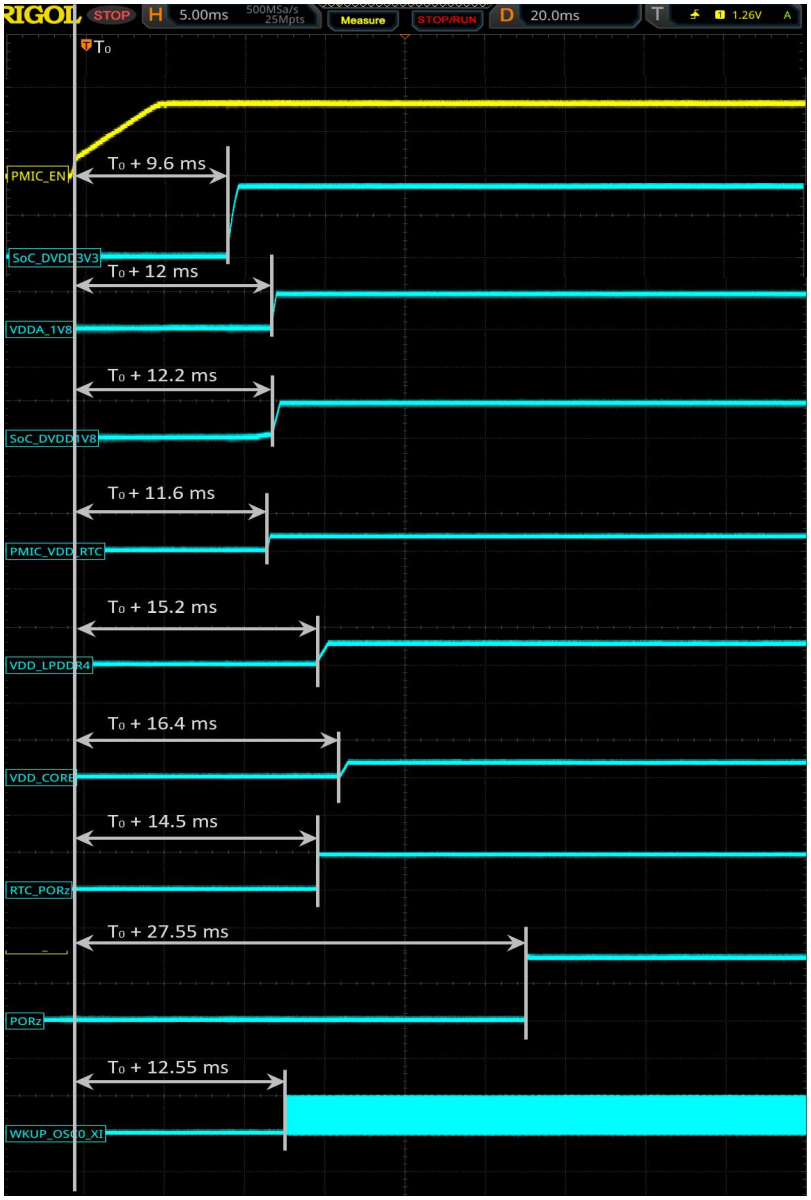
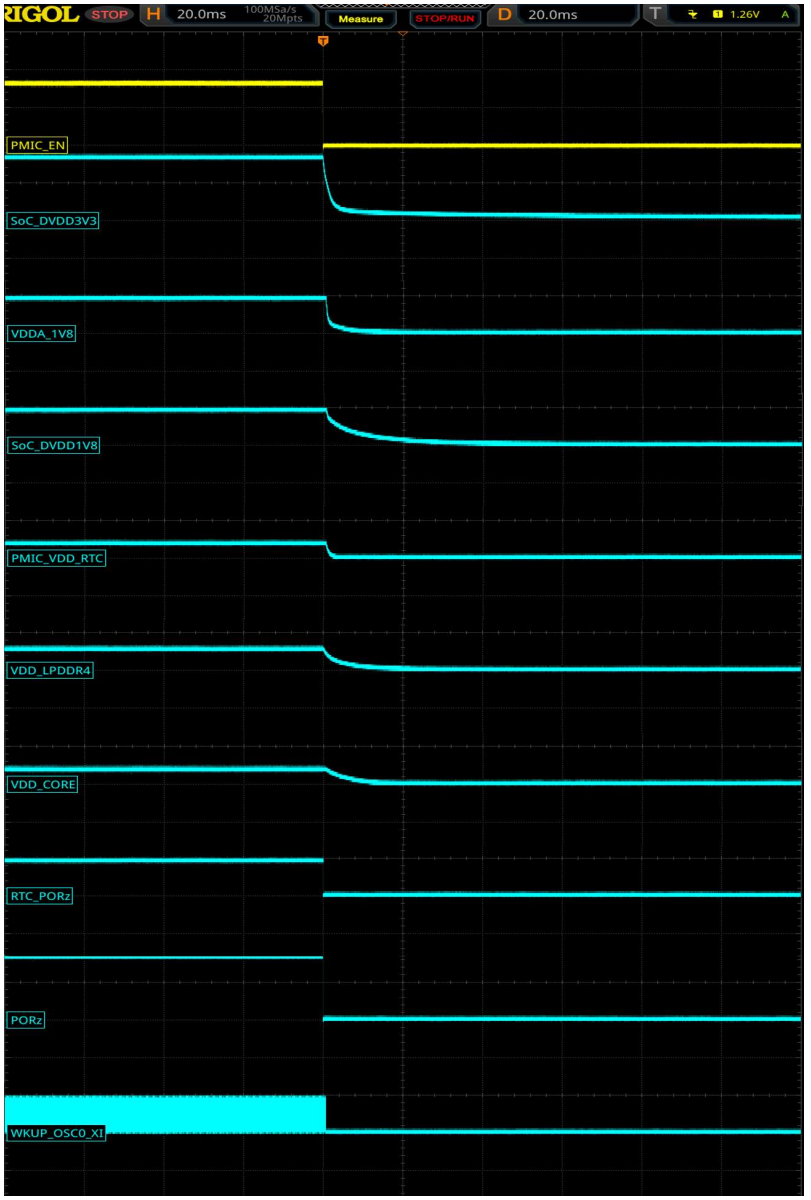
Project:			
File:	04. POWER BLOCK DGM	Size:	
Date:	Saturday, September 06, 2025	Rev:	V1.0
Designed by:	Reviewed by:	Sheet:	4 of 32

POWER SEQUENCE - RTC + IO + DDR MODE

POWER-UP SEQUENCE



POWER-DOWN SEQUENCE



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Project:			
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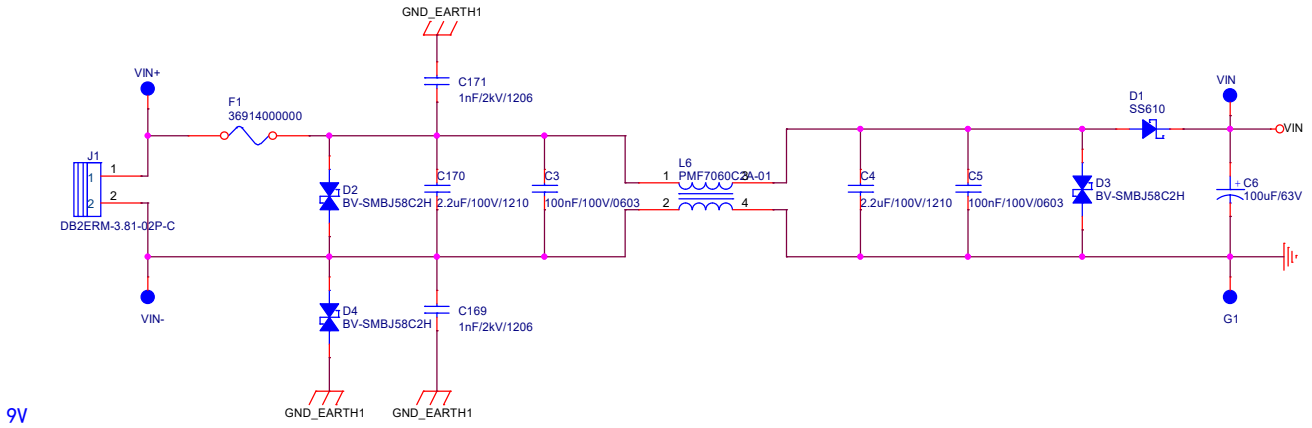
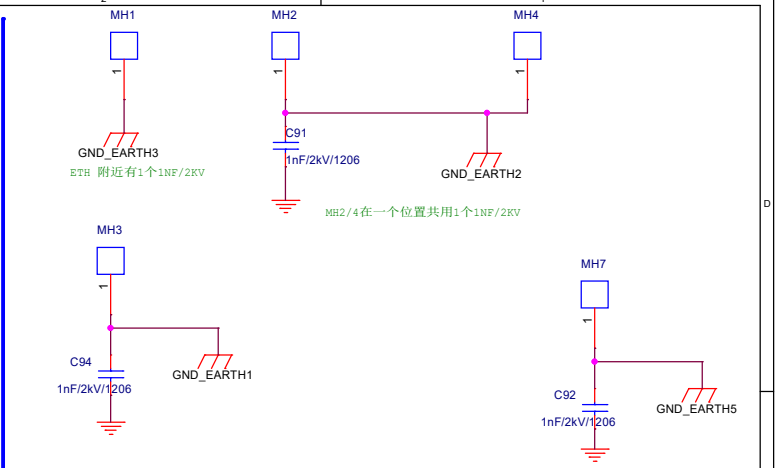
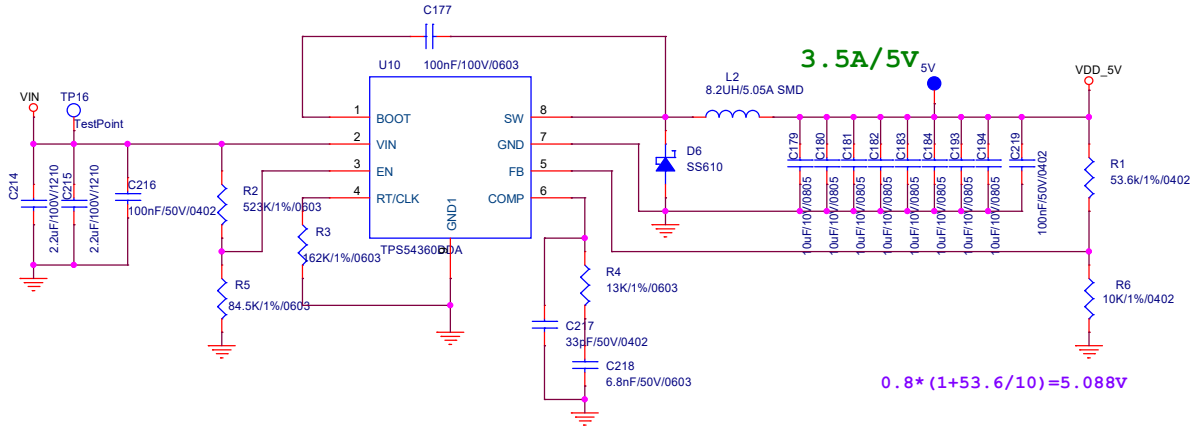
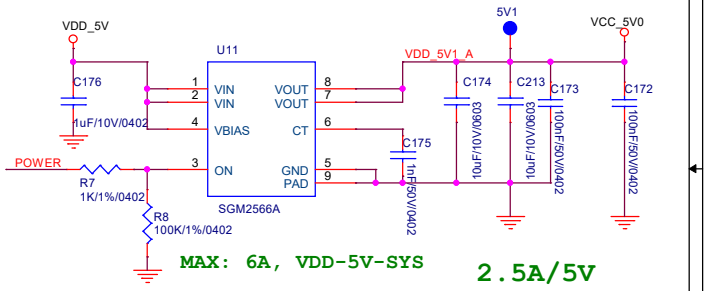
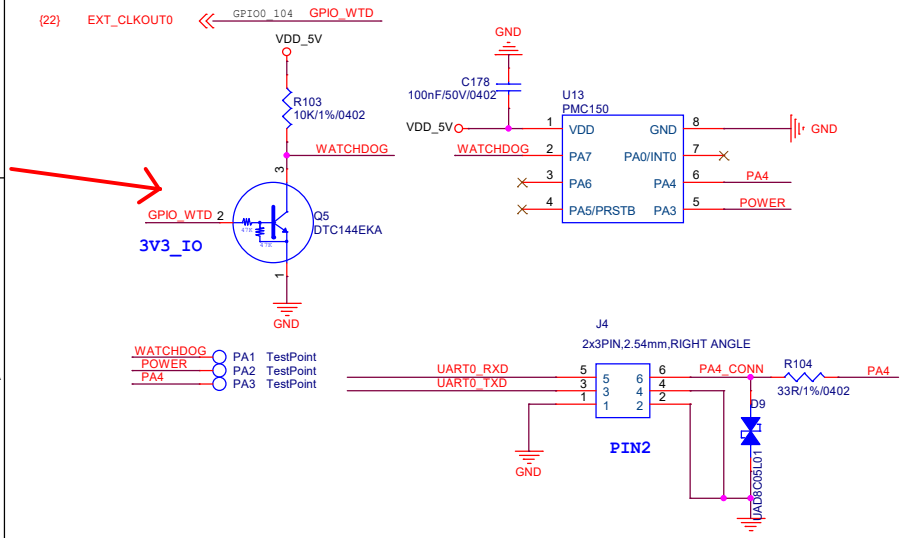
Date:	Saturday, September 06, 2025	Rev:	V1.0
Designed by:	Reviewed by:	Sheet:	5 of 32

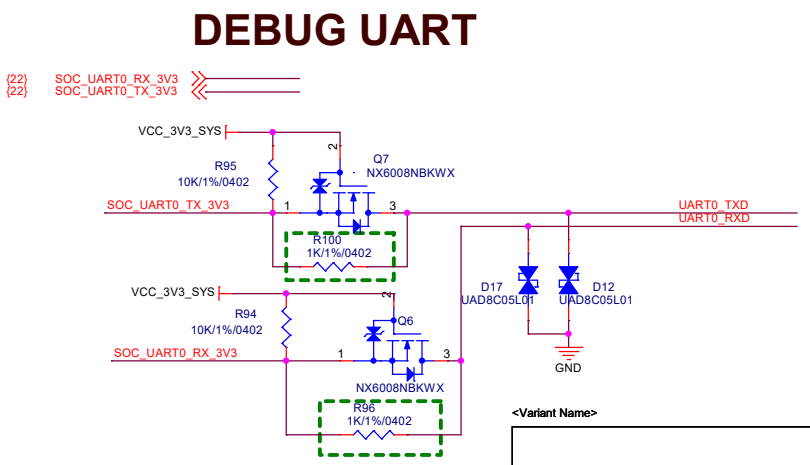












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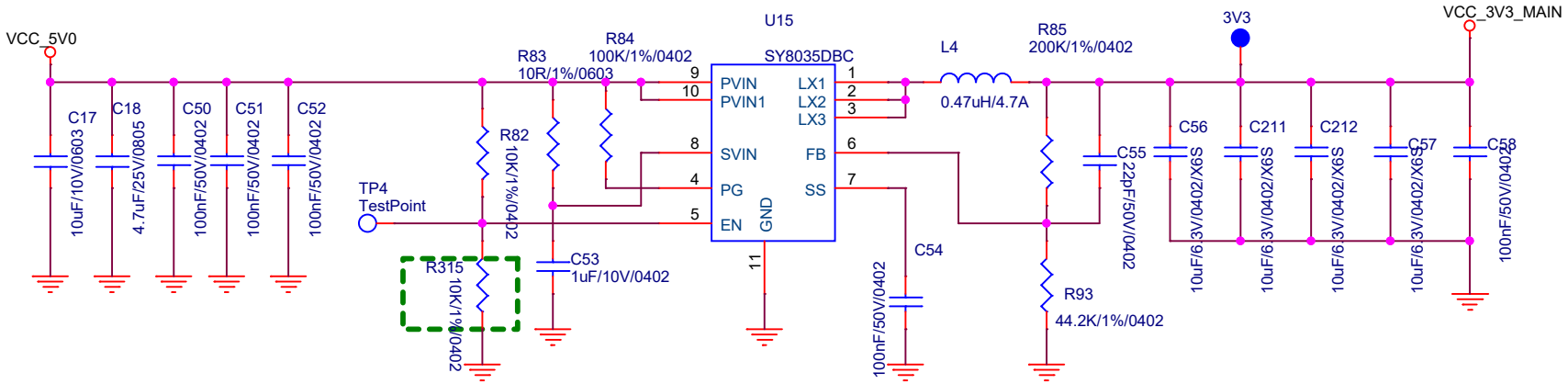
Project:			
File:	06. Main Power&VCC5V&WDT&DEBUG	Size:	
Date:		Rev:	V1.0
Designed by:		Reviewed by:	Sheet: 6 of 32

PRE REGULATOR POWER SUPPLY-1

3.3V, 5.0 AMPS SUPPLY

3.5A/3.3V



0.6*(200/44.2+1)=3.315V

<Variant Name>

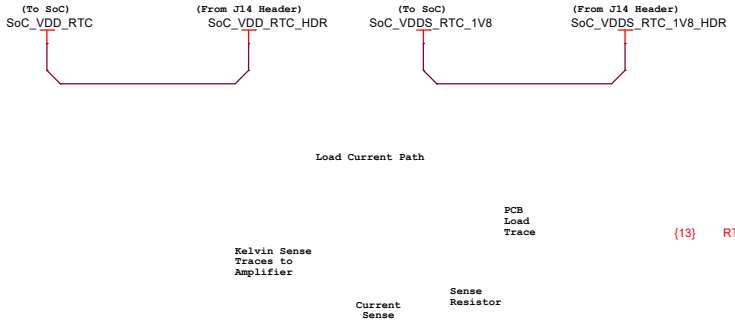
<Doc1>			
Project:			
File:	07. POWER-3V3	Size:	
Date:	Saturday, September 06, 2025	Rev:	V1.0
Designed by:	Reviewed by:	Sheet:	7 of 32

LOW POWER MODE CONFIGURATION

D-Note:-
The enable pin of the discrete RTC supply (LDO) can be driven by the power-good signal of the regulator generating the main supply rail (VCC_3V3_MAIN). In case the regulator does not support a PG signal- output, a resistor pulled up to the LDO supply input can be used as EN input.

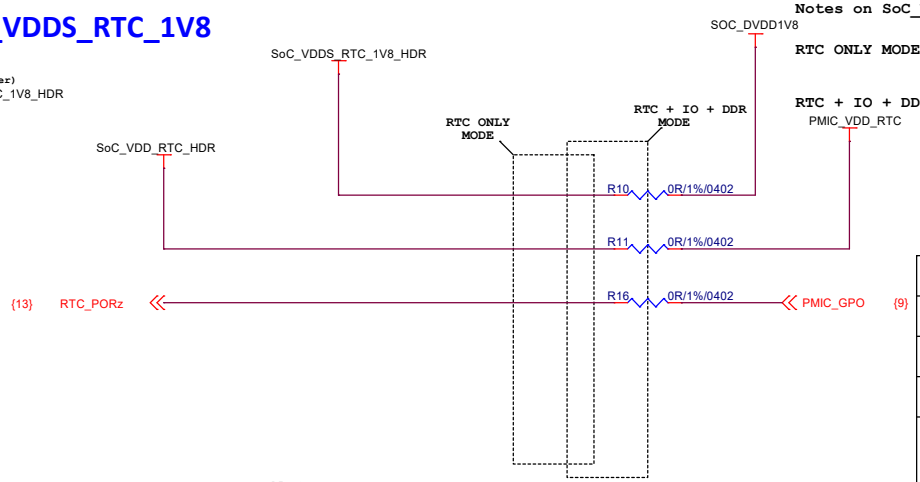
D-Note:-
Adjust RTC_PG pullup value to minimize the output slew.
Keep the RTC_PG to RTC_PORz PCB trace short to minimize trace capacitance. Adjust the value of the external pullup resistor when an open-drain output PG is used as reset input to RTC_PORz. The RTC_PORz input has internal hysteresis and the internal reset could glitch when a slow rising input is applied. The slew rate is recommended to be faster than the limits specified in the LVCMOS IO buffer electrical specification to minimize possible noise coupling.

CURRENT SENSE RESISTOR FOR SoC_VDD_RTC AND SoC_VDDS_RTC_1V8



CAD NOTE:
Follow Kelvin current sense routing for RTC supplies current sense resistor (R505 and R516). Follow the routing shown in the above figure that has been added as reference for kelvin current sense routing.

RTC SUPPLY SELECTION



Notes on SoC_VDD_RTC and SoC_VDDS_RTC_1V8 supply source:

RTC ONLY MODE - external discrete LDOs U113 (for SoC_VDDS_RTC_1V8) and U107 (for SoC_VDD_RTC) are used

RTC + IO + DDR MODE - PMIC Buck2 (for SoC_VDDS_RTC_1V8) and LDO1 (in case of PMIC1 - TPS65215 is used)/ LDO2(in case of PMIC2 - TPS65214 is used) (for SoC_VDD_RTC) are used

Note:
Use 5x2 Female gang jumper to select the mode

RTC Only MODE	TO SOC	RTC + IO + DDR MODE
VDDS_RTC_1V8	SoC_VDDS_RTC_1V8	SOC_DVDD1V8
VDD_RTC	SoC_VDD_RTC	PMIC_VDD_RTC
RTC_PG	RTC_PORz	PMIC_GPO
RTC_PG	PMIC1_RESET (To PMIC 1)	DGND
DGND	PMIC_LPM_SEL	NC

RTC_PG TO PORz_INPUT OPEN DRAIN BUFFER

LOW POWER MODE TRIGGER SELECTION

D-Note:-
In use cases where TMUX154EDGSR is used to support multiple power modes configuration, a glitch can be observed on the output A during power-up when the EVM is configured for RTC Only mode. The analog switch is optional since the custom board is designed to support a fixed, specific low power mode.

D-Note:-
PMIC_LPM_SEL is generated based on 5x2 Female gang jumper configuration. By default the MUX SEL pin is high and PMIC_LPM_EN0 drives the PMIC STBY pin to turn-OFF the CORE and VDDA to support RTC + IO + DDR Mode. When the MUX SEL pin is low, the PMIC_LPM_EN0 drives the PMIC enable pin to support "RTC only". In this low power mode, the entire PMIC is turned-OFF and the RTC domain is supplied by external always-ON LDOs.

nEN	SEL	OUTPUT & MODE	
L	L	A=A0 B=B0	RTC ONLY MODE
L	H (DEFAULT)	A=A1 B=B1	RTC + IO + DDR MODE

<Variant Name>

<Doc1>			
Project:			
File:	08. LOW POWER MODE CONFIG- LDOs	Size:	
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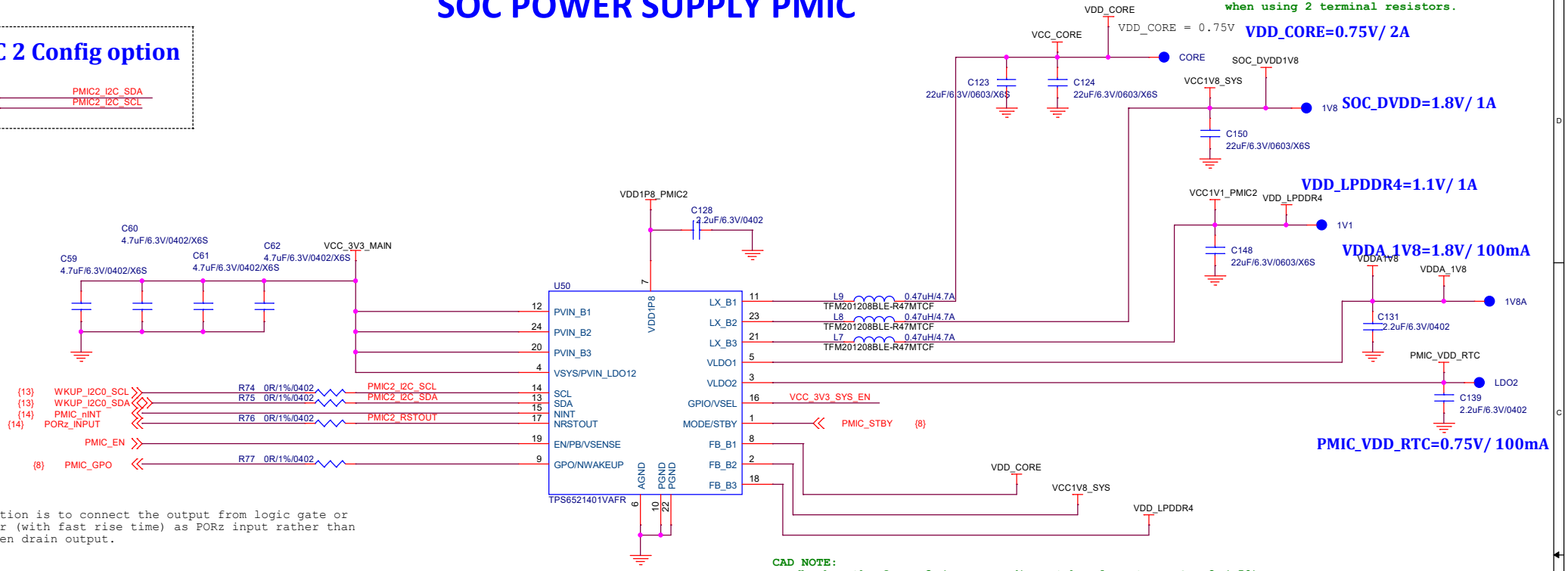
SOC POWER SUPPLY PMIC

CAD Note:
Follow Kelvin connection for current sensing when using 2 terminal resistors.

PMIC 2 Config option

TP96 — PMIC2_I2C_SDA
TP98 — PMIC2_I2C_SCL



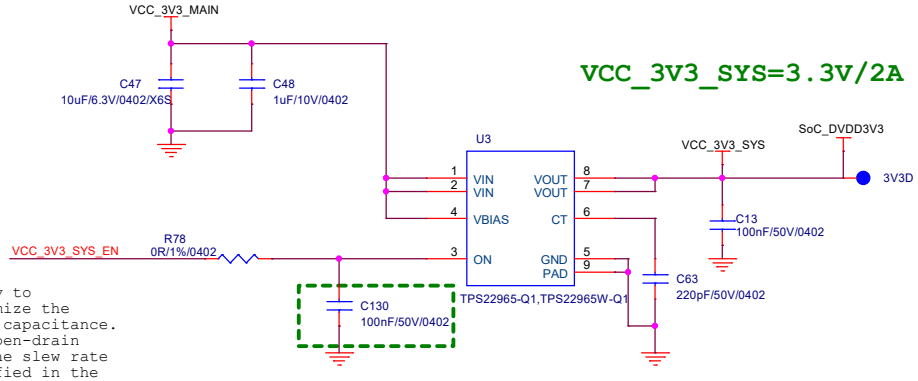
D-Note:-
PORz_INPUT
The recommendation is to connect the output from logic gate or discrete buffer (with fast rise time) as PORz input rather than slow rising open drain output.

CAD NOTE:
Feedback path of FB_B3 (VDD_LPDDR4) must be close to PMIC - 2 (U50)

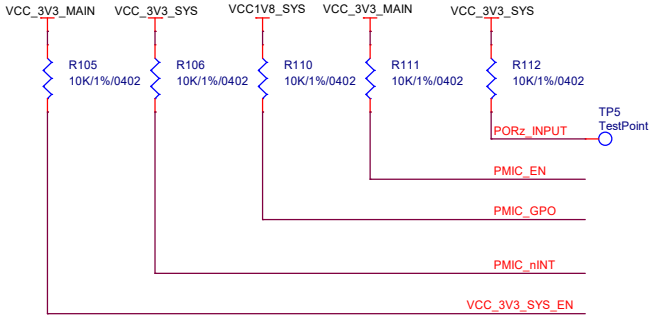
D-Note:-
PORz inputs have slew rate requirements specified. When PMIC nRSTOUT is connected to PORz. Adjust the pull-up to minimize the rise time (100-200 ns) when using an open drain output. PORz is fail-safe and 3.3 V tolerant. The PORz input can be connected to 1.8 V or 3.3 V.

VCC_3V3_SYS LOAD SWITCH

VCC_3V3_SYS=3.3V/2A



COMMON PULL-UPS OF PMIC - 1 AND PMIC - 2



D-Note:-
PORz_INPUT
When nRSTOUT from the PMIC is connected directly to PORz input, adjust nRSTOUT pullup value to minimize the slew. Keep the PCB trace short to minimize trace capacitance. Adjust the external pullup value when using an open-drain output to meet the processor slew requirement. The slew rate is recommended to be faster than the limit specified in the IO buffer electrical specification to minimize possible noise coupling. The recommendation is to connect nRSTOUT through a discrete Schmitt trigger push pull output buffer to the PORz input of the processor. The PORz input has internal hysteresis and the internal reset could glitch when a slow rising input is applied.

<Variant Name>

<Doc1>			
Project:			
File:	09. PMIC&3V3 load sw	Size:	
Date:	Saturday, September 06, 2025	Rev:	V1.0
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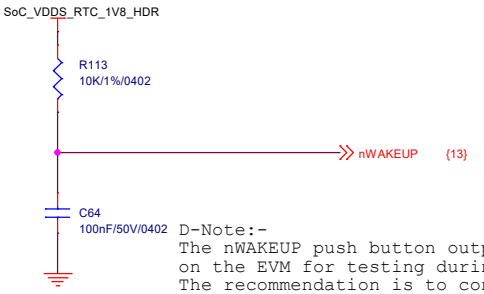
nWAKEUP REQUEST PUSH BUTTON



D-Note:-
The nWAKEUP push button output has been provided on the EVM for testing during software development. The recommendation is to connect the nWAKEUP signal to the processor EXT_WAKEUP0, EXT_WAKEUP1 inputs through a Schmitt trigger based debounce logic (Refer RESET & INT DEBOUNCE CIRCUIT) when reused on the custom board.

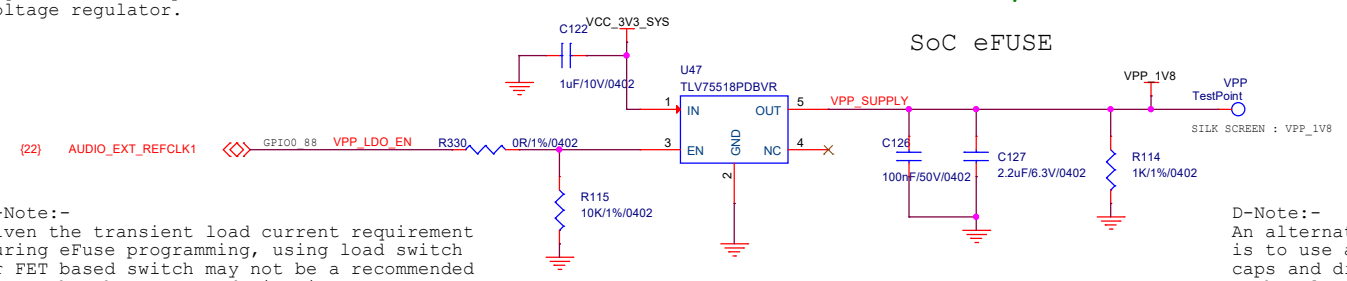
1.8V VPP (eFUSE), 0.5AMPS SUPPLY

D-Note:-
Alternate part suggestion TPS7A21-Q1, Automotive, 500mA, low-noise ultra-low-IQ high-PSRR low-dropout (LDO) voltage regulator.

D-Note:-
Okay to use VCC_3V3_MAIN

VPP=1.8V/0.4A

SoC eFUSE



D-Note:-
The recommendation is to select an LDO with fast load transient current response and connect the LDO output to the VPP supply pin with low loop inductance path to ensure the LDO is able to source the large transient load current, where the VPP supply is within the ROC when programming the eFuse.

D-Note:-
Given the transient load current requirement during eFuse programming, using load switch or FET based switch may not be a recommended approach. The recommendation is to use an LDO with fast load current transient response and quick output discharge that can be enabled by processor IO. A load switch or FET based switch is likely to have too much voltage drop (out of processor VPP supply ROC) that can't be compensated like when using an LDO.

D-Note:-
An alternate way to source the VPP supply is to use an external supply. The recommended caps and discharge resistor are recommended to be placed near to the SOC VPP supply pin. One of the SOC GPIO output can be used to control the timing of the external power supply output.

<Variant Name>

<Doc1>			
Project:			
File:	10. PUSH BUTTON & VPP	Size:	
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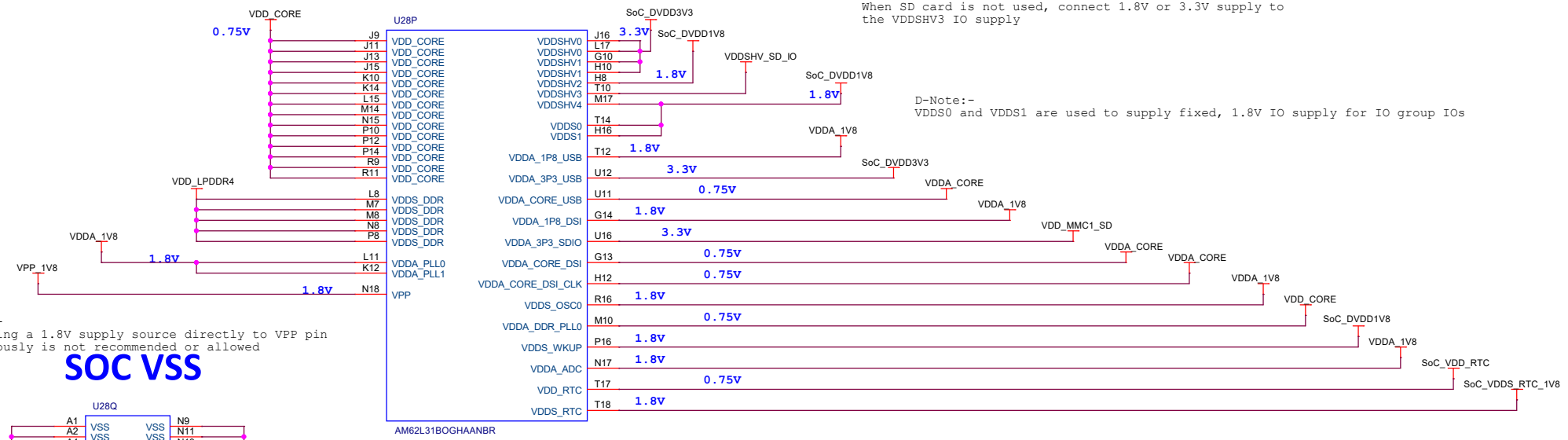
SOC POWER SUPPLIES AND SUPPLY RAILS

D-Note:-
A Trace connected to SOC pad (IO) is effectively an antenna that can pick up noise.
A potential will be generated on the trace when noise couples into the antenna.
This potential will be largest on the highest impedance end of the trace. By placing a pull-up or pull-down near the SoC pin (input), we force the highest potential to the open-circuit end of the trace rather than the SoC IO end of the trace.

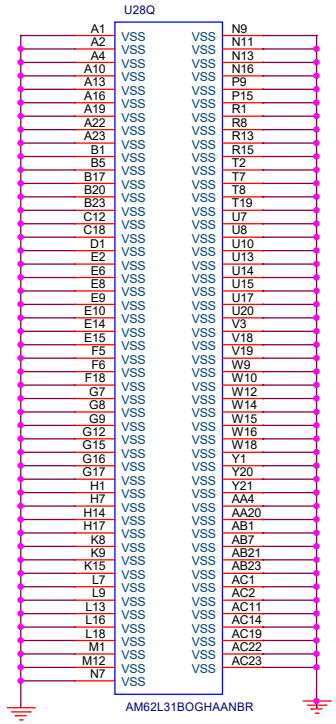


D-Note:-
When SD card is not used, connect 1.8V or 3.3V supply to the VDDSHV3 IO supply

D-Note:-
VDDS0 and VDDS1 are used to supply fixed, 1.8V IO supply for IO group IOs

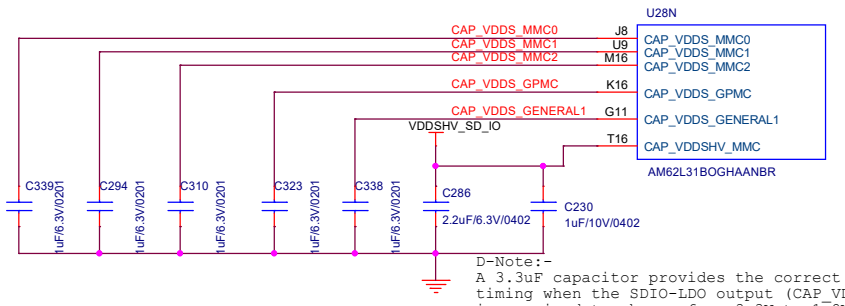
D-Note:-
Connecting a 1.8V supply source directly to VPP pin continuously is not recommended or allowed

SOC VSS



D-Note:-
Refer pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used. It is acceptable to have the supplies connected and all the USB pins left unconnected provided the USB driver is not initialized any time and the USB calibration procedure does not happen. Grounding the USB supplies as per pin connectivity requirements when not used saves power when low power is a critical requirement.

D-Note:-
Common SOC LVCMOS IO interface guidelines
1. Most of the SOC IOs are not fail-safe. No input should be applied before SOC supplies ramps.
2. SOC LVCMOS inputs have minimum slew rate requirements specified
3. SOC IO buffers are off during Reset and after Reset. A pull is required in case SOC IOs or the attached device inputs could float.
4. Any SOC IO that has a trace connected and not being actively driven needs a parallel pull. When adding pull is not feasible, ensure the traces are routed away from noisy signals



D-Note:-
A 3.3uF capacitor provides the correct voltage transition timing when the SDIO-LDO output (CAP_VDDSHV_MMC1) is required to change from 3.3V to 1.8V. A 4.7uF capacitor may not be discharged from 3.3V to 1.8V before communications with the SD card resumes after it is told to change IO operating voltage.

D-Note:-
Select capacitor with ESR < 1 ohm
Ensure the PCB loop inductance is < 2.5 nH
Select 0201 package or smallest possible package nearest to 0201
Refer SOC Data sheet

<Variant Name>

<Doc1>

Project:			
File:	11. SOC POWER SUPPLIES	Size:	
Date:	Saturday, September 06, 2025	Rev:	V1.0
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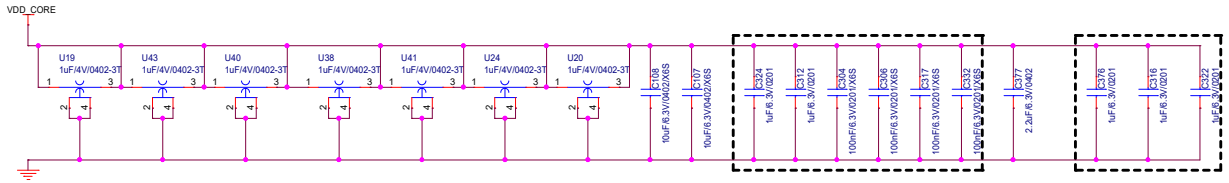
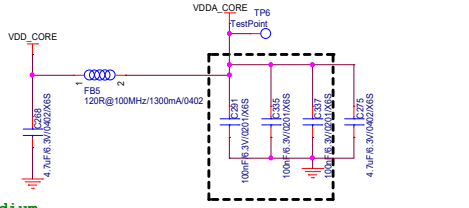
SOC POWER SUPPLIES - DECAPS



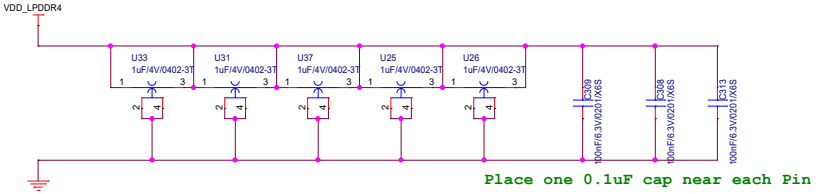
Decap placement priority:- Medium, Place under BGA footprint after placing High priority decaps

Decap placement priority:- Medium, Place under BGA footprint after placing High priority decaps

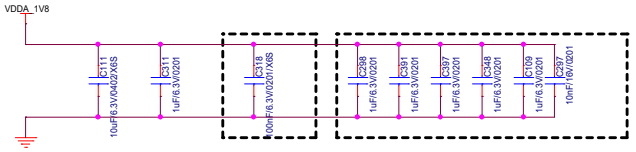
Place one 0.1uF cap near each Pin



Decap placement priority:- Medium, Place under BGA footprint after placing High priority decaps

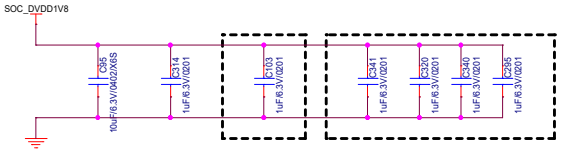


Place one 0.1uF cap near each Pin



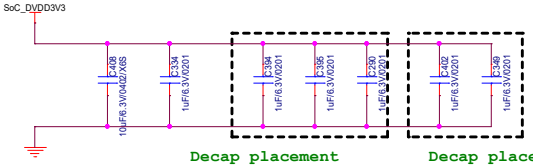
Decap placement priority:- High, place under BGA footprint

Decap placement priority:- Medium, Place under BGA footprint after placing High priority decaps



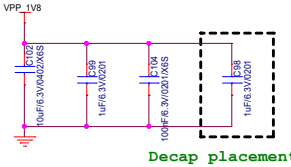
Decap placement priority:- Low, Place under BGA footprint after placing High and medium priority decaps

Decap placement priority:- High, place under BGA footprint

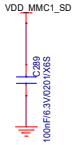


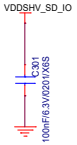
Decap placement priority:- High, place under BGA footprint

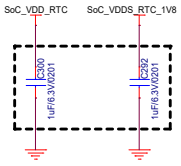
Decap placement priority:- Medium, Place under BGA footprint after placing High priority decaps



Decap placement priority:- Low, Place under BGA footprint after placing High and medium priority decaps







Decap placement priority:- Low, Place under BGA footprint after placing High and medium priority decaps

R-Note:-
Use of 3 terminal caps optimizes use of bulk caps quantity and minimizes the PCB loop inductance

<Variant Name>

<Doc1>			
Project:			
File:	12. SOC POWER SUPPLIES - DECAPS	Size:	
Date:	Saturday, September 06, 2025	Rev:	V1.0
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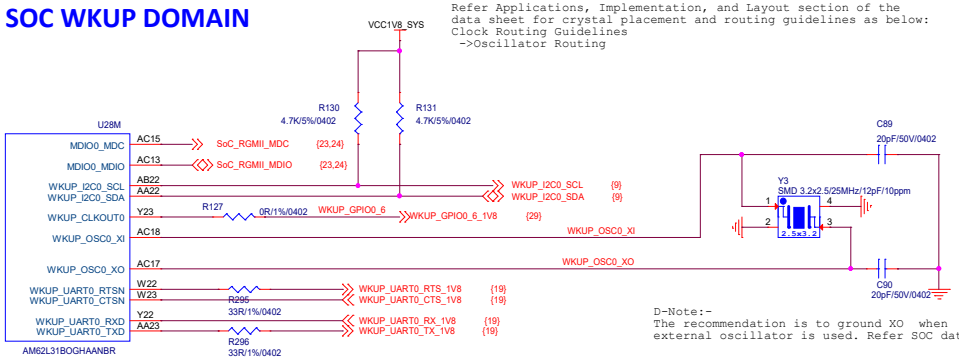
SOC WKUP DOMAIN



D-Note:-
Refer Applications, Implementation, and Layout section of the
data sheet for crystal placement and routing guidelines as below:
Clock Routing Guidelines
->Oscillator Routing

D-Note:-
The recommendation is to ground XO when
external oscillator is used. Refer SOC data sheet

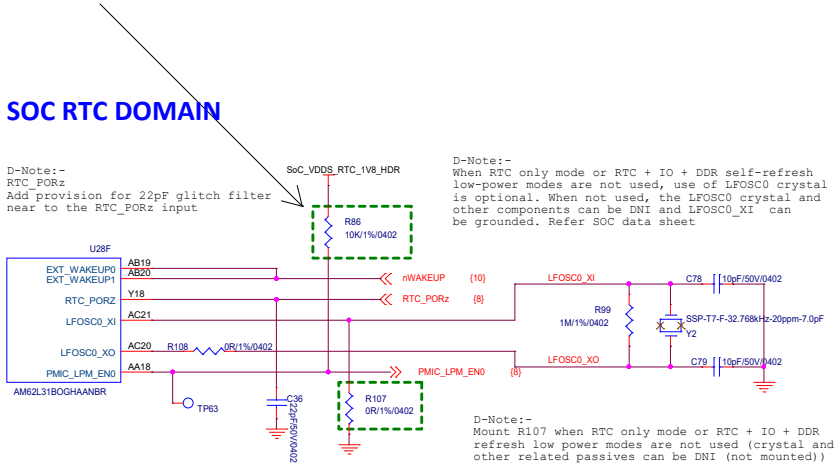
D-Note:-
The processor performance has been validated only
with a 25 MHz Crystal/clock source connected to
WKUP_OSC0 (25 MHz is the only clock frequency
supported). The data sheet shows WKUP_OSC0 not
starting until after the core voltage because there
are some cases where the oscillator may not start until
VDD_CORE is valid. In most cases the oscillator will
start as early as VDDS_OSC0, but this may not always
be the case. This diagram in the data sheet is showing
the maximum start-up time, which must include the case
where the delay is based on VDD_CORE being valid.

D-Note:-
The recommendation is to connect the 25 MHz crystal directly to the SOC XI and XO
pins (no series or parallel resistors are recommended).
The internal oscillator implements AGC (Automatic Gain Control) for amplitude control
The recommendation is to match the SOC crystal and the EPHY crystal specifications

D-Note:-
No WKUP_OSC0 registers are required to be changed. These
registers should remain in their default state.
Select the appropriate crystal circuit components that are
compliant to the values defined in the WKUP_OSC0 Crystal
Circuit Requirements table. Read the Load Capacitance and
Shunt Capacitance sections to select the appropriate
crystal circuit components.

处理器性能仅通过连接到WKUP_OSC0的25 MHz晶体/时钟源进行了验证（25 MHz是唯一支持的时钟频率）。
数据表显示，WKUP_OSC0在核心电压之后才会启动，因为在某些情况下，振荡器可能在VDD_core有效之前不会启动。
在大多数情况下，振荡器最早会在VDDS_OSC0启动，但并非总是如此。
数据表中的此图显示了最大启动时间，其中必须包括延迟基于VDD_CORE有效的情况。

SOC RTC DOMAIN



D-Note:-
RTC_PORz
Add provision for 22pF glitch filter
near to the RTC_PORz input

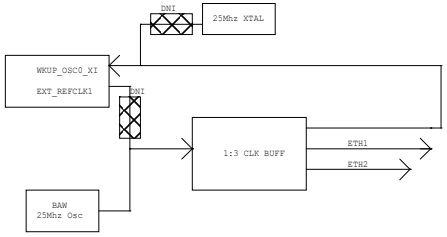
D-Note:-
When RTC only mode or RTC + IO + DDR self-refresh
low-power modes are not used, use of LFOSC0 crystal
is optional. When not used, the LFOSC0 crystal and
other components can be DNI and LFOSC0_XI can
be grounded. Refer SOC data sheet

D-Note:-
Mount R107 when RTC only mode or RTC + IO + DDR
refresh low power modes are not used (crystal and
other related passives can be DNI (not mounted))

D-Note:-
Refer SOC data sheet for the recommended LFOSC0 circuit configuration during
preproduction PCB and the production PCB

D-Note:-
The only LFOSC0 register bits that should be changed by the customer are
BP_C, PD_C, and RTC_RTC_LFXOSC_TRIM[18:16],where PD_C is reset (0) to
enable the oscillator and the BP_C bit is only set (1) to place the
oscillator in bypass mode when using an LVCMOS clock source.The
RTC_RTC_LFXOSC_TRIM[18:16] bits are set based on the actual capacitance
load applied to the crystal, as defined by the Load Capacitance Equation.
The load capacitance range of the crystal will be half of the recommended
capacitor value range since there are connected in series with the crystals
resonate circuit.

OSCILLATOR



D-Note:-
SOC data sheet section for LVCMOS specifications:
WKUP_OSC0 LVCMOS Digital Clock Source Requirements
Match the SOC and the EPHY clock specs

SOC & ETHERNET PHY CLOCK BUFFER

D-Note:-
R74 pulldown is populated when crystal option
is used to clock the SOC and SOC clock output
is used as the clocking option for EPHY.
The Pulldown holds the Buffer input low
(EPHY clock input) until the SOC clock output
is configured. When crystal option is used to
clock the SOC (WKUP_OSC0), DNI SOC_CLKIN series
resistor that is connected to the WKUP_OSC0 Xi.

D-注：-
当晶体选项用于对SOC进行计时，并且SOC时钟输出用作EPHY的计时选项时，R74下拉填充。
下拉将缓冲器输入保持为低电平（EPHY时钟输入），直到配置SOC时钟输出。
当晶体选项用于对SOC（WKUP_OSC0）进行计时时，DNI SOC_CLKIN串联电阻器连接到WKUP_OSC 0 Xi。

<Variant Name>

<Doc1>			
Project:			
File:	13. SOC WKUP DOMAIN& OSCILLATOR	Size:	
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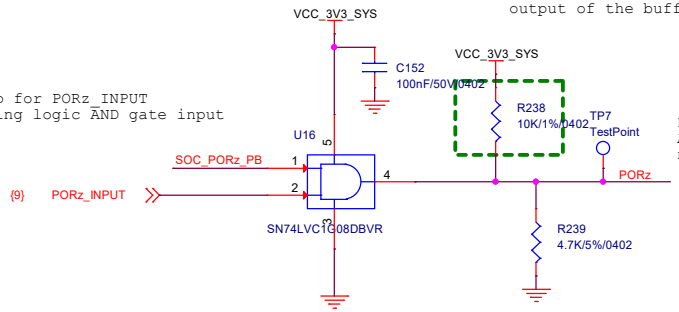
SOC RESET

POWER ON RESET

D-Note:-
Not connecting a valid PORz input could cause unpredictable and probably random behaviour, since the processor is not getting a valid reset, internal circuits could be in random states. Slow rising reset signal could cause glitches internal to the SOC reset circuit. Use of discrete buffer and having the fast rising output of the buffer drive the PORz is recommended

D-Note:-
Place the pullup for PORz_INPUT near to the ANDing logic AND gate input

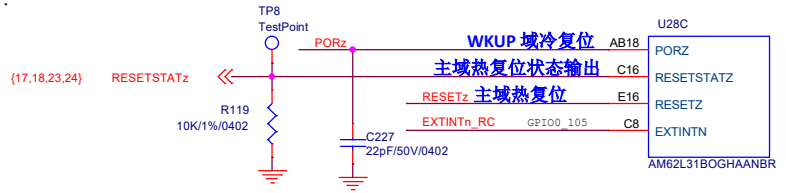


D-Note:-
Add provision for 22pF glitch filter near to the SOC PORz input pin

Note on Open-drain outputs:
XDS_PORZn, VCC_3V3_MAIN_PG, RTC_PG, PMIC_RSTOUT and PMIC1_GPIO (5 output signals) have been tied together as PORz_INPUT

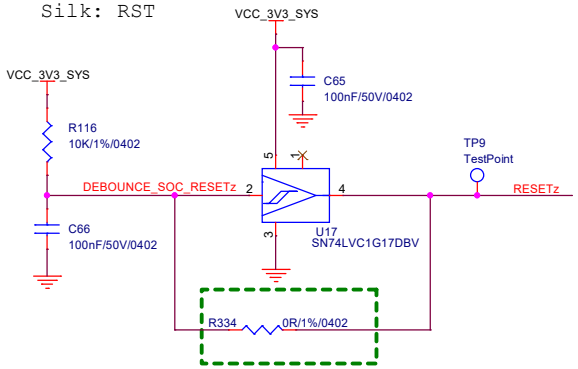
D-Note:-
PORz input is 3.3V tolerant.
PORz ANDing logic AND gate supply is connected to VCC_3V3_SYS. This is within the PORz fail-safe input range.

SOC - RESET

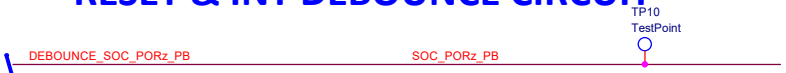


D-Note:-
Open drain output type IO EXTINTn has slew rate limit specified when pulled to 3.3V supply. An RC is recommended at the input. Refer TMDS64EVM.

SOC WARM RESETz PUSH BUTTON



RESET & INT DEBOUNCE CIRCUIT



Processor LVCMOS IOS (inputs) have slew rate requirement specified.
A Schmitt trigger based debouncing logic is recommended for the slow ramp pushbutton output (+ RC) connected to the processor warm reset inputs.
Debouncing logic is recommended when push button + RC or RC is used at the LVCMOS inputs.

SOC PORz RESET PUSH BUTTON

<Variant Name>

<Doc1>			
Project:			
File:	14. SOC RESET	Size:	
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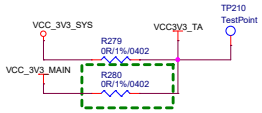
BOOT MODE SWITCHES

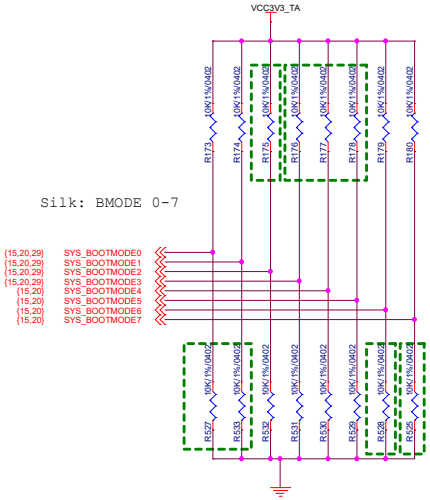


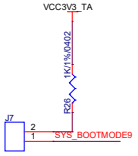
D-NOTE:-
The device supports the following BOOTMODE pin mapping options:
1. Reduced Pincount - Using only 4 of the bootstrap pins BOOTMODE[15:12]
2. Full Pincount - Using all 16 of the bootstrap pins BOOTMODE[15:0]
3. Configuring the reduced pincount bootmode resistors to boot from eFuse

FULL PINCOUNT SWITCHES

D-Note:-
To reduce the number of resistors used for bootmode configuration (pullup/pulldown) when using reduced pin count bootmode, the input buffers for BOOTMODE[11:0] inputs (pins) are disabled during POR (cold reset) unless BOOTMODE[15:14] are configured as '00' (Full pincount bootmode).

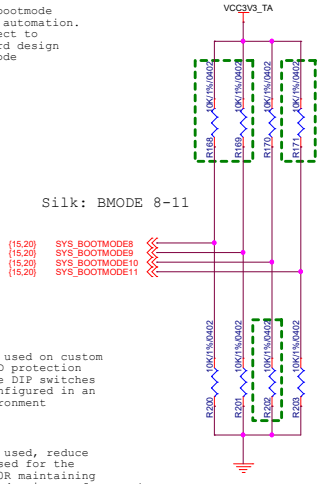
D-Note:-
VCC3V3_TA supply is used for bootmode configuration to support test automation. The recommendation is to connect to SoC_DVDD3V3 on the custom board design when test automation or bootmode buffers are not used.





D-Note:-
When dip switches are used on custom board, an external ESD protection may be required if the DIP switches are expected to be configured in an uncontrolled ESD environment

D-Note:-
When DIP switches are used, reduce the resistor values used for the divider to 47K and 470R maintaining the ratio (for improved noise performance)



D-Note:-
Full Pincount bootmode configuration circuit including pullup, pulldown resistors and DIP switches, buffers are optional when reduced pincount bootmode configuration is used

D-Note:-
Dip switch is optional and used for ease of configuration. A pullup or pulldown resistor can be used to set the BOOTMODE configuration Provide provision for Pullup and Pulldown resistors for the bootmode pins that have configuration capability

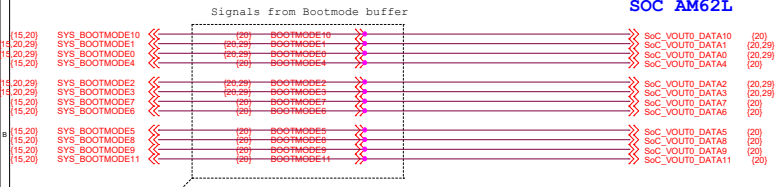
B9 :Port为0从emmc启动，Port为1从SD卡启动
B7=1,0:Filesystem mode, 1: Raw Mode (选1)

B6/B5/B4/b3=1000 : MMCSD Boot

B2/B1/B0=011: 25MHz

BOOTMODE PINS

SOC AM62L



D-Note:-
Connect SYS_BOOTMODE signals when bootmode buffers are not used

D-NOTE:-
1. 1K Resistor at the output of the buffer is recommended
2. Replace 1K Resistor at the output of the buffer with resistor of value 0E when bootmode buffers are not used

Reference clock selections may be limited by the device. Please consult the device specific datasheet to determine which system clock frequencies are valid.

Table 5-5. PLL Reference Clock Selection

PLL Config Pins			Ref Clock (MHz)
B2	B1	B0	
0	1	1	25

5.3.3.1 Primary Boot Mode Selection and Configuration

The primary boot mode is the first mode attempted after reset. Table 5-6 lists all possible primary boot modes.

Table 5-6. Primary Boot Mode Selection

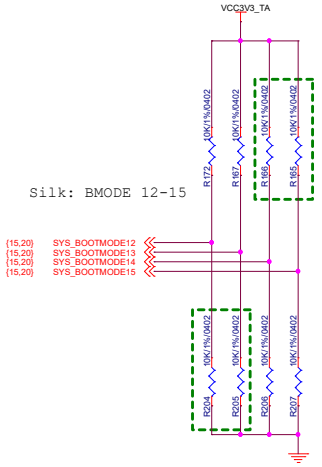
Primary Boot Mode Config							Primary Boot Mode
B9	B8	B7	B6	B5	B4	B3	
Reserved	Read Mode 2	Read Mode 1	0	0	0	0	Serial NAND
Reserved	Reserved	Csel	0	0	0	1	OSPI
Reserved	Reserved	Csel	0	0	1	0	QSPI
Reserved	Mode	Csel	0	0	1	1	SPI
Reserved	Reserved	0	0	1	1	1	UART
Port	Reserved	Fs/raw	1	0	0	0	MMCSD Boot (SD Card Boot or eMMC Boot using UDA)
Reserved	Reserved	Reserved	1	0	0	1	eMMC Boot
Reserved	Mode	Lane Swap	1	0	1	0	USB
Reserved	Reserved	Timing	1	0	1	1	GPMC NAND
SFPD	Read Cmd	Mode	1	1	1	0	xSPI
Reserved	Reserved	No/Dev	1	1	1	1	no-boot/Dev boot

3.4. PLL配置

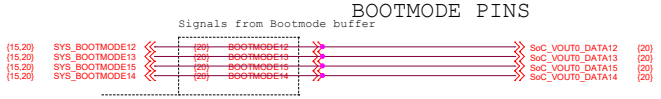
B2	B1	B0	Ref Clock(MHz)
0	0	0	19.2
0	0	1	20
0	1	0	24
0	1	1	25
1	0	0	26
1	0	1	27
1	1	0	Reserved
1	1	1	Reserved

D-Note:-
Boot from eFuse can be configured using the reduced pin count bootmode configuration.

REDUCED PINCOUNT SWITCH



BOOTMODE PINS



D-Note:-
Connect SYS_BOOTMODE signals when bootmode buffers are not used

D-NOTE:-
1. 1K Resistor at the output of the buffer is recommended
2. Replace 1K Resistor at the output of the buffer with resistor of value 0E when bootmode buffers are not used

B15/B14=00: Full Pincount
B13/B12/B11/B10=1101 : MMCSD Boot(SD Card boot)

Backup Mode里B13:port=1,当emmc没固件时从SD卡启动

5.3.3.2 Backup Boot Mode Selection and Configuration

The backup boot mode is selected via pins within the main BOOTMODE map. Table 5-7 lists all possible backup boot modes.

Table 5-7. Backup Mode Selection

Backup Boot Config	Backup Boot Mode Selection			Backup Boot Mode Selected
B13	B12	B11	B10	
Reserved	0	0	0	None
Mode	0	0	1	USB [lane swap = 0]
Reserved	0	1	0	Reserved
0	0	1	1	UART
Port	1	0	1	MMCSD Boot (SD Card Boot or eMMC Boot) [mode=0]
Reserved	1	1	0	SPI [csel=0, mode=0]

5.4 Boot Modes

BOOT MODES SUPPORTED

1. eMMC
2. OSPI
3. MMC1 ?uSD Card
4. UART
5. USB0 DFU
6. USB0 MS

FAQs FOR BOOTMODE CONFIGURATION (WITH BUFFER OR WITHOUT BUFFER)

https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1391522/faq-am625-am623-am644x-am243x-am62a-am62p-am62d-q1-am621---bootmode-implementation-without-buffers

https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1414148/faq-am625-am623-am644x-am243x-am62a-am62p-am62d-q1-am621---bootmode-implementation-with-buffers

<Variant Name>
<Doc1>

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File:	15. BOOT MODE SWITCHES	Size:	
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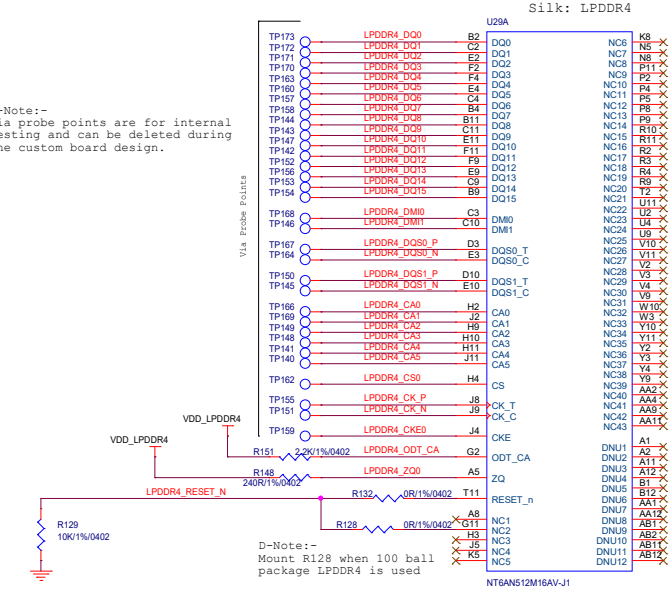
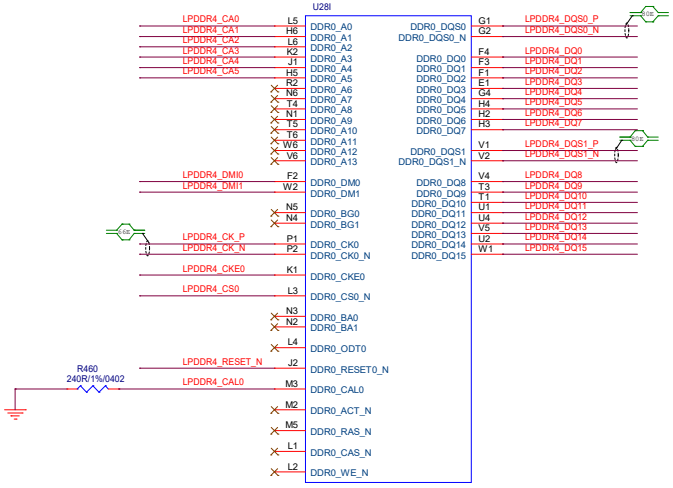
LPDDR4 DEVICE

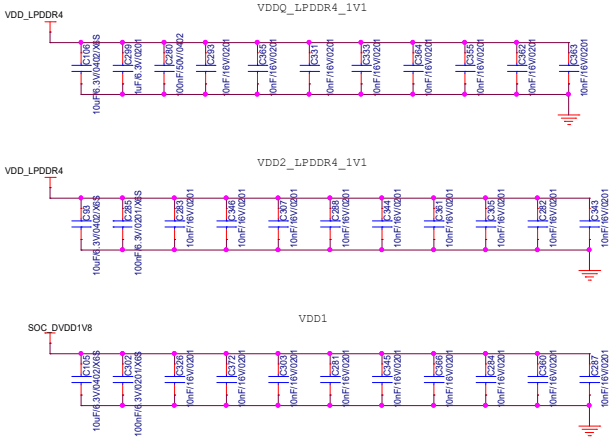


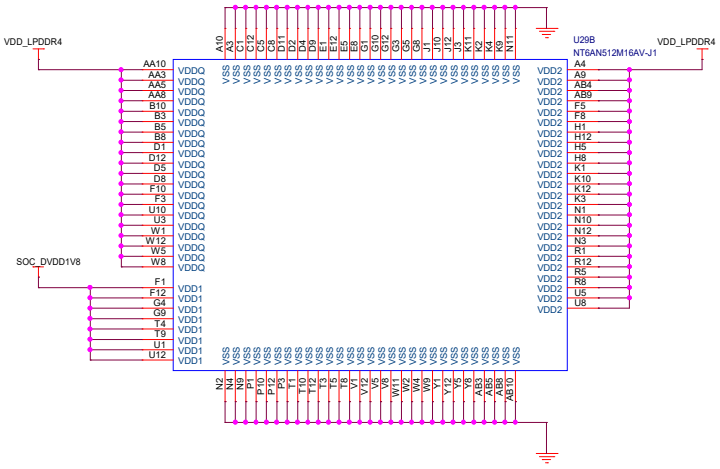
D-Note:-
Use 10K pulldown for the LPDDR4 attached device reset signal (pin) LPDDR4_RESET_N
Refer processor family specific DDR design guide

SOC LPDDR4 INTERFACE



LPDDR4 POWER DECAPS





<Variant Name>

<Doc1>

Project:			
File:	16. SOC DDR AND LPDDR4 DEVICE	Size:	
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eMMC INTERFACE

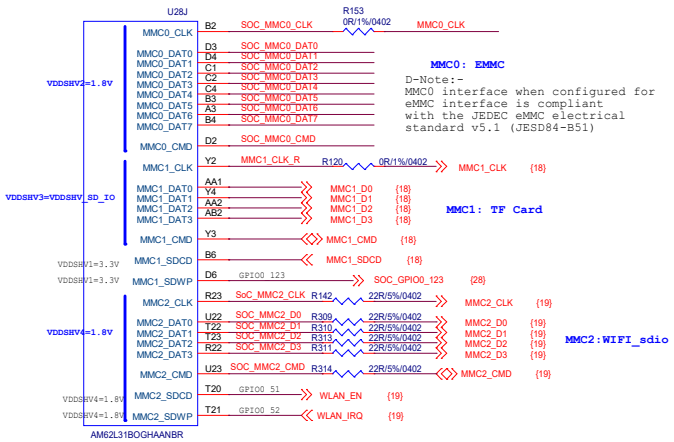
换32GB TLC？？？

SOC - MMC Interface

D-Note:-
Series resistor (0E) provision on MMC0_CLK is recommended to control reflections (for addressing signal integrity related concerns)

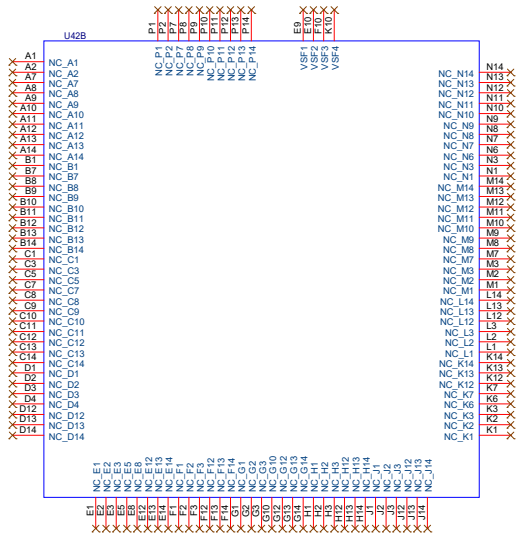
D-Note:-
The processor family implements a soft PHY for eMMC interface. The pulls required for D0, Clock and other eMMC interface control signals are recommended to be implemented externally

D-Note:-
The JEDEC eMMC electrical standard v5.1 (JESD84-B51) requires all eMMC devices to have an internal pull-up that is turned on by default for each DAT[7:1] pin. The eMMC device will turn off the internal pulls on DAT[7:1] when it is configured to operate in 8-bit mode or turn off the internal pulls on DAT[3:1] when it is configured to operate in 4-bit mode. The software driver should turn on the respective AM62x internal pull-ups at the same time it configures the eMMC device to operate in 8-bit mode or 4-bit mode. This ensures the signals are not floating when not driven. External pull-ups are not necessary on the DAT[7:1] signals as long as the software driver is turning on the respective AM62x pull-ups at the appropriate time.



D-Note:-
The processor IOs associated with the MMC0 port will be turned off until software initializes them. This means any signals without internal pulls will be floating until software boots and initializes the IOs. The JEDEC eMMC electrical standard v5.1 (JESD84-B51) requires the eMMC device to have internal pulls on the DAT[7:1] pins, but the other pins do not have internal pulls. We recommend external pull-ups on the CMD and DAT0 signals and an external pull-down on the CLK signal. The eMMC standard also says 10k pull-ups are the min value, so we do not recommend using a 10k resistor because it may be less than 10k. We typically recommend using 47k resistors to minimize loading on the signals since the pulls are only used to hold the signals in a valid logic state when not driven.

eMMC FLASH

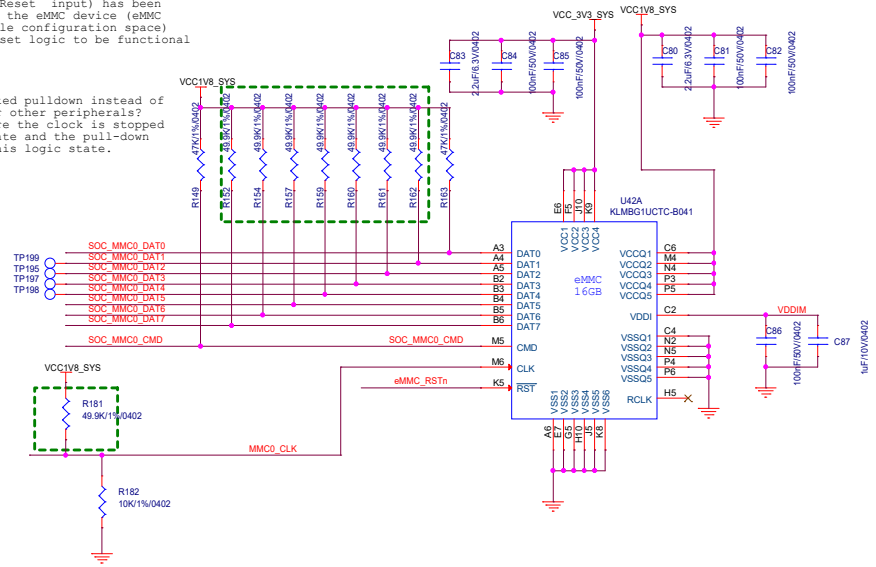


D-Note:-
Ensure eMMC_RSTn (RST_N) pin function (Reset input) has been enabled in the eMMC device (eMMC non-volatile configuration space) for the reset logic to be functional

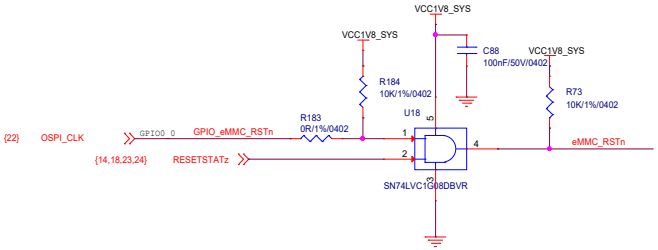
D-Note:-
Use case for GPIO input to the ANDing logic :
The GPIO reset option makes it possible for software to reset the attached device (eMMC or OSPI or SD card or EPHY) without resetting the entire processor if there is a case where the peripheral becomes unresponsive.

R-Note:-
What is the reason we selected pulldown instead of pullup for EMMC, SD card or other peripherals? Because there are cases where the clock is stopped or paused in a low logic state and the pull-down option is consistent with this logic state.

D-Note:-
Use case for ANDing logic :
You could eliminate the GPIO option and only use the reset output (Warm), where software forces a warm reset if the peripheral becomes unresponsive. However, this will reset the entire device rather than trying to recover the specific peripheral without resetting the entire device.



eMMC FLASH RESET



D-Note:-
In case ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level. A resistor divider could be used alternatively for level translation, provided optimum impedance value of the resistor divider is selected. If too high value is used for the resistors, the rise/fall time of the eMMC reset input could be slow and introduce too much delay. If resistor value used is too low it will cause the AM62Lx to source too much steady-state current during normal operation.

D-Note:-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect PMIC (SOC) operation

<Variant Name>

<Doc1>			
Project:			
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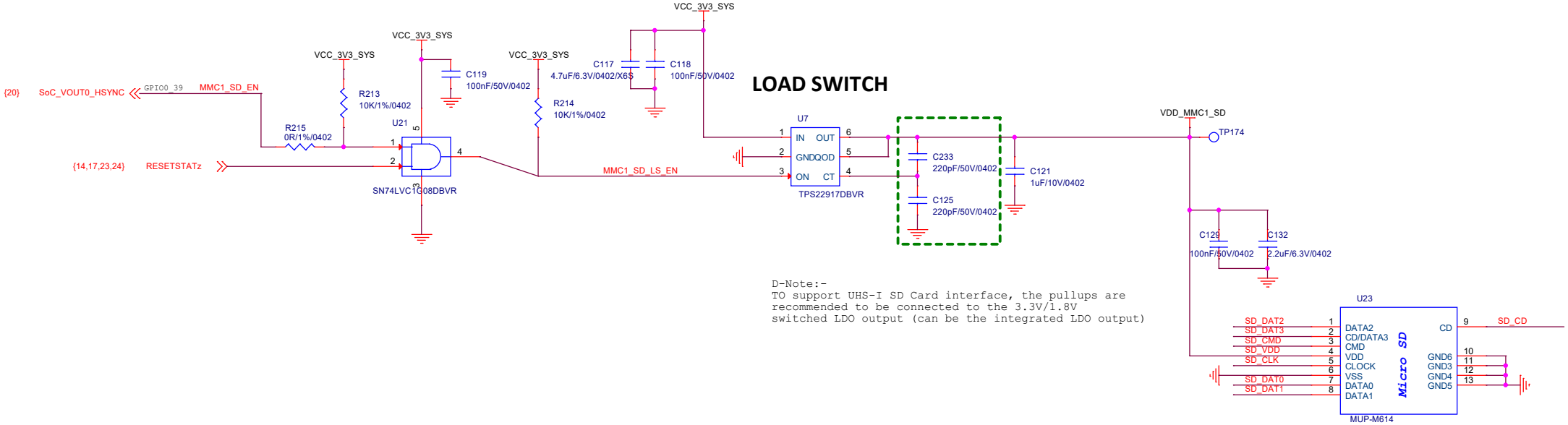
SD CARD INTERFACE

D-Note:-
The SD card supply control power switch, the power switch supply output (EN) reset logic, and the host (processor) IO power supply switching circuit are required to support UHS-I SD Cards which begins communications using 3.3V signal levels and later switches to 1.8V signal levels when configuring to one of the faster data transfer speeds. Cycling power to the SD Card is the only way to put the SD card back to 3.3V mode since SD Cards do not have a reset pin. The host IO power supply must power cycle and change voltage level along with the SD Card. The Power switch logic and the software driver operating the signals sourcing these circuits ensure both devices are power cycled and operating at the same IO voltage at the same time.

SD CARD RESET

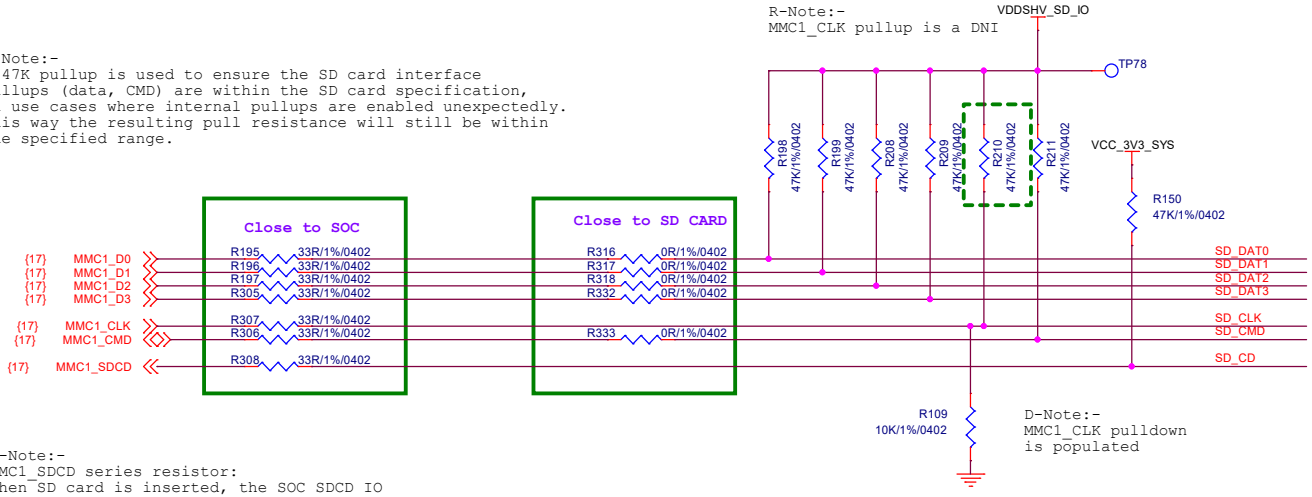
LOAD SWITCH



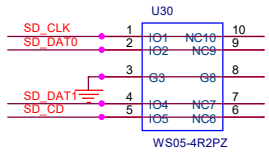
D-Note:-
TO support UHS-I SD Card interface, the pullups are recommended to be connected to the 3.3V/1.8V switched LDO output (can be the integrated LDO output)

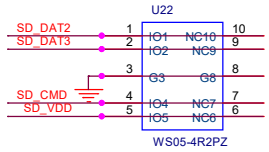
D-Note:-
A 47K pullup is used to ensure the SD card interface pullups (data, CMD) are within the SD card specification, in use cases where internal pullups are enabled unexpectedly. This way the resulting pull resistance will still be within the specified range.

R-Note:-
MMC1_CLK pullup is a DNI



D-Note:-
MMC1_CLK pulldown is populated



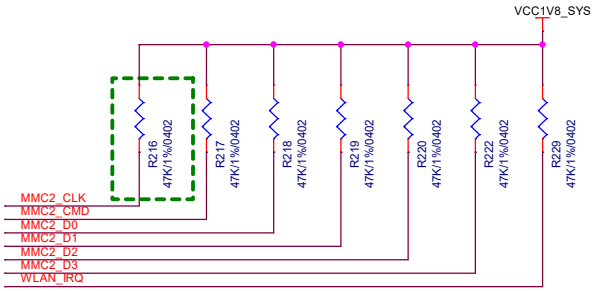


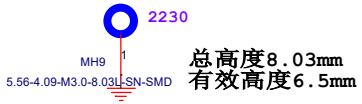
D-Note:-
MMC1_SDCD series resistor:
When SD card is inserted, the SOC SDCD IO connects to ground to indicate the presence of SD card. A 100R is recommended to limit the current in case the SDCD is configured as output unexpectedly.

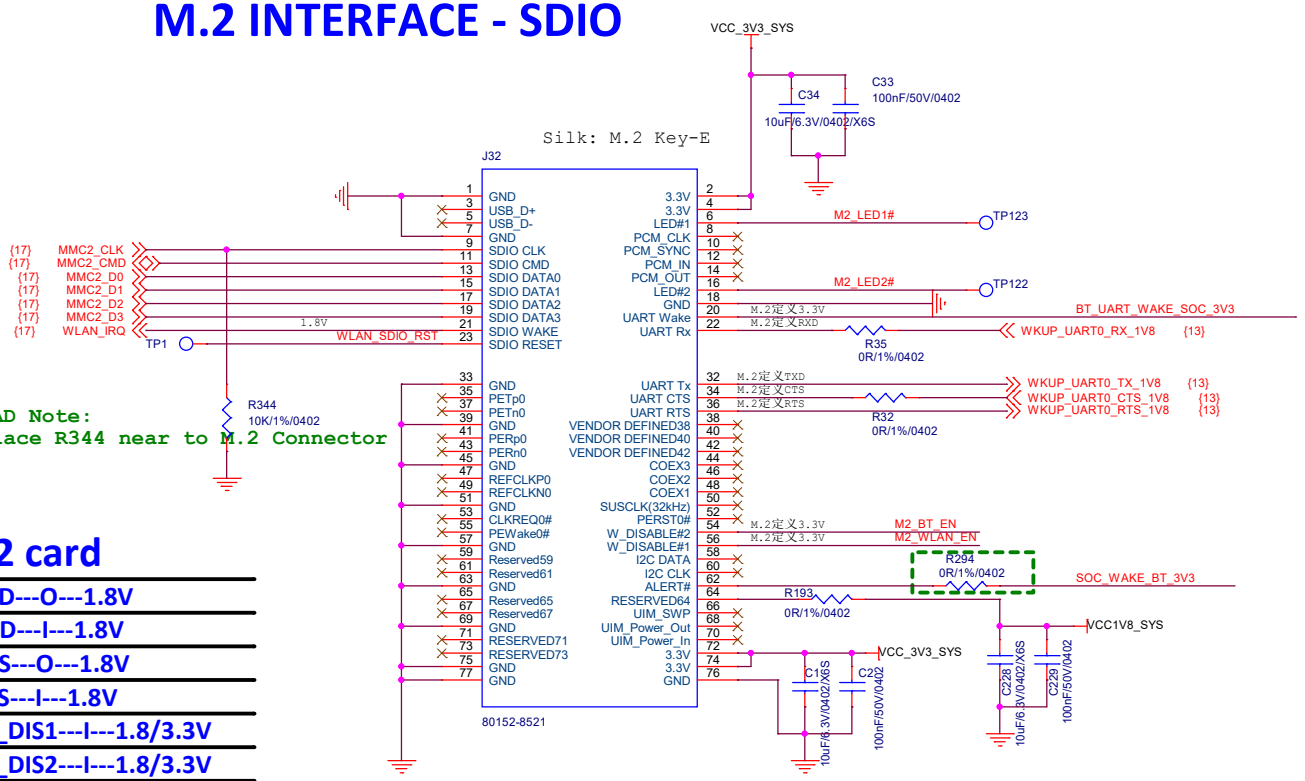
<Variant Name>

<Doc1>			
Project:			
File:	18. SD CARD INTERFACE	Size:	
Date:	Saturday, September 06, 2025	Rev:	V1.0
Designed by:	Reviewed by:	Sheet:	18 of 32

M.2 INTERFACE - SDIO





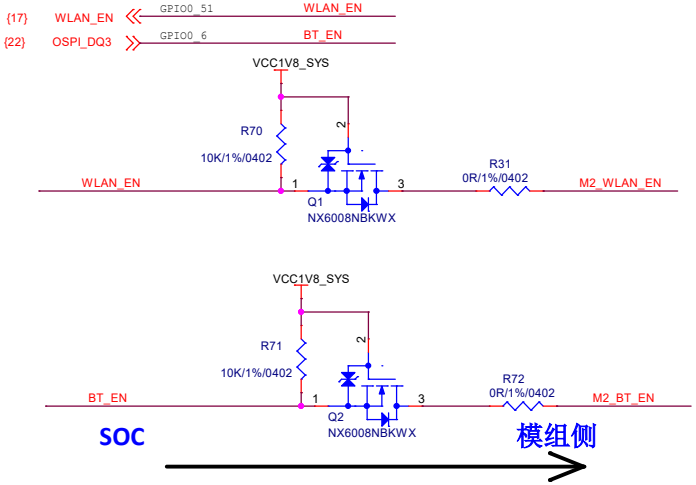


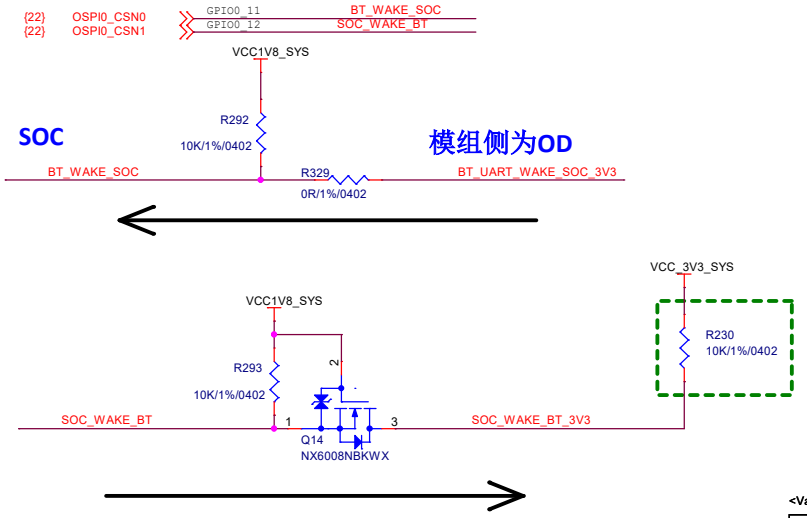
CAD Note:
Place R344 near to M.2 Connector

M.2 Socket KEY E

M.2 Socket KEY E	M.2 card
22---RXD---I---1.8V	22---TXD---O---1.8V
32---TXD---O---1.8V	32---RXD---I---1.8V
34---CTS---I---1.8V	34---RTS---O---1.8V
36---RTS---O---1.8V	36---CTS---I---1.8V
54---W_DIS1---O---1.8/3.3V	54---W_DIS1---I---1.8/3.3V
56---W_DIS2---O---1.8/3.3V	56---W_DIS2---I---1.8/3.3V
20---UART_WAKE---I---3.3V	20---UART_WAKE---O---3.3V
20---SDIO_WAKE---I---1.8V	21---SDIO_WAKE---O---1.8V
62---ALERT#---I---1.8V	62---ALERT#---O---1.8V

M.2 LEVEL TRANSLATORS





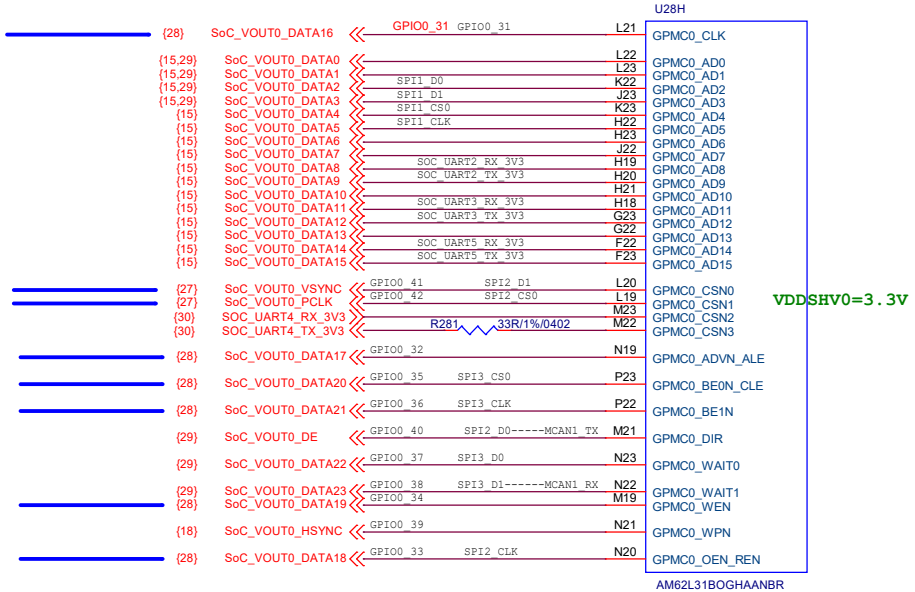
<Variant Name>

<Doc1>

Project:			
File:	19. M.2 CONNECTOR	Size:	
Date:	Saturday, September 06, 2025	Rev:	V1.0
Designed by:	Reviewed by:	Sheet:	19 of 32

D-Note:-
Shorting of multiple bootmode inputs together is not recommended or allowed, since the bootmode inputs have alternate functions that could be configured after boot (can be set as outputs). Shorting the bootmode pins directly to VCC or ground directly is not recommended. Connect each of the bootmode pins through separate resistor. Choose the bootmode resistor value based on the use case (10K or similar)

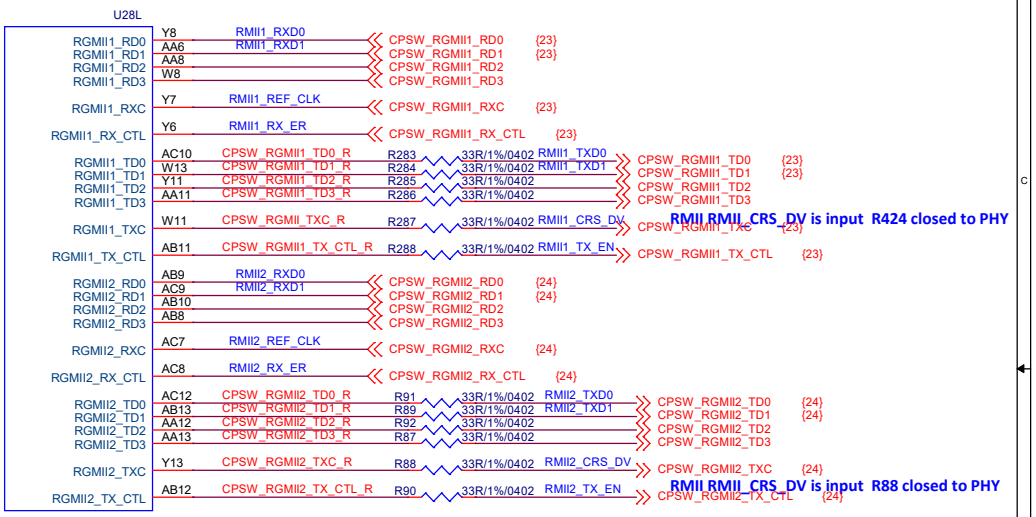
SOC - GPMC



SOC - GPMC

SOC - ETHERNET INTERFACE

D-Note:-
The Ethernet interface (CPSW3G)
interface supports 1.8V IO level only



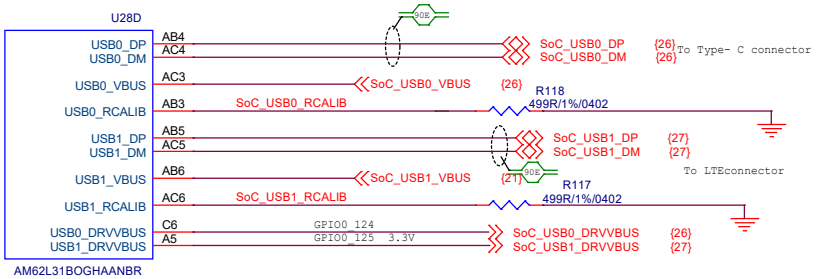
VDDS0=1.8V

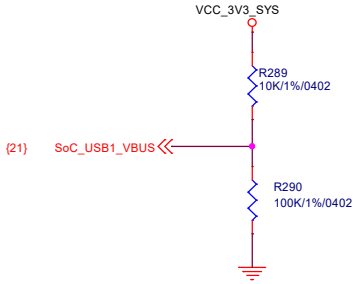
SOC - GPMC

<Variant Name>

<Doc1>			
Project:			
File:	20. SOC PERIPHERALS 1	Size:	
Date:	Saturday, September 06, 2025	Rev:	V1.0
Designed by:	Reviewed by:	Sheet:	20 of 32

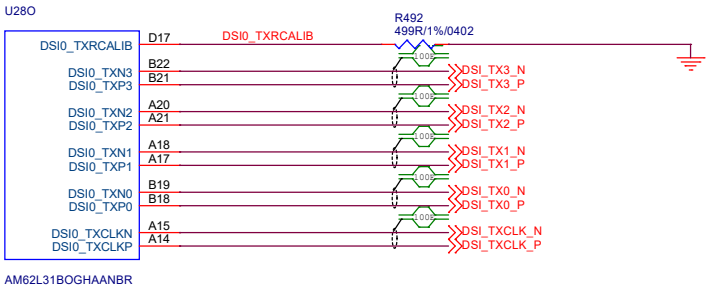
SOC - USB





D-Note:-
Refer USB VBUS Design Guidelines section of SOC data sheet

SOC - DSI

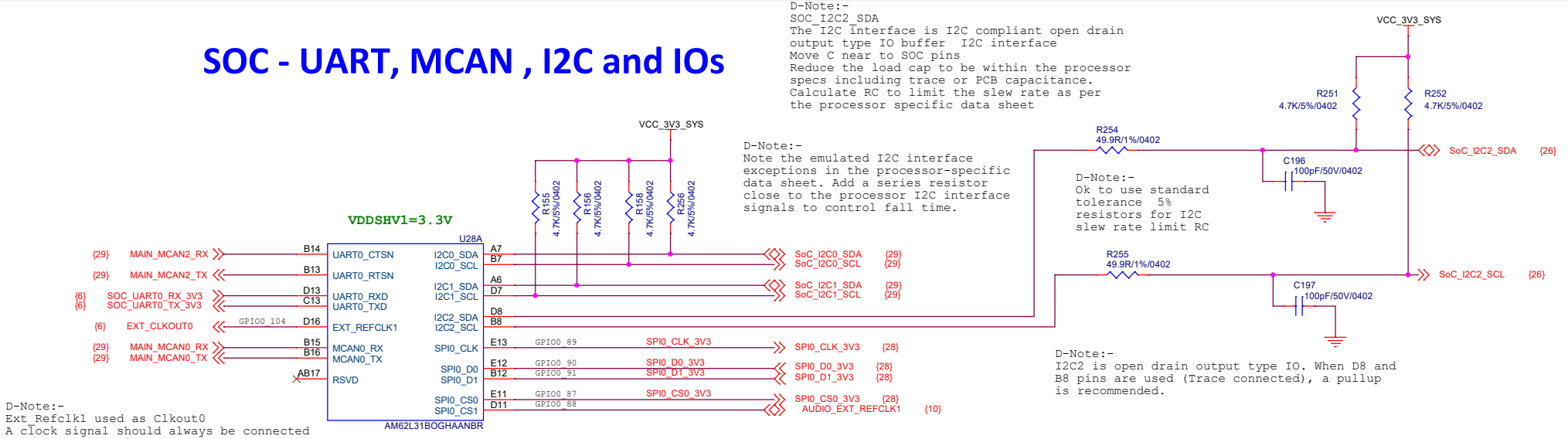


<Variant Name>

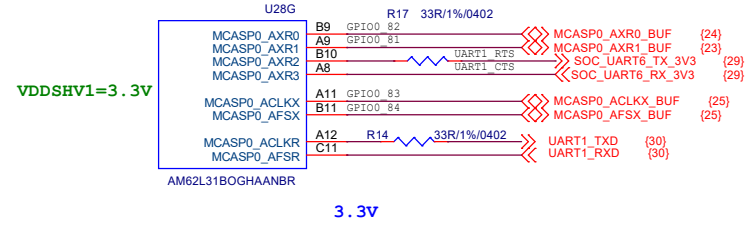
<Doc1>			
Project:			
File:	21. SOC PERIPHERALS 2	Size:	
Date:	Saturday, September 06, 2025	Rev:	V1.0
Designed by:	Reviewed by:	Sheet:	21 of 32

SOC - UART, MCAN , I2C and IOs

D-Note:-
SOC_I2C2_SDA
The I2C interface is I2C compliant open drain output type IO buffer I2C interface
Move C near to SOC pins
Reduce the load cap to be within the processor specs including trace or PCB capacitance.
Calculate RC to limit the slew rate as per the processor specific data sheet

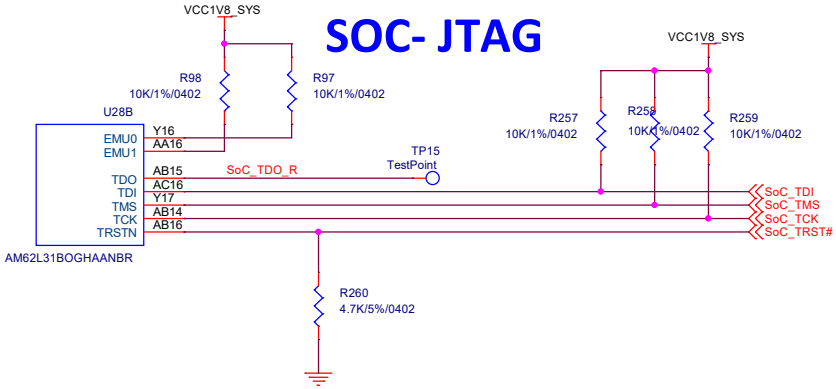


SOC - MCASP and UART



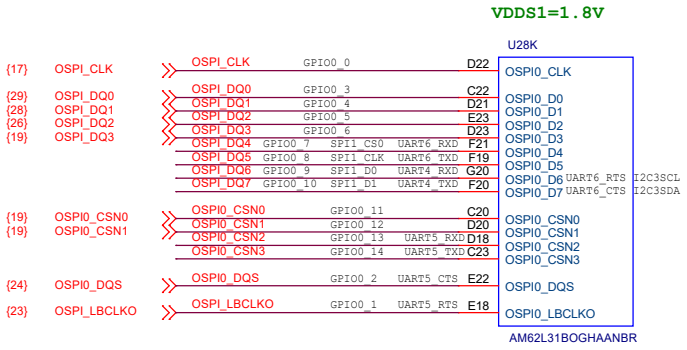
3.3V

SOC- JTAG



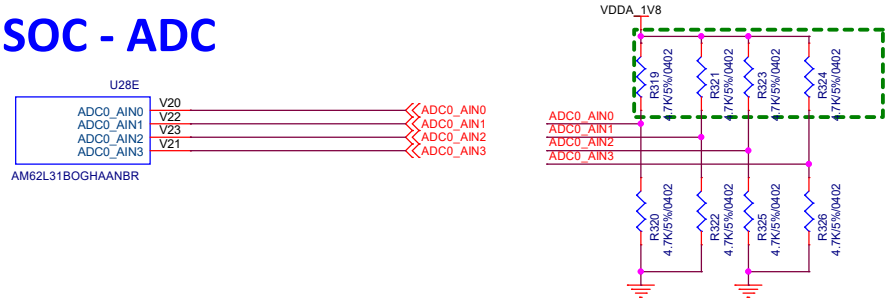
SOC OSPI INTERFACE

VDDS1=1.8V



D-Note:-
The OSPI0 interface supports 1.8V IO level only

SOC - ADC

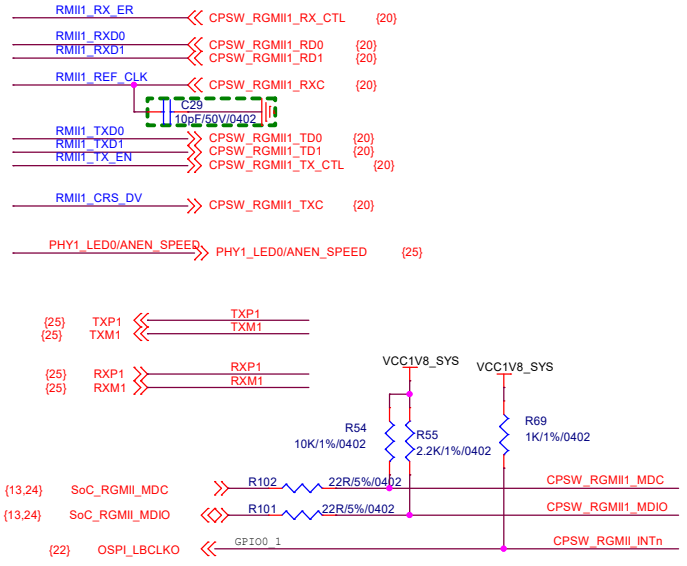


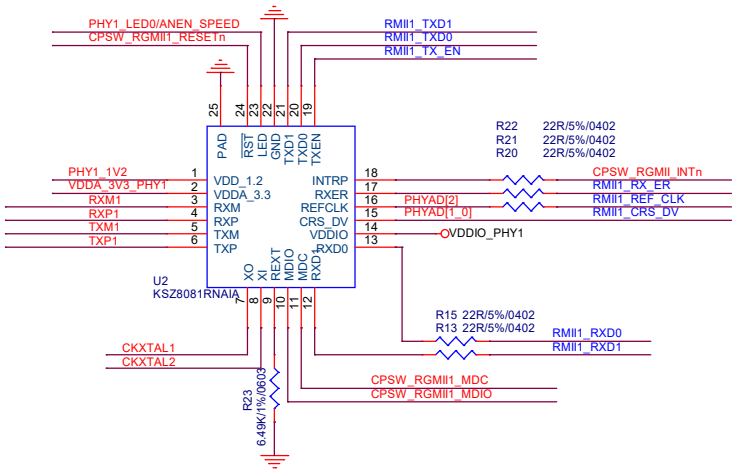
<Variant Name>

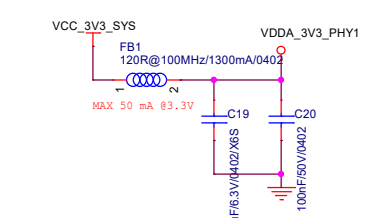
<Doc1>			
Project:			
File:	22. SOC PERIPHERALS 3	Size:	
Date:	Saturday, September 06, 2025	Rev:	V1.0
Designed by:	Reviewed by:	Sheet:	22 of 32

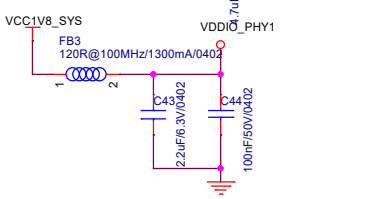
CPSW3G RGMII_1 ETHERNET PHY

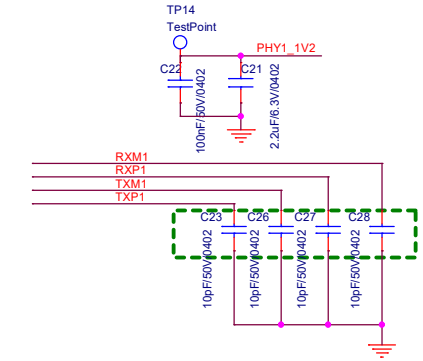
D-Note:-
The caps and values used are as per the EPHY datasheet recommendations.

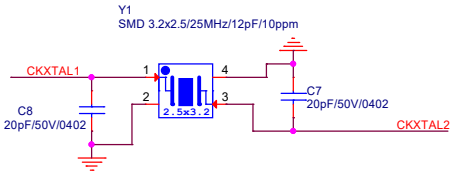




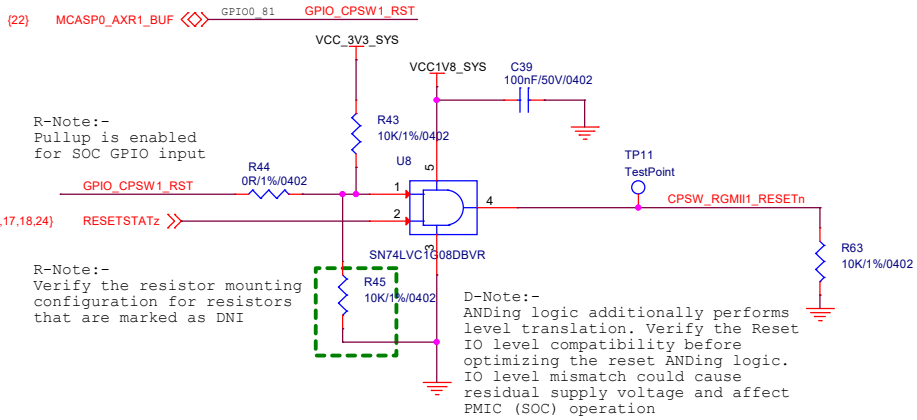


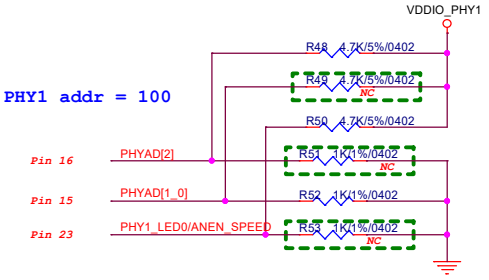






CLOCK





SPEED mode

SPEED

Auto-Negotiation Enable and SPEED Mode
Pull-up (default) = Enable Auto-Negotiation and set 100 Mbps Speed
Pull-down = Disable Auto-Negotiation and set 10 Mbps Speed

PHYAD [1:0]

The PHY Address is latched at the de-assertion of reset
Pull-up = PHY Address bits [1:0] are both set to 1
Pull-down (default) = PHY Address bits [1:0] are both set to 0

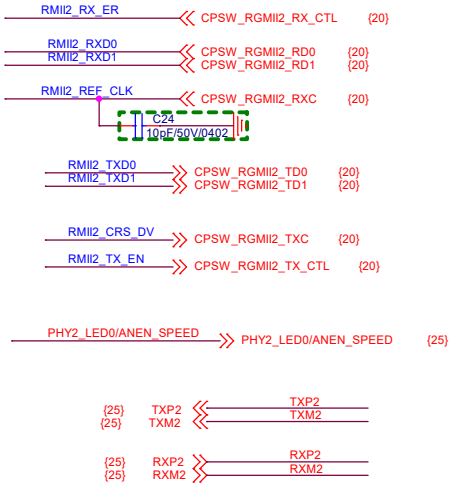
PHY Address bits [4:3] are set to 00b. Configurable PHY addresses are: 0h, 3h, 4h or 7h.

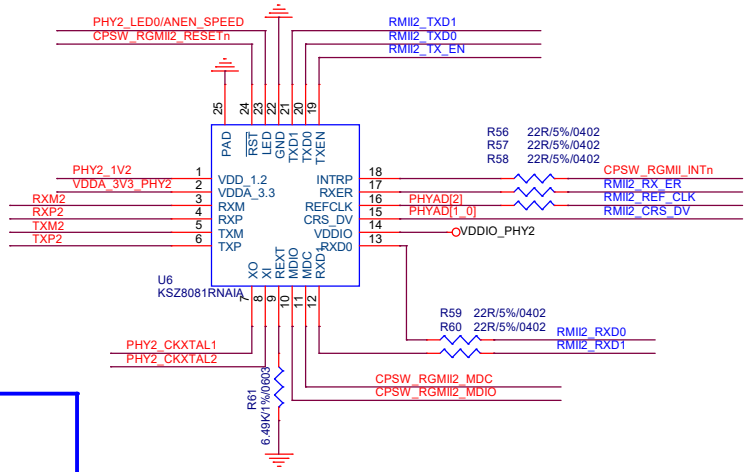
<Variant Name>

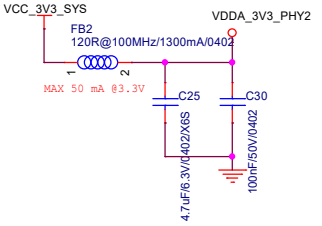
<Doc1>			
Project:			
File:	23. CPSW3G RGMII_1 ETHERNET PHY	Size:	
Date:	Saturday, September 06, 2025	Rev:	V1.0
Designed by:	Reviewed by:	Sheet:	23 of 32

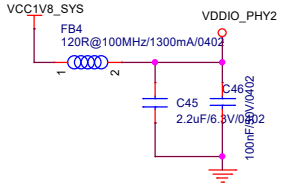
CPSW3G RGMII_2 ETHERNET PHY

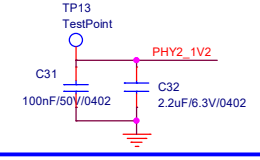
D-Note:-
The caps and values used are as per the EPHY data sheet recommendations.

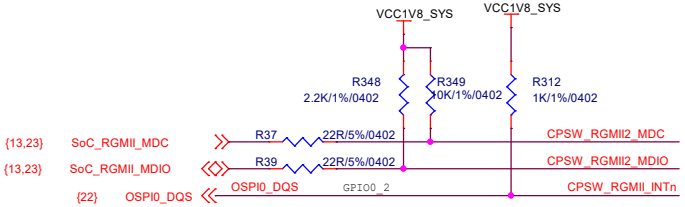


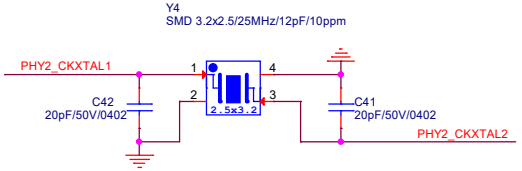




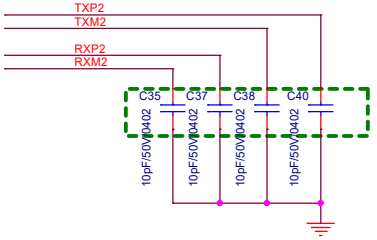


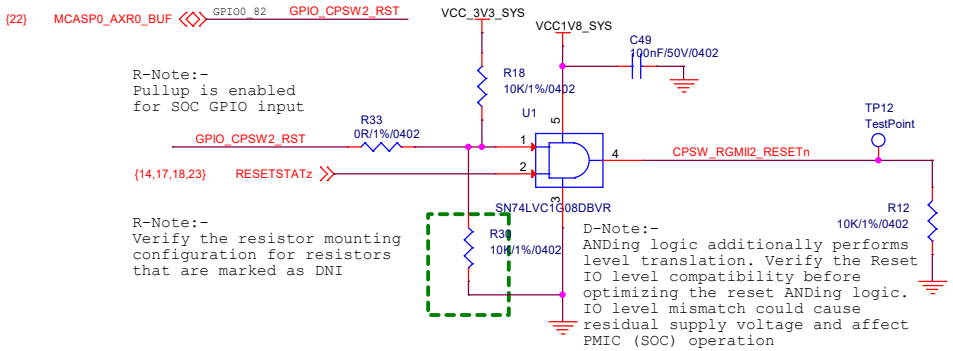


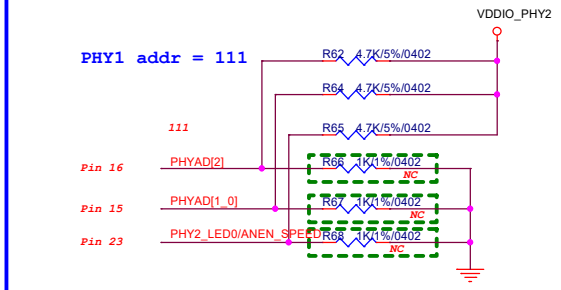




CLOCK







SPEED mode

SPEED

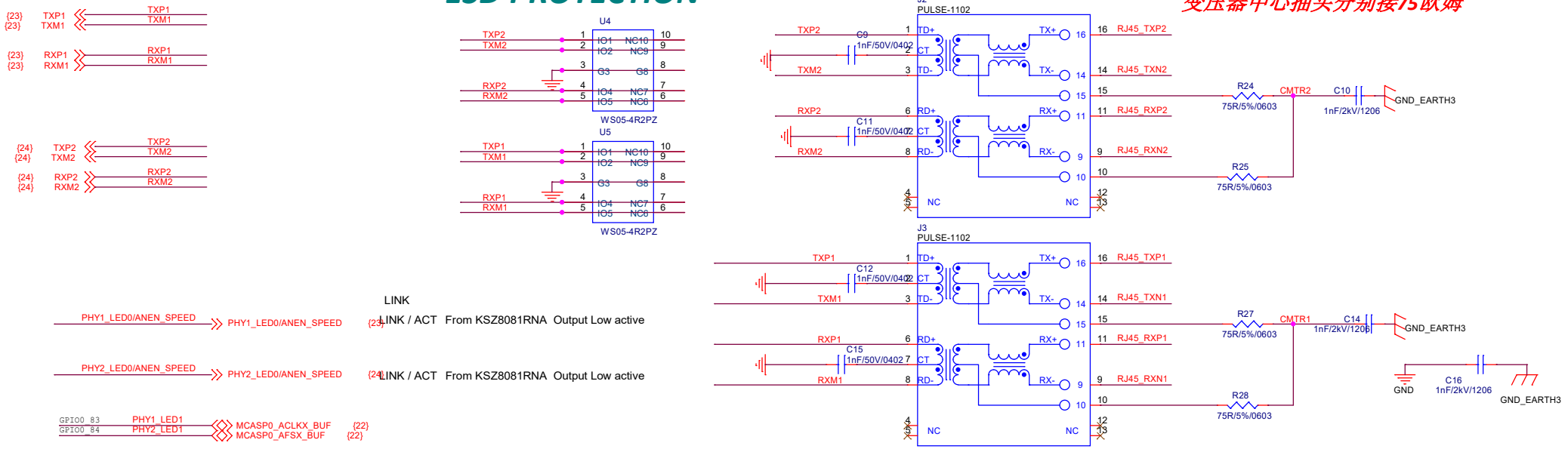
Auto-Negotiation Enable and SPEED Mode
Pull-up (default) = Enable Auto-Negotiation and set 100 Mbps Speed
Pull-down = Disable Auto-Negotiation and set 10 Mbps Speed

<Variant Name>

<Doc1>			
Project:			
File:	24. CPSW3G RGMII_2 ETHERNET PHY	Size:	
Date:	Saturday, September 06, 2025	Rev:	V1.0
Designed by:	Reviewed by:	Sheet:	24 of 32

ESD PROTECTION

变压器中心抽头分别接75欧姆



LINK

PHY1_LED0/ANEN_SPEED → PHY1_LED0/ANEN_SPEED {23}

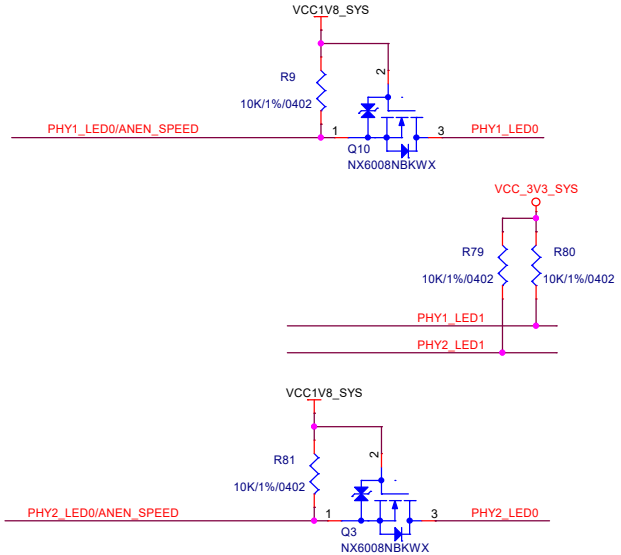
LINK / ACT From KSZ8081RNA Output Low active

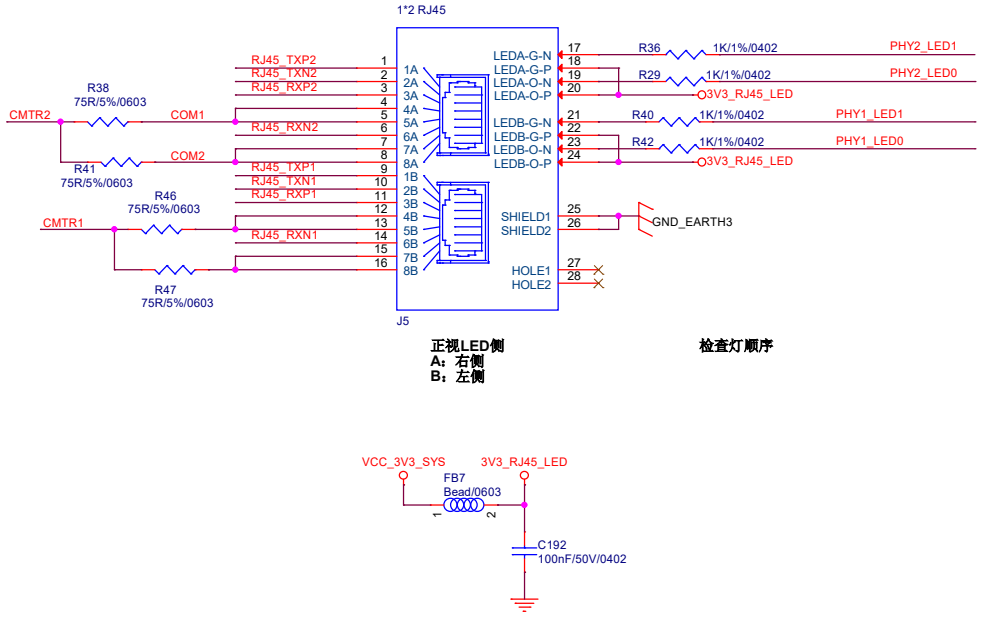
PHY2_LED0/ANEN_SPEED → PHY2_LED0/ANEN_SPEED {24}

LINK / ACT From KSZ8081RNA Output Low active

GPIO0_83 PHY1_LED1 → MCASP0_ACLKX_BUF {22}

GPIO0_84 PHY2_LED1 → MCASP0_AFSX_BUF {22}





正视LED侧
A：右侧
B：左侧

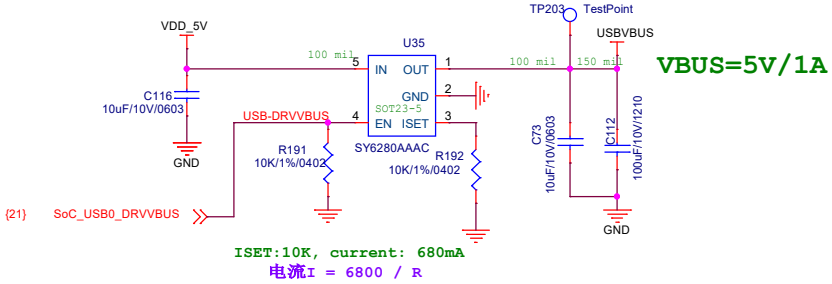
检查灯顺序

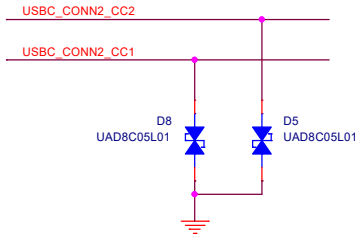
<Variant Name>

<Doc1>			
Project:			
File:	25. RJ45x2	Size:	
Date:	Saturday, September 06, 2025	Rev:	V1.0
Designed by:	Reviewed by:	Sheet:	25 of 32

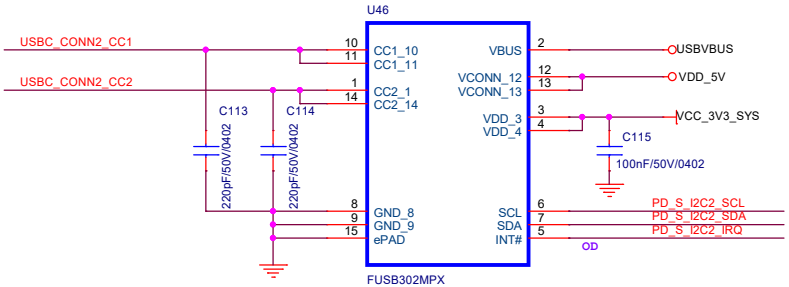
USB0 TYPE-C DRP

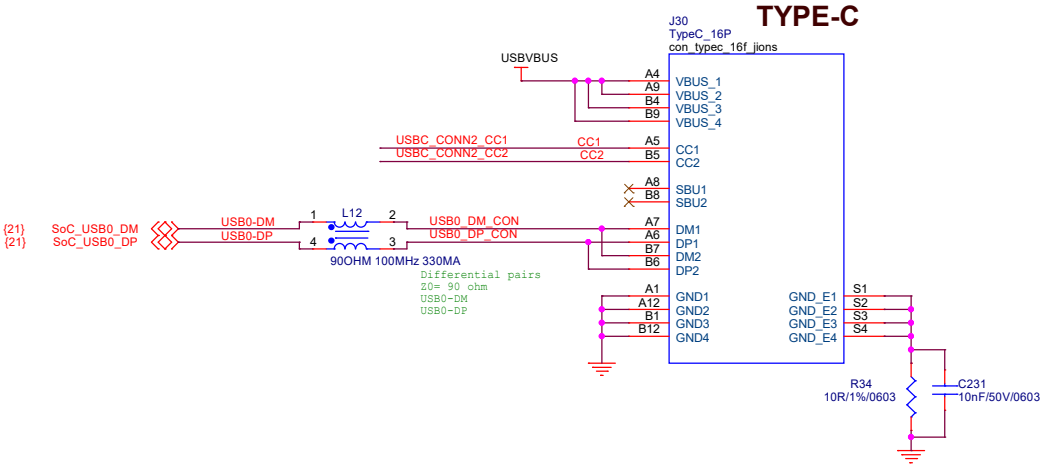
EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A

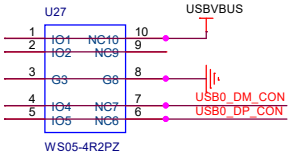


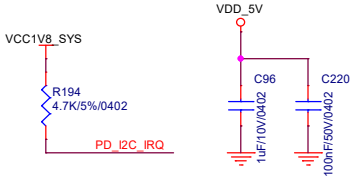


Silk: TYPE-C DRP

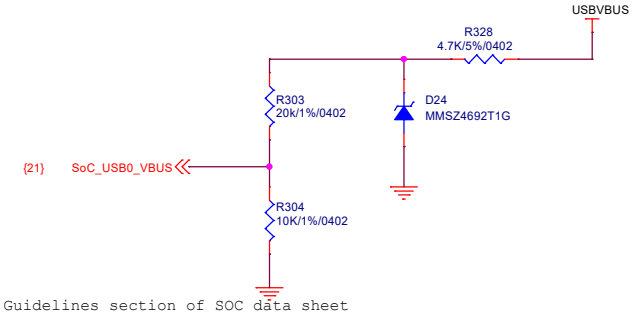








D-Note:-
VBUS connection is optional for Host configuration



D-Note:-
Refer USB VBUS Design Guidelines section of SOC data sheet

<Variant Name>

<Doc1>			
Project:			
File:	26. USB0 TYPE-C DRP	Size:	
Date:	Saturday, September 06, 2025	Rev:	V1.0
Designed by:	Reviewed by:	Sheet:	26 of 32

USB1

{21} SoC_USB1_DM
{21} SoC_USB1_DP

{21} SoC_USB1_DRVVBUS
{20} SoC_VOUT0_VSYNC
{20} SoC_VOUT0_PCLK
GPIO0_125 M_ON/OFF
GPIO0_41 M_RST
GPIO0_42 SIM_SEL

M_VCC
C134 10uF/10V/0603
C135 10uF/10V/0603
C136 10uF/10V/0603
C137 100nF/50V/0402
C133 220uF/6.3V
C138 470uF/10V
C141 10uF/10V/0603
C140 10uF/10V/0603
C142 10uF/10V/0603
VDD_5V
10uF/10V/0603

VDD_5V
5V--3.8V
C143 100nF/50V/0402
R223 10R/1%/0603
R221 100K/1%/0402
R235 10K/1%/0402
20pF/0402
TP3 TestPoint
M_ON/OFF
R241 10K/1%/0402
C156 1uF/10V/0402
U9 SY8035DBC
PVIN PVIN1 LX1 LX2 LX3 SVIN FB PG SS EN GND
L1 0.47uH/4.7A
C157 100nF/50V/0402
R239 53.6K/1%/0402
R237 10K/1%/0402
C144 22uF/50V/0402
C145 C146 C147 C149 C151 10uF/10V/0603
C153 100nF/50V/0402
TP2 TestPoint
M_VCC
3.8V
Imax=2A
EN>1.5, EN<0.4V
0.6*(240/44.2+1)=3.85V

M_VCC
U51
GND54
RESERVED6 RESERVED5(5V) RESERVED4(5V) RESERVED3 GND43 +3.3Vaux_41 +3.3Vaux_39 GND37 GND35 PETp0 PETn0 GND29 GND27 PERp0 PERn0 GND21 RESERVED2 RESERVED1 GND15 REFCLK+ REFCLK- GND9 CLKREQ# COEX2 COEX1 WAKE# GND53
+3.3Vaux_52 GND50 +1.5V(5V) LED_WPAN#(5V) LED_WLAN# LED_WWAN#(5V) GND40 USB_D+ USB_D- GND34 SMB_DATA SMB_CLK +1.5V_28 GND26 +3.3Vaux_24 PERST# W_DISABLE# GND18 UIM_VPP UIM_RESET UIM_CLK UIM_DATA UIM_PWR +1.5V_6 GND4 +3.3Vaux_2
TOP BOT
minipcie socket 8mm/5.7mm
SIM_DET M_LED_CON SoC_USB1_DP SoC_USB1_DM Module_RST
TP41 TestPoint
R231 22R/5%/0402 SIM_RST
R232 22R/5%/0402 SIM_CLK
R233 22R/5%/0402 SIM_DATA
R234 0R/1%/0402 SIM_VCC

MH6 SMTSOM2-5.5
固定LTE模块

M_VCC
VDD_5V
R278 100R/5%/1206
R225 10K/1%/0402
Q9 NX6008NBKWX
M_ON/OFF
Q11 DTC144EKA
TP207 TestPoint
Module_RST
M_RST
Q8 DTC144EKA
R226 10K/1%/0402

SIM_VCC
R250 10K/1%/0402
SIM_DATA

VCC_3V3_SYS
C100 100nF/50V/0402
GND
U45
SIM_SEL
SIM_DET
R249 0R/1%/0402
0: NC
1: NO
V+ Control Pin COM GND NO NC
SIM_DET2
SIM_DET1
SGM3157

U54
FSA2567MPX
SIM_VCC SIM_DATA SIM_CLK SIM_RST SEL1 TestPoint SIM_SEL R228 10K/1%/0402 VCC_3V3_SYS
V_SIM DAT CLK RST SEL VCC
Low High
1V_SIM 2V_SIM 1DAT 2DAT 1CLK 2CLK 1RST 2RST Not Connect NC Thermal Pad GND
SIM1_VCC SIM2_eSIM_VCC SIM1_DATA SIM2_eSIM_DATA SIM1_CLK SIM2_eSIM_CLK SIM1_RST SIM2_eSIM_RST R227 0R/1%/0402 SIM_SEL
C195 100nF/50V/0402

SIM2_eSIM_VCC SIM2_eSIM_DATA SIM2_eSIM_CLK SIM2_eSIM_RST
R240 0R/1%/0402 SIM2_VCC
R242 0R/1%/0402 SIM2_DATA
R243 0R/1%/0402 SIM2_CLK
R244 0R/1%/0402 SIM2_RST
R245 0R/1%/0402 eSIM_VCC
R246 0R/1%/0402 eSIM_DATA
R247 0R/1%/0402 eSIM_CLK
R248 0R/1%/0402 eSIM_RST

U53
TOP BOTTOM
SIM1_VCC SIM1_RST SIM1_CLK SIM1_DATA
SIM2_VCC SIM2_RST SIM2_CLK SIM2_DATA
VCC1 RST1 CLK1 DATA1 VCC2 RST2 CLK2 DATA2 VPP1 VPP2 GND SW1 SW2
SIM_DET1 SIM_DET2
D18 UAD8C05L01
D19 UAD8C05L01
MUP-C7814-01
SIM1 : above
SIM2 : below

U12
WS05-4R2PZ
SIM1_VCC SIM1_RST GND SIM1_DATA SIM1_CLK
IO1 IO2 G3 IO4 IO5 NC10 NC9 G8 NC7 NC6

U52
WS05-4R2PZ
SIM2_VCC SIM2_RST GND SIM2_DATA SIM2_CLK
IO1 IO2 G3 IO4 IO5 NC10 NC9 G8 NC7 NC6

U44
C5,GND C6,VPP C7,DATA C8,NC1 GND C1,VCC C2,RST C3,CLK C4,NC0
SIM_MFF2-GT-A
eSIM_DATA eSIM_VCC eSIM_RST eSIM_CLK
C158 C159 C160 C161 C162 100nF/50V/0402 10pF/50V/0402

SIM1_VCC SIM1_RST SIM1_CLK SIM1_DATA
C163 C164 C165 C166 C167 C168
10pF/50V/0402 100nF/50V/0402 33pF/50V/0402 1uF/10V/0402

SIM2_VCC SIM2_RST SIM2_CLK SIM2_DATA
C191 C186 C187 C188 C189 C190
10pF/50V/0402 100nF/50V/0402 33pF/50V/0402 1uF/10V/0402

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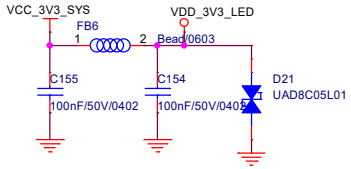
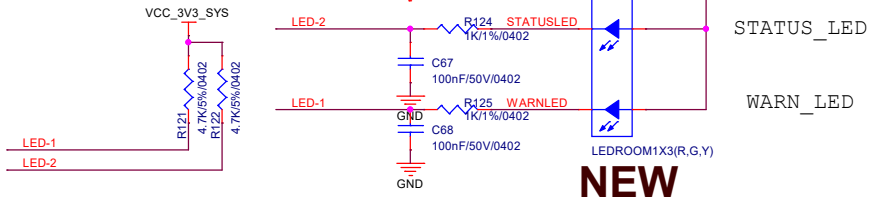
LED





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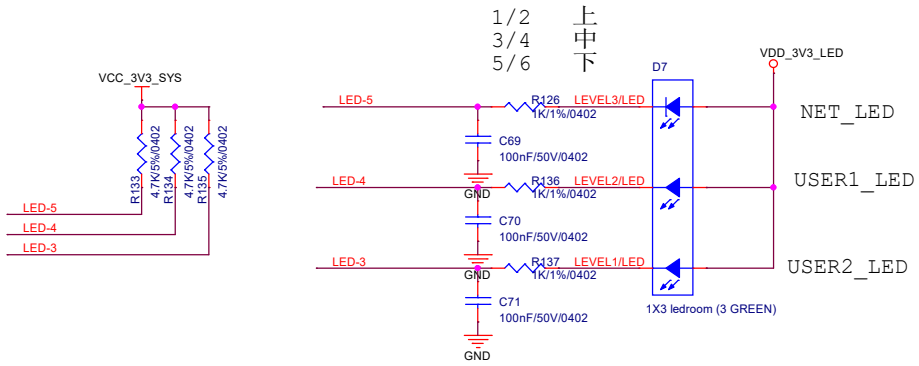
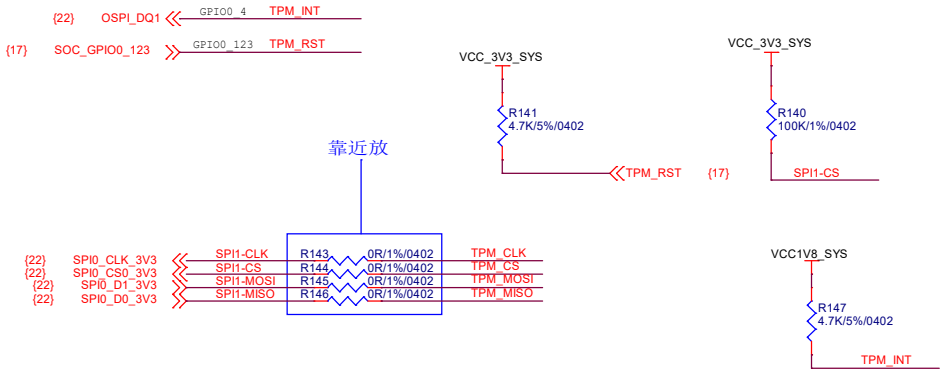
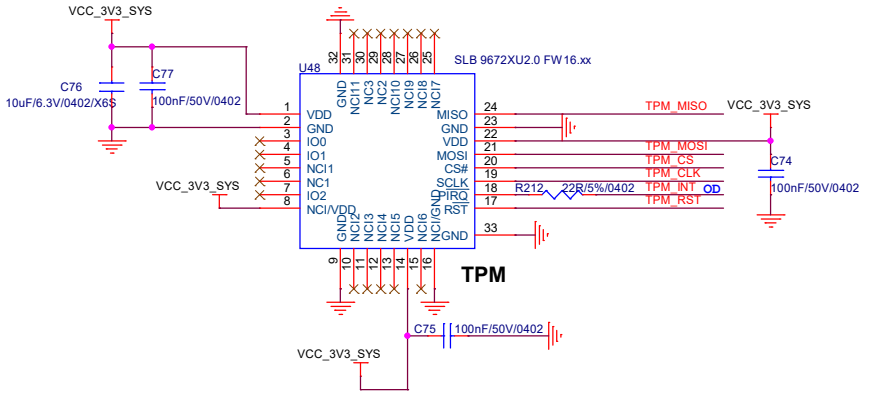
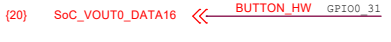


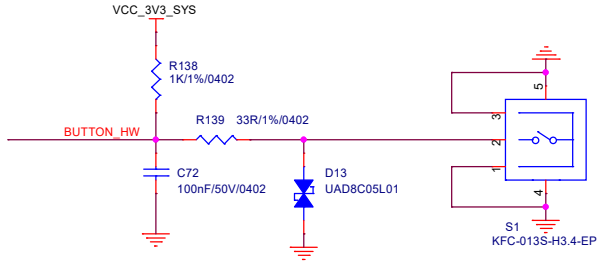
TPM SPI-0





HW KEY





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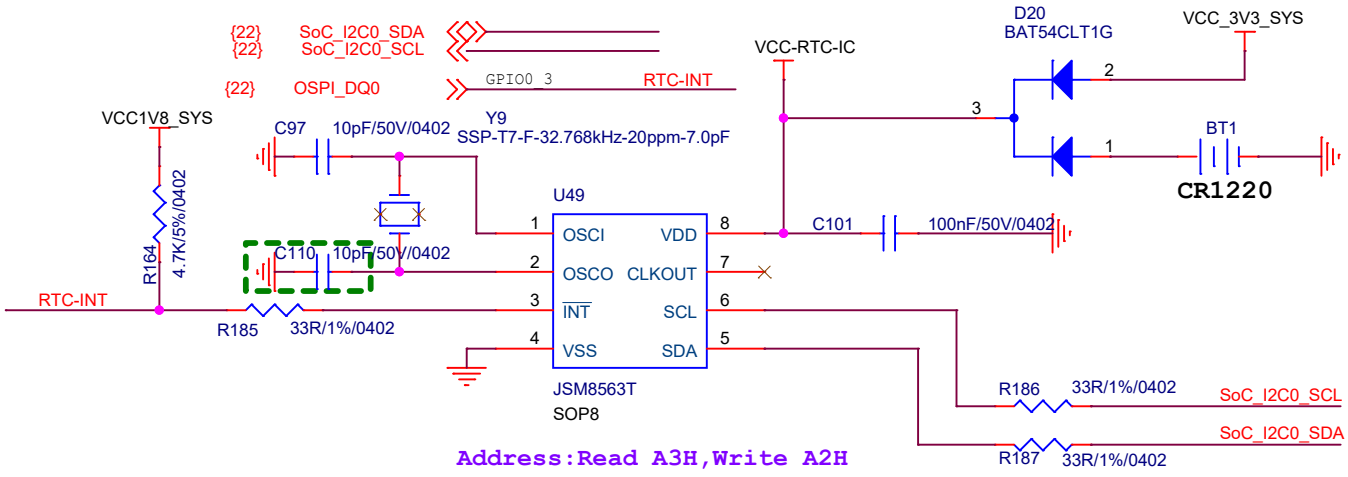
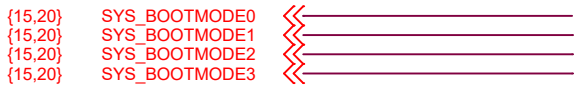
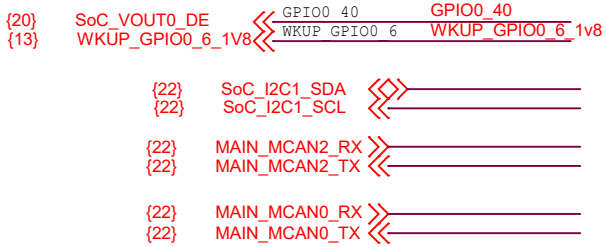
RTC







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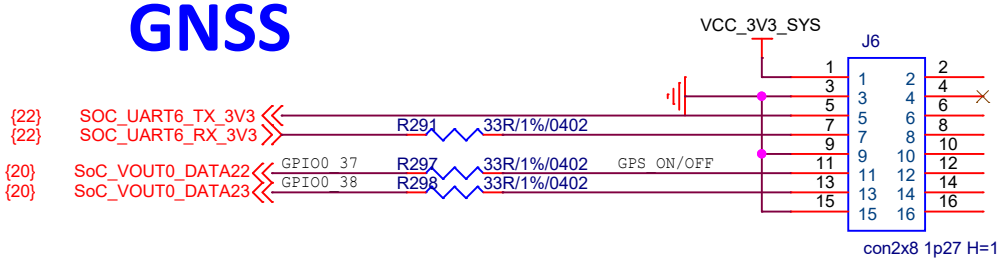

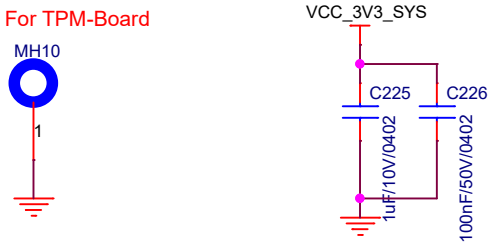

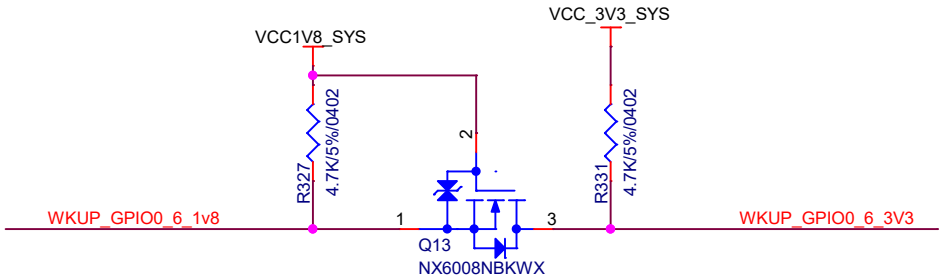

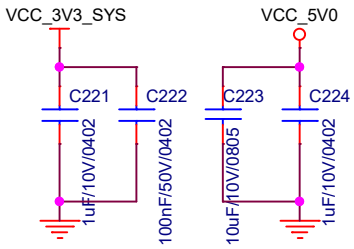

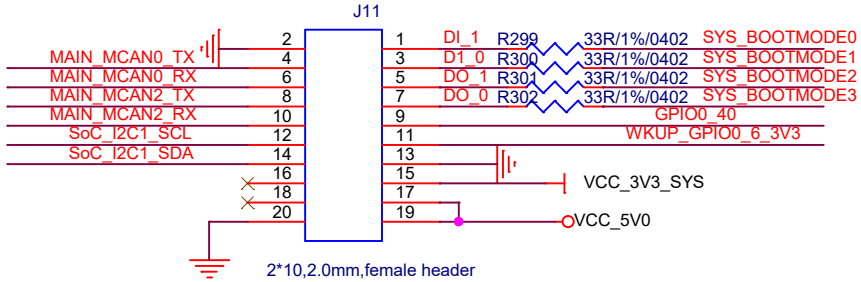

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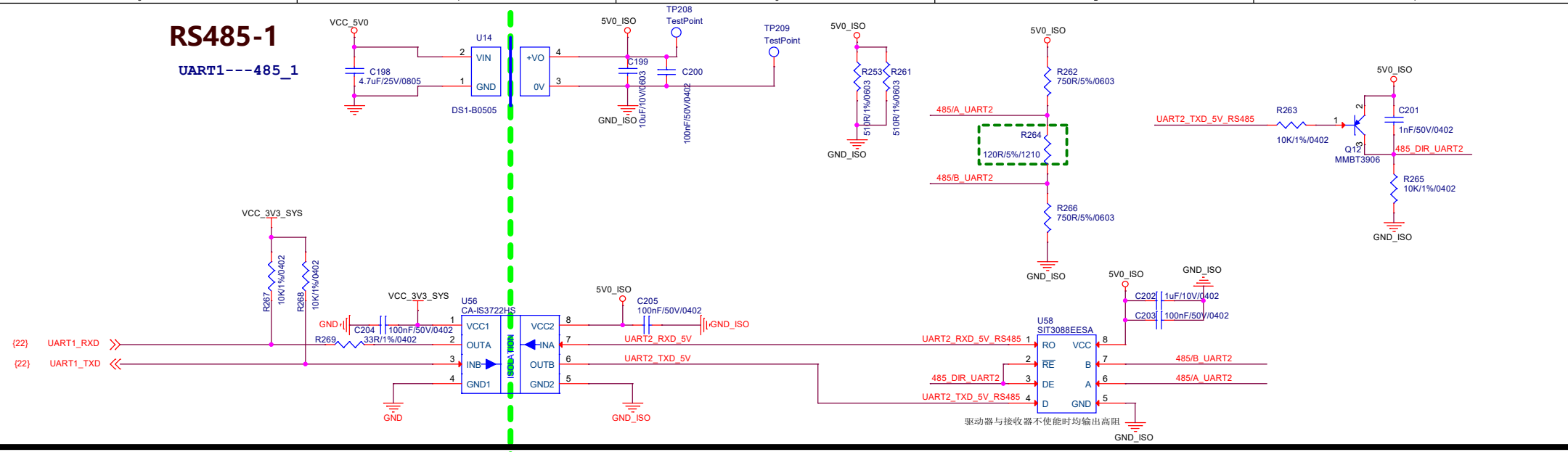
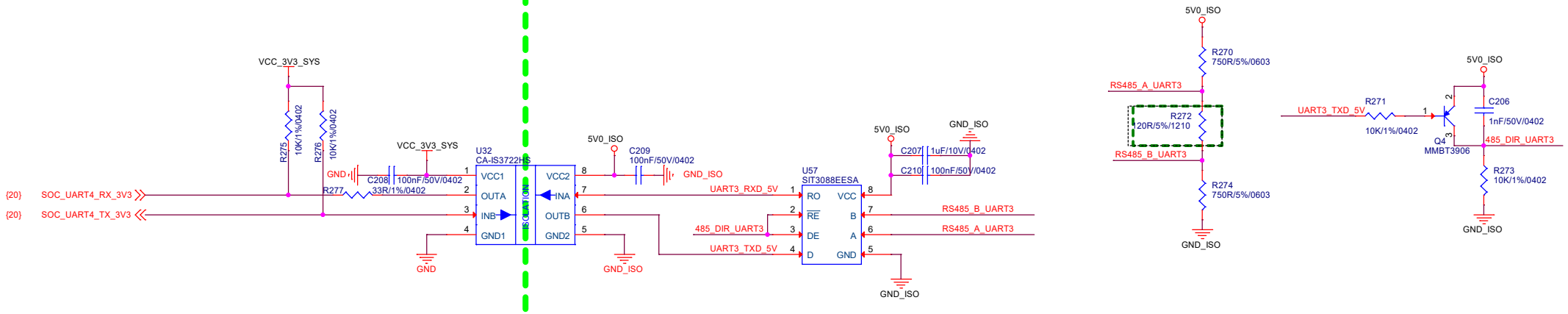
RS485-1

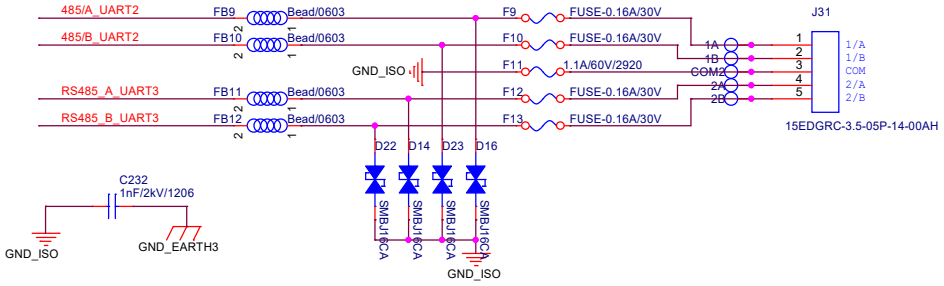
UART1---485_1



UART4---485_2

RS485-2





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