Date: Marcl
Revisio

EMIF Tools: Register Conf

Direc

1) Save the user configuration from the '*Title-README*' worksheet. Values will be auto
   OR
   Copy and paste the following text into corresponding u-boot source files.

```
/* ========================================================
 *   Copyright (C) 2017 Texas Instruments Incorporated
 *
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 *   Restricted rights to use, duplicate or disclose this code are
 *   granted through contract.
 *
 *   The program may not be used without the written permission
 *   of Texas Instruments Incorporated or against the terms and conditior
 *   stipulated in the agreement under which this program has been
 *   supplied.
 * ========================================================

/*
 *  AM571x_DDR3L_532MHz_TI_EVM_revH_config.c
 *    Created on: 06/27/2018
 *    Created with: EMIF_RegisterConfig_v2.0.1
 */

#include "emif4d5_wrapper.h"

const struct dpll_params AM571x_DDR3L_532MHz_TI_EVM_revH_pll_pa
    .m = 266,
    .n = 4,
    .m2 = 2,
    .m4_h11 = 8
};

const struct ctrl_ioregs AM571x_DDR3L_532MHz_TI_EVM_revH_ctrl_ior
    .ctrl_ddr3ch = 0x60606060,
    .ctrl_ddrch = 0x40404040,
    .ctrl_ddrio_0 = 0x00094A40,
    .ctrl_ddrio_1 = 0x00000000,
    .ctrl_emif_sdram_config_ext = 0x0000C123
};

const struct dmm_lisa_map_regs AM571x_DDR3L_532MHz_TI_EVM_rev
    .dmm_lisa_map_0 = 0x00000000,
    .dmm_lisa_map_1 = 0x00000000,
    .dmm_lisa_map_2 = 0x80700100,
    .dmm_lisa_map_3 = 0xFF020100,
    .is_ma_present = 0x1
```

```
};

const struct emif_regs AM571x_DDR3L_532MHz_TI_EVM_revH_emif_reg
    .sdram_config_init = 0x61851BB2,
    .sdram_config = 0x61851BB2,
    .sdram_config2 = 0x00000000,
    .ref_ctrl = 0x000040F1,
    .ref_ctrl_final = 0x00001035,
    .sdram_tim1 = 0xCCCF36B3,
    .sdram_tim2 = 0x30BF7FDA,
    .sdram_tim3 = 0x407F8BA8,
    .read_idle_ctrl = 0x00050000,
    .zq_config = 0x5007190B,
    .temp_alert_config = 0x00000000,
    .emif_rd_wr_lvl_rmp_ctl = 0x80000000,
    .emif_rd_wr_lvl_ctl = 0x00000000,
    .emif_ddr_phy_ctlr_1_init = 0x0824400B,
    .emif_ddr_phy_ctlr_1 = 0x0E24400B,
    .emif_rd_wr_exec_thresh = 0x00000305
};

/*
 * DLL Ratio Values are an estimate based on trace lengths. Either
 * software leveling or hardware leveling should be performed to
 * determine final DLL values.
 */
const unsigned int AM571x_DDR3L_532MHz_TI_EVM_revH_emif1_ext_p
    0x04040100,             // EMIF1_EXT_PHY_CTRL_1
    0x006B00A2,             // EMIF1_EXT_PHY_CTRL_2
    0x006B00A2,             // EMIF1_EXT_PHY_CTRL_3
    0x006B00A6,             // EMIF1_EXT_PHY_CTRL_4
    0x006B00A6,             // EMIF1_EXT_PHY_CTRL_5
    0x006B00AA,             // EMIF1_EXT_PHY_CTRL_6
    0x002F002F,             // EMIF1_EXT_PHY_CTRL_7
    0x002F002F,             // EMIF1_EXT_PHY_CTRL_8
    0x002F002F,             // EMIF1_EXT_PHY_CTRL_9
    0x002F002F,             // EMIF1_EXT_PHY_CTRL_10
    0x002F002F,             // EMIF1_EXT_PHY_CTRL_11
    0x0060006F,             // EMIF1_EXT_PHY_CTRL_12
    0x00600070,             // EMIF1_EXT_PHY_CTRL_13
    0x00600079,             // EMIF1_EXT_PHY_CTRL_14
    0x00600079,             // EMIF1_EXT_PHY_CTRL_15
    0x00600083,             // EMIF1_EXT_PHY_CTRL_16
    0x0040004F,             // EMIF1_EXT_PHY_CTRL_17
    0x00400050,             // EMIF1_EXT_PHY_CTRL_18
    0x00400059,             // EMIF1_EXT_PHY_CTRL_19
    0x00400059,             // EMIF1_EXT_PHY_CTRL_20
    0x00400063,             // EMIF1_EXT_PHY_CTRL_21
    0x00800080,             // EMIF1_EXT_PHY_CTRL_22
    0x00800080,             // EMIF1_EXT_PHY_CTRL_23
    0x40010080,             // EMIF1_EXT_PHY_CTRL_24
    0x08102040,             // EMIF1_EXT_PHY_CTRL_25
    0x005B0092,             // EMIF1_EXT_PHY_CTRL_26
    0x005B0092,             // EMIF1_EXT_PHY_CTRL_27
    0x005B0096,             // EMIF1_EXT_PHY_CTRL_28
```

```
    0x005B0096,             // EMIF1_EXT_PHY_CTRL_29
    0x005B009A,             // EMIF1_EXT_PHY_CTRL_30
    0x0030003F,             // EMIF1_EXT_PHY_CTRL_31
    0x00300040,             // EMIF1_EXT_PHY_CTRL_32
    0x00300049,             // EMIF1_EXT_PHY_CTRL_33
    0x00300049,             // EMIF1_EXT_PHY_CTRL_34
    0x00300053,             // EMIF1_EXT_PHY_CTRL_35
    0x00000077              // EMIF1_EXT_PHY_CTRL_36
};
```

```
struct emif_cfg AM571x_DDR3L_532MHz_TI_EVM_revH = {
    .platform = "AM571x_DDR3L_532MHz_TI_EVM_revH",
    .EMIF2_DEFINED = 0,
    .pll_regs = &AM571x_DDR3L_532MHz_TI_EVM_revH_pll_params,
    .ctrl_regs = &AM571x_DDR3L_532MHz_TI_EVM_revH_ctrl_ioregs,
    .dmm_regs = &AM571x_DDR3L_532MHz_TI_EVM_revH_dmm_regs,
```

```
    .regs = &AM571x_DDR3L_532MHz_TI_EVM_revH_emif_regs,
    .phy_regs1 = AM571x_DDR3L_532MHz_TI_EVM_revH_emif1_ext_phy_re

    .ecc_ctrl = 00000000,
    .ecc_addr1 = 00000000,
    .ecc_addr2 = 00000000,
};
```

h 29th, 2018
n: 2.0.1

iguration - Register Values

tions

matically populated in accompanying software.

==========

ns

========== */

arams = {

egs = {

H_dmm_regs = {

gs = {

hy_regs [] = {

gs,