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EMIF Tools: Register Configuration - Step 3, DDR Timings

Directions

1) Review the DDR datasheet and provide the "*Datasheet Values*" for the corresponding parameters listed in the table in Step 3A.
2) Compare the "*Final Bit Field Values*" to the "*JEDEC Bit Field Values*". For more details, please review the Avatar EMIF Tools User Guide or the notes listed below.

Notes:

1) The "*Final Bit Field Values*" are used to calculate the register values. These are auto-populated based off of the user provided "*Datasheet Values*"
2) The "*JEDEC Bit Field Values*" are dynamically populated based off of the user provided DDR speed grade and frequency operation specified in worksheet '*Step1-SystemDetails*'.
3) The "*Final Bit Field Values*" and "*JEDEC Bit Field Values*" are provided to allow the user to perform a quick sanity check (Example: check for data possibly entered incorrectly)
4) The user is responsible to ensure that the "*Datasheet Values*" adhere to their DDR device datasheet.

3A) Enter the numerical values listed in your DDR datasheet into columns F and G for each timing entry.

Enter Values Here!

Parameter	Description	Datasheet Values		Final Bit Field Values		JEDEC Bit Field Values
		tCK	ns	Value	Units	(DDR3/L-1866 @ 666 MHz)
CAS Latency	Delay between internal READ command and data ready	9		9	tCK	**9**
CWL Latency	Delay between internal WRITE command and data ready	7		7	tCK	**7**
tRP	Precharge command period		13.91	9	tCK	**9**
tRCD	Active to read or write delay		13.91	9	tCK	**9**
tWR	Write recovery time		15	9	tCK	**9**
tRAS	Active to Precharge command period		34	22	tCK	**22**
tRC	Active to Active/Refresh command period		47.91	31	tCK	**31**
tRRD	Active Bank to Active Bank command period	4	6	5	tCK	**5**
tWTR	Internal Write to Read command delay	4	7.5	4	tCK	**4**
tXP	Exit power down mode to first valid command	3	6	3	tCK	**3**
tXSNR/tXS	Exit self refresh to commands not requiring a locked DLL	5	270	179	tCK	**179**
tXSRD/tXSDLL	Exit self refresh to commands requiring a locked DLL	512		511	tCK	**511**
tRTP	Internal Read to Precharge command delay	4	7.5	4	tCK	**4**
tCKE	CKE minimum pulse width	3	5	3	tCK	**3**
tCKESR	Minimum CKE low width for Self Refresh entry to exit	5		4	tCK	**4**
tZQCS	ZQ short calibration time	64	80	63	tCK	**63**
tRFC	Refresh to Active/Refresh command period		260	173	tCK	**173**
tRAS (max)	Active to Precharge command period (Max Value)		70200	8	tREFI intervals	**8**
tREFI	Average periodic refresh interval		7800	5194	tCK	**5194**
tFAW	Minimum Window for 4 Active Bank commands		35	See tRRD	-	**5**