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EMIF Tools: Register Configuration - Step 1, System Details

Directions

1) Enter in your specific system application details for all values. Recommended values are provided for steps 1C and 1D.
   Note: Values shown in red must be changed!

1A) System application details:

Detail	Description	Value	Units
1	Company / Board Name / Revision (Ex: TI_EVM_revC)	Custom_Board	-
2	TI SOC Part Number	AM571x	-
3	SYS_CLK1 Frequency	20	MHz
4	Required EMIF Interfaces	1	-
5	DDR Memory Type	DDR3/L	-
6	DDR Memory Frequency	666	MHz
7	DDR Data Bus Width Per EMIF	32	Bits
8	Leveling Technique: "S/W" or "H/W"	H/W	-
9	Max DRAM Operating Temperature	<= 85	℃
10	Enable ECC (May not apply to all EMIFs)	No	-
11	ECC Region 1: System Start Address	80000000	Disabled
12	ECC Region 1: System End Address	BFFFFFFF	Disabled
13	ECC Region 2: System Start Address	80000000	Disabled
14	ECC Region 2: System End Address	80000000	Disabled

NOTE: Values entered into details 11 - 14 must be a hexadecimal value between "80000000" and "FFFFFFFF". **Set start and end address to equal values to disable region.**

1B) DDR memory specifications:

Detail	Description	Value	Units
15	Speed Bin: Data Rate	1866	MHz
16	Density	4	Gb
17	Width	16	Bits
18	Speed Bin: CAS Latency @ 1866 MHz data rate	13	nCK

NOTE: Detail 18 is only used to determine the "JEDEC" values defined in worksheet "Step3-DDRTimings". Detail 18 does not correspond to the actual CAS latency programmed to the EMIF.

1C) DDR memory I/O settings (termination / output driver impedance):

Detail	Description	Value	Units	TI EVM Values**
19	ODT / Rtt_Nom	RZQ/4	Ohms	RZQ/4
20	Dynamic ODT / Rtt_Wr	Disabled	Ohms	Disabled
21	Output Driver Impedance	RZQ/7	Ohms	RZQ/7

** NOTE: IBIS models should be used for signal integrity analysis. I/O settings programmed should match simulation settings.

1D) EMIF controller I/O settings (termination / output driver impedance / and slew rate):

Detail	Description	Value	Units	TI EVM Values**
22	ODT	60	Ohms	60
23	Slew Rate: Addr/Ctrl/Clk	Fastest: SR[2:0] = 0b000	-	Fastest: SR[2:0] = 0b000
24	Slew Rate: Data/Strobe	Fastest: SR[2:0] = 0b000	-	Fastest: SR[2:0] = 0b000
25	Output Driver Impedance: Addr/Ctrl/Clk	40	Ohms	40
26	Output Driver Impedance: Data/Strobe	48	Ohms	48

** NOTE: IBIS models should be used for signal integrity analysis. I/O settings programmed should match simulation settings.