

EXAMINED BY : Yung Chang Hu	EMERGING DISPLAY TECHNOLOGIES CORPORATION	FILE NO . CAS-0007529
APPROVED BY: David Chang		ISSUE : DEC.27, 2012
		TOTAL PAGE : 34
		VERSION : 2
CUSTOMER ACCEPTANCE SPECIFICATIONS		
MODEL NO. : <u>ET028003DHU</u> (RoHS) FOR MESSRS : _____ CUSTOMER'S APPROVAL DATE : _____ BY : _____		

EMERGING DISPLAY
TECHNOLOGIES CORPORATION

MODEL NO.

ET028003DHU

VERSION

2

PAGE

0-1

RECORDS OF REVISION

DOC . FIRST ISSUE

MAY.30, 2012

DATE

REVISED
PAGE
NO.

SUMMARY

DEC.27, 2012

3

4. ELECTRICAL CHARACTERISTICS
INPUT CURRENT : TYP.=(5)→5, MAX.=(10)→10

14

8. BLOCK DIMENSIONS
PIN 10 : DNC_SCL → DNC

16

10.1 LCD MODULE CONNECTOR

PIN NO.	SYMBOL	REMARK	FUNCTION
10	DNC_SCL	1	(DNC) COMMAND / PARAMETER OR DISPLAY DATA SELECTION PIN. (SCL) SERVER AS SERIAL DATA CLOCK IN SERIAL BUS SYSTEM INTERFACE WHEN IFSEL=1. IF NOT USED, PLEASE FIX THIS PIN AT IOVCC OR GND LEVEL.
13	NWR_SCL	1	(NWR) WRITH ENABLE PIN 180 PARALLEL BUS SYSTEM INTERFACE. (SCL) SERVER AS SERIAL DATA CLOCK IN SERIAL BUS SYSTEM INTERFACE WHEN IFSEL=0. FIX IT TO IOVCC OR VSSD LEVEL WHEN NOT USED.

PIN NO.	SYMBOL	REMARK	FUNCTION
10	DNC	1	REGISTER INDEX OR REGISTER DATA SELECTION PIN. IF NOT USED, PLEASE FIX THIS PIN AT IOVCC OR GND LEVEL.
13	NWR_SCL	1	(NWR) WRITE ENABLE PIN 180 PARALLEL BUS SYSTEM INTERFACE. (SCL) SERVES AS SERIAL DATA CLOCK IN SERIAL BUS SYSTEM. FIX IT TO IOVCC OR GND LEVEL WHEN NOT USED.

→

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1. GENERAL SPECIFICATIONS

1.1 DATA SHEETS FOR CONTROLLER/DRIVER

PLEASE REFER TO :

HIMAX HX8347-I

1.2 MATERIAL SAFETY DESCRIPTION

ASSEMBLIES SHALL COMPLY WITH EUROPEAN ROHS REQUIREMENTS, INCLUDING PROHIBITED MATERIALS/COMPONENTS CONTAINING LEAD, MERCURY, CADMIUM, HEXAVALENT CHROMIUM, POLYBROMINATED BIPHENYLS (PBB) AND POLYBROMINATED DIPHENYL ETHERS (PBDE)

2. MECHANICAL SPECIFICATIONS

(1) DIAGONALS	-----	2.8 inch
(2) NUMBER OF DOTS	-----	240W * (RGB) * 320H DOTS
(3) MODULE SIZE	-----	50.5W * 69.6H * 4.45(D) mm (WITHOUT FPC SIZE)
(4) ACTIVE AREA	-----	43.2W * 57.6H mm (LCD) 44.2W * 58.6H mm (T/P)
(5) PIXEL SIZE	-----	0.18W * 0.18H mm
(6) LCD TYPE	-----	TFT , TRANSMISSIVE
(7) COLOR	-----	262K (18BIT)
(8) VIEWING DIRECTION	-----	12 O'CLOCK
(9) BACK LIGHT	-----	LED , COLOR : WHITE
(10) INTERFACE MODE	-----	RGB : 16/18 BIT MCU : 8/16/18 BIT PARALLEL DATA SPI DATA

3. ABSOLUTE MAXIMUM RATINGS

3.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	REMARK
POWER SUPPLY FOR DIGITAL	IOVCC	-0.3	4.6	V	
POWER SUPPLY FOR ANALOG	VCI	-0.3	4.6	V	
INPUT VOLTAGE	V _{IN}	-0.3	I _{OVCC} +0.5	V	

3.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

I T E M	OPERATING		STORAGE		REMARK
	MIN.	MAX.	MIN.	MAX.	
AMBIENT TEMPERATURE	-20°C	70°C	-30°C	80°C	NOTE (1), (2)
HUMIDITY	—	—	—	—	WITHOUT CONDENSATION NOTE (3)
VIBRATION	—	2.45m/S ² (0.25G)	—	11.76m/S ² (1.2 G)	5~20Hz, 1HR 20~500Hz(20Hz), 1HR 20~500Hz(500Hz), 1HR X, Y, Z, TOTAL 3HR
SHOCK	—	29.4 m/S ² (3G)	—	490m/S ² (50 G)	10 ms XYZ DIRECTIONS 1 TIME EACH
CORROSIVE GAS	NOT ACCEPTABLE		NOT ACCEPTABLE		

NOTE (1) : Ta AT -30°C : 48HR MAX.

80°C : 168HR MAX.

NOTE (2) : BACKGROUND COLOR CHANGES SLIGHTLY DEPENDING ON AMBIENT
TEMPERATURE THIS PHENOMENON IS REVERSIBLE.

NOTE (3) : Ta ≤ 60°C : 90%RH (96HRS MAX .)

Ta > 60°C : ABSOLUTE HUMIDITY MUST BE LOWER THAN THE HUMIDITY OF
90%RH AT 60°C. (96 HRS MAX.)

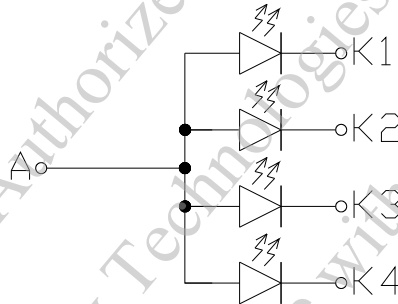
4. ELECTRICAL CHARACTERISTICS

Ta = 25 °C

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
INPUT POWER SUPPLY	VCI	OPERATION VOLTAGE	2.3	2.8	3.3	V	
INTERFACE OPERATION VOLTAGE	IOVCC	I/O SUPPLY VOLTAGE	1.65	2.8	3.3	V	
INPUT CURRENT	I _{DD}	—	—	5	10	mA	NOTE (1)
INPUT VOLTAGE	V _{IH}	H LEVEL	0.7* I _{OVCC}	—	I _{OVCC}	V	
	V _{IL}	L LEVEL	VSSD	—	0.3* I _{OVCC}	V	
OUTPUT VOLTAGE	V _{OH}	H LEVEL	0.8* I _{OVCC}	—	I _{OVCC}	V	
	V _{OL}	L LEVEL	VSSD	—	0.2* I _{OVCC}	V	
POWER SUPPLY FOR LED BACKLIGHT	A-K	I _F =80mA	—	3.3	4	V	NOTE (2)
LED LIFE TIME	—	I _{LED} =20mA (PER.LED)	30K	—	—	hrs	NOTE (3) NOTE (4)

NOTE (1) : I_{DD}=I_{IOVCC}+I_{VCI}

NOTE (2) : INTERNAL CIRCUIT DIAGRAM OF BACKLIGHT



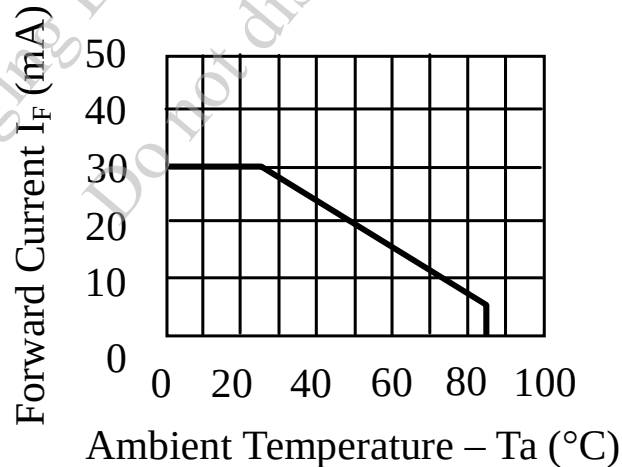
NOTE (3) : CONDITIONS, TA=25°C , CONTINUOUS LIGHTING.

NOTE (4) : DEFINITIONS OF FAILURE.

A. LCD LUMINANCE BECOMES HALF OF THE MINIMUM VALUE.

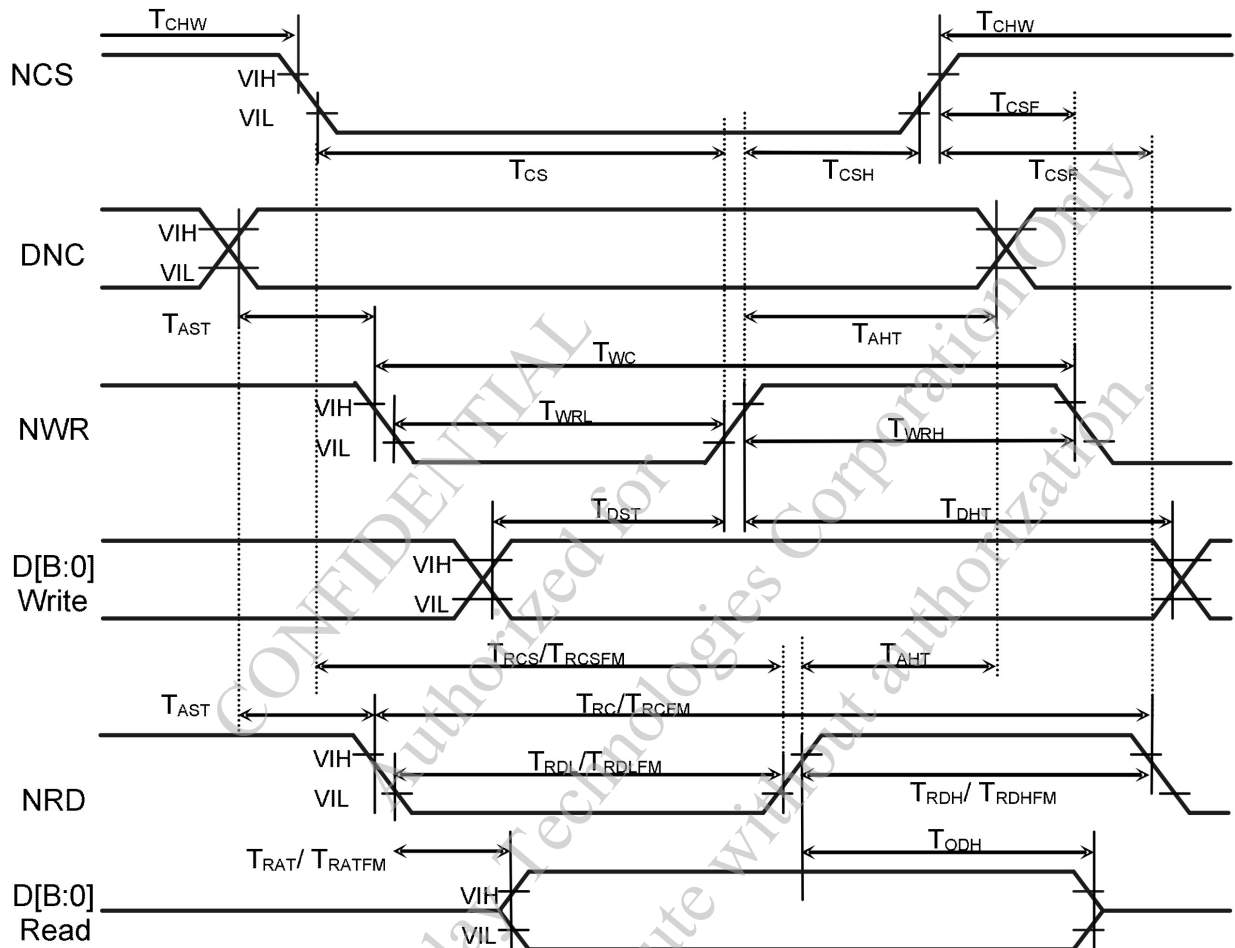
B. LED DOESN'T LIGHT NORMALLY

NOTE (5) : AMBIENT TEMP. VS. ALLOWABLE FORWARD CURRENT. (PER LED)



5. TIMING CHARACTERISTICS

5.1 PARALLEL INTERFACE CHARACTERISTICS (8080-SERIES MPU)

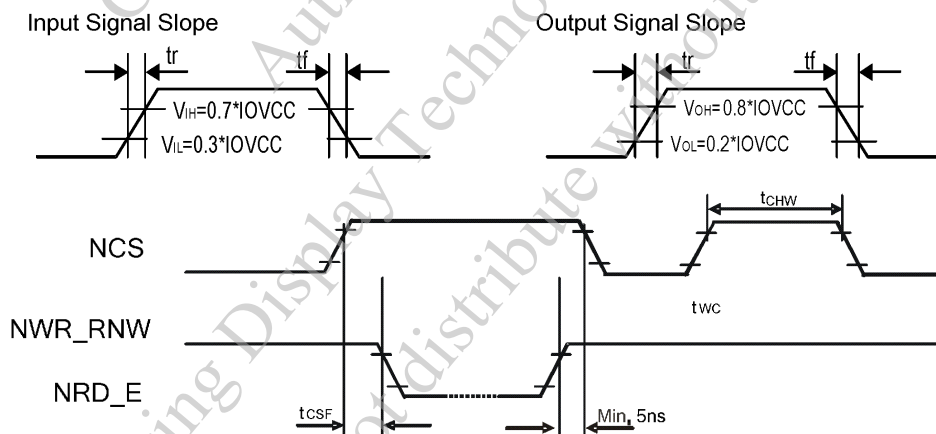


(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, Ta = -30 to 70°C)

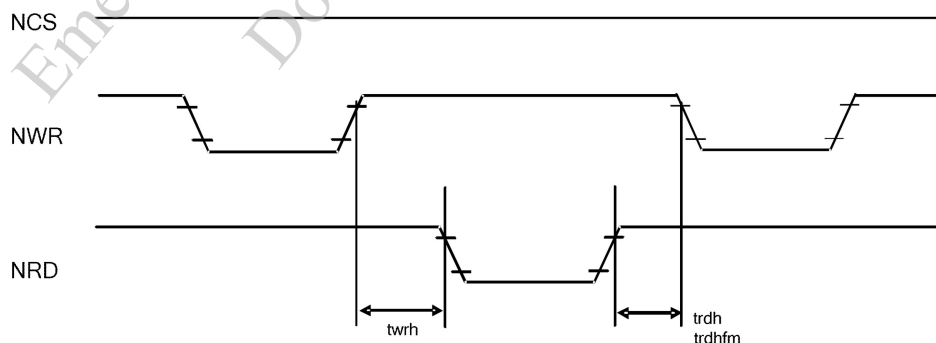
SIGNAL	SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	DESCRIPTION
DNC_SCL	tAST	ADDRESS SETUP TIME	10	—	—	ns	—
	tAHT	ADDRESS HOLD TIME(WRITE/READ)	10	—	—		
NCS	tCHW	CHIP SELECT "H" PULSE WIDTH	0	—	—	ns	—
	tCS	CHIP SELECT SETUP TIME(WRITE)	15	—	—		
	tRCS	CHIP SELECT SETUP TIME(READ ID)	45	—	—		
	tRCSFM	CHIP SELECT SETUP TIME(READ FM)	355	—	—		
	tCSF	CHIP SELECT WAIT TIME(WRITE/READ)	10	—	—		
	tCSH	CHIP SELECT HOLD TIME	10	—	—		
NWR_SCL	tWC	WRITE CYCLE(1 PIXEL FOR ONE WRITE)	100	—	—	ns	—
	tWC	WRITE CYCLE(1 PIXEL FOR 2 OR 3 WRITE)	50	—	—		
	tWRH	CONTROL PULSE "H" DURATION	15	—	—		
	tWRL	CONTROL PULSE "L" DURATION	15	—	—		
NRD(ID)	tRC	READ CYCLE(ID)	160	—	—	ns	WHEN READ ID DATA
	tRDH	CONTROL PULSE "H" DURATION(ID)	90	—	—		
	tRDL	CONTROL PULSE "L" DURATION(ID)	45	—	—		
NRD(FM)	tRCFM	READ CYCLE(FM) (1 PIXEL FOR ONE WRITE)	600	—	—	ns	WHEN READ FROM FRAME MEMORY
	tRCFM	READ CYCLE(FM) (1 PIXEL FOR 2 OR 3 WRITE)	400	—	—		
	tRDHFM	CONTROL PULSE "H" DURATION(FM)	90	—	—		
	tRDLFM	CONTROL PULSE "L" DURATION(FM)	355	—	—		
DB17 TO DB0	tDST	DATA SETUP TIME	10	—	—	ns	FOR MAXIMUM CL=30pF FOR MINIMUM CL=8pF
	tDHT	DATA HOLD TIME	10	—	—		
	tRAT	READ ACCESS TIME(ID)	—	—	100		
	tRATFM	READ ACCESS TIME(FM)	—	—	340		
	tODH	OUTPUT DISABLE TIME	20	—	80		

NOTE : THE INPUT SIGNAL RISE TIME AND FALL TIME (TR, TF) IS SPECIFIED AT 15 ns OR LESS.

LOGIC HIGH AND LOW LEVELS ARE SPECIFIED AS 30% AND 70% OF IOVCC FOR INPUT SIGNALS.

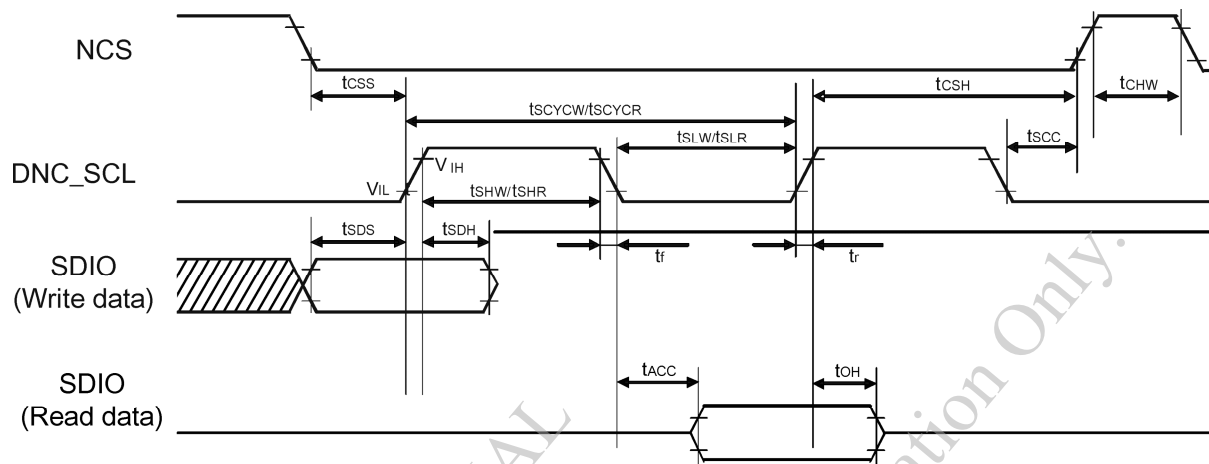


NOTE : LOGIC HIGH AND LOW LEVELS ARE SPECIFIED AS 30% AND 70% OF IOVCC



NOTE : LOGIC HIGH AND LOW LEVELS ARE SPECIFIED AS 30% AND 70% OF IOVCC

5.2 SERIAL INTERFACE CHARACTERISTICS



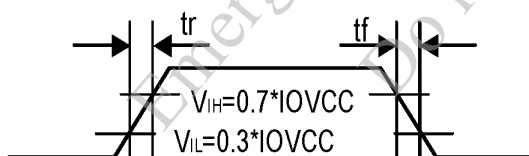
(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, Ta = -30 to 70°C)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
SERIAL CLOCK CYCLE (WRITE)	tSCYCW	SCL	14	—	—	ns
DNC_SCL "H" PULSE WIDTH (WRITE)	tSHW		6	—	—	
DNC_SCL "L" PULSE WIDTH (WRITE)	tSLW		6	—	—	
DATA SETUP TIME (WRITE)	tSDS	SDA	6	—	—	ns
DATA HOLD TIME (WRITE)	tSDH		6	—	—	
SERIAL CLOCK CYCLE (READ)	tSCYCR	SCL	150	—	—	ns
DNC_SCL "H" PULSE WIDTH (READ)	tSHR		60	—	—	
DNC_SCL "L" PULSE WIDTH (READ)	tSLR		60	—	—	
ACCESS TIME	tACC	SDI FOR MAXIMUM CL=30pF FOR MINIMUM CL=8pF	10	—	50	ns
OUTPUT DISABLE TIME	tOH	SDO FOR MAXIMUM CL=30pF FOR MINIMUM CL=8pF	15	—	50	ns
DNC_SCL TO CHIP SELECT	tSCC	SCL, NCS	20	—	—	ns
NCS "H" PULSE WIDTH	tCHW	NCS	40	—	—	ns
CHIP SELECT SETUP TIME	tCSS	NCS	15	—	—	ns
CHIP SELECT HOLD TIME	tCSH		15	—	—	

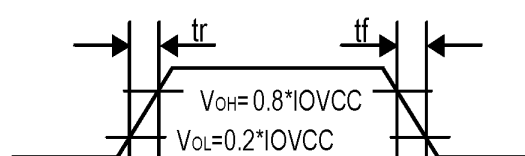
NOTE : THE INPUT SIGNAL RISE TIME AND FALL TIME (TR, TF) IS SPECIFIED AT 15 ns OR LESS.

LOGIC HIGH AND LOW LEVELS ARE SPECIFIED AS 30% AND 70% OF IOVCC FOR INPUT SIGNALS.

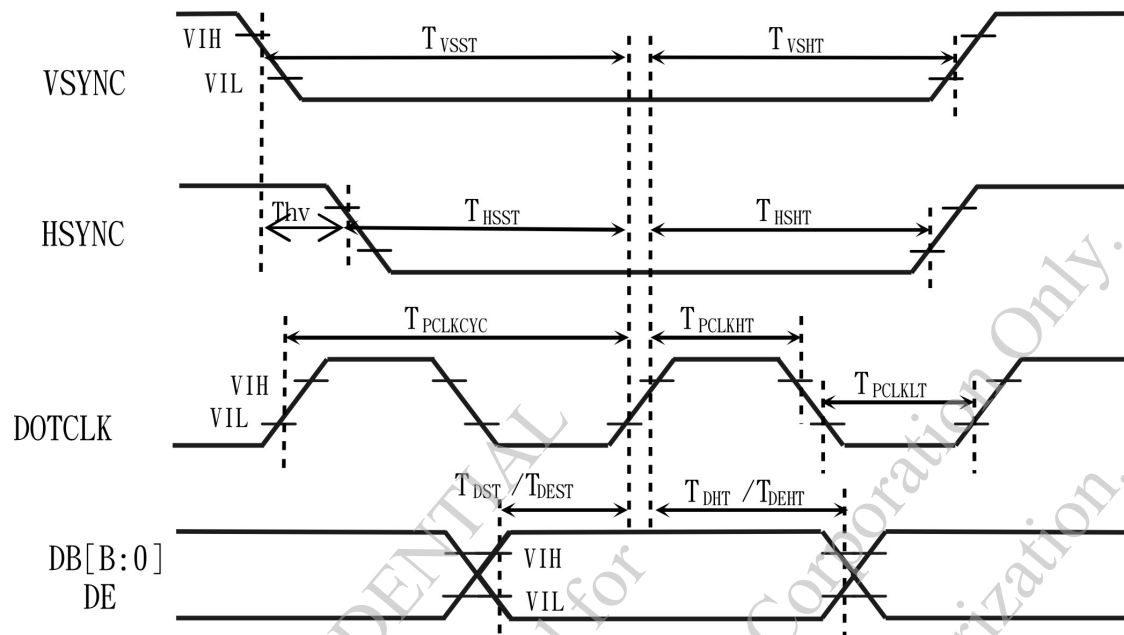
Input Signal Slope



Output Signal Slope



5.3 RGB INTERFACE CHARACTERISTICS

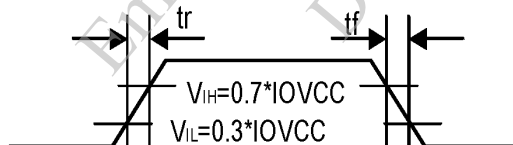


(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, Ta = -30 to 70°C)

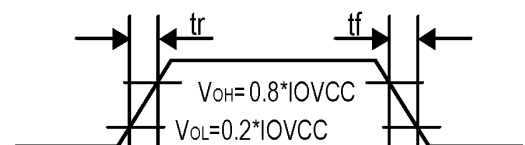
ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PIXEL LOW PULSE WIDTH	T_{CLKLT}	—	15	—	—	ns
PIXEL HIGH PULSE WIDTH	T_{CLKHT}	—	15	—	—	ns
VERTICAL SYNC. SET-UP TIME	T_{VSST}	—	15	—	—	ns
VERTICAL SYNC. HOLD TIME	T_{VSHT}	—	15	—	—	ns
HORIZONTAL SYNC. SET-UP TIME	T_{HSST}	—	15	—	—	ns
HORIZONTAL SYNC. HOLD TIME	T_{HSHT}	—	15	—	—	ns
DATE ENABLE SET-UP TIME	T_{DEST}	—	15	—	—	ns
DATE ENABLE HOLD TIME	T_{DEHT}	—	15	—	—	ns
DATE SET-UP TIME	T_{DST}	—	15	—	—	ns
DATE HOLD TIME	T_{DHT}	—	15	—	—	ns
PHASE DIFFERENCE OF SYNC SIGNAL FALLING EDGE	T_{hv}	—	0	—	240	DOTCLK

NOTE : THE INPUT SIGNAL RISE TIME AND FALL TIME (t_r , t_f) IS SPECIFIED AT 15 ns OR LESS.

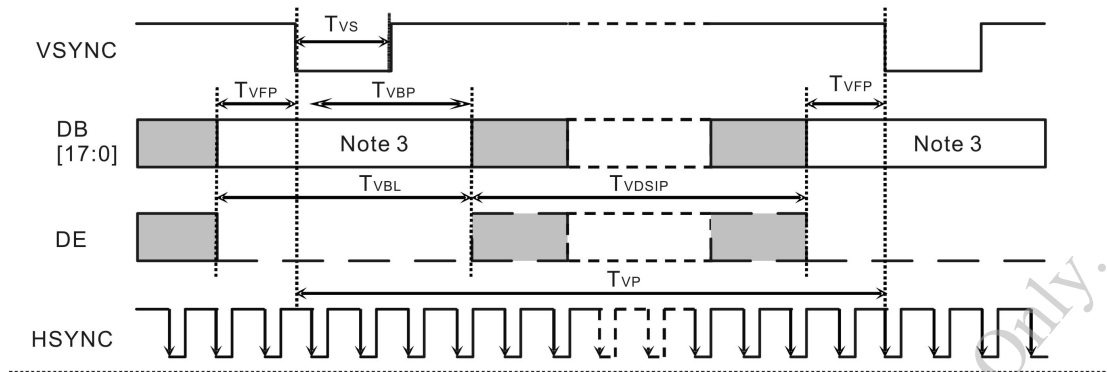
Input Signal Slope



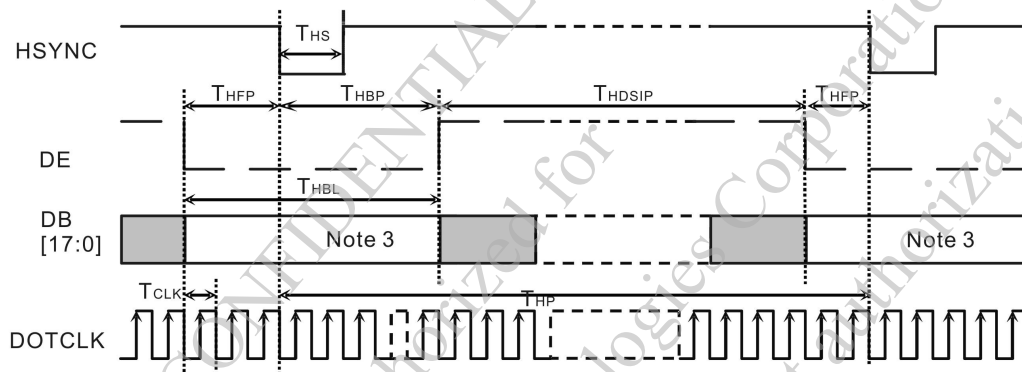
Output Signal Slope



Vertical Timing for RGB I/F



Horizontal Timing for RGB I/F

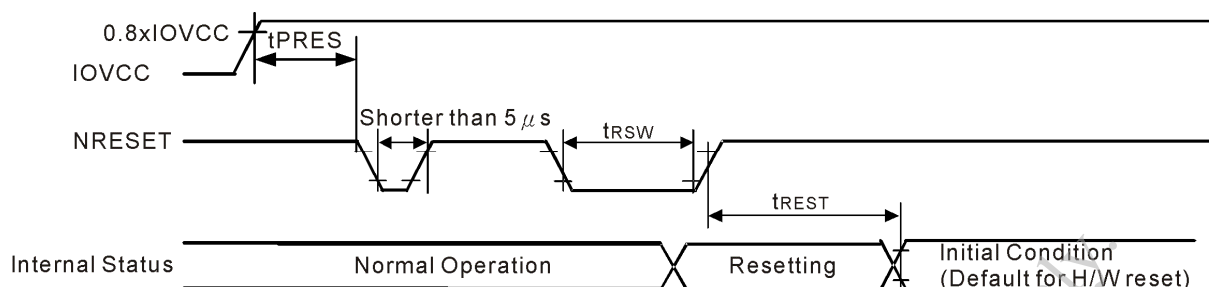


ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical Timing						
Vertical cycle period	T_{VP}	—	324	326	452	HS
Vertical low pulse width	T_{VS}	—	2	2	—	HS
Vertical front porch	T_{VFP}	—	2	2	6	HS
Vertical back porch	T_{VBP}	—	2	4	126	HS
Vertical blanking period	T_{VBL}	$T_{VBP} + T_{VFP}$	4	6	132	HS
Vertical active area	T_{VDSIP}	—	—	320	—	HS
			—		—	HS
			—		—	HS
Vertical refresh rate	$TVRR$	Frame rate	50	60	80	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}	—	244	252	1008	DOTCLK
Horizontal low pulse width	T_{HS}	—	2	2	256	DOTCLK
Horizontal front porch	T_{HFP}	—	2	4	256	DOTCLK
Horizontal back porch	T_{HBP}	—	2	8	256	DOTCLK
Horizontal blanking period	T_{HBL}	$T_{HBP} + T_{VFP}$	4	12	256	DOTCLK
Horizontal active area	T_{HDSIP}	—	—	240	—	DOTCLK
Pixel clock cycle $TVRR=60Hz$	f_{CLKCYC}	—	3.9	—	16.6	MHz

NOTE :

- (1)IOVCC=1.65 TO 3.3V, VCI=2.3 TO 3.3V, VSSA=VSSD=0V, TA=-30 TO 70°C (TO +85°C NO DAMAGE)
- (2)DATA LINES CAN BE SET TO "HIGH" OR "LOW" DURING BLANKING TIME – DON'T CARE.
- (3)HP IS MULTIPLES OF DOTCLK.
- (4)16.6MHz IS USING AT BELOW CONDITION: 324(HS)×1008(DOTCLK)×50(Hz)

5.4 RESET INPUT TIMING

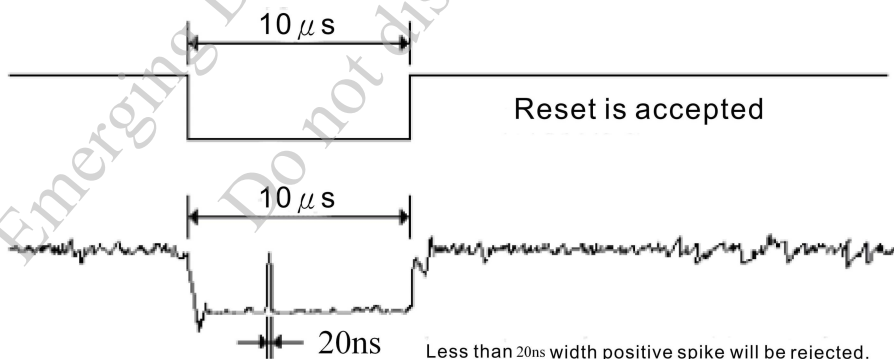


SYMBOL	PARAMETER	RELATED PINS	MIN.	TYP.	MAX.	NOTE	UNIT
t_{RESW}	RESET LOW PULSE WIDTH ⁽¹⁾	NRESET	10	—	—		μs
t_{REST}	RESET COMPLETE TIME ⁽²⁾	—	5	—	—	WHEN RESET APPLIED DURING STB OUT MODE	ms
		—	120	—	—	WHEN RESET APPLIED DURING STB MODE	ms
t_{PRES}	RESET GOES HIGH LEVEL AFTER POWER ON TIME	NRESET & IOVCC	1	—	—	RESET GOES HIGH LEVEL AFTER POWER ON	ms

NOTE : (1) SPIKE DUE TO AN ELECTROSTATIC DISCHARGE ON NRESET LINE DOES NOT CAUSE IRREGULAR SYSTEM RESET ACCORDING TO THE TABLE BELOW.

NRESET PULSE	ACTION
SHORTER THAN $5\mu s$	RESET REJECTED
LONGER THAN $10\mu s$	RESET
BETWEEN $5\mu s$ AND $10\mu s$	RESET START

- (2) DURING THE RESETTING PERIOD, THE DISPLAY WILL BE BLANKED (THE DISPLAY IS ENTERING BLANKING SEQUENCE, WHICH MAXIMUM TIME IS 120 MS, WHEN RESET STARTS IN STB OUT -MODE. THE DISPLAY REMAINS THE BLANK STATE IN STB -MODE) AND THEN RETURN TO DEFAULT CONDITION FOR H/W RESET.
- (3) DURING RESET COMPLETE TIME, ID2 AND VCOMOF VALUE IN OTP WILL BE LATCHED TO INTERNAL REGISTER DURING THIS PERIOD. THIS LOADING IS DONE EVERY TIME WHEN THERE IS H/W RESET COMPLETE TIME (t_{REST}) WITHIN 5MS AFTER A RISING EDGE OF NRESET.
- (4) SPIKE REJECTION ALSO APPLIES DURING A VALID RESET PULSE AS SHOWN BELOW :



- (5) IT IS NECESSARY TO WAIT 5MSEC AFTER RELEASING! RES BEFORE SENDING COMMANDS. ALSO STB OUT COMMAND CANNOT BE SENT FOR 120MSEC.

6. OPTICAL CHARACTERISTICS NOTE (2)

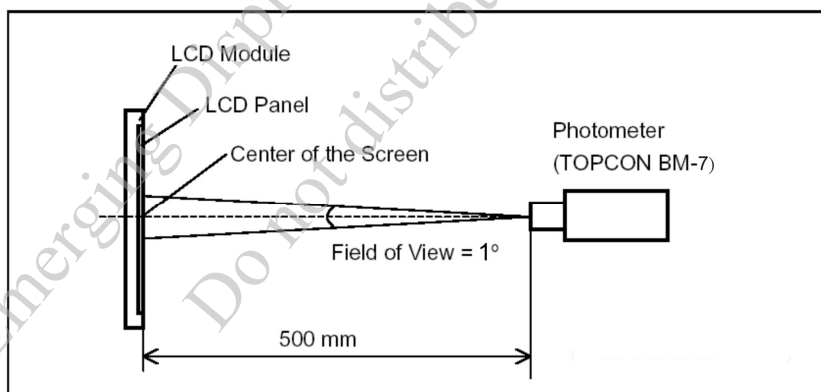
6.1 OPTICAL CHARACTERISTICS

Ta = 25 °C

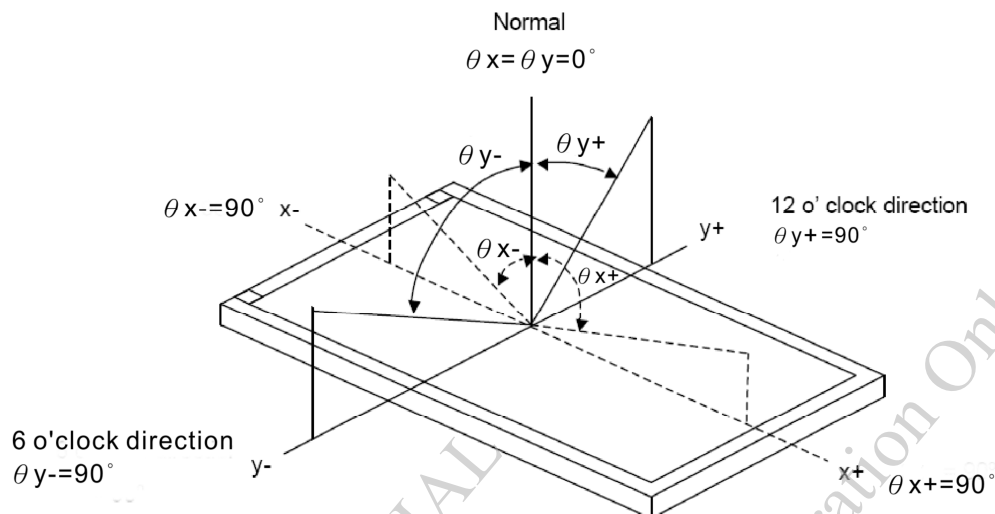
ITEM		SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT	REMARK
VIEWING ANGLE	HOR.	θ_{x+}	CENTER CR≥10	$\theta_{y=0^{\circ}}$	70	75	—	deg .	(2)
		θ_{x-}		65	70	—	(3)		
	VER.	θ_{y+}		$\theta_{x=0^{\circ}}$	70	75	—		
		θ_{y-}		50	55	—			
CONTRAST RATIO		CR	NTSC : 60%		400	500	—	ms	(3)
RESPONSE TIME		t r (rise)			—	10	20		(4)
		t f (fall)			—	20	40		
THE BRIGHTNESS OF MODULE		B	VIEWING NORMAL AUNLE $\theta_x = 0^{\circ}$ $\theta_y = 0^{\circ}$		240	280	—	cd/m ²	(5)
COLOR OF CIE COORDINATE	WHITE	W _x			0.265	0.315	0.365	—	(6)
		W _y			0.280	0.330	0.380		
	RED	R _x			0.565	0.615	0.665	—	
		R _y			0.295	0.345	0.395		
	GREEN	G _x			0.275	0.325	0.375	—	
		G _y			0.550	0.610	0.650		
	BLUE	B _x			0.090	0.140	0.190	—	
		B _y	0.050	0.100	0.150				
THE BRIGHTNESS OF UNIFORMITY		—	IF=80mA		75	80	—	%	—

NOTE (1) : TEST EQUIPMENT SETU :

AFTER STABILIZING AND LEAVING THE PANEL ALONE AT A GIVEN TEMPERATURE FOR 30 MINUTES. WINDLESS AND DARK ROOM. OPTICAL SPECIFICATIONS ARE MEASURED BY TOPCON BM-7 (FAST) WITH A VIEWING ANGLE OF 1° AT A DISTANCE OF 50cm AND NORMAL DIRECTION.



NOTE (2) : DEFINITION OF VIEWING ANGLE :

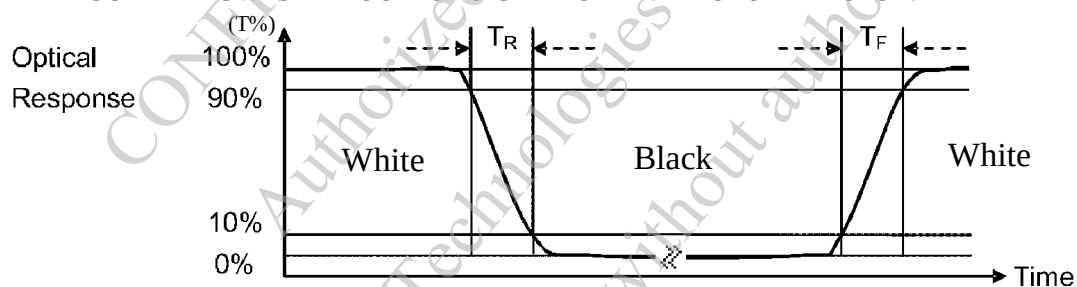


NOTE (3) : DEFINITION OF CONTRAST RATIO :

$$\text{CONTRAST RATIO (CR)} = \frac{\text{BRIGHTNESS MEASURED WHEN LCD IS AT "WHITE STATE"}}{\text{BRIGHTNESS MEASURED WHEN LCD IS AT "BLACK STATE"}}$$

NOTE (4) : DEFINITION OF RESPONSE TIME : TR AND TF

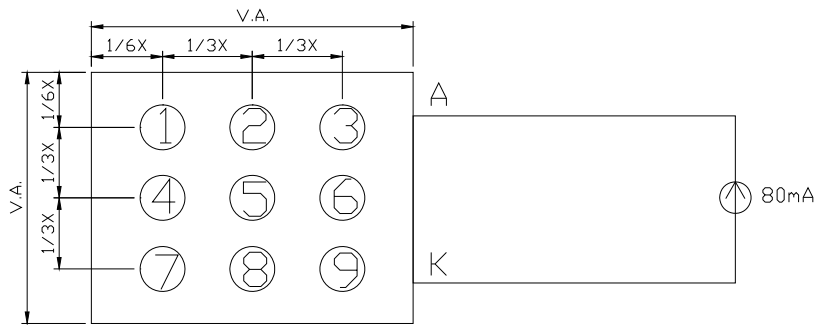
THE FIGURE BELOW IS THE OUTPUT SIGNAL OF THE PHOTO DETECTOR.



NOTE (5) : BRIGHTNESS MEASURED WHEN LCD IS AT "WHITE STATE"

NOTE (6) : THE 100% TRANSMISSION IS DEFINED AS THE TRANSMISSION OF LCD PANEL WHEN ALL THE INPUT TERMINALS OF MODULE ARE ELECTRICALLY OPENED.

6.2 THE TEST METHOD OF BRIGHTNESS AND UNIFORMITY

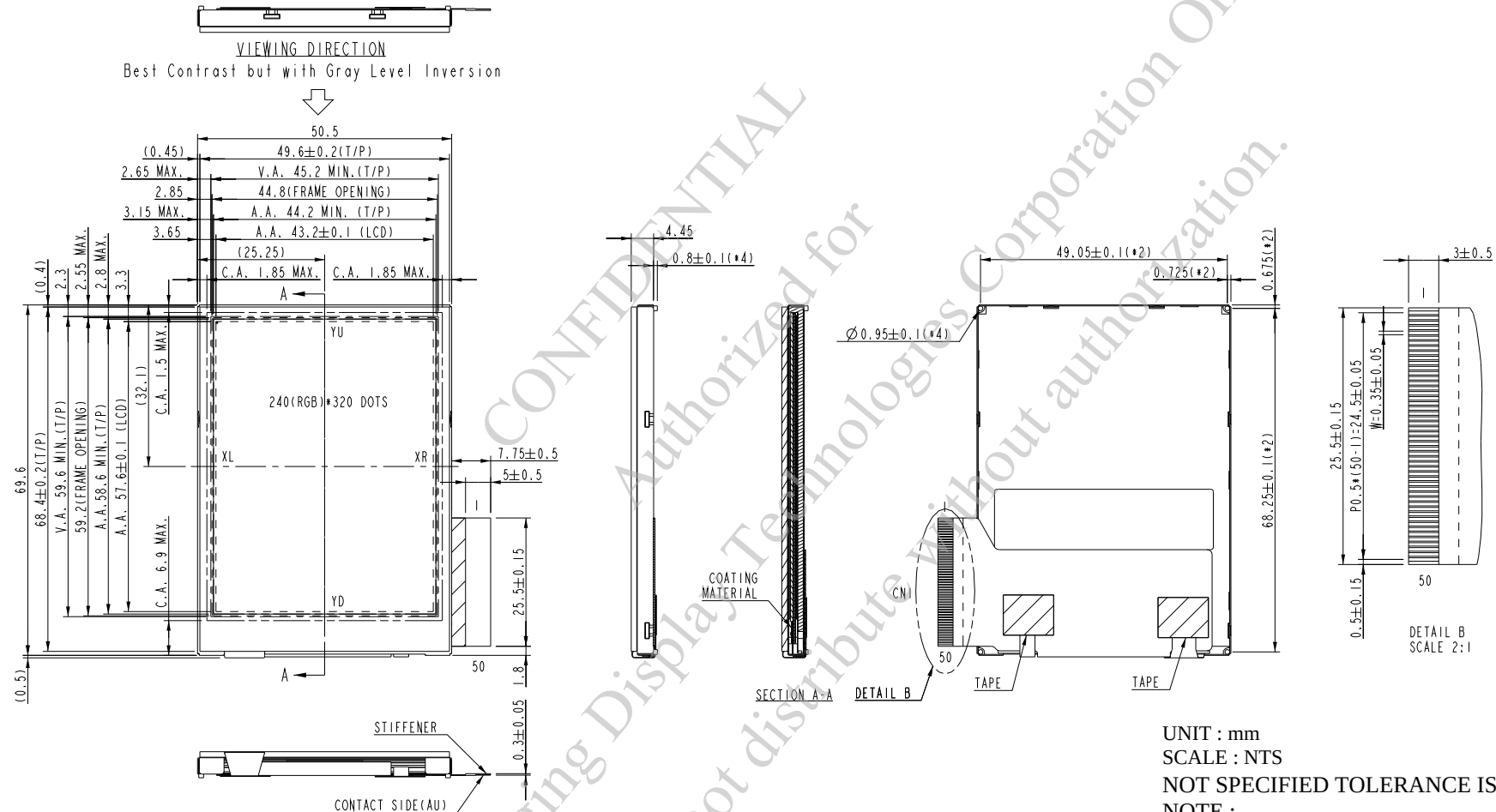


UNIT : mm

6.3 THE CALCULATING METHOD OF UNIFORMITY

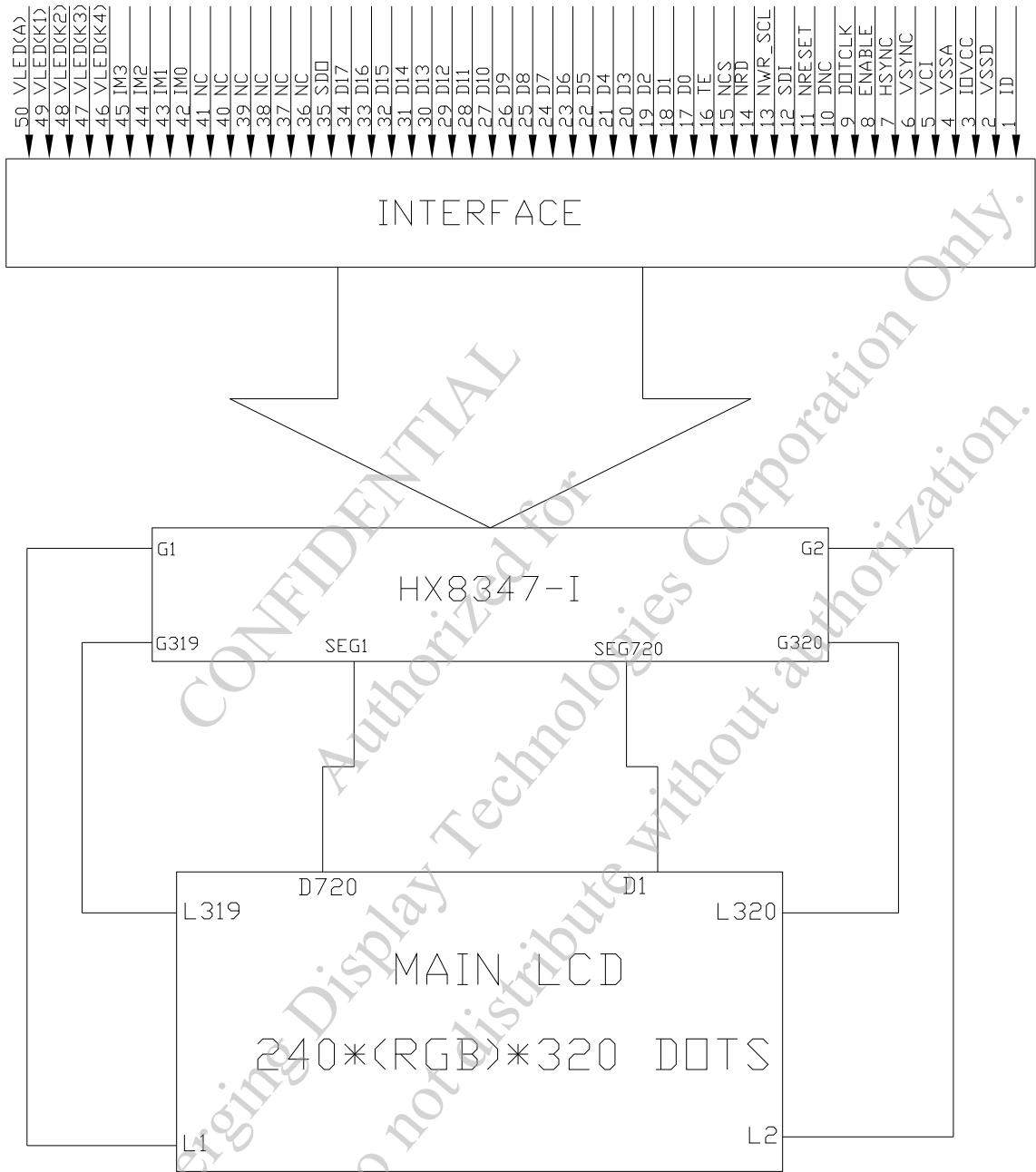
UNIFORMITY: $\left[1 - \frac{\text{MAXIMUM BRIGHTNESS} - \text{MINIMUM BRIGHTNESS}}{\text{AVERAGE BRIGHTNESS}} \right] \times 100\%$

7. OUTLINE DIMENSIONS

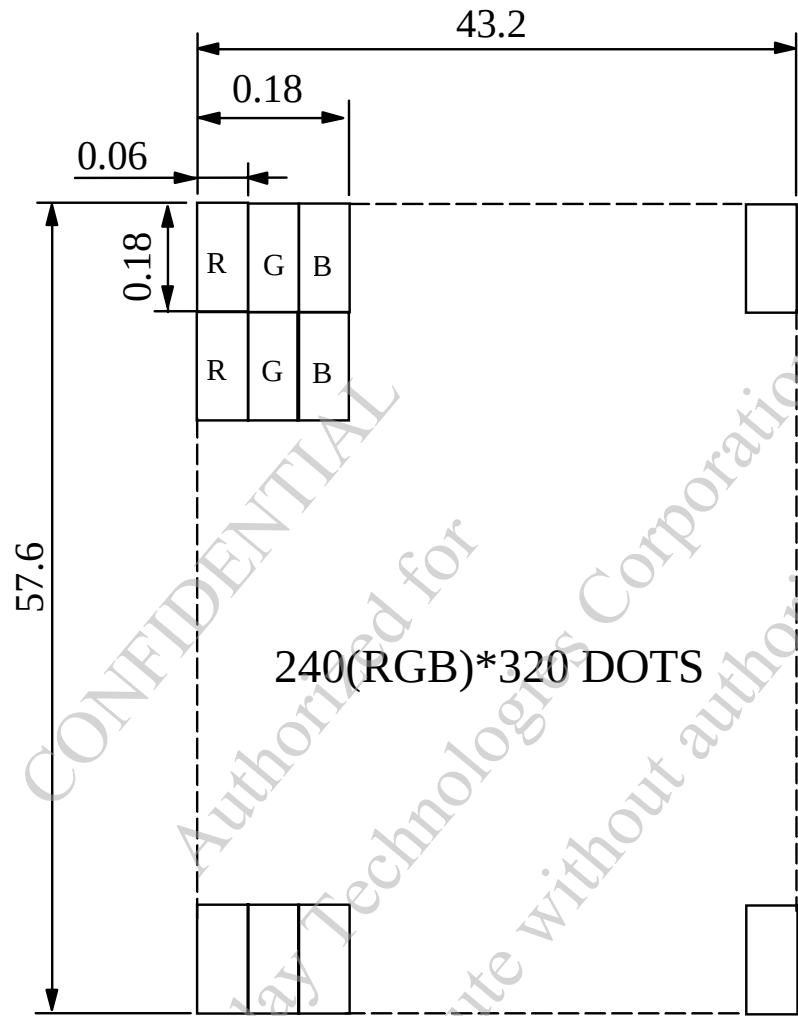


UNIT : mm
SCALE : NTS
NOT SPECIFIED TOLERANCE IS ± 0.3
NOTE :
RECOMMEND MATCH CONNECTOR
KYOCERA:04 6240 050 SERIES

8. BLOCK DIMENSION



9. DETAIL DRAWING OF DOT MATRIX



UNIT : mm
SCALE : NTS
NOT SPECIFIED TOLERANCE IS ± 0.1
DOTS MATRIX TOLERANCE IS ± 0.01

10. INTERFACE SIGNALS

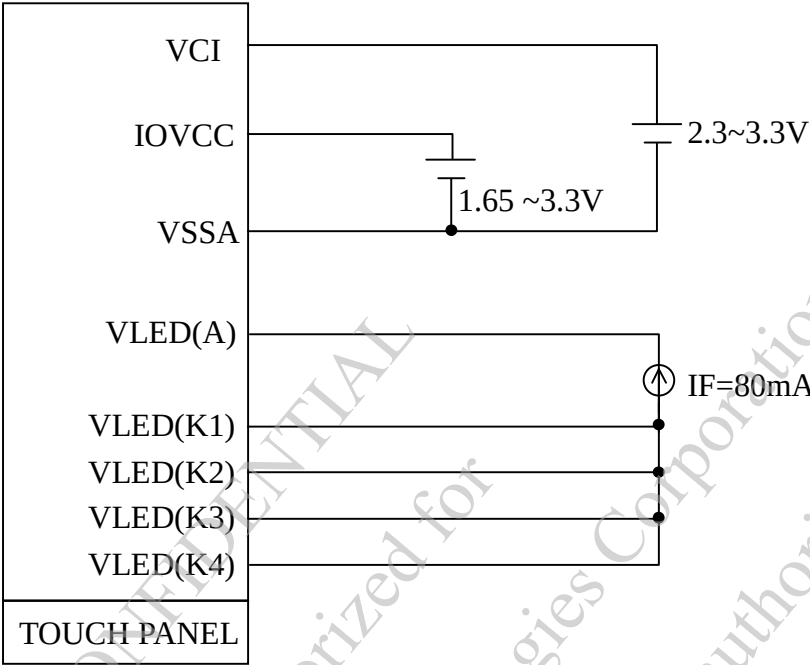
10.1 LCD MODULE CONNECTOR

PIN NO.	SYMBOL	REMARK	FUNCTION
1	ID	O	MAKER'S IDENTIFICATION (MAY ESTABLISH "H", "L" OR "NC") IF THE CUSTOMER HAS MORE THAN TWO MAKERS WHO APPLIED DIFFERENT S/W, CAN USE THIS PIN TO DETECT THE CODE BY THE MPU AND DECIDE THE MAKER'S ID. MOST IMPORTANTLY, THE CUSTOMER MUST DESIGN THIS PIN ON THE MAIN BOARD AS WELL AND LEAVE IT OPEN AS NOT USED. NOTE : EDT MODULE'S SETTING IS "H".
2	VSSD	I	DIGITAL GROUND
3	IOVCC	I	DIGITAL IO PAD POWER SUPPLY
4	VSSA	I	ANALOG GROUND
5	VCI	I	ANALOG POWER SUPPLY
6	VSNC	I	VERTICAL SYNCHRONIZING SIGNAL IN RGB INTERFACE. HAS TO BE FIXED TO VSSD LEVEL IF IT IS NOT USED.
7	HSNC	I	HORIZONTAL SYNCHRONIZING SIGNAL IN RGB INTERFACE. HAS TO BE FIXED TO VSSD LEVEL IF IT IS NOT USED.
8	ENABLE	I	A DATA ENABLE SIGNAL IN RGB I/F MODE. HAS TO BE FIXED TO VSSD LEVEL IF UNUSED (HIGH ACTIVE, IF EPL=0).
9	DOTCLK	I	DOT CLOCK SIGNAL IN RGB INTERFACE. HAS TO BE FIXED TO VSSD LEVEL IF IT IS NOT USED.
10	DNC	I	REGISTER INDEX OR REGISTER DATA SELECTION PIN. IF NOT USED, PLEASE FIX THIS PIN AT IOVCC OR GND LEVEL.
11	NRESET	I	RESET PIN. SETTING EITHER PIN LOW INITIALIZES THE LSI. MUST BE RESET AFTER POWER IS SUPPLIED.
12	SDI	I	SERIAL DATA INPUT PIN AND OUTPUT PIN(SDA) IN SERIAL BUS SYSTEM INTERFACE I. SERIAL DATA INPUT PIN (SDI) IN SERIAL BUS SYSTEM INTERFACE II. THE DATA IS INPUTTED ON THE RISING EDGE OF THE SCL SIGNAL.
13	NWR_SCL	I	(NWR) WRITE ENABLE PIN I80 PARALLEL BUS SYSTEM INTERFACE. (SCL) SERVES AS SERIAL DATA CLOCK IN SERIAL BUS SYSTEM. FIX IT TO IOVCC OR GND LEVEL WHEN NOT USED.
14	NRD	I	(NRD) READ ENABLE PIN I80 PARALLEL BUS SYSTEM INTERFACE. IF NOT USED, PLEASE FIX THIS PIN AT IOVCC OR GND LEVEL
15	NCS	I	CHIP SELECT SIGNAL. LOW : CHIP CAN BE ACCESSED; HIGH : CHIP CANNOT BE ACCESSED. MUST BE CONNECTED TO VSSD IF NOT IN USE.
16	TE	O	TEARING EFFECT OUTPUT, IF NOT USED, PLEASE OPEN THIS PIN.

PIN NO	SYMBOL	REMARK	FUNCTION																																																																	
17	D0	I/O	1. 18-BIT BI-DIRECTIONAL DATA BUS FOR SYSTEM INTERFACE. 8-BIT BUS: USE D7-D0 AND D17-D8 UNUSED. 16-BIT BUS: USE D15-D0 AND D17-D16 UNUSED. 18-BIT BUS: USE D17-D0 2. 18-BIT DATA BUS FOR RGB INTERFACE 16-BIT BUS: USE D11-D1 AND D17-D13 AND D0,D12 UNUSED. 18-BIT BUS: USE D17-D0 CONNECTED UNUSED PINS TO THE VSSD LEVEL.																																																																	
18	D1	I/O																																																																		
19	D2	I/O																																																																		
20	D3	I/O																																																																		
21	D4	I/O																																																																		
22	D5	I/O																																																																		
23	D6	I/O																																																																		
24	D7	I/O																																																																		
25	D8	I/O																																																																		
26	D9	I/O																																																																		
27	D10	I/O																																																																		
28	D11	I/O																																																																		
29	D12	I/O																																																																		
30	D13	I/O																																																																		
31	D14	I/O																																																																		
32	D15	I/O																																																																		
33	D16	I/O																																																																		
34	D17	I/O																																																																		
35	SDO	O	SERIAL DATA OUTPUT. IF NOT USE, LET IT TO OPEN.																																																																	
36	NC	NC	NO USE, LET IT OPEN																																																																	
37	NC	NC	NO USE, LET IT OPEN																																																																	
38	YU	O	TOP PANEL																																																																	
39	XL	O	LEFT PANEL																																																																	
40	YD	O	DOWN PANEL																																																																	
41	XR	O	RIGHT PANEL																																																																	
42	IM3	I	SYSTEM INTERFACE SELECT. <table><thead><tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>INTERFACE</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 16-BIT PARALLEL TYPE I</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 8-BIT PARALLEL TYPE I</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 16-BIT PARALLEL TYPE II</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 8-BIT PARALLEL TYPE II</td></tr><tr><td>0</td><td>1</td><td>0</td><td>ID</td><td>3-WIER SERIAL INTERFACE I</td></tr><tr><td>0</td><td>1</td><td>1</td><td>—</td><td>4-WIER SERIAL INTERFACE I</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 18-BIT PARALLEL TYPE I</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 9-BIT PARALLEL TYPE I</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 18-BIT PARALLEL TYPE II</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 9-BIT PARALLEL TYPE II</td></tr><tr><td>1</td><td>1</td><td>0</td><td>ID</td><td>3-WIER SERIAL INTERFACE II</td></tr><tr><td>1</td><td>1</td><td>1</td><td>—</td><td>4-WIER SERIAL INTERFACE II</td></tr></tbody></table>	IM3	IM2	IM1	IM0	INTERFACE	0	0	0	0	8080 MCU 16-BIT PARALLEL TYPE I	0	0	0	1	8080 MCU 8-BIT PARALLEL TYPE I	0	0	1	0	8080 MCU 16-BIT PARALLEL TYPE II	0	0	1	1	8080 MCU 8-BIT PARALLEL TYPE II	0	1	0	ID	3-WIER SERIAL INTERFACE I	0	1	1	—	4-WIER SERIAL INTERFACE I	1	0	0	0	8080 MCU 18-BIT PARALLEL TYPE I	1	0	0	1	8080 MCU 9-BIT PARALLEL TYPE I	1	0	1	0	8080 MCU 18-BIT PARALLEL TYPE II	1	0	1	1	8080 MCU 9-BIT PARALLEL TYPE II	1	1	0	ID	3-WIER SERIAL INTERFACE II	1	1	1	—	4-WIER SERIAL INTERFACE II
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46	VLED(K4)	I	POWER SUPPLY FOR LED(-)																																																																	
47	VLED(K3)	I	POWER SUPPLY FOR LED(-)																																																																	
48	VLED(K2)	I	POWER SUPPLY FOR LED(-)																																																																	
49	VLED(K1)	I	POWER SUPPLY FOR LED(-)																																																																	
50	VLED(A)	I	POWER SUPPLY FOR LED(+)																																																																	

11. POWER SUPPLY

11.1 POWER SUPPLY FOR LCM



12. TOUCH PANEL SPECIFICATION

12.1 ELECTRICAL CHARACTERISTICS

Ta = 25°C

ITEM	CONDITION	SPEC.	UNIT
LINEARITY	—	≤ 1.5	%
TRANSMISSION	ASTM D1003	Min 80	%
TERMINAL RESISTANCE	X AXIS	160 ~ 640	Ω
	Y AXIS	260 ~ 1040	
INSULATION RESISTANCE	DC25V	≥ 20	MΩ
INPUT VOLTAGE (V)	—	5 (TYP.)	V

12.2 PRECAUTIONS IN USE OF TOUCH PANEL

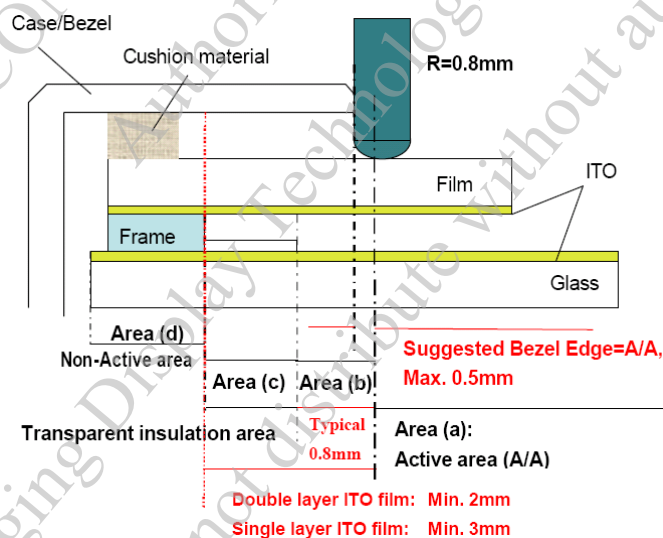
12.2.1 PURPOSE :

IN ORDER TO PREVENT ACCIDENTAL USE AND PERFORMANCE DETERIORATION, PLEASE KEEP THE FOLLOWING PRECAUTIONS AND INHIBITED POINTS.

12.2.2 ITEM AND ILLUSTRATION :

(1) STRUCTURE, AREA DEFINITION

THE STRUCTURE AND THE PERFORMANCE GUARANTEED AREA OF THIS TOUCH PANEL ARE DEFINED BELOW :



THE ABOVE FIGURE IS OUR DESIGN RULE OF TOUCH PANEL.

IF IT CANNOT MEET YOUR REQUIREMENT, PLEASE CONTACT WITH OUR ENGINEERS FOR FURTHER DISCUSSION.

ABOVE FIGURE ILLUSTRATES THE RECOMMENDED BEZEL AND CUSHION DESIGN. IN ORDER TO PREVENT UNUSUAL PERFORMANCE DEGRADATION AND MALFUNCTION OF A TOUCH PANEL, PLEASE CARRY OUT THE SET CASE DESIGNING AND A TOUCH PANEL ASSEMBLING METHOD AFTER SURELY CONSIDERING THE DEFINITION OF EACH AREA ILLUSTRATED IN ABOVE FIGURE.

AREA(a) : ACTIVE AREA

THE ACTIVE AREA IS GUARANTEED THE POSITION DATA DETECTABLE PRECISION, OPERATION FORCE AND OTHER OPERATIONS. IT IS STRONGLY RECOMMENDED TO PLACE THE OPERATION BUTTON OR MENU KEYS WITHIN THE ACTIVE AREA. DUE TO STRUCTURE, THE ACTIVE AREA IS LESS DURABLE AT THE EDGE OR CLOSE TO THE EDGE.

AREA(b) : OPERATION NON-GUARANTEED AREA

THIS AREA DOES NOT GUARANTEE A TOUCH PANEL OPERATION AND ITS FUNCTION. WHEN THIS AREA IS PRESSED, TOUCH PANEL SHOWS DEGRADATION OF ITS PERFORMANCE AND DURABILITY SUCH AS A PEN SLIDING DURABILITY BECOMES ABOUT ONE-TENTH COMPARED WITH THE ACTIVE AREA (AREA-(A) AS GUARANTEED AREA) AND ITS OPERATION FORCE REQUIRES ABOUT DOUBLE. ABOUT 0.5 MM OUTSIDE FROM A BOUNDARY OF THE ACTIVE AREA CORRESPONDS TO THIS AREA.

AREA(c) : PRESSING PROHIBITION AREA

THE AREA WHICH FORBIDS PRESSING, BECAUSE AN EXCESSIVE LOAD IS APPLIED TO A TRANSPARENT ELECTRODE (ITO) AND A SERIOUS DAMAGE IS GIVEN TO A TOUCH PANEL FUNCTION BY PRESSING.

AREA(d) : NON-ACTIVE AREA

THE AREA DOES NOT ACTIVATE EVEN IF PRESSED.

(2) CAUTIONS FOR INSTALLING AND ASSEMBLING

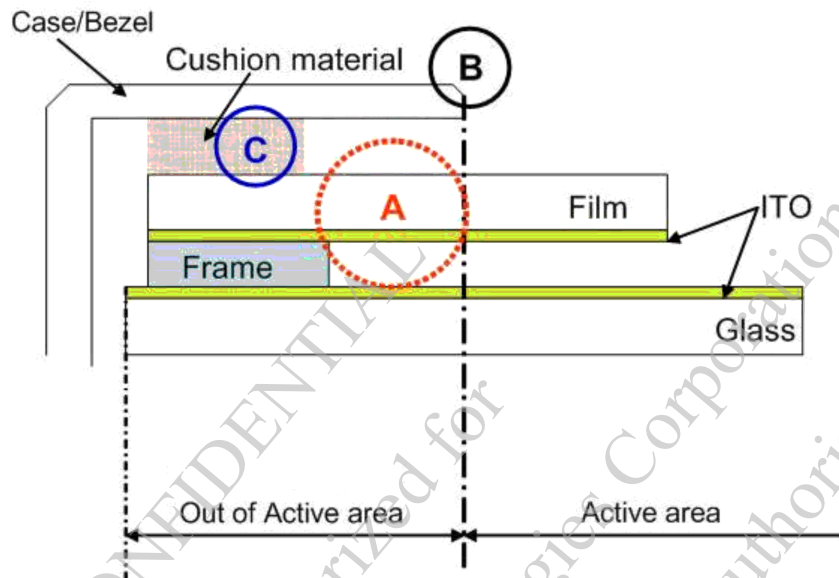
(i) DO NOT GIVE EXCESSIVE STRAIN TO THE PRODUCT.

(ii) FLEXIBLE PATTERN CABLE IS CONNECTED TO THE BODY BY THERMAL PRESSURE METHOD. SO, DO NOT APPLY EXCESSIVE FORCES TO THE FLEXIBLE PATTERN. DO NOT ADD AN EXCESSIVE FORCE TO A FPC (FLEX TAIL) THAT MAKES PEELING OFF OF THE FPC FROM THE PRODUCT. DO NOT FIX, ADHERE OR MOUNT ANY ADDITIONAL GOODS ON THE FPC SUCH AS ADDITIONAL FILM/PLATE ON THE FPC, BECAUSE SUCH ADDITIONAL GOODS WILL APPLY A STRESS AT THE FPC BONDING AREA. IT MAY AFFECT THE CONDUCTIVITY OF FPC WITH TOUCH PANEL.

(iii) IN ORDER NOT TO APPLY LOAD ON THE DISPLAY, PROVIDE A CLEARANCE OF AT LEAST 0.3MM BETWEEN THE PRODUCT AND DISPLAY.

(iv) WE RECOMMEND THE DESIGN OF A CASE OR BEZEL SHOULD COVERS THE BOUNDARY OF THE ACTIVE AREA INSIDE IN ORDER TO PREVENT AN OPERATION AT OUTSIDE OF THE ACTIVE AREA WHICH CAN NOT GUARANTEE THE FUNCTION OR DURABILITY.
BEZEL'S EDGE PART MAY GUIDE THE PEN SLIDING ON THE SAME POSITION REPEATEDLY. IF THE BEZEL IS PLACED OUTSIDE OF THE ACTIVE AREA, IT MAY CAUSE THE DAMAGE OF THE ITO FILM.

- (v) PRESSING INSIDE OF BOUNDARY OF THE FRAME(PART (A) AS SHOWN IN BELOW) MAY CAUSES FAULT OPERATION, SO PLEASE DESIGN TO AVOID PRESSING OF TOUCH PANEL AT PART (A) SUCH AS HAVING GASKET/CUSHION AT PART (C). PARTICULARLY THE AREA (B) SHALL BE FREE FROM BURR. THE GASKET/CUSHION MATERIAL AT THE PART (C) SHOULD NOT BE EXCEEDED TO INSIDE OF THE BOUNDARY OF THE FRAME.



- (vi) TO PREVENT GIVING DISTORTION TO THE FILM OF THE PRODUCT AND PEELING OFF OF THE FILM FROM THE PRODUCT, DO NOT FIX THE FILM AND A SET CASE OR A SHOCK ABSORBING MATERIAL ADHERED TO A SET CASE BY ADHESION.
- (vii) WIPE OFF THE STAIN ON THE PRODUCT BY USING SOFT CLOTH MOISTENED WITH ETHANOL. TAKE CARE NOT TO ALLOW ETHANOL TO SOAK INTO THE JOINT OF UPPER FILM AND BOTTOM GLASS. IT MAY OTHERWISE CAUSE PEELING OR DEFECTIVE OPERATION. DO NOT USE ANY ORGANIC SOLVENT OR DETERGENT OTHER THAN ETHANOL.
- (viii) THE CORNERS OF THE PRODUCT ARE NOT CHAMFERED AND ARE SHARP. WHEN POSITIONING AND FIXING THE PRODUCT ON THE CASE, PROVIDE A ROUND PART ON THE CORNER OF THE CASE SO AS NOT TO APPLY LOAD ON THE CORNER OF THE TRANSPARENT TOUCH PANEL.
- (ix) DO NOT PRESS THE FILM OF THE PRODUCT WHEN THIS PRODUCT IS BUILT INTO A SET.
- (3) CAUTIONS FOR OPERATION
- (i) OPERATE IT WITH A POLYACETAL PEN (TIP R0.8 OR OVER) OR A BELLY OF A FINGER WITHOUT APPLYING EXCESSIVE LOAD. NEVER USE ANY MECHANICAL PENCILS, BALL POINT PENS AND HARD FINGERTIPS WHO'S TIP IS HARD FOR INPUT, OTHERWISE MALFUNCTIONS MAY RESULT.

- (ii) THE INPUT POSITION MAY BE FLUCTUATED A LITTLE THROUGH LONG-TIME USE. IT IS DESIRABLE TO PROVIDE A ZERO-ADJUSTMENT FUNCTION BY USING A CIRCUIT AND SOFTWARE.
- (iii) OPERATION AT THE OUT OF ACTIVE AREA IS OUT OF OUR GUARANTEE. IT CAUSES A SERIOUS DAMAGE OF A TRANSPARENT ELECTRODE. DO NOT OPERATE AT THE OUT OF ACTIVE AREA.
- (iv) IN CASE OF CLEANING THE PART OF THE CASE BOUNDARY OF ACCOMPLISHED SET, USE A SOFT CLOTH WITH A FINGER BERRY OR A COTTON BUD. DO NOT CLEAN WITH A THING OTHER THAN THE FINGER SUCH AS HARD OR SHARP EDGES LIKE A FINGER NAIL ETC. ON THE CLOTH, BECAUSE IT CAUSE TRANSPARENT CONDUCTIVE FILM CRACKS. PLEASE ADVISE THIS PROHIBITION TO YOUR LAST CUSTOMERS.

12.3 DURABILITY

12.3.1 STYLUS HITTING :

ONE MILLION TIMES OR OVER
NO DAMAGE ON FILM SURFACE

PEN : R8 mm SILICON RUBBER

LOAD : 250g

FREQUENCY : 120 times/min

MEASUREMENT POSITION:

1 POINT OF TOUCH PANEL ACTIVE AREA

REPEATED : OVER 1,000,000 TIMES

12.3.2 PEN TOUCH SLIDING DURABILITY :

100,000 TIMES OR OVER

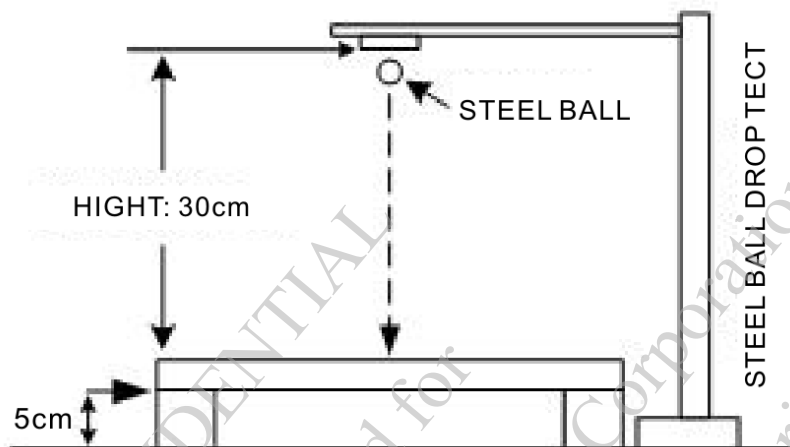
WRITING WITH R0.8mm PLASTIC STYLUS PEN; WRITING FORCE 150g
IN ACTIVE AREA.

SPEED IS 70mm/sec.

12.4 STEEL BALL DROP TEST

BY USING Ø9mm STEEL BALL FROM THE HEIGHT OF 30cm AND FALLING ON TOUCH PANEL SURFACE, MUST PASS BELOW CONDITIONS :

APPEARANCE : THE APPEARANCE WITHOUT ANY CHANGE, INCLUDING THE PANEL BROKEN.



12.5 APPEARANCE INSPECTION

PURPOSE :

TO ESTABLISH APPEARANCE STANDARD AND MAINTAIN PRODUCT QUALITY .

SCOPE :

TOUCH PANEL VIEW AREA WITHIN TOUCH PANEL .

12.5.1 RULE :

INSPECTION CONDITION

(A) ENVIRONMENTAL LUMINANCE : 500 LUX .

(B) DISTANCE BETWEEN HUMAN EYES AND PANEL : 30 CM

(PANEL MUST BE TESTED UNDER LIGHT TRANSPARENT) .

(C) VISUAL ANGEL : $> 60^\circ$.

(D) LIGHT SOURCE : FLUORESCENT LIGHT SOURCE .

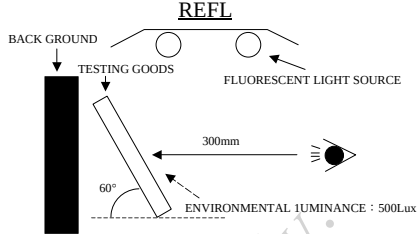
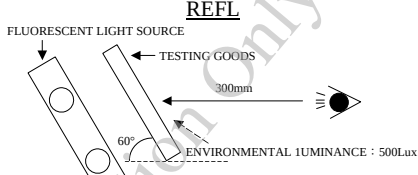
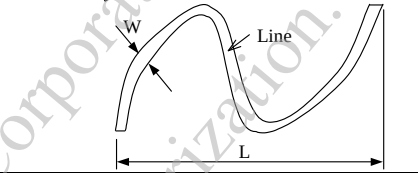
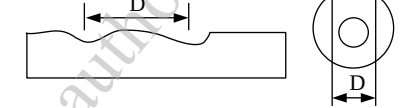
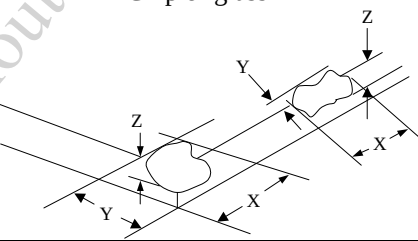
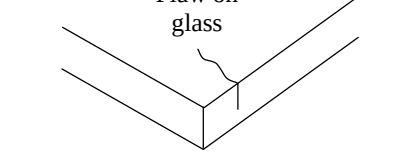
12.5.2 JUDGE CRITERION :

JUDGEMENT UNDER ABOVE MENTIONED CRITERION (PANEL MUST BE TESTED UNDER LIGHT TRANSPARENT),

TESTING GOODS DEFECT CAN BE VISIBLE WITHIN 10 SECONDS, WHICH WILL BE JUDGED AS MAJOR DEFECTS .

12.5.3 SAMPLING STANDARD :

THE SAMPLING STANDARD WILL BE CONFIRMED BY BOTH OF EDT AND CUSTOMER.

INSPECTION ITEMS	SEPC.		JUDGE CRITERION	OPERATION GUIDELINE
SCRATCH	$W \leq 0.05\text{mm} \ \& \ L \leq 5\text{mm}$		ACCEPTABLE	
	$W > 0.05\text{mm} \ \text{or} \ L > 5\text{mm}$		NOT ACCEPTABLE	
LINEAR FOREIGN OBJECT	$W \leq 0.05\text{mm} \ \& \ L \leq 5\text{mm}$		ACCEPTABLE	
	$W > 0.05\text{mm} \ \text{or} \ L > 5\text{mm}$		NOT ACCEPTABLE	
GRANULAR FOREIGN OBJECT	$D \leq 0.15\text{mm}$		ACCEPTABLE	
	$0.15\text{mm} < D \leq 0.2\text{mm}$		MAX. 2 EA	
	$0.2\text{mm} < D \leq 0.3\text{mm}$		MAX. 1 EA	
	$D > 0.3\text{mm}$		NOT ACCEPTABLE	
PET BUBBLES	$D \leq 0.5\text{mm}$		ACCEPTABLE	
	$D > 0.5\text{mm}$		NOT ACCEPTABLE	
CHIP ON GLASS	CORNER	$X \leq 3\text{mm} \ \& \ Y \leq 3\text{mm} \ \& \ Z < t$ (t = thickness)	ACCEPTABLE	
	EDGE	$W \leq 2\text{mm} \ \& \ Y \leq 3\text{mm} \ \& \ Z < t$		
FLAW	—		NOT ACCEPTABLE	

13. INSPECTION CRITERION

13.1 APPLICATION

This inspection standard is to be applied to the LCD module delivered from EMERGING DISPLAY TECHNOLOGIES CORP.(E.D.T) to customers

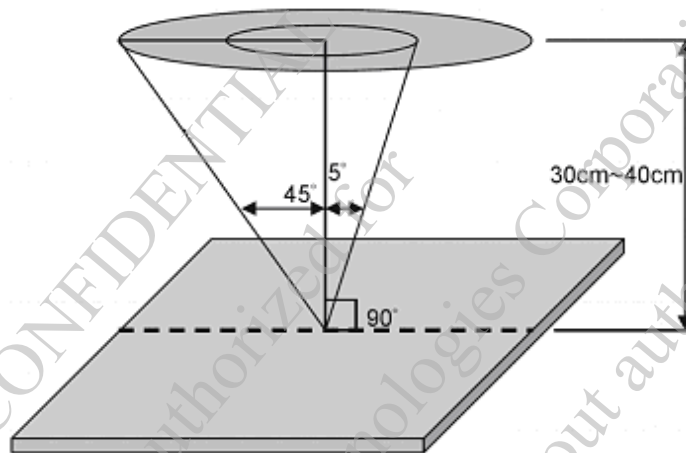
13.2 INSPECTION CONDITIONS

13.2.1 (1)Observation Distance : 35cm±5cm

(2)View Angle :

Non-operation Condition : $\pm 5^\circ$ (perpendicular to LCD panel surface)

Operation Condition : $\pm 45^\circ$ (perpendicular to LCD panel surface)



13.2.2 Environment Conditions :

Ambient Temperature		20°C~25°C
Ambient Humidity		65±20%RH
Ambient Illumination	Cosmetic Inspection	More than 600Lux
	Functional Inspection	300~500 Lux

13.2.3 Inspection lot

Quantity per delivery lot for each model

13.2.4 Inspection method

A sampling inspection shall be made according to the following provisions to judge The acceptability

(a)Applicable standard : MIL-STD-105E

Normal inspection, single sampling

Level II

(b)AQL : Major defect : AQL 0.65

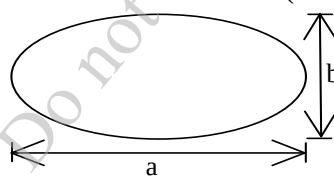
Minor defect : AQL 1.0

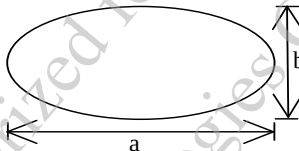
13.3 INSPECTION STANDARDS

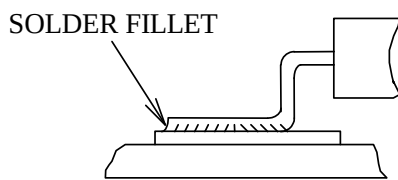
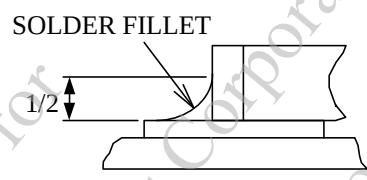
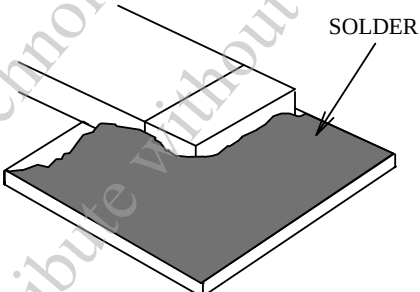
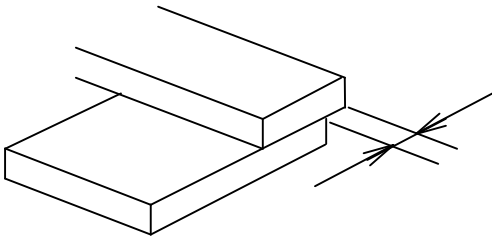
13.3.1 VISUAL DEFECTS CLASSIFICATION

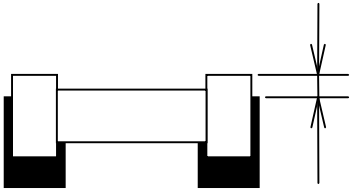
TYPE OF DEFECT	INSPECTION ITEM	DEFECT FEATURE	AQL
MAJOR DEFECT	1.DISPLAY ON	• DEFECT TO MISS SPECIFIED DISPLAY FUNCTION, FOR ALL AND SPECIFIED DOTS - EX: DISCONNECTION, SHORT CIRCUIT ETC	0.65
	2.BACKLIGHT	• NO LIGHT • FLICKERING AND OTHER ABNORMAL ILLUMINATION	
	3.DIMENSIONS	• SUBJECT TO INDIVIDUAL ACCEPTANCE SPECIFICATIONS	
MINOR DEFECT	1.DISPLAY ZONE	• BLACK/WHITE SPOT • BUBBLES ON POLARIZER • NEWTON RING • BLACK/WHITE LINE • SCRATCH • CONTAMINATION • LEVER COLOR SPREAD	1.0
	2.BEZEL ZONE	• STAINS • SCRATCHES • FOREIGN MATTER	
	3.SOLDERING	• INSUFFICIENT SOLDER • SOLDERED IN INCORRECT POSITION • CONVEX SOLDERING SPOT • SOLDER BALLS • SOLDER SCRAPS	
	4.DISPLAY ON (ALL ON)	• LIGHT LINE	

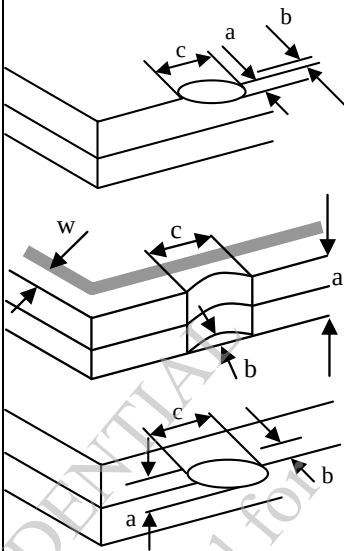
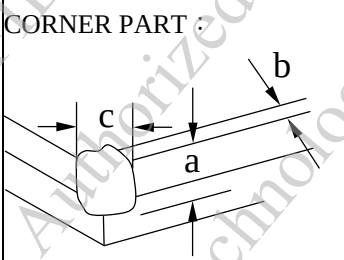
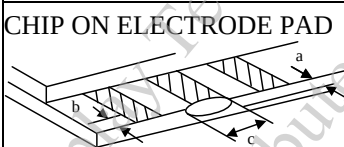
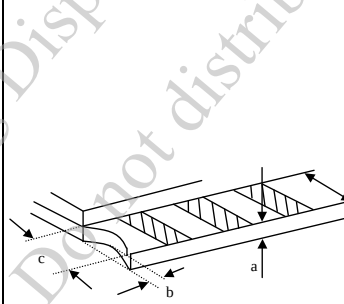
13.3.2 MODULE DEFECTS CLASSIFICATION

NO.	ITEM	CRITERIA												
1.	DISPLAY ON INSPECTION	(1)INCORRECT PATTERN (2)MISSING SEGMENT (3)DIM SEGMENT (4)OPERATING VOLTAGE BEYOND SPEC												
2.	OVERALL DIMENSIONS	(1)OVERALL DIMENSION BEYOND SPEC												
3.	DOT DEFECT	(1) INSPECTION PATTERN: FULL WHITE, FULL BLACK, RED, GREEN AND BLUE SCREENS. (2) <table><tr><th>ITEMS</th><th>ACCEPTABLE COUNT</th></tr><tr><td>BRIGHT DOT</td><td>$N \leq 2$</td></tr><tr><td>DARK DOT</td><td>$N \leq 3$</td></tr><tr><td>TOAL BRIGHT AND DARK DOTS</td><td>$N \leq 4$</td></tr></table> NOTE : 1. THE DEFINITION OF DOT : THE SIZE OF A DEFECTIVE DOT OVER 1/2 OF WHOLE DOT IS REGARDED AS ONE DEFECTIVE DOT. 2. BRIGHT DOT : DOTS APPEAR BRIGHT AND UNCHANGED IN SIZE IN WHICH LCD PANEL IS DISPLAYING UNDER BLACK PATTERN. 3. DARK DOT : DOTS APPEAR DARK AND UNCHANGED IN SIZE IN WHICH LCD PANEL IS DISPLAYING UNDER PURE RED, GREEN, BLUE PICTURE.	ITEMS	ACCEPTABLE COUNT	BRIGHT DOT	$N \leq 2$	DARK DOT	$N \leq 3$	TOAL BRIGHT AND DARK DOTS	$N \leq 4$				
ITEMS	ACCEPTABLE COUNT													
BRIGHT DOT	$N \leq 2$													
DARK DOT	$N \leq 3$													
TOAL BRIGHT AND DARK DOTS	$N \leq 4$													
4.	FOREIGN BLACK/WHITE/ BRIGHT LINE/ SCRATCH OF VIEWING AREA	<table><tr><th>LENGTH : L</th><th>WIDTH : W</th><th>PERMISSIBLE NO.</th></tr><tr><td>$L \leq 0.3$</td><td>$W \leq 0.05$</td><td>IGNORE</td></tr><tr><td>$0.3 < L \leq 2$</td><td>$0.05 < W \leq 0.1$</td><td>4</td></tr><tr><td>$2 < L$</td><td>$0.1 < W$</td><td>NONE</td></tr></table> WIDTH : W mm, LENGH : L mm	LENGTH : L	WIDTH : W	PERMISSIBLE NO.	$L \leq 0.3$	$W \leq 0.05$	IGNORE	$0.3 < L \leq 2$	$0.05 < W \leq 0.1$	4	$2 < L$	$0.1 < W$	NONE
LENGTH : L	WIDTH : W	PERMISSIBLE NO.												
$L \leq 0.3$	$W \leq 0.05$	IGNORE												
$0.3 < L \leq 2$	$0.05 < W \leq 0.1$	4												
$2 < L$	$0.1 < W$	NONE												
5.	FOREIGN MATTER \ BLACK SPOTS \ WHITE SPOTS \ DENT (INCLUDING LIGHT LEAKAGE DUE TO POLARIZING PLATES PINHOLES, ETC.)	<table><tr><th>AVERAGE DIAMETER (mm): D</th><th>NUMBER OF PIECES PERMITTED</th></tr><tr><td>$D \leq 0.1$</td><td>IGNORE</td></tr><tr><td>$0.1 < D \leq 0.3$</td><td>4</td></tr><tr><td>$0.3 < D$</td><td>NONE</td></tr></table> NOTE : DIAMETER $D=(a+b)/2$ 	AVERAGE DIAMETER (mm): D	NUMBER OF PIECES PERMITTED	$D \leq 0.1$	IGNORE	$0.1 < D \leq 0.3$	4	$0.3 < D$	NONE				
AVERAGE DIAMETER (mm): D	NUMBER OF PIECES PERMITTED													
$D \leq 0.1$	IGNORE													
$0.1 < D \leq 0.3$	4													
$0.3 < D$	NONE													

NO.	ITEM	CRITERIA																				
6.	BUBBLES OF POLARIZER /DIRT/CF FAIL /SURFACE STAINS	<table><tr><td></td><td>AVERAGE DIAMETER (mm) : D</td><td>NUMBER OF PIECES PERMITTED</td></tr><tr><td rowspan="3">BUBBLE ON THE POLARIZER</td><td>$D \leq 0.25$</td><td>IGNORE</td></tr><tr><td>$0.25 < D \leq 0.5$</td><td>$N \leq 5$</td></tr><tr><td>$0.5 < D$</td><td>NOTE</td></tr><tr><td rowspan="2">SURFACE STATUS</td><td>$D < 0.1 \text{ mm}$</td><td>IGNORE</td></tr><tr><td>$0.1 < D \leq 0.3\text{mm}$</td><td>$N \leq 3$</td></tr><tr><td rowspan="2">CF FAIL / SPOT</td><td>$D < 0.1 \text{ mm}$</td><td>IGNORE</td></tr><tr><td>$0.1 < D \leq 0.3\text{mm}$</td><td>$N \leq 3$</td></tr></table>		AVERAGE DIAMETER (mm) : D	NUMBER OF PIECES PERMITTED	BUBBLE ON THE POLARIZER	$D \leq 0.25$	IGNORE	$0.25 < D \leq 0.5$	$N \leq 5$	$0.5 < D$	NOTE	SURFACE STATUS	$D < 0.1 \text{ mm}$	IGNORE	$0.1 < D \leq 0.3\text{mm}$	$N \leq 3$	CF FAIL / SPOT	$D < 0.1 \text{ mm}$	IGNORE	$0.1 < D \leq 0.3\text{mm}$	$N \leq 3$
			AVERAGE DIAMETER (mm) : D	NUMBER OF PIECES PERMITTED																		
		BUBBLE ON THE POLARIZER	$D \leq 0.25$	IGNORE																		
			$0.25 < D \leq 0.5$	$N \leq 5$																		
			$0.5 < D$	NOTE																		
		SURFACE STATUS	$D < 0.1 \text{ mm}$	IGNORE																		
			$0.1 < D \leq 0.3\text{mm}$	$N \leq 3$																		
		CF FAIL / SPOT	$D < 0.1 \text{ mm}$	IGNORE																		
			$0.1 < D \leq 0.3\text{mm}$	$N \leq 3$																		
		NOTE : (1)POLARIZER BUBBLE IS DEFINED AS THE BUBBLE APPEARS ON ACTIVE DISPLAY AREA. THE DEFECT OF POLARIZER BUBBLE SHALL BE IGNORED IF THE POLARIZER BUBBLE APPEARS ON THE OUTSIDE OF ACTIVE DISPLAY AREA. (2)THE EXTRANEIOUS SUBSTANCE IS DEFINED AS IT CAN BE OBSERVED WHEN THE MODULE IS POWER ON. (3)THE DEFINITION OF AVERAGE DIAMETER, D IS DEFINED AS FOLLOWING. AVERAGE DIAMETER (D)=(a+b)/2																				
																						
7.	LINE DEFECT ON DISPLAY	OBVIOUS VERTICAL OR HORIZONTAL LINE DEFECT IS NOT ALLOW																				
8.	MURA ON DISPLAY	IT'S OK IF MURA IS SLIGHT VISIBLE THROUNG 6% ND FILTER																				
9.	UNEVEN COLOR SPREAD, COLORATION	(1)TO BE DETERMINED BASED UPON THE STANDARD SAMPLE.																				
10.	BEZEL APPEARANCE	(1)BEZEL MAY NOT HAVE RUST, BE DEFORMED OR HAVE FINGER PRINTS STAINS HAVE OTHER CONTAMINATION. (2)BEZEL MUST COMPLY WITH JOB SPECIFICATIONS.																				
11	PCB	(1)THERE MAY NOT BE MORE THAN 2mm OF SEALANT OUTSIDE THE SEAL AREA ON THE PCB, AND THERE SHOULD BE NO MORE THAN THREE PLACES. (2)NO OXIDATION OR CONTAMINATION PCB TERMINALS (3)PARTS ON PCB MUST BE THE SAME AS ON THE PRODUCTION CHARACTERISTIC CHART. THERE SHOULD BE NO WRONG PARTS, MISSING PARTS OR EXCESS PARTS. (4)THE JUMPER ON THE PCB SHOULD CONFORM TO THE PRODUCT CHARACTERISTIC CHART. (5)IF SOLDER GETS ON BEZEL TAB PADS, LED PAD, ZEBRA PAD OR SCREW HOLD PAD; MAKE SURE IT IS SMOOTHED DOWN.																				

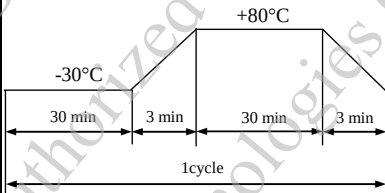
NO.	ITEM	CRITERIA
12.	SOLDERING	(1)NO SOLDERING FOUND ON THE SPECIFIED PLACE (2)INSUFFICIENT SOLDER (a)LSI, IC A POOR WETTING OF SOLDER IS BETWEEN LOWER BEND OR "HEEL" OF LEAD AND PAD  (b)CHIP COMPONENT - SOLDER IS LESS THAN 50% OF SIDES AND FRONT FACE WETTING  - SOLDER WETS 3 SIDES OF TERMINAL, BUT LESS THAN 25% OF SIDES AND FRONT SURFACE AREA ARE COVERED  (3)PARTS ALIGNMENT (a)LSI, IC LEAD WIDTH IS MORE THAN 50% BEYOND PAD OUTLINE 

NO.	ITEM	CRITERIA
12.	SOLDERING	(b)CHIP COMPONENT COMPONENT IS OFF CENTER, AND MORE THAN 50% OF THE LEADS IS OFF THE PAD OUTLINE  (4)NO UNMELTED SOLDER PASTE MAY BE PRESENT ON THE PCB. (5)NO COLD SOLDER JOINTS, MISSING SOLDER CONNECTIONS, OXIDATION OR ICICLE. (6)NO RESIDUE OR SOLDER BALLS ON PCB. (7)NO SHORT CIRCUITS IN COMPONENTS ON PCB.
13.	BACKLIGHT	(1)NO LIGHT (2)FLICKERING AND OTHER ABNORMAL ILLUMINATION (3)SPOTS OR SCRATCHES THAT APPEAR WHEN LIT MUST BE JUDGED USING LCD SPOT, LINES AND CONTAMINATION STANDARDS. (4)BACKLIGHT DOESN'T LIGHT OR COLOR IS WRONG.
14.	GENERAL APPEARANCE	(1)NO OXIDATION, CONTAMINATION, CURVES OR, BENDS ON INTERFACE PIN (OLB) OF TCP. (2)NO CRACKS ON INTERFACE PIN (OLB) OF TCP. (3)NO CONTAMINATION, SOLDER RESIDUE OR SOLDER BALLS ON PRODUCT. (4)THE IC ON THE TCP MAY NOT BE DAMAGED, CIRCUITS. (5)THE UPPERMOST EDGE OF THE PROTECTIVE STRIP ON THE INTERFACE PIN MUST BE PRESENT OR LOOK AS IF IT CAUSE THE INTERFACE PIN TO SEVER. (6)THE RESIDUAL ROSIN OR TIN OIL OF SOLDERING (COMPONENT OR CHIP COMPONENT) IS NOT BURNED INTO BROWN OR BLACK COLOR. (7)SEALANT ON TOP OF THE ITO CIRCUIT HAS NOT HARDENED. (8)PIN TYPE MUST MATCH TYPE IN SPECIFICATION SHEET. (9)LCD PIN LOOSE OR MISSING PINS. (10)PRODUCT PACKAGING MUST THE SAME AS SPECIFIED ON PACKAGING SPECIFICATION SHEET. (11)PRODUCT DIMENSION AND STRUCTURE MUST CONFORM TO PRODUCT SPECIFICATION SHEET. (12)THE APPEARANCE OF HEAT SEAL SHOULD NOT ADMIT ANY DIRT AND BREAK.

NO.	ITEM	CRITERIA									
15.	CRACKED GLASS	THE LCD WITH EXTENSIVE CRACK IS NOT ACCEPTABLE									
		GENERAL GLASS CHIP :  <table><tr><th>a</th><th>b</th><th>c</th></tr><tr><td>$\leq t/2$</td><td>< VIEWING AREA</td><td>$\leq 1/8X$</td></tr><tr><td>$t/2 > , \leq 2t$</td><td>$\leq W/2$</td><td>$\leq 1/8X$</td></tr></table> *W=DISTANCE BETWEEN SEALANT AREA AND LCD PANEL EDGE X = LCD SIDE LENGTH t = GLASS THICKNESS	a	b	c	$\leq t/2$	< VIEWING AREA	$\leq 1/8X$	$t/2 > , \leq 2t$	$\leq W/2$	$\leq 1/8X$
		a	b	c							
		$\leq t/2$	< VIEWING AREA	$\leq 1/8X$							
$t/2 > , \leq 2t$	$\leq W/2$	$\leq 1/8X$									
CORNER PART :  <table><tr><th>a</th><th>b</th><th>c</th></tr><tr><td>$\leq t/2$</td><td>< VIEWING AREA</td><td>$\leq 1/8X$</td></tr><tr><td>$> t/2 , \leq 2t$</td><td>$\leq W/2$</td><td>$\leq 1/8X$</td></tr></table> *W=DISTANCE BETWEEN SEALANT AREA AND LCD PANEL EDGE X = LCD SIDE LENGTH t = GLASS THICKNESS	a	b	c	$\leq t/2$	< VIEWING AREA	$\leq 1/8X$	$> t/2 , \leq 2t$	$\leq W/2$	$\leq 1/8X$		
a	b	c									
$\leq t/2$	< VIEWING AREA	$\leq 1/8X$									
$> t/2 , \leq 2t$	$\leq W/2$	$\leq 1/8X$									
CHIP ON ELECTRODE PAD  <table><tr><th>a</th><th>b</th><th>c</th></tr><tr><td>$\leq t$</td><td>$\leq 0.5\text{mm}$</td><td>$\leq 1/8X$</td></tr></table> * X=LCD SIDE WIDTH t=GLASS THICKNESS	a	b	c	$\leq t$	$\leq 0.5\text{mm}$	$\leq 1/8X$					
a	b	c									
$\leq t$	$\leq 0.5\text{mm}$	$\leq 1/8X$									
 <table><tr><th>a</th><th>b</th><th>c</th></tr><tr><td>$\leq t$</td><td>$\leq 1/8X$</td><td>$\leq L$</td></tr></table> *X=LCD SIDE WIDTH t = GLASS THICKNESS L=ELECTRODE PAD LENGTH ①IF GLASS CHIPPING THE ITO TERMINAL, OVER 2/3 OF THE ITO MUST REMAIN AND BE, INSPECTED ACCORDING TO ELECTRODE TERMINAL SPECIFICATIONS ②IF THE PRODUCT WILL BE HEAT SEALED BY THE CUSTOMER, THE ALIGNMENT MARK MUST NOT BE DAMAGED	a	b	c	$\leq t$	$\leq 1/8X$	$\leq L$					
a	b	c									
$\leq t$	$\leq 1/8X$	$\leq L$									

13.4 RELIABILITY TEST

13.4.1 STANDARD SPECIFICATIONS FOR RELIABILITY OF LCD MODULE

NO	ITEM	DESCRIPTION
1	HIGH TEMPERATURE OPERATION	THE SAMPLE SHOULD BE ALLOWED TO STAND AT +70°C FOR 240 hrs
2	LOW TEMPERATURE OPERATION	THE SAMPLE SHOULD BE ALLOWED TO STAND AT -20°C FOR 240 hrs
3	HIGH TEMPERATURE STORAGE	THE SAMPLE SHOULD BE ALLOWED TO STAND AT +80°C FOR 240 hrs
4	LOW TEMPERATURE STORAGE	THE SAMPLE SHOULD BE ALLOWED TO STAND AT -30°C FOR 240 hrs
5	HIGH TEMPERATURE / HIGH HUMIDITY STORAGE	THE SAMPLE SHOULD BE ALLOWED TO STAND AT 60°C, 90% RH 240 hrs
6	THERMAL SHOCK (NOT OPERATED)	THE SAMPLE SHOULD BE ALLOWED TO STAND THE FOLLOWING 10 CYCLES OF OPERATION :  The diagram illustrates a single cycle of thermal shock. It begins at -30°C, where it remains for 30 minutes. This is followed by a 3-minute ramp up to +80°C. The sample then remains at +80°C for 30 minutes. Finally, there is a 3-minute ramp down back to -30°C. The entire sequence, from the start of the first 30-minute hold to the end of the final 3-minute ramp, is labeled as '1cycle'.
7	ESD (ELECTROSTATIC DISCHARGE) (NOT OPERATED)	AIR DISCHARGE $\pm 12KV$ CONTACT DISCHARGE $\pm 8KV$

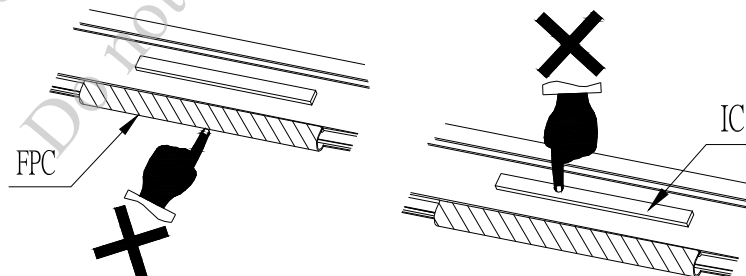
13.4.2 TESTING CONDITIONS AND INSPECTION CRITERIA

FOR THE FINAL TEST THE TESTING SAMPLE MUST BE STORED AT ROOM TEMPERATURE FOR 24 HOURS, STANDARD SPECIFICATIONS FOR RELIABILITY HAVE BEEN EXECUTED IN ORDER TO ENSURE STABILITY.

NO	ITEM	TEST MODEL	INSPECTION CRITERIA
1	CURRENT CONSUMPTION	REFER TO SPECIFICATION	THE CURRENT CONSUMPTION SHOULD CONFORM TO THE PRODUCT SPECIFICATION.
2	CONTRAST	REFER TO SPECIFICATION	AFTER THE TESTS HAVE BEEN EXECUTED, THE CONTRAST MUST BE LARGER THAN HALF OF ITS INITIAL VALUE PRIOR TO THE TESTS.
3	APPEARANCE	VISUAL INSPECTION	DEFECT FREE

13.5 OPERATION

- 13.5.1 Do not connect or disconnect modules to or from the main system while power is being supplied .
- 13.5.2 Use the module within specified temperature ; lower temperature causes the retardation of blinking speed of the display ; higher temperature makes overall display discolor . When the temperature returns to normality , the display will operate normally .
- 13.5.3 Adjust the LC driving voltage to obtain the optimum contrast .
- 13.5.4 Power On Sequence input signals should not be supplied to LCD module before power supply voltage is applied and reaches the specified value ($5 \pm 0.25v$) .
If above sequence is not followed , CMOS LSIs of LCD modules may be damaged due to latch - up problem .
- 13.5.5 Not allowed to inflict any external stress and to cause any mechanical interference on the bending area of FPC during the tail bending backwards!
Do NOT stress FPC and IC on the Module!



13.6 NOTICE

- 13.6.1 Use a grounded soldering iron when soldering connector I/O terminals . For soldering or repairing , take precaution against the temperature of the soldering iron and the soldering time to prevent peeling off the through-hole-pad .
- 13.6.2 Do not disassemble . EDT shall not be held responsible if the module is disassembled and upon the reassembly the module failed .
- 13.6.3 Do not charge static electricity , as the circuit of this module contains CMOS LSIs. A workman's body should always be static-protected by use of an ESD STRAP . Working clothes for such personnel should be of static-protected material .
- 13.6.4 Always ground the electrically-powered driver before using it to install the LCD module. While cleaning the work station by vacuum cleaner, do not bring the sucking mouth near the module ; static electricity of the electrically-powered driver or the vacuum cleaner may destroy the module .
- 13.6.5 Don't give external shock.
- 13.6.6 Don't apply excessive force on the surface.
- 13.6.7 Liquid in LCD is hazardous substance. Must not lick and swallow. When the liquid is attached to your, skin, cloths etc. wash it out thoroughly and immediately.
- 13.6.8 Don't operate it above the absolute maximum rating.
- 13.6.9 Storage in a clean environment, free from dust, active gas, and solvent.
- 13.6.10 Store without any physical load.
- 13.6.11 Rewiring : no more than 3 times .