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AM6441: GPMC configuration in SYSCONFIG

Oba
139.187.34.34

Genius 15640 points

Texas Instruments

Part Number: AM6441
Other Parts Discussed in Thread: SYSCONFIG

Hello,

My customer has a question for GPMC configuration in SYSCONFIG(mcu_plus_sdk_am64x_09_00_00_35).
Now they are facing 2 problems.

1. Only 8bit can be selected for "Device Size". They want to use 16bit or 32bit.
2. Only one CS area can be configured. They want to use several CS areas.

I found the below similar post and I understand the above case 1 will be support in the future release.
How about case 2?

.

And I understand that only 8bit cab be selected from SYSCONFIG. But is it possible to select 16bit or 32bit and configure multiple CS areas through driver API call?

Regards,
Satoshi Obata

3 months ago

Swargam Anil *139.187.34.34* *3 months ago*   TI__Mastermind 18860 points

Hello Satoshi Obata,

I am looking at your queries, and you may expect a delayed reply .
Regards,
S.Anil

Swargam Anil *139.187.34.34* *3 months ago* *in reply to* *Swargam Anil*   TI__Mastermind 18860 points

Hello Satoshi Obata,

Can you please confirm which memory interface you are using—NAND memory or NOR memory?

Regards,

S.Anil.

Oba *139.187.34.35* *3 months ago* *in reply to* *Swargam Anil*   TI__Genius 15640 points

Hello,

It's NOR type memory.

Regards,
Oba

Swargam Anil *139.187.34.35* *2 months ago* *in reply to* *Oba*   TI__Mastermind 18860 points

Hello Oba,

In AM62X variants, there is a NAND interface card that is connected to AM62X SK kits. On the NAND interface cards, we currently support only 8-bit NAND devices, and the same AM62X code is integrated into AM64X devices.

> *Oba said:*
>
> *And I understand that only 8bit cab be selected from SYSCONFIG. But is it possible to select 16bit or 32bit and configure multiple CS areas through driver API call?*

Currently, we don't have API calls to change bit size and CS size.

For bit selection and CS, you need to update this below generated code and make sure that for other than 8-bit GPMC, you have to update pin settings for remaining pins as well since there is no support for selecting other than 8 bits in the system configuration.

.

```
/* GPMC attributes */
static GPMC_HwAttrs gGpmcHwAttrs[CONFIG_GPMC_NUM_INSTANCES] =
{
    {
        .gpmcBaseAddr      = CSL_GPMC_CFG_BASE,
        .dataBaseAddr      = CSL_GPMC_DATA_BASE,
        .elmBaseAddr       = CSL_ELM0_BASE,
        .inputClkFreq      = 133333333U,
        .intrNum           = (CSLR_R5FSS0_CORE0_INTR_GPMC0_GPMC_SINTERRUPT_0,
        .intrPriority      = 4U,
        .chipSelBaseAddr   = 0x50000000U,
        .chipSelAddrSize   = GPMC_CS_NAND_ADDR_SIZE_16M,
        .clkDivider        = CSL_GPMC_CONFIG1_GPMCACLKDIVIDER_DIV0Y1,
        .waitPinNum        = CSL_GPMC_CONFIG1_WAITPINSELECT_W0,
        .addrDataMux       = CSL_GPMC_CONFIG1_MUXADDDATA_NONMUX,
        .timeLatency       = CSL_GPMC_CONFIG1_TIMEPARAGRANULARITY_X1,
        .waitPinPol        = CSL_GPMC_CONFIG1_WAITPINPOLARITY_W0ACTIVEL,
        .timingParams      =
        {
            .csOnTime                    = GPMC_NAND_CS_ON_TIME,
            .csRdOffTime                 = GPMC_NAND_CS_RD_OFF_TIME,
            .csWrOffTime                 = GPMC_NAND_CS_WR_OFF_TIME,
            .advOnTime                   = GPMC_NAND_ADV_ON_TIME,
            .advRdOffTime                = GPMC_NAND_ADV_RD_OFF_TIME,
            .advWrOffTime                = GPMC_NAND_ADV_WR_OFF_TIME,
            .advAadMuxOnTime             = GPMC_NAND_ADV_AADMUX_ON_TIME,
            .advAadMuxRdOffTime          = GPMC_NAND_ADV_AADMUX_RD_OFF_TIME,
            .advAadMuxWrOffTime          = GPMC_NAND_ADV_AADMUX_WR_OFF_TIME,
            .weOnTime                    = GPMC_NAND_WE_ON_TIME,
            .weOffTime                   = GPMC_NAND_WE_OFF_TIME,
            .oeOnTime                    = GPMC_NAND_OE_ON_TIME,
            .oeOffTime                   = GPMC_NAND_OE_OFF_TIME,
            .oeAadMuxOnTime              = GPMC_NAND_OE_AADMUX_ON_TIME,
            .oeAadMuxOffTime             = GPMC_NAND_OE_AADMUX_OFF_TIME,
            .pageBurstAccess             = GPMC_NAND_PAGEBURST_ACCESS_TIME,
            .rdAccessTime                = GPMC_NAND_RD_ACCESS_TIME,
            .wrAccessTime                = GPMC_NAND_WR_ACCESS_TIME,
            .rdCycleTime                 = GPMC_NAND_RD_CYCLE_TIME,
            .wrCycleTime                 = GPMC_NAND_WR_CYCLE_TIME,
            .wrDataOnMuxBusTime          = GPMC_NAND_WRDATA_DATA_VALID,
            .cycle2CycleDelay            = GPMC_NAND_C2C_DELAY,
            .cycleDelaySameChipSel       = CSL_GPMC_CONFIG6_CYCLE2CYCLESAMECSEN_C2CSCDELAY,
            .cycleDelayDiffChipSel       = CSL_GPMC_CONFIG6_CYCLE2CYCLEDIFFCSEN_NOC2CDELAY,
            .busTurnAroundTime           = GPMC_NAND_BUS_TURNAROUND_TIME,
        },
        .attIdg       = GPMC_NAND_ECC_ALGO_BCH_8BIT,
        .readType     = CSL_GPMC_CONFIG1_READTYPE_RDASYNC,
        .csExtDelay   = CSL_GPMC_CONFIG2_CSEXTRADELAY_NOTDELAYED,
        .accessType   = CSL_GPMC_CONFIG1_READMULTIPLE_RDSINGLE,
        .dmaRestrictedRegions = gGpmcDmaRestrictRegions,
    },
};
```

```
/* GPMC Driver Parameters */
GPMC_Params gGpmcParams[CONFIG_GPMC_NUM_INSTANCES] =
{
    {
        .gpmcDmaChIndex = 0,
        .devType        =    CSL_GPMC_CONFIG1_DEVICETYPE_NANDLIKE,
        .devSize        =    CSL_GPMC_CONFIG1_DEVICESIZE_EIGHTBITS,
        .chipSel        =    GPMC_CHIP_SELECT_CS0,
        .intrEnable     =    FALSE,
        .dmaEnable      =    TRUE,
        .transferMode   =    GPMC_TRANSFER_MODE_BLOCKING,
        .transferCallBckFunc =    NULL,
    },
};
```

```
static Pinmux_PerCfg_t gPinMuxMainDomainCfg[] = {
    /* GPMC0 pin config */
    /* GPMC0_CSAN -> GPMC0_CSAN (R19) */
    {
        PIN_GPMC0_CSAN,
        ( PIN_MODE(0) | PIN_PULL_DISABLE )
    },
    /* GPMC0 pin config */
    /* GPMC0_OEn_REn -> GPMC0_OEn_REn (R16) */
    {
        PIN_GPMC0_OEN_REN,
        ( PIN_MODE(0) | PIN_PULL_DISABLE )
    },
    /* GPMC0 pin config */
    /* GPMC0_WAITN -> GPMC0_WAITN (W19) */
    {
        PIN_GPMC0_WAITN,
        ( PIN_MODE(0) | PIN_INPUT_ENABLE | PIN_PULL_DISABLE )
    },
    /* GPMC0 pin config */
    /* GPMC0_WEn -> GPMC0_WEn (T16) */
    {
        PIN_GPMC0_WEN,
        ( PIN_MODE(0) | PIN_PULL_DISABLE )
    },
    /* GPMC0 pin config */
    /* GPMC0_BE0n_CLE -> GPMC0_BE0n_CLE (P17) */
    {
        PIN_GPMC0_BE0N_CLE,
        ( PIN_MODE(0) | PIN_PULL_DISABLE )
    },
    /* GPMC0 pin config */
    /* GPMC0_ADV_ALE -> GPMC0_ADV_ALE (T16) */
    {
        PIN_GPMC0_ADVN_ALE,
        ( PIN_MODE(0) | PIN_PULL_DISABLE )
    },
    /* GPMC0 pin config */
    /* GPMC0_AD0 -> GPMC0_AD0 (T20) */
    {
        PIN_GPMC0_AD0,
        ( PIN_MODE(0) | PIN_INPUT_ENABLE | PIN_PULL_DISABLE )
    },
    /* GPMC0 pin config */
    /* GPMC0_AD1 -> GPMC0_AD1 (U21) */
    {
        PIN_GPMC0_AD1,
        ( PIN_MODE(0) | PIN_INPUT_ENABLE | PIN_PULL_DISABLE )
    },
};
```

Currently, timing parameters are supported for NAND memories and not for NOR memories.

Since the user needs to change the above changes, the timing parameters should also be updated for the NOR type.

I need to confirm internally if there are any gpmc examples of NOR memory types in the future or not and let you know.

Regards,

S.Anil.

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